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H8/300L SLP Series

Setting Standby Time to Cover Clock Stabilization (H8/3867)

Introduction

When switching to active mode by canceling standby or watch mode through a specific interrupt request, the standby time period waiting for stabilization of a clock is specified for the CPU and the peripheral functions. The standby time period must be specified so as to exceed the oscillation stabilization time according to the operating frequency.

Target Device

H8/3867

Contents

1. Used

When switching to active mode by canceling standby or watch mode through a specific interrupt request, the standby time period waiting for stabilization of a clock is specified for the CPU and the peripheral functions. The standby time period must be specified so as to exceed the oscillation stabilization time according to the operating frequency.

1.1 Setting of the Standby Time Period

The standby time period is set by setting the standby timer select bits 2 to 0 (STS2 to STS0) in the system control register 1 (SYSCR1).

1.2 Description of STS2 to STS0

Table 1.1 shows the description of STS2 to STS0 in SYSCR1.

Table 1.1 Description of STS2 to STS0

SYSCR1				
Bit 6	Bit 5	Bit 4		
STS2	STS1	STS0	Description	
0	0	0	Standby time period = 8,192 states	(initial setting)
0	0	1	Standby time period = 16,384 states	
0	1	0	Standby time period = 32,768 states	
0	1	1	Standby time period = 65,536 states	
1	0	0	Standby time period = 131,072 states	
1	0	1	Standby time period = 2 states	(external clock input mode)
1	1	0	Standby time period = 8 states	
1	1	1	Standby time period = 16 states	

Note: To input an external clock, the standby timer select bits must be set to the external clock input mode prior to mode transition. Do not set those bits to the external clock input mode if an external clock is not used.

1.3 Operating Frequency and Oscillation Stabilization Time when Using a Crystal Oscillator

Table 1.2 shows the operating frequency and standby time relative to the settings of STS2 to STS0 when a crystal oscillator is used. The STS2 to STS0 must be set so that the standby time is longer than the oscillation stabilization time.

Table 1.2 Operating Frequency and Oscillation Stabilization Time when Using a Crystal Oscillator

(Unit: ms)

STS2	STS1	STS0	Standby time	2 MHz	1 MHz	0.5 MHz
0	0	0	8,192 states	4.1	8.2	16.4
0	0	1	16, 384 states	8.2	16.4	32.8
0	1	0	32,768 states	16.4	32.8	65.5
0	1	1	65,536 states	32.8	65.5	131.1
1	0	0	131,072 states	65.5	131.1	262.1
1	0	1	2 states (prohibited)	0.001	0.002	0.004
1	1	0	8 states	0.004	0.008	0.016
1	1	1	16 states	0.008	0.016	0.032

1.4 External Clock

It is recommended that the values of STS2 to STS0 are set to 1, 0, 1, respectively. Other settings are available however, if other settings are used besides those which are recommended, the LSI may begin its operation even though standby time has not ended.

1.5 Oscillation Stabilization Time

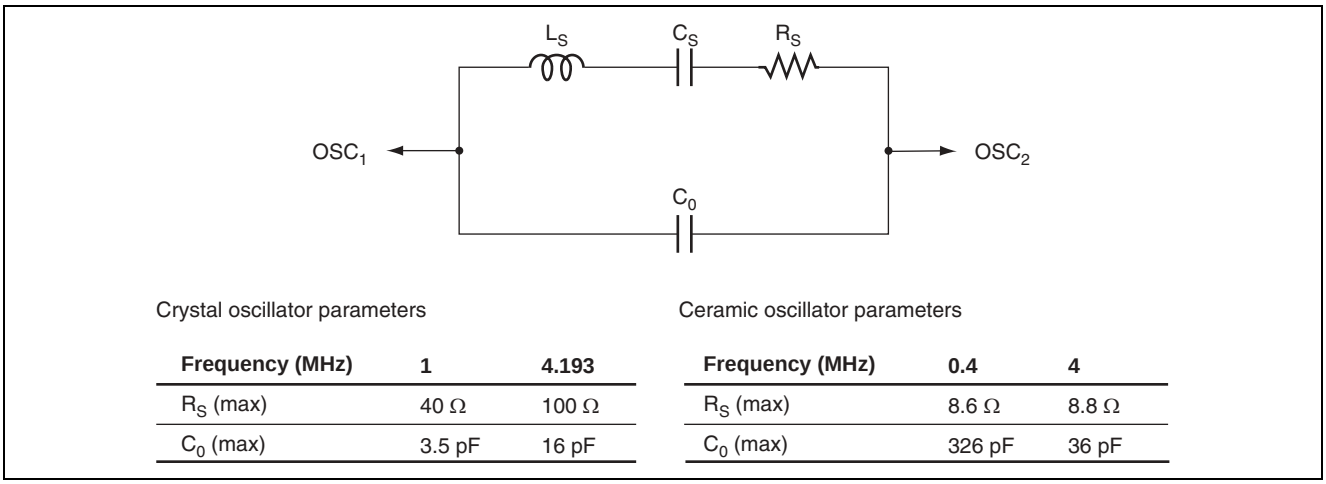
Table 1.3 shows the AC characteristics of oscillation stabilization time.

Table 1.3 AC characteristics of Oscillation Stabilization Time

(Vcc = 1.8 to 5.5 V, AVcc = 1.8 to 5.5 V, Vss = AVss = 0.0 V, Ta = -20 to +75°C, including sub active mode)

Item	Symbol	Pin	Measurement condition	Specification min.	typ.	max.	Unit	Reference
Oscillation stabilization time	t_{rc}	OSC_1, OSC_2	In the case of figure 1, Vcc = 2.2 to 5.5 V	—	20	45	us	Figure 1*
			In the case of figure 1, Vcc = 2.2 to 5.5 V		0.1	8	ms	Figure 1
			Other than the above	—	—	50	ms	
Oscillation stabilization time	t_{rc}	X_1, X_2		—	—	2.0	s	—

Note: * The internal power supply voltage step down circuit is not used.



Crystal oscillator parameters

Frequency (MHz)	1	4.193
R_S (max)	40 Ω	100 Ω
C_0 (max)	3.5 pF	16 pF

Ceramic oscillator parameters

Frequency (MHz)	0.4	4
R_S (max)	8.6 Ω	8.8 Ω
C_0 (max)	326 pF	36 pF

Figure 1.1 Equivalent Circuit of Oscillator

1.6 Oscillation Stabilization Time Setting Example

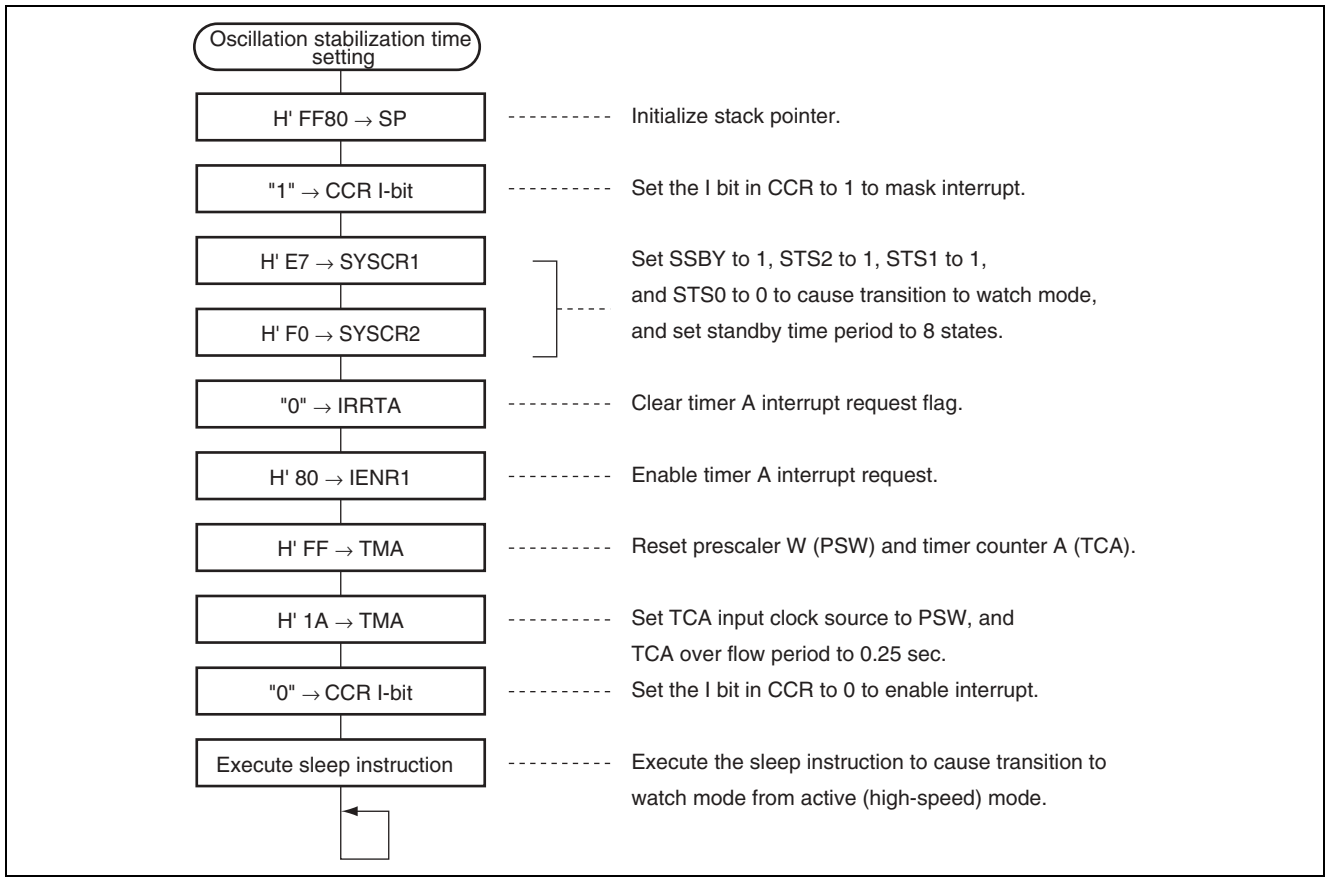
1. Function
   Transit to watch mode from active (high-speed) mode, cancel the watch mode through a timer A interrupt after 250 ms has passed, and then transit to the active (high-speed) mode. When transiting to the active (high-speed) mode from the watch mode, the CPU and the peripheral functions wait for 8 states until the clock becomes stable.
2. Cautions
   In this example, when canceling the watch mode through the timer A interrupt, the timer A interrupt request is prohibited in timer A interrupt processing. Accordingly, the processing ends after transiting to the watch mode from the active (high-speed) mode, canceling the watch mode through the timer A interrupt, and then transiting to the active (high-speed) mode.

3. Watch mode
   A. Transition to watch mode
      Executing the SLEEP instruction when the software standby bit (SSBY) in the system control register 1 (SYSCR1) is 1 and the internal clock select 3 bit (TMA3) in the timer mode register A (TMA) is 1 during active mode or sub active mode causes a transition to watch mode. In watch mode, the on-chip peripheral functions except for the timer A, the timer F, the timer G, the asynchronous event counter, and the LCD (operate/ stop selectable) stop its operation. As long as a specific voltage is applied, the contents of the CPU, the internal registers of a part of on-chip peripheral functions, and internal RAM are retained, and the I/O ports retain its pre-transition status.

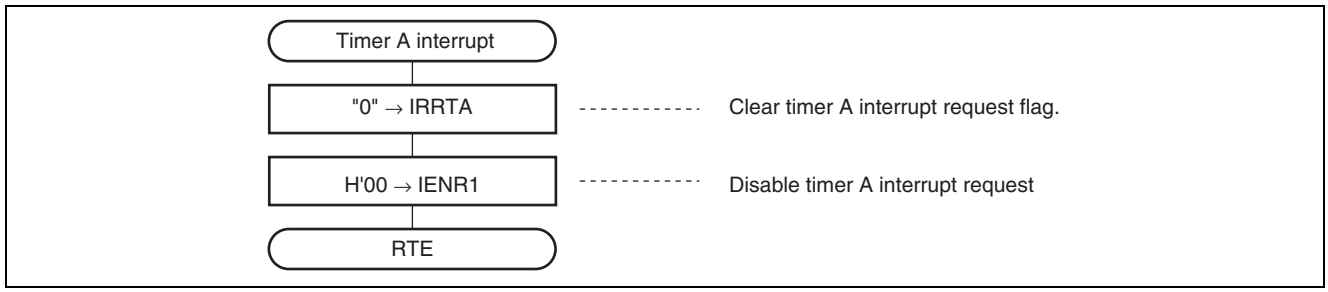
   B. Cancellation of watch mode
      Watch mode is cancelled through an interrupt (IRQ0, WKP7 to WKP0, timer A, timer F, or timer G) or a RES pin input.
      In the case of cancellation through an interrupt, when an interrupt is generated, watch mode is cancelled, and transition to active (high-speed) mode when the low speed on flag (LSON) in SYSCR1 = 0 and the middle speed on flag (MSON) in the system control register 2 (SYSCR2) = 0, active (intermediate-speed) mode when LSON = 0 and MSON = 1, or sub active mode when LSON = 1 occurs. When transiting to active mode, after the time period specified by STS2 to STS0 in SYSCR1 has elapsed, a stable clock is supplied to the entire LSI, and interrupt exception handling is begun. Note that when the I bit in CCR is 1, or when acceptance of the interrupt is prohibited by the interrupt enable register, watch mode is not cancelled.
      In the case of cancellation through a RES pin, when the RES pin is set to low, the system clock starts its oscillation. When the RES pin is set to high after the oscillation stabilization time has elapsed, the CPU starts reset exception handling. Note that the system clock is supplied to the entire LSI as soon as the system clock starts its oscillation. Therefore, the RES pin must be held low until the system clock oscillation becomes stable.

2. Flowchart

1. Main routine



2. Timer A interrupt processing routine



3. Program listing

```
;*****************************************************************************
;*      H8/3867 Application Note                                             *
;*                                                                           *
;*     'Oscillator Settling Time -8 States'                                  *
;*                                                                           *
;*     Function : Oscillator Settling Time                                   *
;*                                                                           *
;*     External Clock : 6MHz                                                 *
;*     Internal Clock : 3MHz                                                 *
;*     Sub Clock      : 32.768kHz                                            *
;*****************************************************************************
;
          .cpu         300l
;
;*****************************************************************************
;*  Symbol Defnition                                                         *
;*****************************************************************************
;
TMA       .equ         h'ffb0        ;Timer Mode Register A
SYSCR1    .equ         h'fff0        ;System Control Register 1
SYSCR2    .equ         h'fff1        ;System Control Register 2
IENR1     .equ         h'fff3        ;Interrupt Enable Register 1
IRR1      .equ         h'fff6        ;Interrupt Request Register 1
;
;*****************************************************************************
;*  Vector Address                                                           *
;*****************************************************************************
;
          .org         h'0000
          .data.w      MAIN          ;No.0 Reset Interrupt(H'0000-H'0001)
;
          .org         h'0008
          .data.w      MAIN          ;No.4 _IRQ0 Interrupt(H'0008-H'0009)
          .data.w      MAIN          ;No.5 _IRQ1 Interrupt(H'000A-H'000B)
          .data.w      MAIN          ;No.6 _IRQ2 Interrupt(H'000C-H'000D)
          .data.w      MAIN          ;No.7 _IRQ3 Interrupt(H'000E-H'000F)
          .data.w      MAIN          ;No.8 _IRQ4 Interrupt(H'0010-H'0011)
          .data.w      MAIN          ;No.9 _WKP0-_WKP7 Interrupt(H'0012-H'0013)
;
          .org         h'0016
          .data.w      TAINT         ;No.11 Timer A Interrupt(H'0016-H'0017)
          .data.w      MAIN          ;No.12 AEC Interrupt(H'0018-H'0019)
          .data.w      MAIN          ;No.13 Timer C Interrupt(H'001A-H'001B)
          .data.w      MAIN          ;No.14 Timer FL Interrupt(H'001C-H'001D)
          .data.w      MAIN          ;No.15 Timer FH Interrupt(H'001E-H'001F)
          .data.w      MAIN          ;No.16 Timer G Interrupt(H'0020-H'0021)
          .data.w      MAIN          ;No.17 SCI31 Interrupt(H'0022-H'0023)
          .data.w      MAIN          ;No.18 SCI32 Interrupt(H'0024-H'0025)
          .data.w      MAIN          ;No.19 A/D Converter Interrupt(H'0026-H'0028)
          .data.w      MAIN          ;No.20 Direct Transfer Interrupt(H'0028-H'0029)
;
```

```
;*************************************************************************************
;*  MAIN : Main Routine                                                              *
;*************************************************************************************
;
          .org          h'1000
;
MAIN:     equ           $
          mov.w         #h'ff80,sp    ;Initialize Stack Pointer
          orc           #h'80,ccr     ;Interrupt Disable
;
          mov.b         #h'e7,r0l     ;Initialize System Control Register
          mov.b         r0l,@SYSCR1
          mov.b         #h'f0,r0l
          mov.b         r0l,@SYSCR2
;
          bclr          #7,@IRR1
          mov.b         #h'80,r0l
          mov.b         r0l,@IENR1

;
          mov.b         #h'ff,r0l
          mov.b         r0l,@TMA
          mov.b         #h'1a,r0l
          mov.b         r0l,@TMA
;
          andc          #h'7f,ccr
;
          sleep
;
          nop
;
EXIT:     bra           EXIT
;
;*************************************************************************************
;*  TMAINT : Timer A Interrupt Routine                                               *
;*************************************************************************************
;
TAINT:    .equ          $
          bclr          #7,@IRR1
;
          mov.b         #h'00,r0l
          mov.b         r0l,@IENR1
;
          rte

;
          .end
```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.03	—	First edition issued

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