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Renesas Electronics Corporation

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H8/300L SLP Series

Setting Standby Time to Cover Clock Stabilization

Introduction

This sample task shows how to set a standby time, during which the CPU and peripheral functions are kept in a standby state until the clock stabilizes.

Target Device

H8/38024

Contents

1. Specifications

A standby time, during which the CPU and peripheral functions are kept in a standby state until the clock stabilizes, is set. This standby time is applied after a transition is made from standby mode or watch mode to active mode by means of a specific interrupt. The standby time must be set appropriately for the operating frequency so that it is longer than the clock oscillation stabilization time.

1.1 Setting the standby time

The standby time is set by setting the standby timer select bits 2 to 0 (STS2 to STS0) in system control register 1 (SYSCR1).

1.2 Description of the STS2 to STS0 bits

Table 1.1 describes the STS2 to STS0 bits in SYSCR1 register.

Table 1.1 Description of STS2 to STS0

SYSCR1				
Bit 6	Bit 5	Bit 4		
STS2	STS1	STS0	Description	
0	0	0	Standby time = 8,192 states	(Initial value)
		1	Standby time = 16,384 states	
	1	0	Standby time = 1,024 states	
		1	Standby time = 2,048 states	
1	0	0	Standby time = 4,096 states	
		1	Standby time = 2 states	(External clock mode)
	1	0	Standby time = 8 states	
		1	Standby time = 16 states	

Note: When an external clock signal is to be input, the standby timer select bits must be set to external clock mode before execution of the mode transition. When an external clock is not used, the external clock mode must not be set.

1.3 Operating frequency and oscillation stabilization time when a crystal oscillator is used

Table 1.2 shows the standby times for various operating frequencies and STS2 to STS0 settings. STS2 to STS0 must be set so that the standby time is longer than the time required for oscillation stabilization.

Table 1.2 Operating Frequency and Oscillation Stabilization Times

STS2	STS1	STS0	Standby Time	5 MHz	2 MHz
0	0	0	8,192 states	1.638	4.1
		1	16,384 states	3.277	8.2
	1	0	1,024 states	0.205	0.512
		1	2,048 states	0.410	1.024
1	0	0	4,092 states	0.819	2.048
		1	2 states (Use prohibited)	0.0004	0.001
	1	0	8 states	0.0002	0.004
		1	16 states	0.003	0.008

Unit: ms

1.4 When an external clock is used

Recommended setting is STS2 = 1, STS1 = 0, and STS0 = 1. Other settings are possible, but operation may start before the standby time ends.

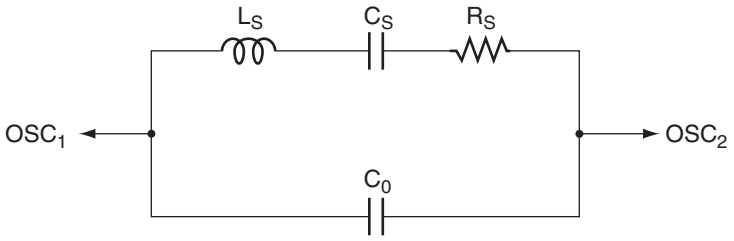
1.5 Oscillation stabilization time

Table 1.3 shows the AC characteristics of oscillation stabilization times.

Table 1.3 AC Characteristics of Oscillation Stabilization Time

(V_{CC} = 1.8 to 5.5 V, AV_{CC} = 1.8 to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20 to +75°C, including subactive mode)

Item	Symbol	Applicable Pins	Measurement Conditions	Values Min	Typ	Max	Unit	Reference Figure
Oscillation stabilization time	t_{rc}	OSC_1, OSC_2	V_{CC} = 2.2 V to5.5 V (as shown in figure 1.1)	—	20	45	us	Figure 1.1
			Other than the above	—	—	50	ms	Figure 1.1
Oscillation stabilization time	t_{rc}	X_1, X_2	V_{CC} = 2.7 V to5.5 V	—	—	2.0	s	—
			V_{CC} = 2.2 V to5.5 V	—	—	10.0	s	—



Crystal oscillator parameters

Frequency (MHz)	4.193
R_S (max)	100Ω
C_0 (max)	16 pF

Ceramic oscillator parameters

Frequency (MHz)	4
R_S (max)	8.8Ω
C_0 (max)	36 pF

Figure 1.1 Oscillator Equivalent Circuit

1.6 Example of setting the standby time to cover clock stabilization

1. Functions

   A transition from active (high-speed) to watch mode is induced. The watch mode is terminated after 250 ms by a timer A interrupt, and a transition is made to high-speed active mode. The standby time applied when returning from watch mode to high-speed active mode is set to eight states, during which the CPU and peripheral functions stay in a standby state waiting for the clock to stabilize.

2. Notes

   In this example, when the watch mode is terminated by a timer A interrupt, timer A interrupt requests are disabled in timer A interrupt handling. Hence when a transition from high-speed active mode to watch mode is made, watch mode is then terminated by a timer A interrupt and high-speed active mode has been entered, the processing ends.

3. Watch mode

   A. Transition to watch mode

   In active mode or subactive mode, when the software standby bit (SSBY) in system control register 1 (SYSCR1) is 1 and the internal clock selector 3 bit (TMA3) in timer mode register A (TMA) is 1, executing a SLEEP instruction induces a transition to watch mode. In watch mode, operation of all on-chip peripheral functions other than timer A, timer F, timer G, the asynchronous event counter, and the LCD module (operation/halted selectable), is halted. As long as the rated voltage is supplied, the contents of CPU registers, some on-chip peripheral module registers, and on-chip RAM are retained. The I/O ports are held in the same states as before the transition.

   B. Termination of watch mode

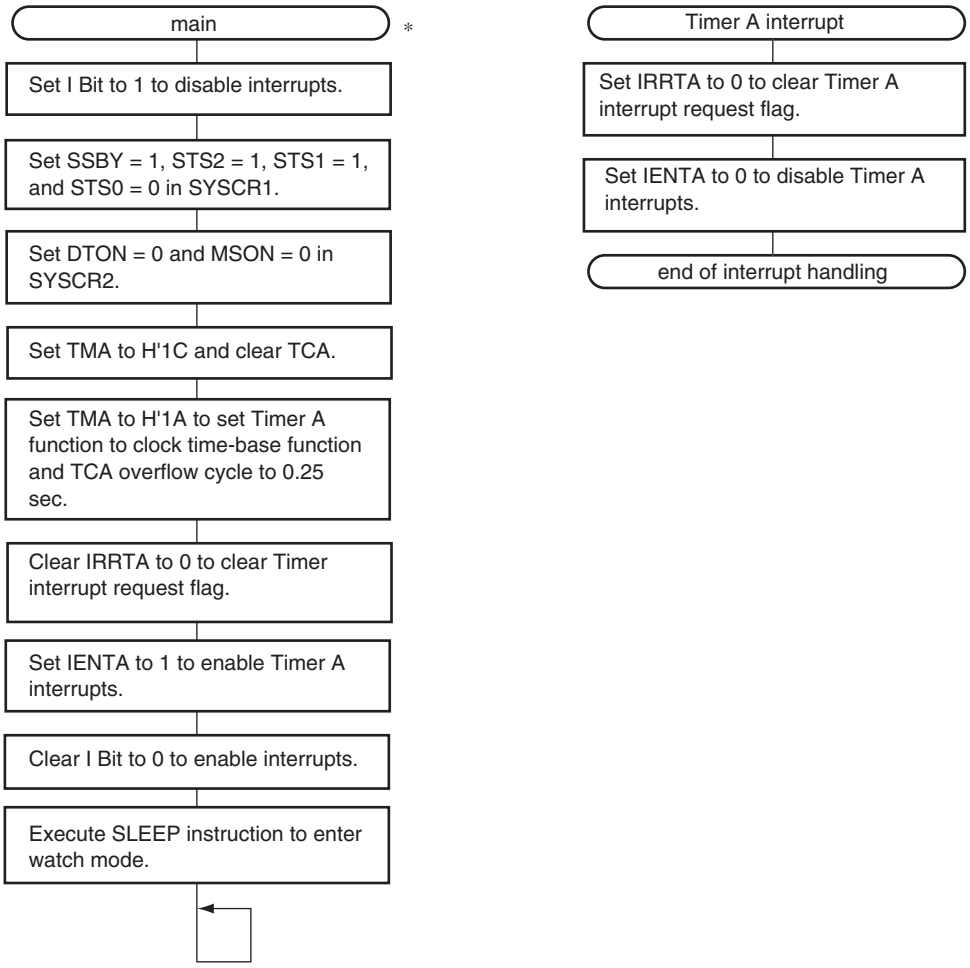
   Watch mode is terminated by an interrupt (IRQ0, WKP7 to WKP0, timer A, timer F and timer G) or by RES pin input.

   In the case of terminating the mode by an interrupt, the watch mode is terminated upon generation of a specific interrupt, and the system enters an operating mode according to the combination of the low-speed on-flag (LSON) in SYSCR1 and medium-speed on-flag (MSON) in system control register 2 (SYSCR2): high-speed active mode if LSON = 0 and MSON = 0, medium-speed active mode if LSON = 0 and MSON = 1, and subactive mode if LSON = 1. On transitions to active mode, after the time set by the STS2 to STS0 bits in SYSCR1 has elapsed, a stable clock signal is supplied to the entire LSI, and interrupt exception handling starts. When the I bit in CCR is 1 or when acceptance of the interrupt is disabled by the interrupt enable register, watch mode will not be terminated.

   In the case of terminating the mode by the input on the RES pin, if the RES pin is driven low, system clock oscillation is started. After the time for oscillation stabilization has elapsed, if the RES pin is driven high, the CPU starts reset exception handling. The system clock is supplied to the entire LSI as soon as the system clock oscillation is started. The RES pin must be held at the low level until the system clock oscillation stabilizes.

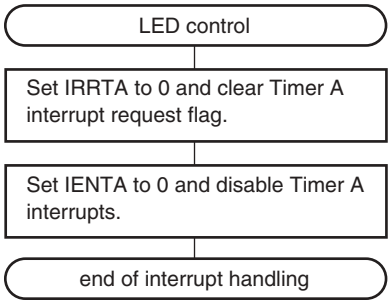
2. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer A interrupt handling routine



3. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'Oscillator Settling Time -8 States'                                                                                */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : Oscillator Settling Time                                                                                          */
/*                                                                                                                      */
/*  External Clock : 0.8KHz                                                                                             */
/*  Internal Clock : 0.4KHz                                                                                             */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     TMA         *(volatile unsigned char *)0xFFB0       /* Timer Mode Register A                */
#define     TCA         *(volatile unsigned char *)0xFFB1       /* Timer Counter A                      */
#define     SYSCR1      *(volatile unsigned char *)0xFFF0       /* System Control Register 1            */
#define     SYSCR1_BIT  (*(struct BIT *)0xFFF0)                 /* System Control Register 1            */
#define     SSBY        SYSCR1_BIT.b7                           /* Software Standby                     */
#define     STS2        SYSCR1_BIT.b6                           /* Standby Timer Select 2               */
#define     STS1        SYSCR1_BIT.b5                           /* Standby Timer Select 1               */
#define     STS0        SYSCR1_BIT.b4                           /* Standby Timer Select 0               */
#define     LSON        SYSCR1_BIT.b3                           /* Low Speed On Flag                    */
#define     MA1         SYSCR1_BIT.b1                           /* Active Mode Clock Select 1           */
#define     MA0         SYSCR1_BIT.b0                           /* Active Mode Clock Select 0           */
```

```
#define     SYSCR2      *(volatile unsigned char *)0xFFF1       /* System Control Register 2               */
#define     SYSCR2_BIT  (*(struct BIT *)0xFFF1)                 /* System Control Register 2               */
#define     NESEL       SYSCR2_BIT.b4                           /* Noise Elimination Sampling              */
                                                                /*                          Frequency Select */
#define     DTON        SYSCR2_BIT.b3                           /* Direct Transfer On Flag                 */
#define     MSON        SYSCR2_BIT.b2                           /* Middle Speed On Flag                    */
#define     SA1         SYSCR2_BIT.b1                           /* Subactive Mode Clock Select 1           */
#define     SA0         SYSCR2_BIT.b0                           /* Subactive Mode Clock Select 0           */
#define     IENR1_BIT   (*(struct BIT *)0xFFF3)                 /* Interrupt Enable Register 1             */
#define     IENTA       IENR1_BIT.b7                            /* Timer A Interrupt Enable                */
#define     IRR1_BIT    (*(struct BIT *)0xFFF6)                 /* Interrupt Request Register 1            */
#define     IRRTA       IRR1_BIT.b7                             /* Timer A Interrupt Request Flag          */

#pragma interrupt   (taint)
/************************************************************************************************************/
/*  Function define                                                                                         */
/************************************************************************************************************/
extern void INIT ( void );                                      /* SP Set                                  */
void        main ( void );
void        taint ( void );

/************************************************************************************************************/
/*  Vector Address                                                                                          */
/************************************************************************************************************/
#pragma section     V1                                          /* Vector Section Set                      */
void (*const VEC_TBL1[])(void) = {
    INIT                                                        /* 0x0000 Reset Vector                     */
};
#pragma section     V2                                          /* Vector Section Set                      */
void (*const VEC_TBL2[])(void) = {
    taint                                                       /* 0x0016 timer A  Interrupt Vector        */
};

#pragma section                                                 /* P                                       */
/************************************************************************************************************/
/*  Main Program                                                                                            */
/************************************************************************************************************/
void    main ( void )
{
    set_imask_ccr(1);                                           /* Interrupt Disable                       */

    SYSCR1 = 0xE7;                                              /* Set SYSCR1                              */
    SYSCR2 = 0xE0;                                              /* Set SYSCR2                              */

    TMA = 0x1C;                                                 /* Initialize TCA                          */
    TMA = 0x1A;                                                 /* Initialize TCA Overflow Period          */
    IRRTA = 0;                                                  /* Clear IRRTA                             */
    IENTA = 1;                                                  /* Timer A Interrupt Enable                */

    set_imask_ccr(0);                                           /* Interrupt Enable                        */

    sleep();                                                    /* Transition to Sleep Mode                */

    while(1){
        ;
    }
}
```

```
/*****************************************************************************************************************/
/*  Timer A Interrupt                                                                                            */
/*****************************************************************************************************************/
void    taint ( void )
{
    IRRTA = 0;                                          /* Clear IRRTA                          */
    IENTA = 0;
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'001A
CV3	H'0026
P	H'0100
B	H'FB80

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.03	—	First edition issued

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