
SH7231 Group

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Setting the SRAM Interface for Bus State Controller

Abstract

This application note describes an example to access an SRAM. The operation is achieved by using the function of the SRAM interface with byte selection equipped in the SH7231 bus state controller.

Products

SH7231

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1.	Specifications	3
2.	Operation Conditions.....	4
3.	Related Application Note.....	4
4.	Hardware.....	5
4.1	SRAM Specification	5
4.2	Pins Used.....	5
4.3	A Diagram for Reference	6
5.	Software	7
5.1	Operation Overview	7
5.2	Flowchart.....	7
5.2.1	Initial Setting for Bus State Controller.....	7
5.3	Timing Chart	8
6.	Sample Code.....	10
7.	Reference Documents.....	10

1. Specifications

Get SRAM accessed using the SRAM interface function with byte selection pin on the bus state controller. The SRAM of 2M bytes (1 Mwords x 16 bits) connects to the bus state controller in the bus width of 16 bits.

Table 1.1 lists the peripheral functions used and their applications. Figure 1.1 shows their memory map

Table 1.1 Peripheral Functions and Applications

Peripheral Function	Application
Bus state controller	Interface for connecting the SRAM with byte selection

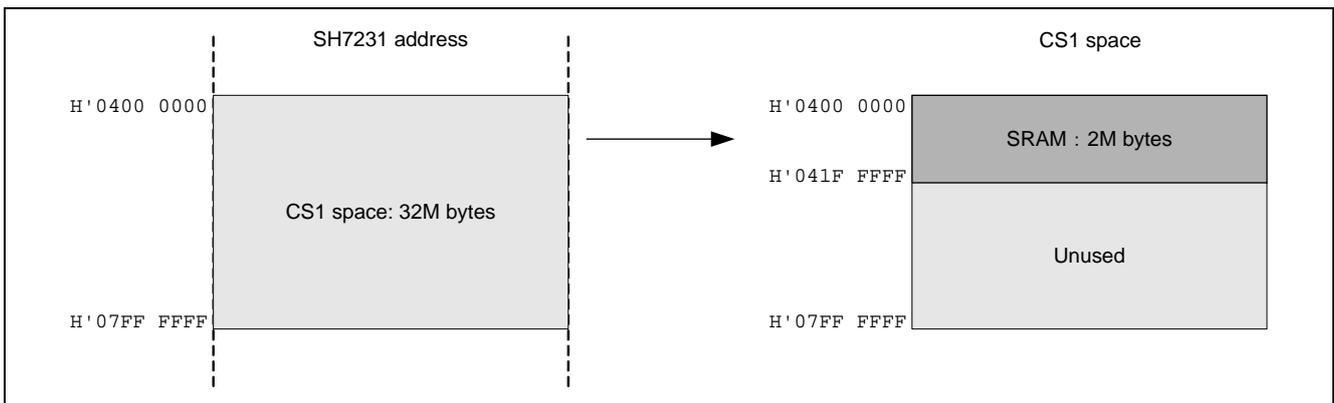


Figure 1.1 SRAM Memory Map

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operating Conditions

Item	Contents
MCU used	SH7231
Devices used	Renesas Electronics Corporation SRAM (model: R1LV1616RSA-7S)
Operating frequency	<ul style="list-style-type: none"> • CPU clock: 100MHz • Bus clock: 50MHz • Peripheral clock: 50MHz
Operating voltage	<ul style="list-style-type: none"> • Vcc: 3.3V • PVcc: 3.3V or 1.8V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Ver.4.08.00
C compiler	Renesas Electronics Corporation SuperH RISC engine family C/C++ compiler package V.9.04 Release 00 Compile options: -cpu=sh2afpu -fpu=single -include="\$(WORKSPDIR)\inc" -object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Operating mode	MCU expansion mode 2
Sample code version	1.00

3. Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- SH7231 Group Example of Initialization (document No.: R01AN0322EJ)
- SH7231 Group Setting the SDRAM Interface for Bus Controller (Document No.: R01AN0848EJ)

4. Hardware

4.1 SRAM Specification

Table 4.1 lists the specification of SRAM adopted in this application.

Table 4.1 SRAM Specification in the Application

Item	Description
Model	R1LV1616RSA-7S
Volume, Configuration	16M bits (1 Mwords x 16 bits) x 1
Data bus width	16 bits

4.2 Pins Used

Table 4.2 lists the pins used and their functions. All the pins are set to I/O ports by default. The change for pin function by the pin function controller is required. This application uses the SRAM interface function with byte selection, therefore the BAS bit in the CS1 space wait control register (CS1WCR) is set to 1.

Table 4.2 Pins Used and their Function

Pin Name	I/O	Function
A20 to A1	Output	Address pass
D15 to D0	Input	Data bus
$\overline{\text{CS1}}$	Output	Chip select 1
$\overline{\text{RD/WR}}$	Output	Write enable
$\overline{\text{RD}}$	Output	Read pulse signal (read data output enable)
$\overline{\text{WRH}}$	Output	Selection for upper byte in data bus (D15 to D8)
$\overline{\text{WRL}}$	Output	Selection for lower byte in data bus (D7 to D0)

4.3 A Diagram for Reference

Figure 4.1 shows the sample connection to the SRAM.

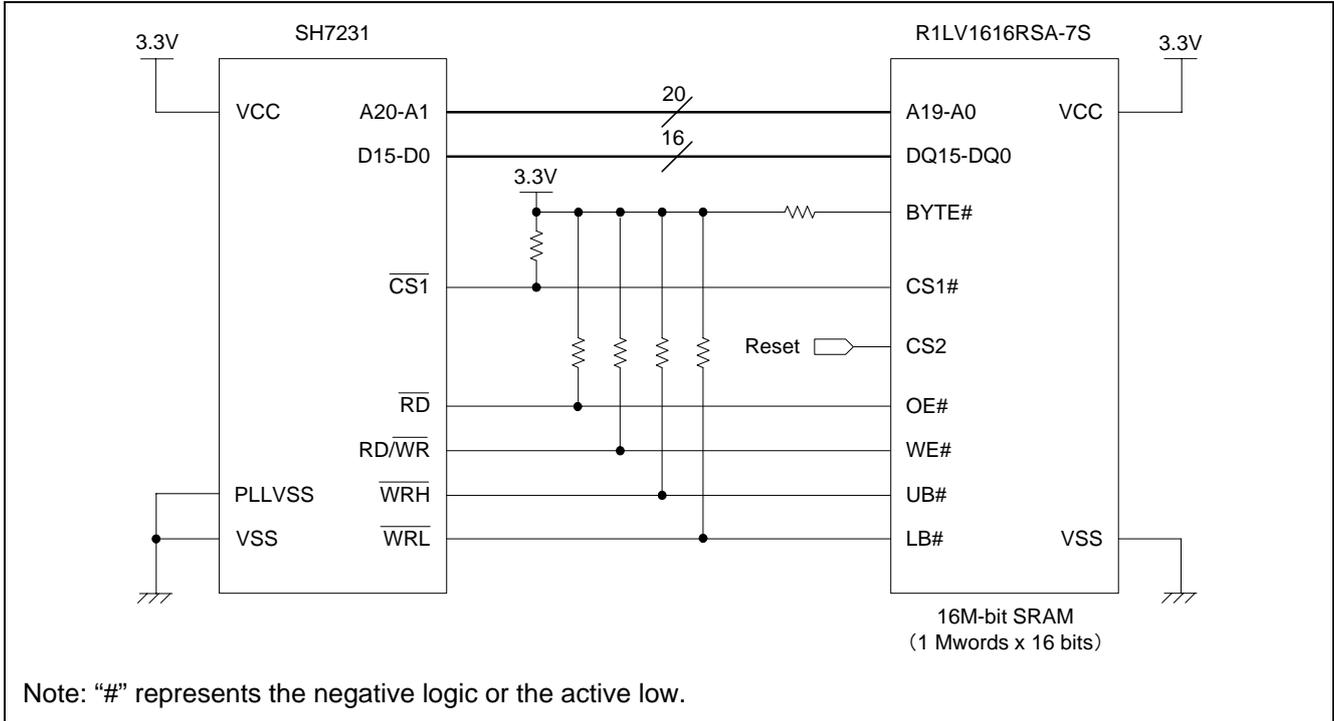


Figure 4.1 Connection to SRAM

5. Software

5.1 Operation Overview

The sample code sets the bus state controller before executing the main function, and sets the interface with the SRAM with byte selection. The main function carries out no processing but the processing of the endless loop. Therefore this chapter describes only the initial setting for the bus state controller.

5.2 Flowchart

5.2.1 Initial Setting for Bus State Controller

Figure 5.1 shows the procedure for initializing the bus state controller.

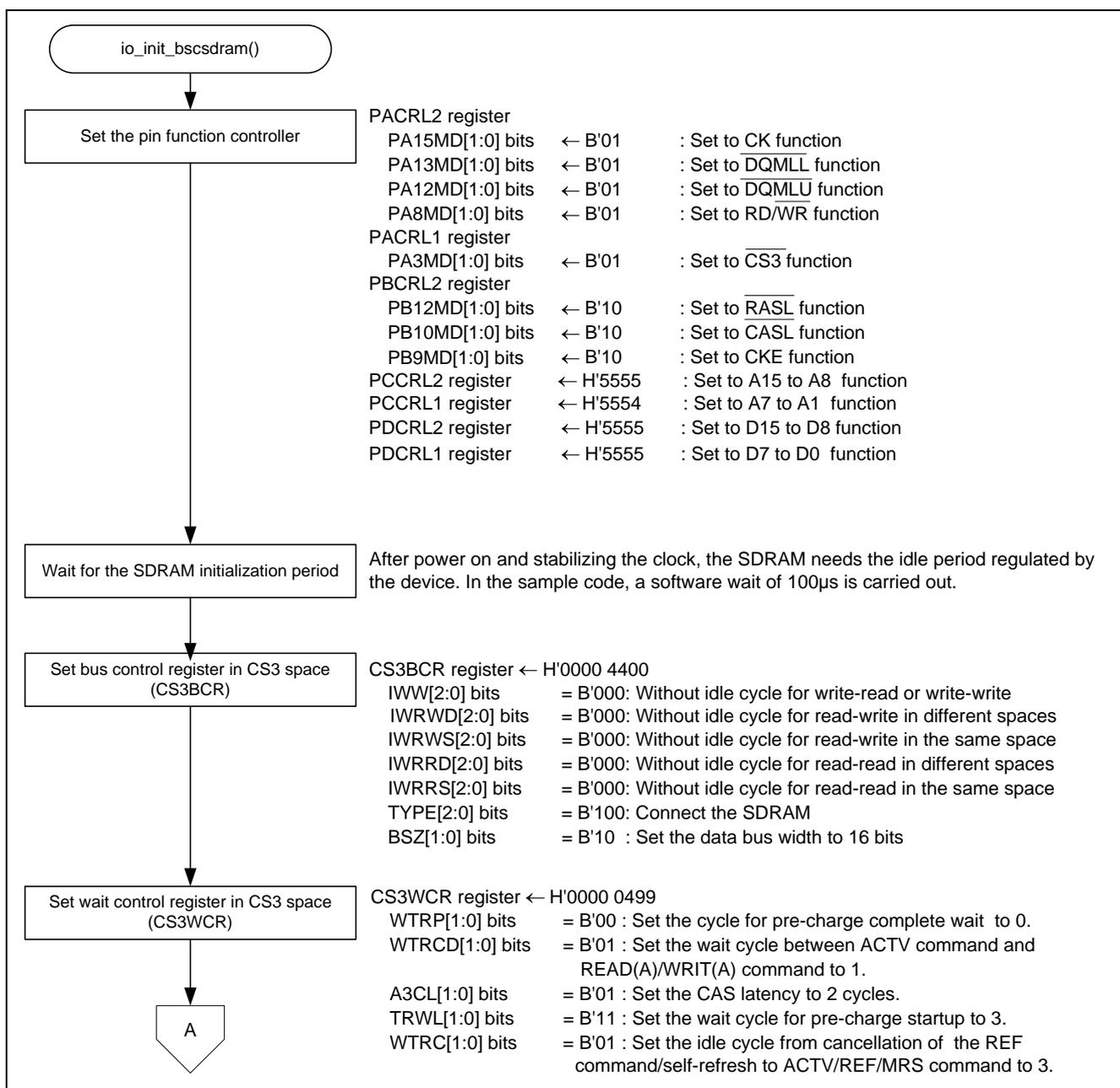


Figure 5.1 Initial Setting for Bus State Controller

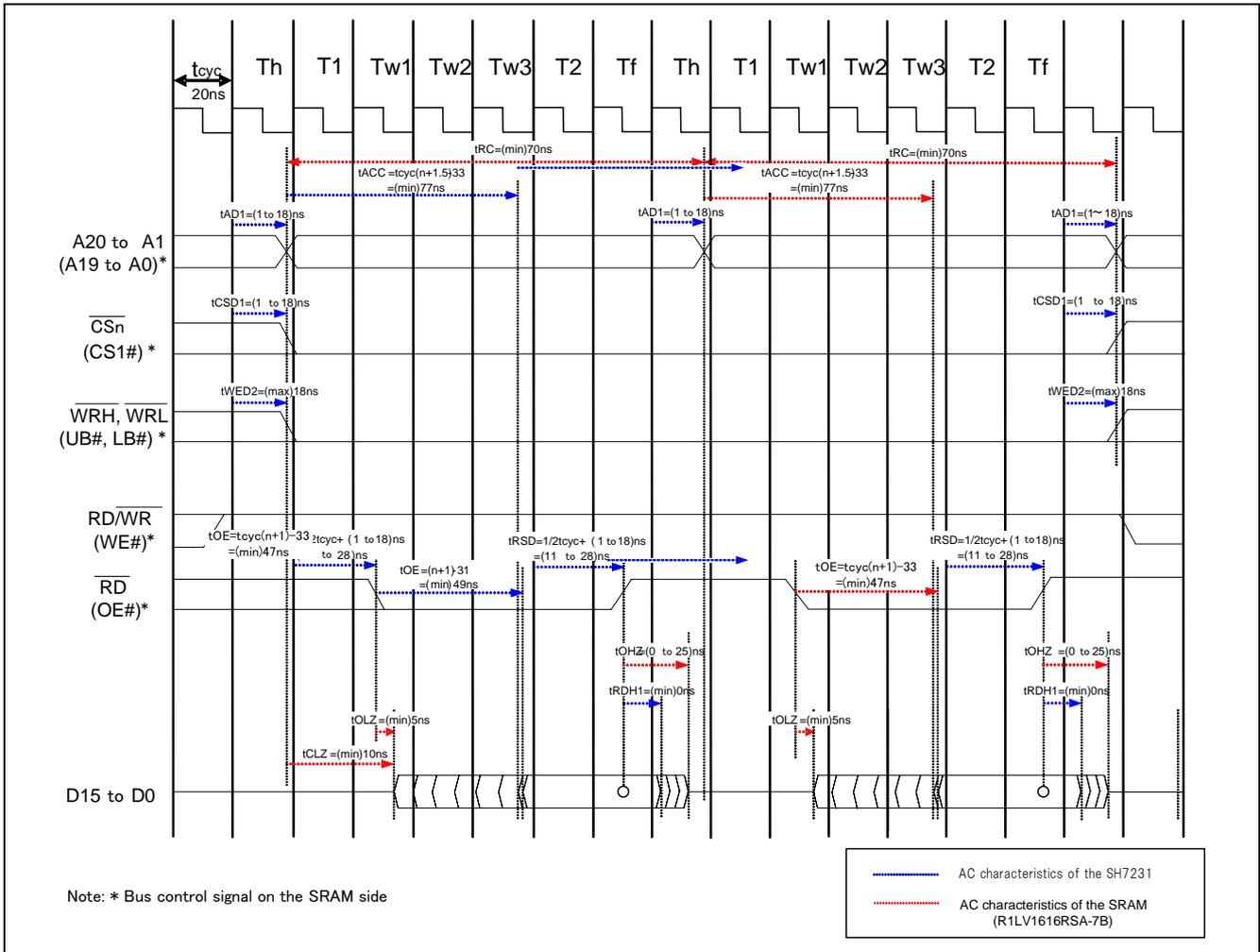


Figure 5.3 Read-read Access Timing with t_{ACC} and t_{OE}

[Remarks] Specification of t_{OE} set up timing for the data signal when reading

The SH-2/SH-2A series products with the general flash ROM (including this MCU) prescribes two times besides the read data set up time as t_{RDS} for the data set up timing when reading the general external memory. Refer to the following.

- Read data access time (t_{ACC})
- Access time from read strobe (t_{OE})

Design the read timing to fulfill the following relationship at the same time along with the specification in the t_{ACC} and t_{OE} . In this case, the prescription in the t_{PDS} does not need to be considered.

- The address access time on the SRAM side $t_{AA}^* (\max) \leq t_{ACC} (\min)$ on the MCU side.
- The access time from the read strobe on the SRAM side $t_{OE}^* (\max) \leq t_{OE} (\min)$ on the MCU side.

When designing the read timing to fulfill the prescription in the t_{PDS} , the above mentioned prescription on the MCU as t_{ACC} and t_{OE} do not need to be considered.

Note: "*" is the symbol which represents the timing prescription on the SRAM (R1LV1616RSA-7S) side used in this application.

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

Hardware Manual

SH7231 Group User's Manual: Hardware Rev.1.00

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest version can be downloaded from the Renesas Electronics website

Development Tool Manual

SuperH C/C++ Compiler Package V.9.04 User's Manual Rev.1.01

The latest version can be downloaded from the Renesas Electronics website.

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Revision History	SH7231 Group Application Note Bus State Controller SRAM Interface Setting
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Rev.	Date	Description	
		Page	Summary
1.00	Dec. 28, 2011	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

— The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flow internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

— The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

— The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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