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Serial Interface Transmit/Receive Using DMAC

1. Abstract

This document describes how to perform serial communication using DMAC.

2. Introduction

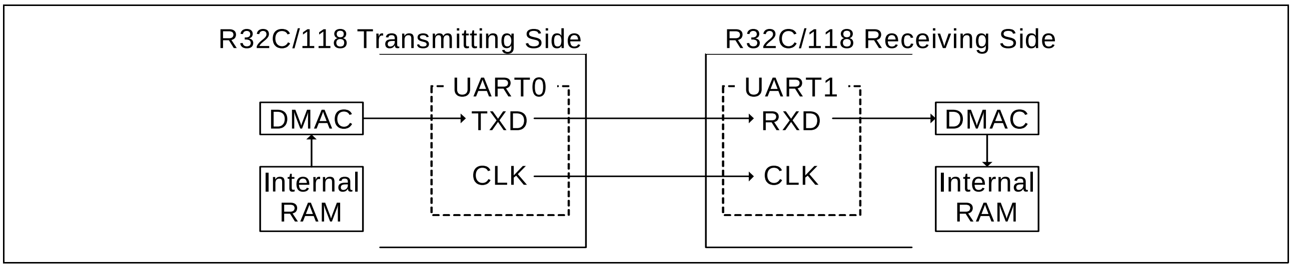
The application described in this document applies to the following MCU:

- MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Overview

This document describes an example of using DMA to write to the transmit buffer and read from the receive buffer. No CPU instructions are used, and multiple bytes are transmitted/received through the serial interface.



3.1 Connections

In this document, UART0 and UART1 of the same MCU are connected outside of the MCU to perform transmit and receive operations in clock synchronous serial interface mode. Connections described in this document are shown in the figure below.

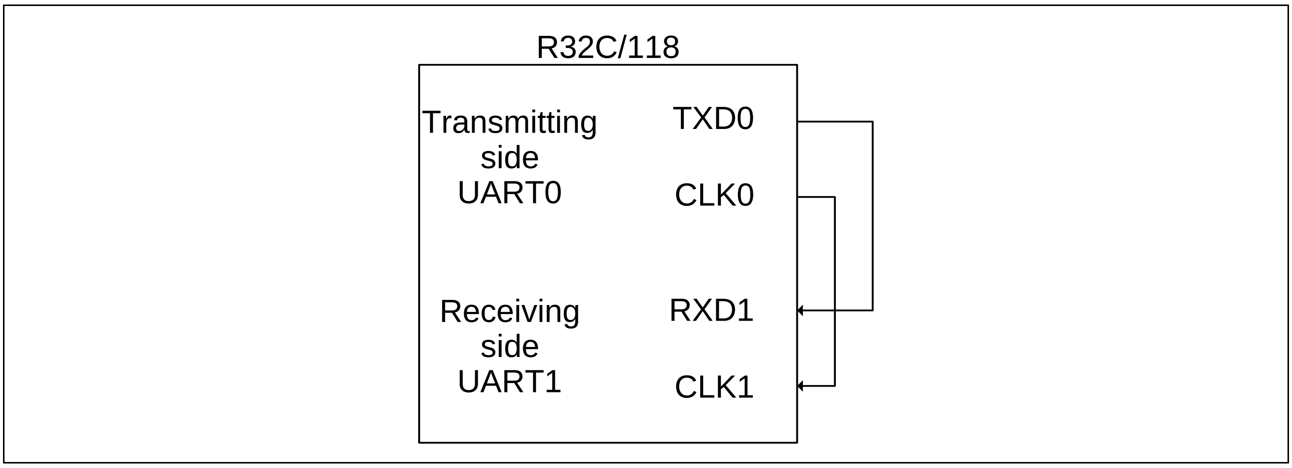


Figure 3.1 Connections Used in this Document

3.2 Operations

In this example, DMAC and UART are used to transfer 8 bytes of data (see **Figure 3.2**). Numbers in parenthesis ((1) to (5)) indicate the order of the data transfer.

- Transmitting Side
  1. (1) Write the first byte of data to be transmitted to the UART0 transmit buffer register.
  2. (2) Data written to the UART0 transmit buffer register is transmitted in clock synchronous serial interface mode through the TXD0 pin. When the first bit of data is transmitted, a UART0 transmit interrupt request is generated.
  3. (3) When a UART0 transmit interrupt request is generated, DMA0 reads the transmit data in the internal RAM address (specified by the DMA0 source address register), and writes it to the UART0 transmit buffer register (specified by the DMA0 destination address register). At the same time, the value in the DMA0 source address register is incremented, and the value in the DMA0 terminal count register is decremented.

- Receiving Side
  4. (4) When 1 byte of data is received through the RXD1 pin (in clock synchronous serial interface mode), a UART1 receive interrupt request is generated.
  5. (5) When a UART1 receive interrupt request is generated, DMA1 reads the received data in the UART1 receive buffer register (specified by the DMA1 source address register), and writes it to the internal RAM address (specified by the DMA1 destination address register). At the same time, the value in the DMA1 destination address register is incremented, and the value in the DMA1 terminal count register is decremented.

Repeat steps (2) to (5) until either the DMA0 terminal count register or DMA1 terminal count register becomes 0.

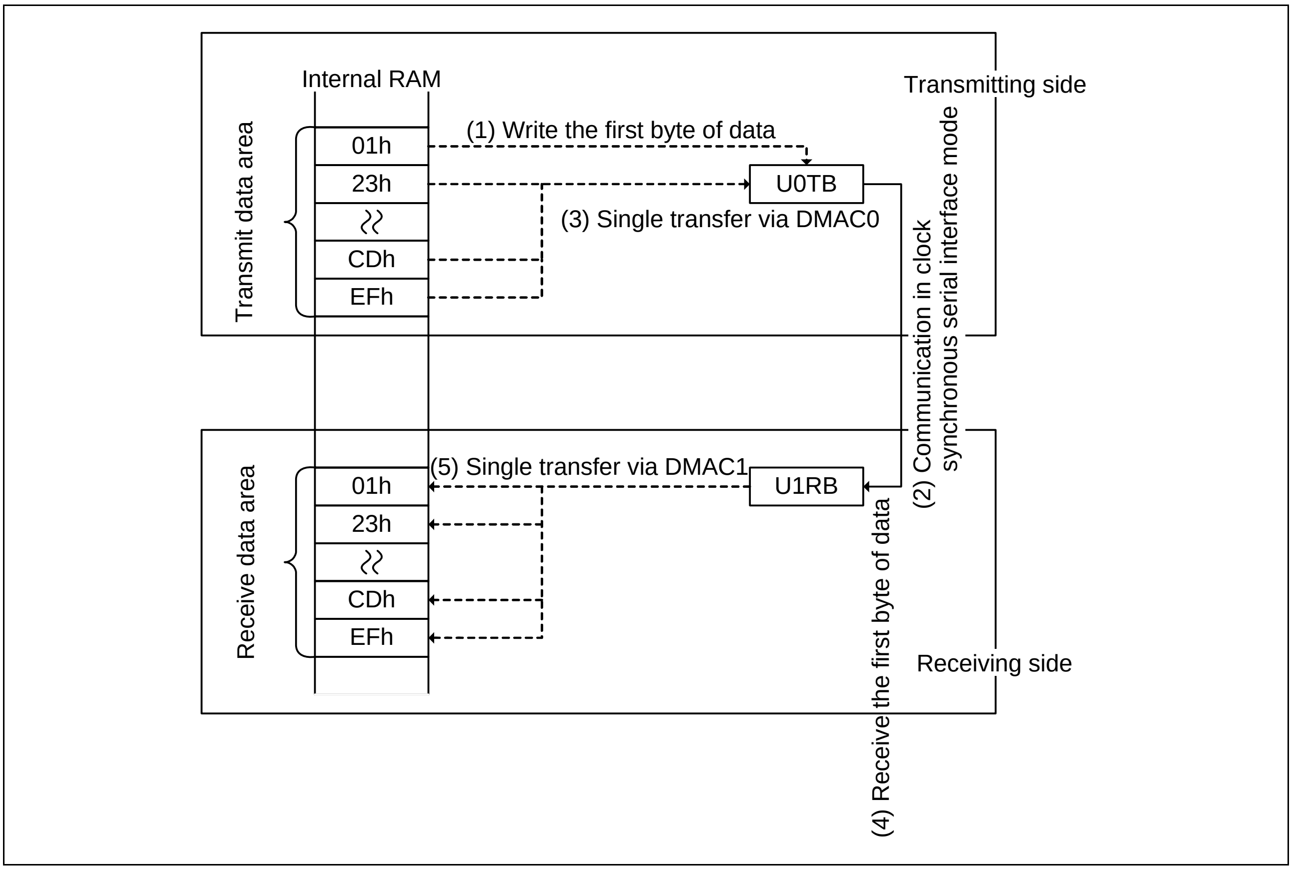


Figure 3.2 DMAC and UART Operation

4. Settings

This section describes the settings for serial communication using DMAC. Settings for each function are explained below. The tables below show the settings for the clock frequency, DMAC, and serial I/O, respectively.

Table 4.1 Clock Frequency Settings

Clock	Frequency
Main clock	16 MHz
PLL clock	100 MHz
Base Clock	50 MHz
CPU clock	50 MHz
Peripheral bus clock	25 MHz
Peripheral function clock source	25 MHz

Table 4.2 DMAC Settings

Item	Transmitting Side	Receiving Side
DMAC channel	DMA0	DMA1
Transfer mode	Single transfer	
Transfer size	8-bit	
DMA start source	UART0 transmit interrupt request	UART1 receive interrupt request
Transfer source update	Updated	Not updated
Transfer destination update	Not updated	Updated
Number of transfers	7	8

Table 4.3 Serial I/O Settings

Item	Transmitting Side	Receiving Side
UART channel	UART0	UART1
Operating mode	Clock synchronous serial interface mode	
Transmit/Receive clock	Internal clock	External clock
UiBRG (i = 0 to 8)	f8 = 3.125 MHz	—
Transmit clock frequency	6.25 kHz	—
Continuous receive mode	—	Enabled
CTS/RTS function	Disabled	Disabled
CLK polarity	Outputs transmit data synchronized with the falling edge or the transmit/receive clock.	Inputs received data synchronized with the rising edge of the transmit/ receive clock.
Bit order	LSB first	LSB first
Data logic switch	Not inverted	Not inverted
Interrupt request source	No data present in U0TB register	Data present in U1RB register
Port P6_1	CLK0 output	—
Port P6_3	TXD0 output	—
Port P6_5	—	CLK1 input
Port P6_6	—	RXD1 input

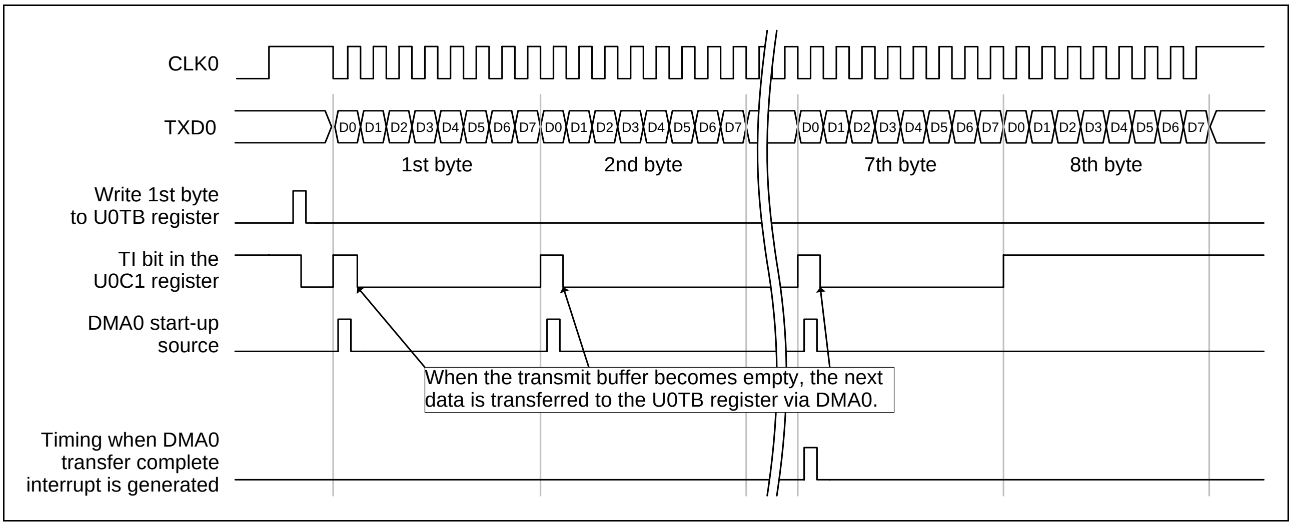


Figure 4.1 Continuous Transmit Timing Diagram

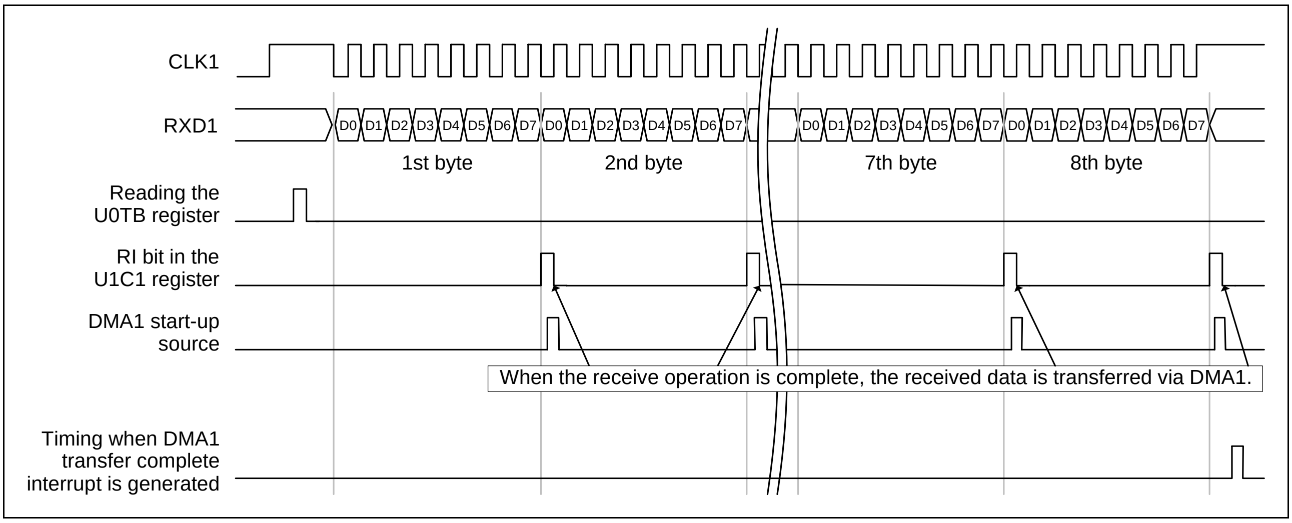


Figure 4.2 Continuous Receive Timing Diagram

4.1 Notes on Settings

4.1.1 Accessing DMAC Registers

Some of the DMAC registers in the R32C/100 Series MCUs are allocated to the CPU address space. By declaring “#pragma DMAC” in the R32C/100 Series C compiler, DMAC associated registers in the CPU can be accessed by allocating them to external variables.

The statement is as follows: #pragma DMAC function name DMAC register name

However, functions to be specified must be declared before stating “#pragma DMAC”.

- Specifiable DMAC registers and variable types are listed in the following table.

Table 4.4 Specifiable DMAC Registers and Variable Types (i = 0 to 3)

Symbol	Register	Variable Type
DMD0 to DMD3	DMAi Mode Register	unsigned long
DCT0 to DCT3	DMAi Terminal Count Register	
DCR0 to DCR3	DMAi Terminal Count Reload Register	
DSA0 to DSA3	DMAi Source Address Register	far pointer to an arbitrary type. However, a pointer to a function is not possible.
DSR0 to DSR3	DMAi Source Address Reload Register	
DDA0 to DDA3	DMAi Destination Address Register	
DDR0 to DDR3	DMAi Destination Address Reload Register	

- Multiple “#pragma DMAC” cannot be stated to the same DMAC register.
- Functions specified by “#pragma DMAC” cannot be specified by “&” (address operator), “( )” (function-call operator), “[ ]” (array subscript operator), or “- >” (member operator).

The following figure shows “#pragma DMAC” usage.

```
void    _far*dda0  ;
#pragma   DMAC   dda0   DDA0

void func(void)
{
        unsigned char buff[10] ;
        dda0 = buff ;
}
```

Figure 4.3 #pragma DMAC Usage

4.1.2 Transmit Block Frequency

If the UiBRG register count source is fx, and the UiBRG setting value is n, then the transmit block frequency is $\frac{fx}{2} \times (n+1)$

In this example, by setting the peripheral clock frequencies to (f1) = 25 MHz, fx(f8) = 3.125 MHz, and *n = 249*, the transmit clock frequency is:

$\frac{3.125}{2} \times (249+1)$ = 0.00625 MHz = 6.25 KHz

The following table shows the setting values for registers related to the transmit clock frequency.

Table 4.5 Settings Values for Transmit Clock Frequency Related Registers

Register	Bit	Value
U0MR	CKDIR	0 (internal clock)
U0C0	CLK1 to CLK0	01b (f8)
U0BRG	—	249

4.1.3 Pins

Set the corresponding port direction register to select each I/O direction of ports used as pins CLK0, CLK1, TXD0, and RXD1. Each bit in the port direction register corresponds to an individual pin. The following table shows the ports used in this application note, their corresponding port direction register bits, and the setting values.

Ports, Their Direction Registers, and Setting Values

Port	Bit in the Port Direction Register	I/O Direction	Value
P6_1	PD6_1	Output	1
P6_3	PD6_3	Output	1
P6_5	PD6_5	Input	0
P6_6	PD6_6	Input	0

Furthermore, set the function select register when using the UART0 signal output as a peripheral function. The following table shows ports used as output pins, their corresponding function select registers, and the setting values.

Table 4.6 Output Ports, Their Corresponding Function Select Registers, and Setting Values

Output Port	Function Select Register	Output Function	Value
P6_1	P6_1S	CLK0 is output	03h
P6_3	P6_3S	TXD0 is output	03h

4.2 Transmit Settings

The following figure shows how to set serial transmit using DMAC. Refer to section **4.4 "Detailed Settings"** for details on each item.

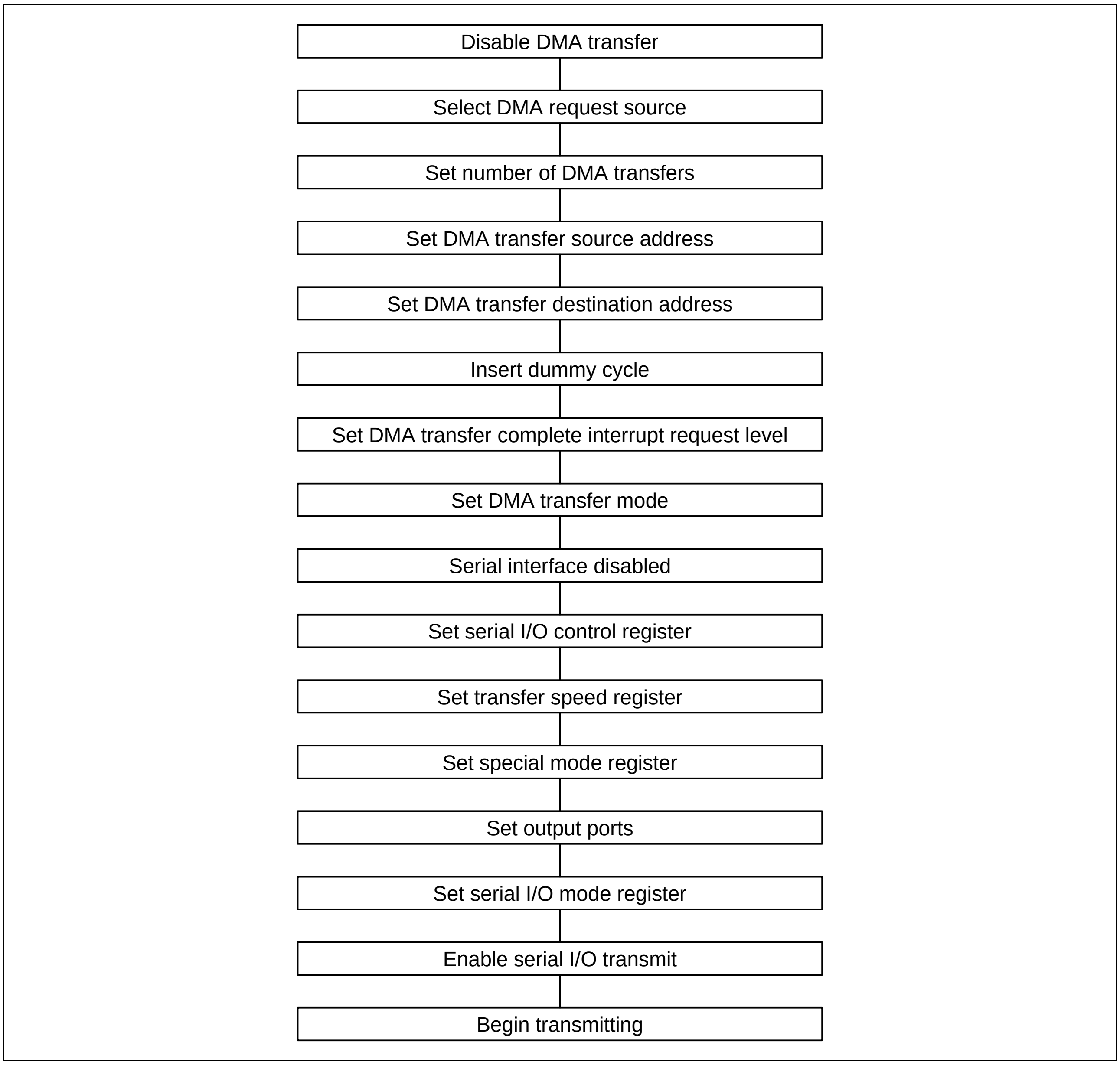


Figure 4.4 Serial Transmit Using DMAC

4.3 Continuous Receive Settings

The following figure shows how to set serial receive using DMAC. Refer to section **4.4 "Detailed Settings"** for more details on each item.

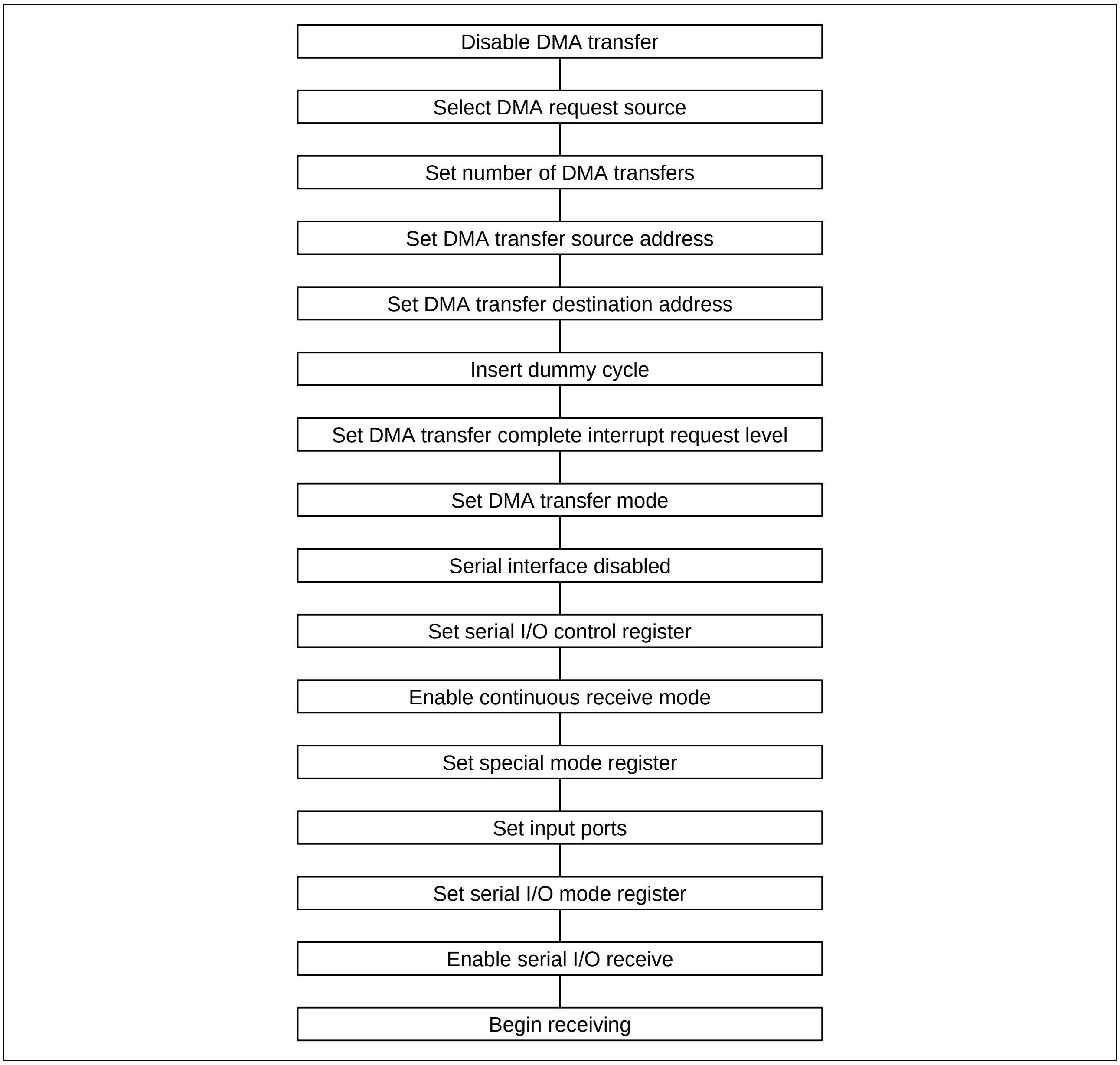


Figure 4.5 Receiving Side of Multi UART Transmit/Receive Using DMAC

4.4 Detailed Settings

Detailed settings mentioned in sections **4.2 "Transmit Settings"** and **4.3 "Continuous Receive Settings"** are below.

(1) Disable DMA transfer.

b31 b24 b23 b16 b15 b8 b7 b0

b7 b0
0 0

DMA0 Mode Register (DMD0) (Transmitting Side)
DMA1 Mode Register (DMD1) (Receiving Side)

MD01 to MD00	Transfer Mode Select Bit 00b: DMA transfer disabled	
b7 to b6	Set to 0.	
b31 to b8	Set to 0.	

Note:
1. When setting the DMAC register, set bits MD01 to MD00 to 00b (DMA transfer disabled). Then set these bits to 01b (single transfer) or 11b (repeat transfer).

(2) Select the DMA request source.

b7 b0
0 1 1 1 0

DMA0 Request Source Select Register (DM0SL) (Transmitting Side)

DSEL4 to DSEL0	DMA Request Source Select Bit 01110b: UART0 transmit interrupt request
b7 to b5	Set to 0.

b7 b0
1 0 0 0 1

DMA1 Request Source Select Register (DM1SL) (Receiving Side)

DSEL4 to DSEL0	DMA Request Source Select Bit 10001b: UART1 receive interrupt request
b7 to b5	Set to 0.

b7 b0
0 0 0 0 0 0

DMA0 Request Source Select Register 2 (DM0SL2) (Transmitting Side)
DMA1 Request Source Select Register 2 (DM1SL2) (Receiving Side)

DSEL24 to DSEL20	DMA Request Source Select Bit 00000b: Software trigger
DSR	Software DMA Transfer Request Bit When a software trigger is selected, a DMA transfer request is generated by setting this bit to 1
b7 to b6	Set to 0.

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(3) Set number of DMA transfers.

b31–b24	b23–b0
00h	000007h

DMA0 Terminal Count Register (DCT0) (Transmitting Side)
DMA1 Terminal Count Register (DCT1) (Receiving Side)

- b23–b0: Set number of transfers.
- b31–b24: Set to 00h.

Note:
1. After setting the DCT register to 000000h, even if a DMA transfer is requested, data is not transferred.

(4) Set DMA transfer source address.

b31–b24	b23–b16	b15–b8	b7–b0

DMA0 Source Address Register (DSA0) (Transmitting Side)
DMA1 Source Address Register (DSA1) (Receiving Side)

- Set a source address

(5) Set DMA transfer destination address.

b31–b24	b23–b16	b15–b8	b7–b0

DMA0 Destination Address Register (DDA0) (Transmitting Side)
DMA1 Destination Address Register (DDA1) (Receiving Side)

- Set a destination address

(6) Insert a dummy cycle.
After setting the DM0SL register (transmitting side) or DM1SL register (receiving side), wait six clocks of BCLK before enabling DMA transfer.

(7) Select the DMA transfer complete interrupt request level.

b7							b0
X	X	X	X	0	1	1	1

Interrupt Control Register (DM0IC) (Transmitting Side)
Interrupt Control Register (DM1IC) (Receiving Side)

- ILVL2 to ILVL0: Interrupt Request Level Select Bit
  - 111b: Level 7
- IR (1): Interrupt Request Flag
  - 0: Interrupt not requested
  - 1: Interrupt requested
- b7 to b4: Set to 0.

Note:
1. Set this bit to 0.

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(8) Set the DMA transfer mode.

DMA0 Mode Register (DMD0) (Transmitting Side)

b7 – b0: X X 0 1 0 0 0 1 (b31 to b8: X)

Bit	Function	Setting
MD01 to MD00 (1)	Transfer Mode Select Bit	01b: Single transfer
BW01 to BW00 (2)	Transfer Size Select Bit	00b: 8-bit
USA0	Source Addressing Mode Select Bit	1: Incrementing addressing
UDA0	Destination Addressing Mode Select Bit	0: Non-incrementing addressing
b7 to b6		Set to 0.
b31 to b8		Set to 0.

DMA1 Mode Register (DMD1) (Receiving Side)

b7 – b0: X X 1 0 0 0 0 1 (b31 to b8: X)

Bit	Function	Setting
MD11 to MD10 (1)	Transfer Mode Select Bit	01b: Single transfer
BW11 to BW10 (2)	Transfer Size Select Bit	00b: 8-bit
USA1	Source Addressing Mode Select Bit	0: Non-incrementing addressing
UDA1	Destination Addressing Mode Select Bit	1: Incrementing addressing
b7 to b6		Set to 0.
b31 to b8		Set to 0.

Notes:
1. Do not set these bits to 10b.
2. Do not set these bits to 11b.

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(9) Disable the serial interface.

b7							b0
					0	0	0

UART0 Transmit/Receive Mode Register (U0MR) (Transmitting Side)
UART1 Trnasmit/Receive Mode Register (U1MR) (Receiving Side)

- SMD2 to SMD0 — Serial Interface Mode Select Bit
  000b: Serial Interface disabled

(10) Set the serial I/O control register.

b7							b0
0	0	0	1		0	0	1

UART0 Transmit/Receive Control Register 0 (U0C0) (Transmitting Side)

- CLK1 to CLK0 (1) — U0BRG Count Source Select Bit
  01b: f8 selected
- Set to 0.
- TEXPT — Transmit Shift Register Empty Flag
  Read only bit
- CRD — CTS Disable Bit
  1: CTS disabled
- Set to 0.
- CKPOL — CLK Polarity Select Bit
  0: Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge
- UFORM — Bit Order Select Bit
  0: LSB first

b7							b0
0	0	0	1		0	0	0

UART1 Transmit/Receive Control Register 1 (U1C0) (Receiving Side)

- CLK1 to CLK0 (1) — U1BRG Count Source Select Bit
  00b: f1 selected
- Set to 0.
- TEXPT — Transmit Shift Register Empty Flag
  Read only bit
- CRD — CTS Disable Bit
  1: CTS disabled
- Set to 0.
- CKPOL — CLK Polarity Select Bit
  0: Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge
- UFORM — Bit Order Select Bit
  0: LSB first

Note:
1. Do not set these bits to 11b.

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(11) Set the serial I/O control register.

UART0 Transmit/Receive Control Register 1 (U0C1) (Transmitting Side)

b7							b0
0	0	0	0		0		0

b0	TE	Transmit Enable Bit 0: Transmission disabled
b1	TI	Transmit Buffer Empty Flag Read only bit
b2	RE	Receive Enable Bit 0: Reception disabled
b3	RI	Receive Complete Flag Read only bit
b4	U0IRS	UART0 Transmit Interrupt Source Select Bit 0: U0TB register is empty (TI = 1)
b5	U0RRM	UART0 Continuous Receive Mode Enable Bit 0: Continuous receive mode disabled
b6	U0LCH	Logical Inversion Select Bit 0: Data non logic-inverted
b7		Set to 0.

UART1 Transmit/Receive Control Register 1 (U1C1) (Receiving Side)

b7							b0
0	0	1			0		0

b0	TE	Transmit Enable Bit 0: Transmission disabled
b1	TI	Transmit Buffer Empty Flag Read only bit
b2	RE	Receive Enable Bit 0: Reception disabled
b3	RI	Receive Complete Flag Read only bit
b5	U1RRM	UART1 Continuous Receive Mode Enable Bit 1: Continuous receive mode enabled
b6	U0LCH	Logical Inversion Select Bit 0: Data non logic-inverted
b7		Set to 0.

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(12) Set the transfer speed.

b7 b0
249 — **UART0 Transfer Speed Register (U0BRG)**

249: Divided by 250

(13) Set the special mode registers. Set the following registers to 00h:
U0SMR (UART0 Special Mode Register), U0SMR2 (UART0 Special Mode Register 2)
U0SMR3 (UART0 Special Mode Register 3), U0SMR4 (UART0 Special Mode Register 4),
U1SMR (UART1 Special Mode Register), U1SMR2 (UART1 Special Mode Register 2),
U1SMR3 (UART1 Special Mode Register 3), U1SMR4 (UART1 Special Mode Register 4)

(14) Set the I/O ports.

b7 b0
_ 0 0 _ 1 _ 1 _ — **Port P6 Direction Register (PD6)**

PD6_1 — Port P6_1 Direction Bit
1: Output port

PD6_3 — Port P6_3 Direction Bit
1: Output port

PD6_5 — Port P6_5 Direction Bit
0: Input port

PD6_6 — Port P6_6 Direction Bit
0: Input port

b7 b0
X _ X X X 0 1 1 — **Port P6_1 Function Select Register (P6_1S)**

PSEL2 to PSEL0 — Port P6_1 Output Function Select Bit
011b: CLK0 is output

Set to 0.

NOD — N-channel Open Drain Output Select Bit
0: Push-pull output
1: N-channel open drain output

Set to 0.

b7 b0
X _ X X X 0 1 1 — **Port P6_3 Function Select Register (P6_3S)**

PSEL2 to PSEL0 — Port P6_3 Output Function Select Bit
011b: TXD0 is output

Set to 0

NOD — N-channel Open Drain Output Select Bit
0: Push-pull output
1: N-channel open drain output

Set to 0

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(15) Set the serial I/O mode registers.

b7 b0
0	0	0	0	0	0	0	1

UART0 Transmit/Receive Mode Register (U0MR) (Transmitting Side)

- SMD2 to SMD0 — Serial Interface Mode Select Bit
  - 001b: Clock synchronous serial interface mode
- CKDIR — Internal/External Clock Select Bit
  - 0: Internal clock
- Set to 0.

b7 b0
0	0	0	0	1	0	0	1

UART1 Transmit/Receive Mode Register (U1MR) (Receiving Side)

- SMD2 to SMD0 — Serial Interface Mode Select Bit
  - 001b: Clock synchronous serial interface mode
- CKDIR — Internal/External Clock Select Bit
  - 1: External clock
- Set to 0.

(16) Enable serial I/O transmission.

b7 b0
0							1

UART0 Transmit/Receive Control Register 1 (U0C1) (Transmitting Side)

- TE — Transmit Enable Bit
  - 1: Transmit enabled
- Set to 0.

(17) Enable serial I/O reception.

b7 b0
0					1		1

UART1 Transmit/Receive Control Register (U1C1) (Receiving side)

- TE — Transmit Enable Bit
  - 1: Transmit enabled
- RE — Receive Enable Bit
  - 1: Receive enabled
- Set to 0.

(18) Start transmission.
Transmission starts after writing the first byte of continuous transmit data to the U0TB register. Thereafter, data is continuously transmitted to the U0TB register via DMA0.

(19) Start reception.
Reception starts after reading the U1RB register.

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.

5.1 Explanation

In the sample program, the transmitting side uses UART0 in clock synchronous serial interface mode to perform seriaol communication, with DMA0 to write transmit data (except the first byte of data) to the transmit buffer register.

The receiving side uses UART1 in clock synchronous serial interface mode, with DMA1 to read received data from the receive buffer register.

Both DMA0 and DMA1 operate in single transfer mode. When all data is transferred, a DMA transfer complete interrupt is generated.

The following table shows the content of the DMAC channel transfer complete interrupt process.

Table 5.1 DMAC Channel Transfer Complete Interrupt Process

DMAC Channel	DMA Transfer Complete Interrupt Process
DMAC0	Set the P0_0 bit to 1.
DMAC1	Set the P0_1 bit to 1.

5.2 Program Flow

The sample program is comprised of a main function, DMAC and a UART transmit initialization function, DMAC and a UART receive initialization function, and a transfer complete interrupt function for each DMAC channel.

The following pages contain flowcharts regarding the above program flow. Numbers in parenthesis ((1) to (20)) correspond to program flow numbers.

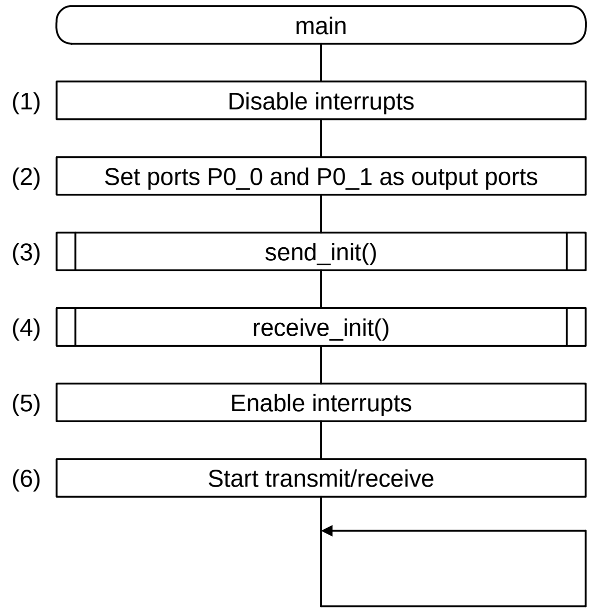

Figure 5.1 Main Function Flowchart

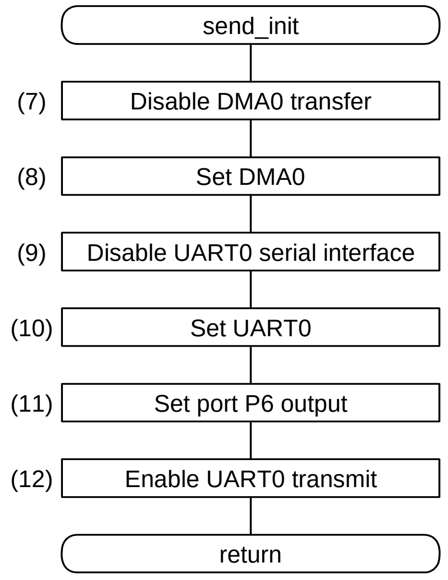

Figure 5.2 DMAC and UART Transmit Initialization Function

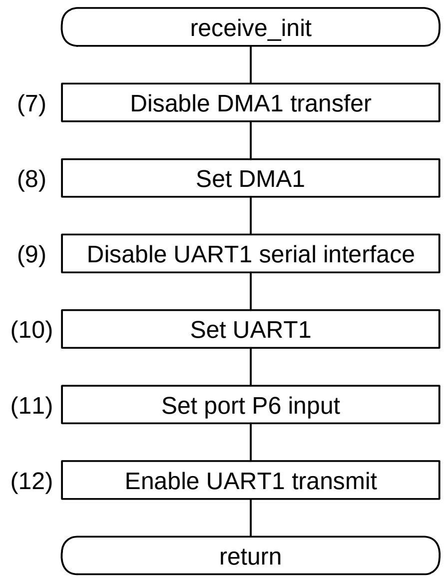

Figure 5.3 DMAC and UART Receive Initialization Function

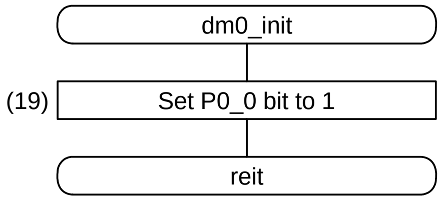

Figure 5.4 DMA0 Transfer Complete Interrupt Function

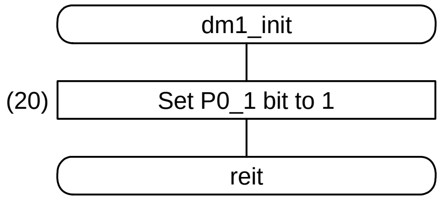

Figure 5.5 DMA1 Transfer Complete Interrupt Function

6. Reference Documents

Hardware Manual
R32C/118 Group Hardware Manual Rev.1.00
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual
R32C/100 Series C Compiler Package Ver. 1.02 Compiler User’s Manual Rev. 1.00
The latest version can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http:/www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	Serial Interface Transmit/Receive using DMAC

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 12, 2010	—	Initial release

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