1. Abstract

This document describes a method for receiving data from an external device synchronized with the internal clock using synchronous serial interface mode.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

This application note can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above groups. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Application Example

This document describes the setting procedure for receiving data using synchronous serial interface mode (UART3). Table 3.1 and Table 3.2 list the Clock Frequency Settings and Setting Conditions for Data Reception Using Synchronous Serial Interface Mode, respectively.

### Table 3.1 Clock Frequency Settings

<table>
<thead>
<tr>
<th>Clock</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main clock</td>
<td>16 MHz</td>
</tr>
<tr>
<td>PLL clock</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Base clock</td>
<td>50 MHz</td>
</tr>
<tr>
<td>CPU clock</td>
<td>50 MHz</td>
</tr>
<tr>
<td>Peripheral bus clock</td>
<td>25 MHz</td>
</tr>
<tr>
<td>Peripheral function clock source</td>
<td>25 MHz</td>
</tr>
</tbody>
</table>

### Table 3.2 Setting Conditions for Data Reception Using Synchronous Serial Interface Mode

<table>
<thead>
<tr>
<th>Item</th>
<th>Setting Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Character length</td>
<td>8-bit</td>
</tr>
<tr>
<td>Transmit/receive clock</td>
<td>Internal</td>
</tr>
<tr>
<td>Transmit control</td>
<td>CTS</td>
</tr>
<tr>
<td>Bit order</td>
<td>LSB first</td>
</tr>
<tr>
<td>Continuous receive mode</td>
<td>Not used</td>
</tr>
<tr>
<td>CLK polarity</td>
<td>Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge</td>
</tr>
<tr>
<td>TXD/RXD I/O polarity switch bit</td>
<td>Non inverted</td>
</tr>
<tr>
<td>Bit rate</td>
<td>500 kbps (1)</td>
</tr>
</tbody>
</table>

Note:

1. The bit rate is calculated by the formula below.
   \[ \text{Bit rate} = \frac{f_x}{2(m+1)} \]
   - \( f_x \): Count source for transmit/receive clock \((f_1, f_8, \text{and } f_{2n})\)
   - \( m \): Setting value \((00h \text{ to } FFh)\) in the \(UiBRG\) register \((i = 0 \text{ to } 6)\)
When data is received from an external device, the transmit/receive clock is output from the MCU. To output the transmit/receive clock, set the port direction bit and the function select register for the port corresponding to the CLK pin.

Table 3.3 lists the CLK Pin, Port Direction Bits, and Function Select Register Settings.

### Table 3.3  CLK Pin, Port Direction Bits, and Function Select Register Settings

<table>
<thead>
<tr>
<th>CLK Pin</th>
<th>Port</th>
<th>Port Direction Bit</th>
<th>Setting Value</th>
<th>Function Select Register</th>
<th>Setting Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK0</td>
<td>P6_1</td>
<td>PD6_1</td>
<td>1</td>
<td>P6_1S</td>
<td>03h</td>
</tr>
<tr>
<td>CLK1</td>
<td>P6_5</td>
<td>PD6_5</td>
<td>1</td>
<td>P6_5S</td>
<td>03h</td>
</tr>
<tr>
<td>CLK2</td>
<td>P7_2</td>
<td>PD7_2</td>
<td>1</td>
<td>P7_2S</td>
<td>03h</td>
</tr>
<tr>
<td>CLK3</td>
<td>P4_1</td>
<td>PD4_1</td>
<td>1</td>
<td>P4_1S</td>
<td>03h</td>
</tr>
<tr>
<td>CLK4</td>
<td>P9_5</td>
<td>PD9_5 (1)</td>
<td>1</td>
<td>P9_5S (1)</td>
<td>03h</td>
</tr>
<tr>
<td>CLK5</td>
<td>P7_7</td>
<td>PD7_7</td>
<td>1</td>
<td>P7_7S</td>
<td>03h</td>
</tr>
<tr>
<td>CLK6</td>
<td>P4_5</td>
<td>PD4_5</td>
<td>1</td>
<td>P4_5S</td>
<td>03h</td>
</tr>
</tbody>
</table>

**Note:**
1. The instruction to set these registers should be written immediately after the instruction to set the PRC2 bit to 1 (write enabled). Any interrupt or DMA transfer should not be generated between these two instructions.

### 3.1 Data Reception In Synchronous Serial Interface Mode

(1) In the U3C1 register, set the TE bit to 1 (transmission enabled) and set the RE bit to 1 (reception enabled).
(2) When dummy data is set in the U3TB register, the MCU switches to wait status.
(3) When the input signal to the CTS3 pin becomes low, the transmit/receive clock is output. (1) The MCU receives the first bit of the RXD3 pin synchronized with the initial rising edge of transmit/receive clock. Then, data from the second bit on is received synchronized with the rising edge of transmit/receive clock.
(4) When 1-byte data accumulates in the UART3 receive register, the value in the UART3 receive register is transferred to the U3RB register. Simultaneously, the RI bit in the U3C1 register becomes 1 (data held in the U3RB register), indicating that data reception is completed. Also, the IR bit in the S3RIC register becomes 1 (interrupt requested).
(5) When the lower byte in the U3RB register is read, the RI bit becomes 0 (no data held in the U3RB register).

**Note:**
1. The input signal to the CTS3 pin is controlled by the transmit device.

Figure 3.1 and Figure 3.2 show the Connection Example and Receive Operation, respectively.

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**Figure 3.1  Connection Example**
Serial Interface Operation When Receiving Data in Synchronous Serial Interface Mode

Figure 3.2 Receive Operation

The data is transmitted from the U3TB register to the UART3 transmit register.

The data is transferred from the UART3 receive register to the U3RB register.

Received data is loaded

Read the U3RB register.

Set to 0 by an interrupt request acceptance or by a program.

Received data is loaded

Clock is not output because CTS3 is high.

fx: U3BRG count source frequency (f1, f8, f2n)
m: Setting value of the U3BRG register

\[ TCLK = \frac{2(m+1)}{fx} \]
3.2 Settings

This section describes the setting procedures and values for “3.1 Data Reception In Synchronous Serial Interface Mode”. Refer to the hardware user's manual for details of each register. Figure 3.3 and Figure 3.4 show the Main Function Flowchart and UART3 Initialization Flowchart, respectively.

**Figure 3.3 Main Function Flowchart**

```
main
  SetPLLClock() Initialize clock. 
  uart3_init() Initialize UART3. 
  U3TB ← FFh Write dummy data to the UART3 transmit buffer register. 
  IR bit in the S3RIC register = 1 ? UART3 receive interrupt requested? 
    Yes
      Clear the IR bit in the S3RIC register
      Read the data received from the U3RB register
      U3TB ← FFh Write dummy data to the UART3 transmit buffer register.
    No
      Clear UART3 receive interrupt request.
```

Note:
1. Refer to the hardware user's manual for initializing the clock.
Serial Interface Operation When Receiving Data in Synchronous Serial Interface Mode

UART3 transmit/receive mode register:
- Synchronous serial interface mode
- Internal clock

UART3 transmit/receive control register 0
- Count source: f1, CTS enabled, LSB first

UART3 bit rate register:
- Transmit/receive bit rate: set to 500 kbps

UART3 transmit/receive control register 1:
- Continuous receive mode disabled, data non logic-inverted

Interrupt control register:
- Transmit interrupt request level: 0
- Receive interrupt request level: 0

Output function select register:
- CLK3 selected

Port direction register:
- Input (CTS3), output (CLK3), input (RXD3)

UART3 transmit/receive control register 1:
- Transmission enabled, reception enabled

Figure 3.4 UART3 Initialization Flowchart
4. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

5. Reference Documents

User’s Manuals
R32C/116 Group User’s Manual: Hardware  Rev.1.10
R32C/117 Group User’s Manual: Hardware  Rev.1.10
R32C/118 Group User’s Manual: Hardware  Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02 C Compiler User’s Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
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<table>
<thead>
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<th>Rev.</th>
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<th>Description</th>
<th>Page</th>
<th>Summary</th>
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<tr>
<td>1.00</td>
<td>Nov. 26, 2010</td>
<td>First edition issued</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
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