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R32C/100 Series

Serial Interface Operation (Receiving in Synchronous Serial Interface Mode)

1. Abstract

This document describes an example of the setting procedure with a usage example for receiving data from an external device synchronized with the transmit/receive clock using the synchronous serial interface mode.

2. Introduction

The application example described in this document applies to the following MCU:

•MCU: R32C/111 Group

The sample program in this application note can be used with other R32C/100 Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Overview

This document describes the setting procedure for receiving data synchronized with the transmit/receive clock supplied from an external device using the synchronous serial interface mode.

Table 3.1 shows the setting conditions for receiving data using the synchronous serial interface mode.

Table 3.1 Setting Conditions for Data Reception Using Synchronous Serial Interface Mode

Item	Setting
Character length	8-bit
Transmit/receive clock	External
Receive control	RTS
Bit order	LSB first
Continuous receive mode	N/A
CLK polarity	Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge
TXD, RXD input/output polarity switch bit	Non inverted

RTS output is used for receive control. To output RTS in the R32C/111 group, you must set the direction bits and the function select registers for the $\overline{\text{RTS}}$ pin ports.
Table 3.2 shows the port direction bit and function select register settings for each $\overline{\text{RTS}}$ pin.

Table 3.2 $\overline{\text{RTS}}$ Pin, Port Direction Bits and Function Select Register Settings

$\overline{\text{RTS}}$ Pin	Port	Port Direction Bit	Setting Value	Function Select Register	Setting Value
$\overline{\text{RTS0}}$	P6_0	PD6_0	1	P6_0S	03h
$\overline{\text{RTS1}}$	P6_4	PD6_4	1	P6_4S	03h
$\overline{\text{RTS2}}$	P7_3	PD7_3	1	P7_3S	03h
$\overline{\text{RTS3}}$	P4_0	PD4_0	1	P4_0S	03h
$\overline{\text{RTS4}}$	P9_4	PD9_4(1)	1	P9_4S(1)	03h
$\overline{\text{RTS5}}$	P8_1	PD8_1	1	P8_1S	03h
$\overline{\text{RTS6}}$	P4_4	PD4_4	1	P4_4S	03h

Note:
1. The instruction to set these registers should be written immediately after the instruction to set the PRC2 bit to 1 (write enabled). Any interrupt or DMA transfer should not be generated between these two instructions.

3.1 Data Reception in Synchronous Serial Interface Mode

1)The MCU switches to receive wait status when the TE bit in the UiC1 register (i = 0 to 6) is set to 1 (transmission enabled), the RE bit in the UiC1 register (i = 0 to 6) is set to 1 (reception enabled) and dummy data is set in the UiTB register. Simultaneously, output level at the $\overline{\text{RTSi}}$ pin becomes low and a message is sent to the transmit device notifying it that data can be received. (Output the transmit/receive clock on the transmit device after confirming that $\overline{\text{RTS}}$ output is low.)

2)When the MCU synchronizes with the initial falling edge of transmit/receive clock, output level at the $\overline{\text{RTSi}}$ pin becomes high. The MCU receives the first bit of the RXDi pin synchronized with the initial rising edge of transmit/receive clock. The second bit and later are then received, synchronized with the rising edge of transmit/receive clock.

3)When 1 byte of data accumulates in the UARTi receive register, the contents of the UARTi receive register are transferred to the UiRB register. Simultaneously, RI bit in the UiC1 register becomes 1 (data held in the UiRB register), showing that receipt is complete. Also, IR bit in the SiRIC register becomes 1 (interrupt request enabled).

4)When the lower byte in the UiRB register are read, the RI bit becomes 0 (no data held in the UiRB register). When dummy data is written in the UiTB register again, the MCU can receive data and output level at the $\overline{\text{RTSi}}$ pin becomes low.

Figure 3.1 shows an example of the receive connection, and Figure 3.2 the operation timing.

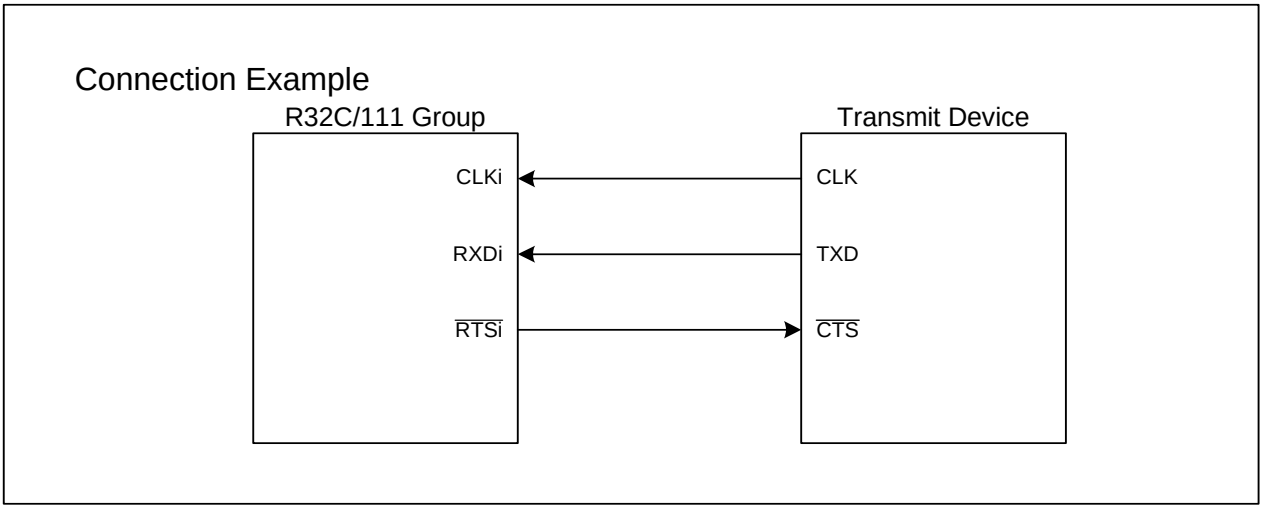
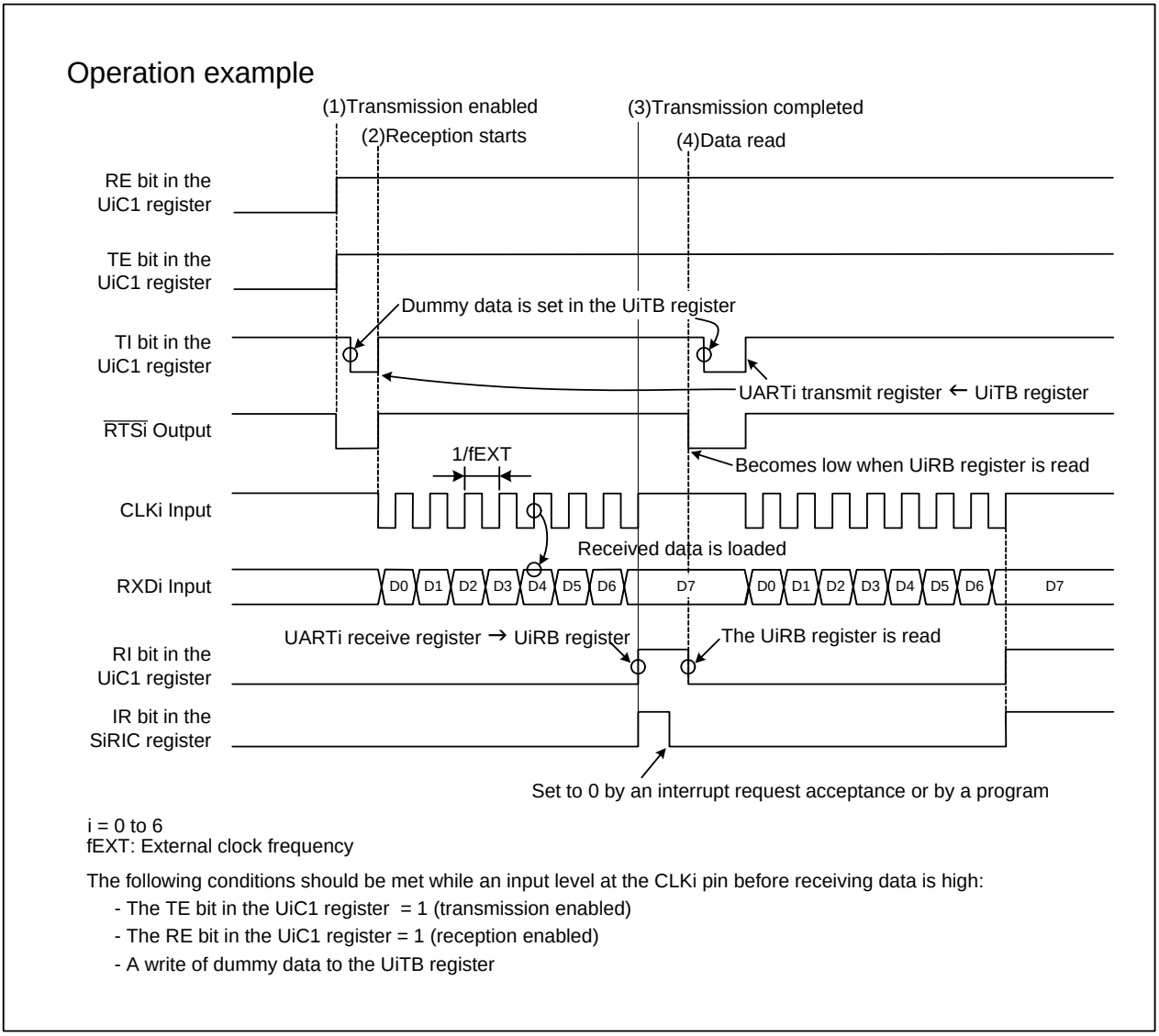


Figure 3.1 Receive Connection Example



i = 0 to 6
fEXT: External clock frequency

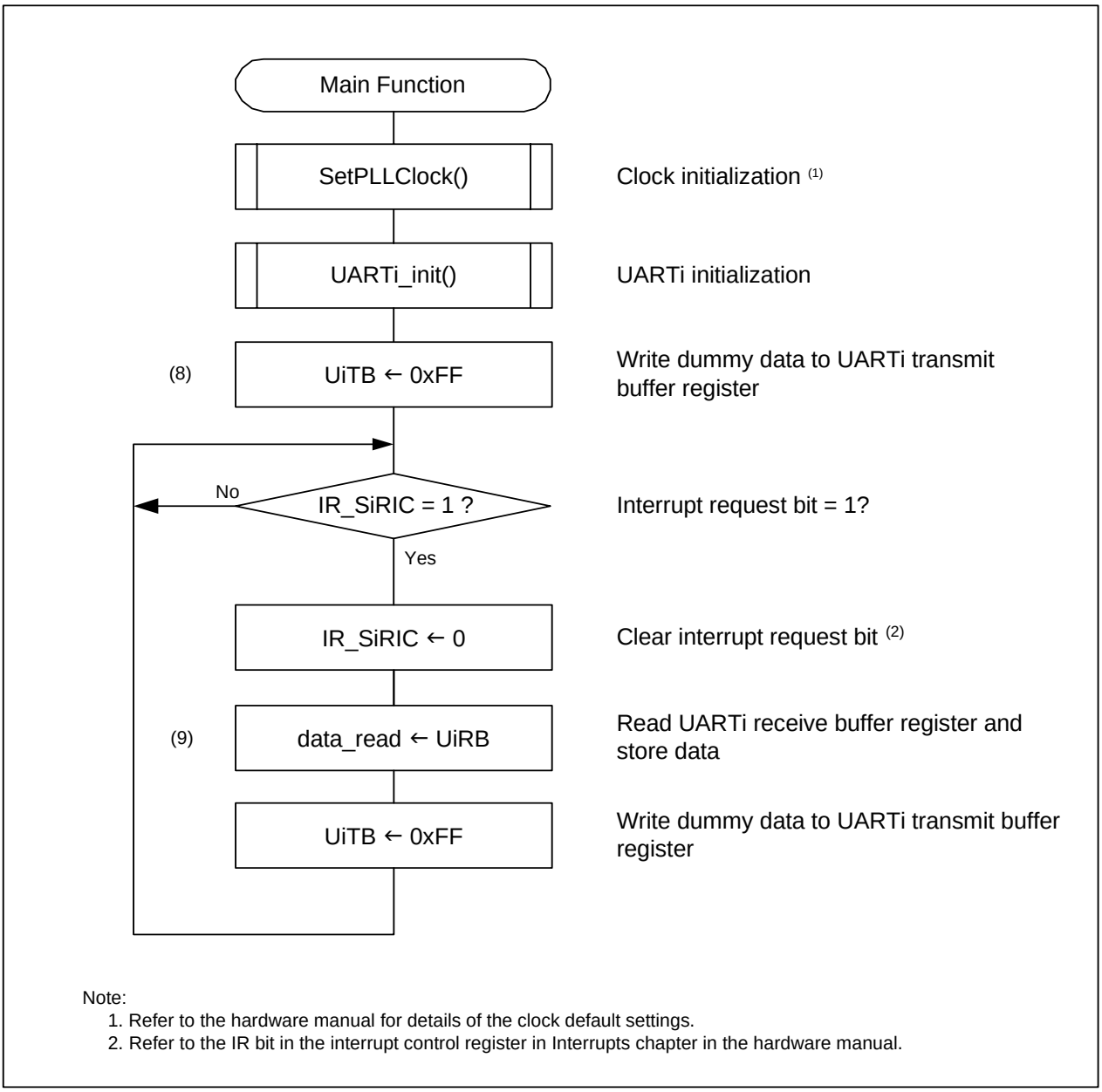
The following conditions should be met while an input level at the CLKi pin before receiving data is high:

- The TE bit in the UiC1 register = 1 (transmission enabled)
- The RE bit in the UiC1 register = 1 (reception enabled)
- A write of dummy data to the UiTB register

Figure 3.2 Receive Operation Timing

3.2 Setting

The following provides the setting procedure and values for 3.1 “Data Reception in Synchronous Serial Interface Mode”. Refer to the hardware manual for details of each register.
The MCU switches to receive wait status by writing dummy data to the UARTi transmit buffer register after the UARTi (i = 0 to 6) initialization. In the sample program, the program detects that the interrupt request bit for the UARTi receive interrupt is 1 (interrupt request enabled) and stores the received data.
Figure 3.3 shows the main process flowchart, and Figure 3.4 shows the UARTi initialization process flowchart and the register settings.



Note:
1. Refer to the hardware manual for details of the clock default settings.
2. Refer to the IR bit in the interrupt control register in Interrupts chapter in the hardware manual.

Figure 3.3 Main Process Flowchart (i = 0 to 6)

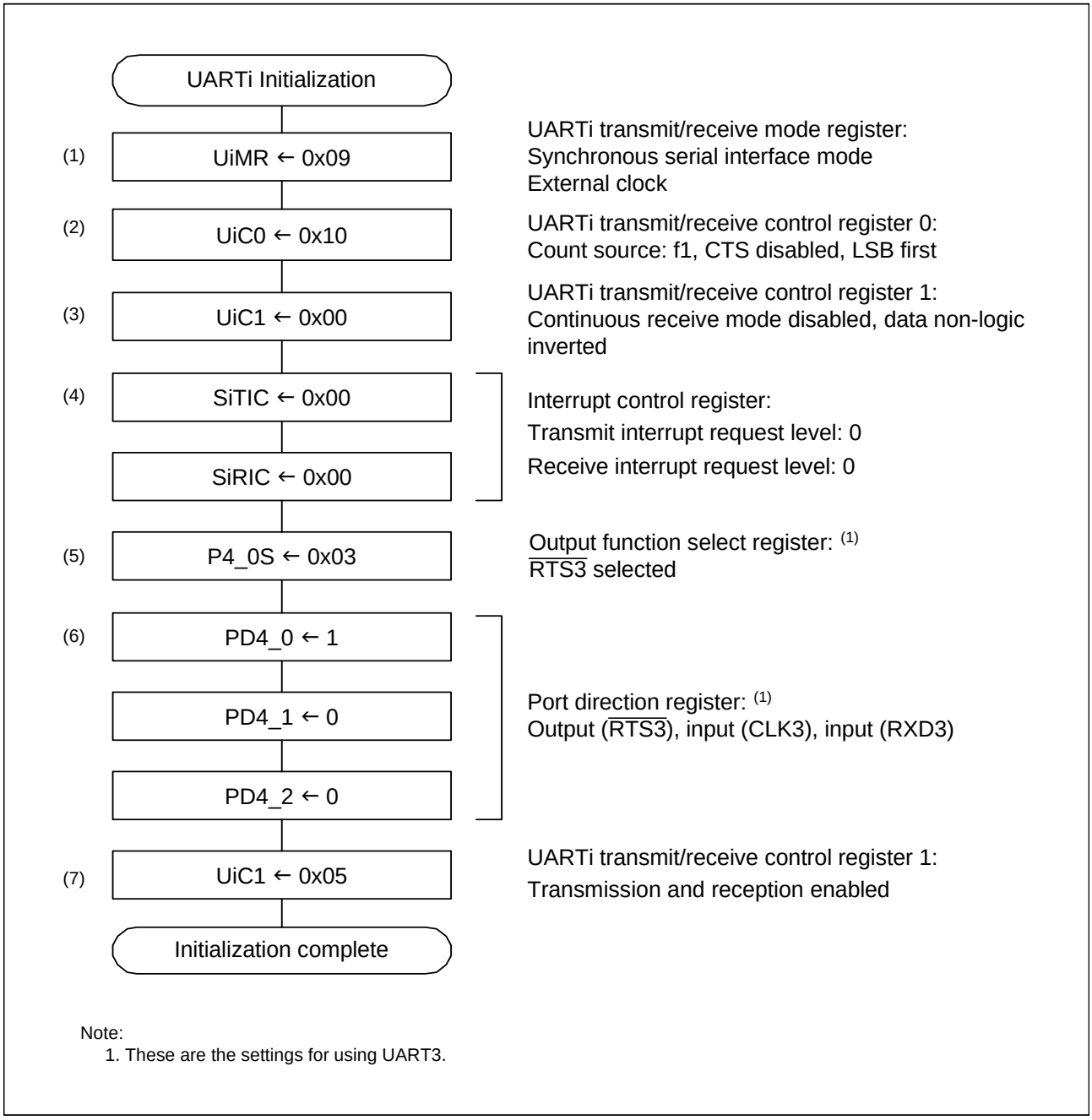
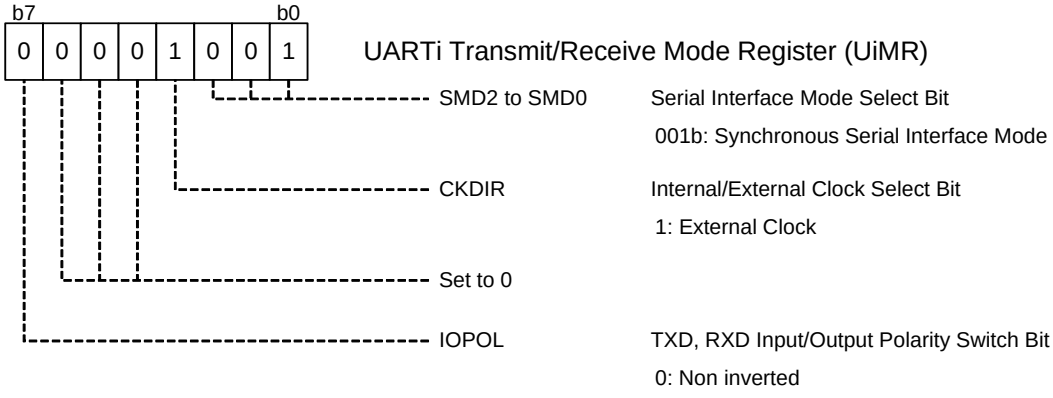


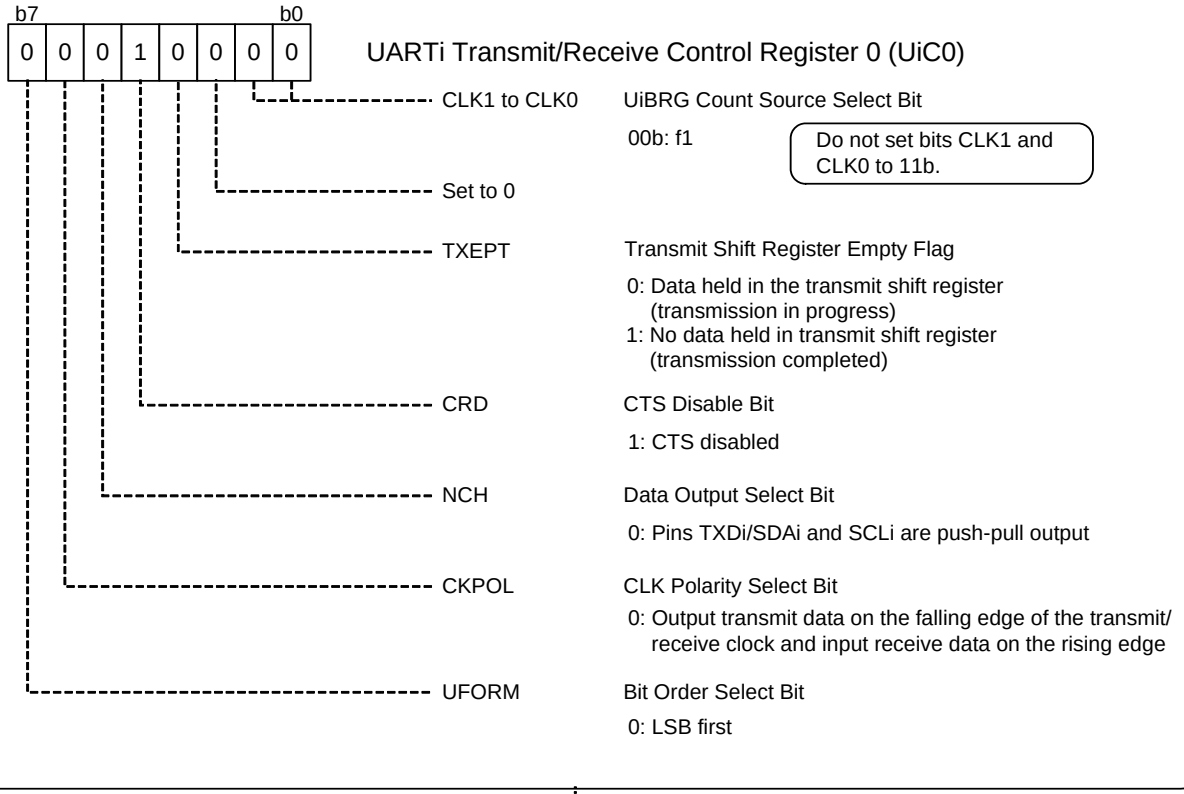
Figure 3.4 UARTi Initialization Process Flowchart (i = 0 to 6)

3.3 Detailed Settings

(1) UARTi Transmit/Receive Mode Register Setting (i = 0 to 6)



(2) UARTi Transmit/Receive Control Register 0 Setting



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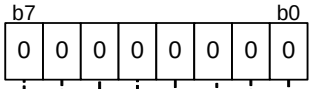
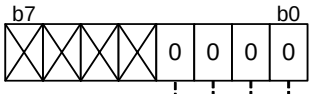
(3) UARTi Transmit/Receive Control Register 1 Setting (i = 0 to 6)



UARTi Transmit/Receive Control Register 1 (UiC1)

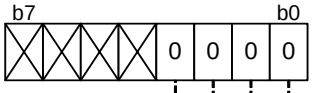
TE	Transmit Enable Bit	0: Transmission disabled
TI	Transmit Buffer Empty Flag	0: Data held in the UiTB register 1: No data held in the UiTB register
RE	Receive Enable Bit	0: Reception disabled
RI	Receive Complete Flag	0: No data held in the UiRB register 1: Data held in the UiRB register
UiIRS	UARTi Transmit Interrupt Source Select Bit	0: UiTB register is empty (TI = 1)
UiRRM	UARTi Continuous Receive Mode Enable Bit	0: Continuous receive mode disabled
UiLCH	Logical Inversion Select Bit	0: Data non logic-inverted
Set to 0		

(4) Interrupt Control Register Setting



UARTi Transmit Interrupt Control Register (SiTIC)

ILVL2 to ILVL0	Interrupt Request Level Select Bit	000b: Level 0 (Interrupt disabled)
IR	Interrupt Request Bit	0: No interrupt requested



UARTi Receive Interrupt Control Register (SiRIC)

ILVL2 to ILVL0	Interrupt Request Level Select Bit	000b: Level 0 (Interrupt disabled)
IR	Interrupt Request Bit	0: No interrupt requested

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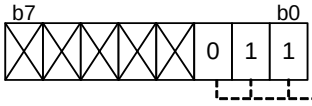
(5) Function Select Register Setting

These are the settings for using UART3.



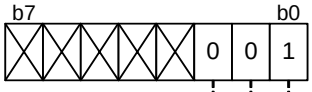
Port P4_0 Function Select Register (P4_0S)

PSEL2 to PSEL0 — Port P4_0 Output Function Select Bit

011b: $\overline{RTS3}$ output

(6) Port Direction Register Setting

These are the settings for using UART3.



Port P4 Direction Register (PD4)

PD4_0 — Port P4_0 Direction Bit

1: Output port

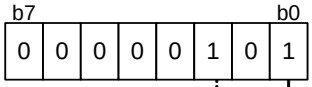
PD4_1 — Port P4_1 Direction Bit

0: Input port

PD4_2 — Port P4_2 Direction Bit

0: Input port

(7) UARTi Transmit/Receive Control Register 1 Setting (i = 0 to 6)



UARTi Transmit/Receive Control Register 1 (UiC1)

TE — Transmit Enable Bit

1: Transmission enabled

RE — Receive Enable Bit

1: Reception enabled

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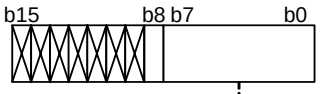
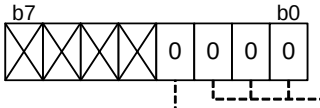
(8) Transmitted Dummy Data Write



UARTi Transmit Buffer Register (UiTB) (i = 0 to 6)

Data transmitted — Set dummy data

Interrupt Request Bit Confirm and Interrupt Control Register Setting

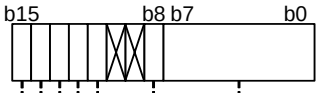


UARTi Receive Interrupt Control Register (SiRIC)

ILVL2 to ILVL0 — Interrupt Request Level Select Bit
000b: Level 0 (interrupt disabled)

IR — Interrupt Request Bit
0: No interrupt requested
1: Interrupt requested

(9) Received Data Read and Error Check



UARTi Receive Buffer Register (UiRB) (i = 0 to 6)

Data(D7 to D0) received

Data (D8) received

ABT — Arbitration Lost Detection Flag
0: Not detected (win)
1: Detected (lose)

OER — Overrun Error Flag
0: No overrun error occurred
1: Overrun error occurred

FER — Framing Error Flag
0: No framing error occurred
1: Framing error occurred

PER — Parity Error Flag
0: No parity error occurred
1: Parity error occurred

SUM — Error Sum Flag
0: No error occurred
1: Error occurred

4. Sample Programs

Sample programs can be downloaded from the Renesas Technology website.
To download, click "Application Notes" in the left-hand side menu of the R32C/100 Family page.

5. Reference Documents

Hardware Manual
R32C/111 Group Hardware Manual Rev.1.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C compiler manual
R32C/100 Family C compiler package V.1.02 C compiler user manual Rev.1.00
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REVISION HISTORY	R32C/100 Series Serial Interface Operation (Receiving in Synchronous Serial Interface Mode)

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		Page	Summary
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