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April 1\(^{st}\), 2010
Renesas Electronics Corporation

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1. Abstract

This document describes an example of the setting procedure with a usage example for receiving data from an external device synchronized with the transmit/receive clock using the synchronous serial interface mode.

2. Introduction

The application example described in this document applies to the following MCU:

- MCU: R32C/111 Group

The sample program in this application note can be used with other R32C/100 Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Overview

This document describes the setting procedure for receiving data synchronized with the transmit/receive clock supplied from an external device using the synchronous serial interface mode.

Table 3.1 shows the setting conditions for receiving data using the synchronous serial interface mode.

<table>
<thead>
<tr>
<th>Item</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Character length</td>
<td>8-bit</td>
</tr>
<tr>
<td>Transmit/receive clock</td>
<td>External</td>
</tr>
<tr>
<td>Receive control</td>
<td>RTS</td>
</tr>
<tr>
<td>Bit order</td>
<td>LSB first</td>
</tr>
<tr>
<td>Continuous receive mode</td>
<td>N/A</td>
</tr>
<tr>
<td>CLK polarity</td>
<td>Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge</td>
</tr>
<tr>
<td>TXD, RXD input/output polarity switch bit</td>
<td>Non inverted</td>
</tr>
</tbody>
</table>

RTS output is used for receive control. To output RTS in the R32C/111 group, you must set the direction bits and the function select registers for the RTS pin ports. Table 3.2 shows the port direction bit and function select register settings for each RTS pin.
Table 3.2 RTS Pin, Port Direction Bits and Function Select Register Settings

<table>
<thead>
<tr>
<th>RTS Pin</th>
<th>Port</th>
<th>Port Direction Bit</th>
<th>Setting Value</th>
<th>Function Select Register</th>
<th>Setting Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTS0</td>
<td>P6_0</td>
<td>PD6_0</td>
<td>1</td>
<td>P6_0S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS1</td>
<td>P6_4</td>
<td>PD6_4</td>
<td>1</td>
<td>P6_4S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS2</td>
<td>P7_3</td>
<td>PD7_3</td>
<td>1</td>
<td>P7_3S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS3</td>
<td>P4_0</td>
<td>PD4_0</td>
<td>1</td>
<td>P4_0S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS4</td>
<td>P9_4</td>
<td>PD9_4(1)</td>
<td>1</td>
<td>P9_4S(1)</td>
<td>03h</td>
</tr>
<tr>
<td>RTS5</td>
<td>P8_1</td>
<td>PD8_1</td>
<td>1</td>
<td>P8_1S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS6</td>
<td>P4_4</td>
<td>PD4_4</td>
<td>1</td>
<td>P4_4S</td>
<td>03h</td>
</tr>
</tbody>
</table>

Note:
1. The instruction to set these registers should be written immediately after the instruction to set the PRC2 bit to 1 (write enabled). Any interrupt or DMA transfer should not be generated between these two instructions.

3.1 Data Reception in Synchronous Serial Interface Mode

1) The MCU switches to receive wait status when the TE bit in the UiC1 register (i = 0 to 6) is set to 1 (transmission enabled), the RE bit in the UiC1 register (i = 0 to 6) is set to 1 (reception enabled) and dummy data is set in the UiTB register. Simultaneously, output level at the RTSi pin becomes low and a message is sent to the transmit device notifying it that data can be received. (Output the transmit/receive clock on the transmit device after confirming that RTS output is low.)

2) When the MCU synchronizes with the initial falling edge of transmit/receive clock, output level at the RTSi pin becomes high. The MCU receives the first bit of the RXDi pin synchronized with the initial rising edge of transmit/receive clock. The second bit and later are then received, synchronized with the rising edge of transmit/receive clock.

3) When 1 byte of data accumulates in the UARTi receive register, the contents of the UARTi receive register are transferred to the UiRB register. Simultaneously, RI bit in the UiC1 register becomes 1 (data held in the UiRB register), showing that receipt is complete. Also, IR bit in the SiRIC register becomes 1 (interrupt request enabled).

4) When the lower byte in the UiRB register are read, the RI bit becomes 0 (no data held in the UiRB register). When dummy data is written in the UiTB register again, the MCU can receive data and output level at the RTSi pin becomes low.

Figure 3.1 shows an example of the receive connection, and Figure 3.2 the operation timing.
The following conditions should be met while an input level at the CLKi pin before receiving data is high:
- The TE bit in the UiC1 register = 1 (transmission enabled)
- The RE bit in the UiC1 register = 1 (reception enabled)
- A write of dummy data to the UiTB register

\[ \begin{align*}
R32C/100 Series & \\
Serial Interface Operation (Receiving in Synchronous Serial Interface Mode) & \\
Figure 3.2 Receive Operation Timing & \\
\end{align*} \]
3.2 Setting

The following provides the setting procedure and values for 3.1 “Data Reception in Synchronous Serial Interface Mode”. Refer to the hardware manual for details of each register. The MCU switches to receive wait status by writing dummy data to the UARTi transmit buffer register after the UARTi (i = 0 to 6) initialization. In the sample program, the program detects that the interrupt request bit for the UARTi receive interrupt is 1 (interrupt request enabled) and stores the received data. Figure 3.3 shows the main process flowchart, and Figure 3.4 shows the UARTi initialization process flowchart and the register settings.

![Main Process Flowchart](image)

Note:
1. Refer to the hardware manual for details of the clock default settings.
2. Refer to the IR bit in the interrupt control register in Interrupts chapter in the hardware manual.

Figure 3.3 Main Process Flowchart (i = 0 to 6)
Figure 3.4  UARTi Initialization Process Flowchart (i = 0 to 6)

UARTi Initialization

1. UiMR ← 0x09
   UARTi transmit/receive mode register:
   Synchronous serial interface mode
   External clock

2. UiC0 ← 0x10
   UARTi transmit/receive control register 0:
   Count source: f1, CTS disabled, LSB first

3. UiC1 ← 0x00
   UARTi transmit/receive control register 1:
   Continuous receive mode disabled, data non-logic inverted

4. SiTIC ← 0x00
   Interrupt control register:
   Transmit interrupt request level: 0
   Receive interrupt request level: 0

5. P4_0S ← 0x03
   Output function select register: (1)
   RTS3 selected

6. PD4_0 ← 1
   Port direction register: (1)
   Output (RTS3), input (CLK3), input (RXD3)

7. UiC1 ← 0x05
   UARTi transmit/receive control register 1:
   Transmission and reception enabled

Initialization complete

Note:
1. These are the settings for using UART3.
3.3 Detailed Settings

(1) UART\textsubscript{i} Transmit/Receive Mode Register Setting (i = 0 to 6)

UART\textsubscript{i} Transmit/Receive Mode Register (UiMR)

\begin{tabular}{cccc}
\hline
b7 & b6 & b5 & b4 \\
\hline
0 & 0 & 0 & 1 \\
\hline
\end{tabular}

- SMD2 to SMD0: Serial Interface Mode Select Bit
  - 001b: Synchronous Serial Interface Mode
- CKDIR: Serial Interface Mode Select Bit
- Set to 0
- IOPOL: Internal/External Clock Select Bit
  - TXD, RXD Input/Output Polarity Switch Bit
  - 0: Non inverted

(2) UART\textsubscript{i} Transmit/Receive Control Register 0 Setting

UART\textsubscript{i} Transmit/Receive Control Register 0 (UiC0)

\begin{tabular}{cccc}
\hline
b7 & b6 & b5 & b4 \\
\hline
0 & 0 & 1 & 0 \\
\hline
\end{tabular}

- CLK1 to CLK0: UiBRG Count Source Select Bit
  - 00b: $f_1$
- TXEPT: Transmit Shift Register Empty Flag
  - 0: Data held in the transmit shift register (transmission in progress)
  - 1: No data held in transmit shift register (transmission completed)
- CRD: CTS Disable Bit
  - 1: CTS disabled
- NCH: Data Output Select Bit
  - 0: Pins TXDi/SDAi and SCLi are push-pull output
- CKPOL: CLK Polarity Select Bit
  - 0: Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge
- UFORM: Bit Order Select Bit
  - 0: LSB first

Continued on next page
(3) UARTi Transmit/Receive Control Register 1 Setting (i = 0 to 6)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>Transmit Enable Bit</td>
<td>0</td>
</tr>
<tr>
<td>b0</td>
<td>Transmit Buffer Empty Flag</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Receive Enable Bit (RE)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Receive Complete Flag</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>UARTi Transmit Interrupt Source Select (UIIRS)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>UARTi Continuous Receive Mode Enable (UIRRM)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Logical Inversion Select Bit (UILCH)</td>
<td>0</td>
</tr>
</tbody>
</table>

(4) Interrupt Control Register Setting

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Interrupt Request Level Select Bit (ILVL2 to ILVL0)</td>
<td>000b: Level 0 (Interrupt disabled)</td>
</tr>
<tr>
<td></td>
<td>Interrupt Request Bit (IR)</td>
<td>0</td>
</tr>
</tbody>
</table>

Continued on next page
Continued from previous page

(5) Function Select Register Setting

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Port P4_0 Function Select Register (P4_0S)

PSEL2 to PSEL0 Port P4_0 Output Function Select Bit
01b: RTS3 output

These are the settings for using UART3.

(6) Port Direction Register Setting

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Port P4 Direction Register (PD4)

PD4_0 Port P4_0 Direction Bit
1: Output port

PD4_1 Port P4_1 Direction Bit
0: Input port

PD4_2 Port P4_2 Direction Bit
0: Input port

These are the settings for using UART3.

(7) UARTi Transmit/Receive Control Register 1 Setting (i = 0 to 6)

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

UARTi Transmit/Receive Control Register 1 (UIC1)

TE Transmit Enable Bit
1: Transmission enabled

RE Receive Enable Bit
1: Reception enabled

These are the settings for using UART3.
(8) Transmitted Dummy Data Write

UART\textsubscript{i} Transmit Buffer Register (UiTB) \((i = 0\text{ to } 6)\)

Data transmitted Set dummy data

Interrupt Request Bit Confirm and Interrupt Control Register Setting

UART\textsubscript{i} Receive Interrupt Control Register (SiRIC)

ILVL2 to ILVL0 Interrupt Request Level Select Bit
000b: Level 0 (interrupt disabled)

IR Interrupt Request Bit
0: No interrupt requested
1: Interrupt requested

(9) Received Data Read and Error Check

UART\textsubscript{i} Receive Buffer Register (UiRB) \((i = 0\text{ to } 6)\)

Data(D7 to D0) received

Data (D8) received

ABT Arbitration Lost Detection Flag
0: Not detected (win)
1: Detected (lose)

OER Overrun Error Flag
0: No overrun error occurred
1: Overrun error occurred

FER Framing Error Flag
0: No framing error occurred
1: Framing error occurred

PER Parity Error Flag
0: No parity error occurred
1: Parity error occurred

SUM Error Sum Flag
0: No error occurred
1: Error occurred
4. **Sample Programs**

Sample programs can be downloaded from the Renesas Technology website. To download, click "Application Notes" in the left-hand side menu of the R32C/100 Family page.

5. **Reference Documents**

Hardware Manual
R32C/111 Group Hardware Manual Rev.1.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C compiler manual
R32C/100 Family C compiler package V.1.02 C compiler user manual Rev.1.00
The latest version can be downloaded from the Renesas Technology website.
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