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April 1st, 2010
Renesas Electronics Corporation

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1. **Abstract**

This document describes an example of the setting procedure for transmitting in the asynchronous serial interface mode (UART mode) using an arbitrary bit rate and data format.

2. **Introduction**

The application example described in this document applies to the following MCU:

- MCU: R32C/111 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/111 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. **Application Example**

This section describes how to transmit data at a bit rate of 9600bps (Xin = 16 MHz, PLL clock = 100 MHz and actual bit rate = 9586bps) using asynchronous serial interface mode. Table 3.1 lists specifications of asynchronous serial interface mode.

| Table 3.1 Setting Conditions for Receiving Data Using Asynchronous Serial Interface Mode |
|-----------------------------------------|-----------------|
| Item                                    | Setting         |
| Bit rate                                | 9600bps         |
| Character length                        | 8 bit-length    |
| Parity                                  | Odd             |
| Stop bit length                         | 1 bit-length    |
| Transmit/receive clock                  | Internal clock  |
| Receive control                         | RTS             |
| Bit order                               | LSB first       |
The following is the formula for calculating the actual bit rate.

\[
\text{Actual bit rate} = \frac{\text{UiBRG register } (i = 0 \text{ to } 6) \text{ count source}}{16 \times (\text{UiBRG register value } + 1)}
\]

Table 3.2 lists examples of bit rate settings.

### Table 3.2 Bit Rate Setting Examples

<table>
<thead>
<tr>
<th>Target Bit Rate (bps)</th>
<th>Count Source of UiBRG</th>
<th>PLL Clock: 96 MHz</th>
<th>PLL Clock: 100 MHz</th>
<th>PLL Clock: 120 MHz</th>
<th>PLL Clock: 128 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Setting value of UiBRG</td>
<td>Actual bit rate (bps)</td>
<td>Setting value of UiBRG</td>
<td>Actual bit rate (bps)</td>
<td>Setting value of UiBRG</td>
</tr>
<tr>
<td>1200</td>
<td>f8</td>
<td>155(9Bh)</td>
<td>1202</td>
<td>162(A2h)</td>
<td>1198</td>
</tr>
<tr>
<td>2400</td>
<td>f8</td>
<td>77(4Dh)</td>
<td>2404</td>
<td>80(50h)</td>
<td>2411</td>
</tr>
<tr>
<td>4800</td>
<td>f8</td>
<td>38(26h)</td>
<td>4808</td>
<td>40(28h)</td>
<td>4764</td>
</tr>
<tr>
<td>9600</td>
<td>f1</td>
<td>155(9Bh)</td>
<td>9615</td>
<td>162(A2h)</td>
<td>9586</td>
</tr>
<tr>
<td>14400</td>
<td>f1</td>
<td>103(67h)</td>
<td>14423</td>
<td>108(6Ch)</td>
<td>14335</td>
</tr>
<tr>
<td>19200</td>
<td>f1</td>
<td>77(4Dh)</td>
<td>19231</td>
<td>80(50h)</td>
<td>19290</td>
</tr>
<tr>
<td>28800</td>
<td>f1</td>
<td>51(33h)</td>
<td>28846</td>
<td>53(35h)</td>
<td>28935</td>
</tr>
<tr>
<td>31250</td>
<td>f1</td>
<td>47(2Fh)</td>
<td>31250</td>
<td>49(31h)</td>
<td>31250</td>
</tr>
<tr>
<td>38400</td>
<td>f1</td>
<td>38(26h)</td>
<td>38462</td>
<td>40(28h)</td>
<td>38109</td>
</tr>
<tr>
<td>51200</td>
<td>f1</td>
<td>28(1Ch)</td>
<td>51724</td>
<td>30(1Eh)</td>
<td>50403</td>
</tr>
</tbody>
</table>

In this application note, the RTS output is used for receive control. To output the RTS in the R32C/111 Group, set the direction bits and the function select registers for the RTS pin.

Table 3.3 lists the RTS Pin, Port Direction Bit and Function Select Register Settings.

### Table 3.3 RTS Pin, Port Direction Bit and Function Select Register Settings

<table>
<thead>
<tr>
<th>Channel</th>
<th>Port</th>
<th>Port Direction Bit</th>
<th>Setting Value</th>
<th>Function Select Register</th>
<th>Setting Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTS0</td>
<td>P6_0</td>
<td>PD6_0</td>
<td>1</td>
<td>P6_0S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS1</td>
<td>P6_4</td>
<td>PD6_4</td>
<td>1</td>
<td>P6_4S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS2</td>
<td>P7_3</td>
<td>PD7_3</td>
<td>1</td>
<td>P7_3S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS3</td>
<td>P4_0</td>
<td>PD4_0</td>
<td>1</td>
<td>P4_0S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS4</td>
<td>P9_4 (1)</td>
<td>PD9_4 (1)</td>
<td>1</td>
<td>P9_4S (1)</td>
<td>03h</td>
</tr>
<tr>
<td>RTS5</td>
<td>P8_1</td>
<td>PD8_1</td>
<td>1</td>
<td>P8_1S</td>
<td>03h</td>
</tr>
<tr>
<td>RTS6</td>
<td>P4_4</td>
<td>PD4_4</td>
<td>1</td>
<td>P4_4S</td>
<td>03h</td>
</tr>
</tbody>
</table>

Notes:
1. N-channel open drain output.
2. Set the PRC2 bit in the PRCR register to 1 (write enabled) just before rewriting this register. Do not generate any interrupts or DMA transfers between setting the PRC2 bit to 1 and rewriting this register.
3.1 Data Reception in Asynchronous Serial Interface Mode

1) When setting the RE bit in the UiC1 register to 1 (write enabled), the MCU waits for data reception (i = 0 to 6). At the same time, the output level of the RTSi pin becomes low, notifying the transmitting side that reception is enabled.

2) When the first bit of received data (start bit) is input to the RXDi pin, the output level of the RTSi pin becomes high. Then the remaining data is received bit by bit in the following order: data bit (LSB) through data bit (MSB), parity bit, and stop bit.

3) When the stop bit is received, the value in UARTi receive register is transferred to the UiRB register. At the same time, the RI bit in the UiC1 register becomes 1 (data held in the UiRB register), indicating the reception is completed. The IR bit in the SiRIC register becomes 1 (interrupt requested).

4) When reading the lower byte in the UiRB register, RI bit becomes 0 (no data held in the UiRB register). At the same time, the output level of the RTSi pin becomes low.

Figure 3.1 shows a Connection Example for Transmission, and Figure 3.2 shows the Transmit Operation Timing.
Figure 3.1 Connection Example for Transmission

Figure 3.2 Transmit Operation Timing
### 3.2 Settings

This section describes the procedure and values to execute the examples shown in section 3.1 “Data Reception in Asynchronous Serial Interface Mode”. For details on each register, refer to hardware manual. The MCU enters reception standby mode by initializing UART\(_i\) (\(i = 0\) to 6). The sample program detects that the interrupt request bit in the UART\(_i\) receive interrupt becomes 1 (interrupt requested) and stores the received data. Figure 3.3 shows the main Processing Flowchart (\(i = 0\) to 6) and Figure 3.4 shows the UART\(_i\) Initialization Process Flowchart (\(i = 0\) to 6).

![Flowchart](image)

**Figure 3.3 main Processing Flowchart (\(i = 0\) to 6)**

**Notes:**
1. Refer to the hardware manual for details of the clock initialization.
2. Refer to the IR bit in the interrupt control register in the Interrupts chapter in the hardware manual.
Figure 3.4 UART{i} Initialization Process Flowchart (i = 0 to 6)

1. These are the settings when using UART3.
3.3 Detailed Settings

Set UARTi Transmit/Receive Mode Register (i = 0 to 6)

UARTi Transmit/Receive Mode Register (UiMR)

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**SMOD2 to SMOD0** Serial Interface Mode Select Bit

101b: UART Mode, 8–bit Character Length

**CKDIR** Internal/External Clock Select Bit

0: Internal clock

**STPS** Stop Bit Length Selection Bit

0: 1 stop bit

**PRY** Odd/Even Parity Select Bit

0: Odd parity

**PRYE** Parity Enable Bit

1: Parity enabled

**IOPOL** TXD, RXD Input/Output Polarity Switch Bit

0: Non inverted

---

Set UARTi Transmit/Receive Control Register 0

UARTi Transmit/Receive Control Register 0 (UiC0)

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**CLK1,CLK0** UiBRG Count Source Select Bit

00b: f1

**TXEPT** Transmit Shift Register Empty Flag

0: Data held in the transmit shift register (transmission in progress)
1: No data held in the transmit shift register (transmission completed)

**CRD** CTS Disable Bit

1: CTS disabled

**NCH** Data Output Select Bit

0: Pins TXDi/SDA and SCLi are push–pull output
1: Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge

**CKPOL** CLK Polarity Select Bit

The TXD2 pin is an N channel open drain output; it will not switch to push–pull output even if set to 0.

**UFORM** Bit Order Select Bit

0: LSB first

---

Do not set bits CK1 and CK0 to 11b.

Continued on next page
Set UARTi Bit Rate Register (i = 0 to 6)

UARTi Bit Rate Register (UiBRG)

The UiBRG register divides the count source by n+1 (n = setting value)
162: Divided by 163

Set UARTi Transmit/Receive Control Register 1

UARTi Transmit/Receive Control Register 1 (UiC1)

- **TE** Transmit Enable Bit
  - 0: Transmission disabled
- **TI** Transmit Buffer Empty Flag
  - 0: Data held in UiTB register
  - 1: No data held in UiTB register
- **RE** Receive Enable Bit
  - 0: Reception disabled
- **RI** Receive Complete Flag
  - 0: No data held in UiRB register
  - 1: Data held in UiRB register
- **UiIRS** UARTi Transmit Interrupt Source Selection Bit
  - 0: UiTB register is empty (TI = 1)
- **UiRRM** UARTi Continuous Receive Mode Enable Bit
  - 0: Continuous receive mode disabled
- **UiLCH** Logical Inversion Select Bit
  - 0: Data non logic-inverted

Set to 0
Set the interrupt control register (i = 0 to 6).

**UARTi Transmit Interrupt Control Register (SiTIC)**

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **ILVL2 to ILVL0**: Interrupt Request Level Select Bits
- **IR**: Interrupt Request Flag
  - 000b: Level 0 (Interrupt disabled)
  - 0: No interrupt requested

**UARTi Receive Interrupt Control Register (SiRIC)**

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **ILVL2 to ILVL0**: Interrupt Request Level Select Bits
- **IR**: Interrupt Request Flag
  - 000b: Level 0 (Interrupt disabled)
  - 0: No interrupt requested

Continued from previous page

Set the function select register.

**Port P4_0 Function Select Register (P4_0S)**

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **PSEL2 to PSEL0**: Port P4_0 Output Function Select Bits
  - 011b: RTS3 output

Setting when UART3 is used.

Set the port direction register.

**Port P4 Direction Register (PD4)**

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **PD4_0**: Port P4_0 Direction Bit
  - 1: Output
- **PD4_2**: Port P4_2 Direction Bit
  - 0: Input

Setting when UART3 is used.

Continued on next page
Continued from previous page

Set the UARTi transmit/receive control register 1 (i = 0 to 6).

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**UARTi Transmit/Receive Control Register 1 (UIC1)**

- **TE** (Transmit Enable Bit)
  - 0: Transmission disabled
- **RE** (Receive Enable Bit)
  - 1: Reception enabled

Read the interrupt request bit and set the interrupt control register.

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
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</thead>
<tbody>
<tr>
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<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**UARTi Receive Interrupt Control Register (SiRIC)**

- **ILVL2 to ILVL0** (Interrupt Request Level Select Bits)
  - 000b: Level 0 (interrupt disabled)
- **IR** (Interrupt Request Flag)
  - 0: No interrupt requested
  - 1: Interrupt requested

Read the receive data and check error.

<table>
<thead>
<tr>
<th>b15</th>
<th>b14</th>
<th>b13</th>
<th>b12</th>
<th>b11</th>
<th>b10</th>
<th>b9</th>
<th>b8</th>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**UARTi Receive Buffer Register (UiRB)**

- **Data Received (D7 to D0)**
- **Data Received (D8)**
- **ABT** (Arbitration Lost Detection Flag)
  - 0: Not detected (win)
  - 1: Detected (lose)
- **OER** (Overrun Error Flag)
  - 0: No overrun error occurred
  - 1: Overrun error occurred
- **FER** (Framing Error Flag)
  - 0: No framing error occurred
  - 1: Framing error occurred
- **PER** (Parity Error Flag)
  - 0: No parity error occurred
  - 1: Parity error occurred
- **SUM** (Error Sum Flag)
  - 0: No error occurred
  - 1: Error occurred
4. **Sample Programs**
   A sample program can be downloaded from the Renesas Technology website.

5. **Reference Documents**
   Hardware Manual
   R32C/111 Group Hardware Manual Rev.1.10
   The latest version can be downloaded from the Renesas Technology website.

   Technical Update/Technical News
   The latest information can be downloaded from the Renesas Technology website.

   C compiler manual
   R32C/100 Family C compiler package V.1.02 C compiler user manual Rev.1.00
   The latest version can be downloaded from the Renesas Technology website.
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csc@renesas.com

<table>
<thead>
<tr>
<th>REVISION HISTORY</th>
<th>R32C/100 Series Serial Interface Operation (Receiving in Asynchronous Serial Interface Mode)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev.</td>
<td>Date</td>
</tr>
<tr>
<td>1.00</td>
<td>Mar 12, 2010</td>
</tr>
</tbody>
</table>

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