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Serial EEPROM of HN58X25xxx Series

Control Using Clock Synchronous Serial I/O (UART) of M16C

Introduction

This document should be used for reference when implementing control of the HN58X25xxx Series serial EEPROM manufactured by Renesas Technology Corp., using the clock synchronous serial communication interface (hereafter referred to as UART) of the M16C family manufactured by Renesas Technology Corp.

The M16C family incorporates a clock synchronous serial I/O. The HN58X25xxx Series serial EEPROM can be controlled through the clock synchronous serial I/O and software.

This document describes sample programs for controlling the HN58X25xxx Series serial EEPROM by using the clock synchronous serial I/O.

Target Device

The application examples described in this document are applicable when the following MCU and condition are used.

- MCU: M16C family
- Condition: Clock synchronous serial I/O is used
- Software Version: Ver.1.21

The programs can be executed by any M16C family MCU with the serial I/O.

Note however that since some functions may be altered by function addition, etc., the functions should be confirmed against the MCU manual.

Be sure to perform evaluation sufficiently when using this application note.

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1. Control Method for HN58X25xxx Series Serial EEPROM

1.1 Overview of Operation

Control of the HN58X25xxx Series serial EEPROM is implemented by using the clock synchronous Serial I/O in the M16C.

The sample programs execute the following control operations.

- Connects the S# pin of the serial EEPROM to a M16C port and controls it using output of the M16C general port.
- Controls data input/output by the clock synchronous serial I/O (using the internal clock).
  Assign the clock synchronous serial I/O pins for which CMOS output is possible and set the CMOS output to them, in order to implement the high-speed operation.
  In order to control the data transmission, the empty of transmit buffer is detected and interrupt is not used but transmit interrupt request bit is used.
  Therefore the register setting related to interrupt is described below.
  — Set the interrupt priority level to 000b (Level 0; Interrupt disable).
  — Set the transmit interrupt cause select bit to 0 (No data present in transmit buffer). (Set the DMA request cause to UART transmit interrupt request if DMA is used.)
- Control data transmission using DMAC as option.
  Refer to the data sheets of the MCU and serial EEPROM and specify a usable clock frequency.

The connection method is described below.

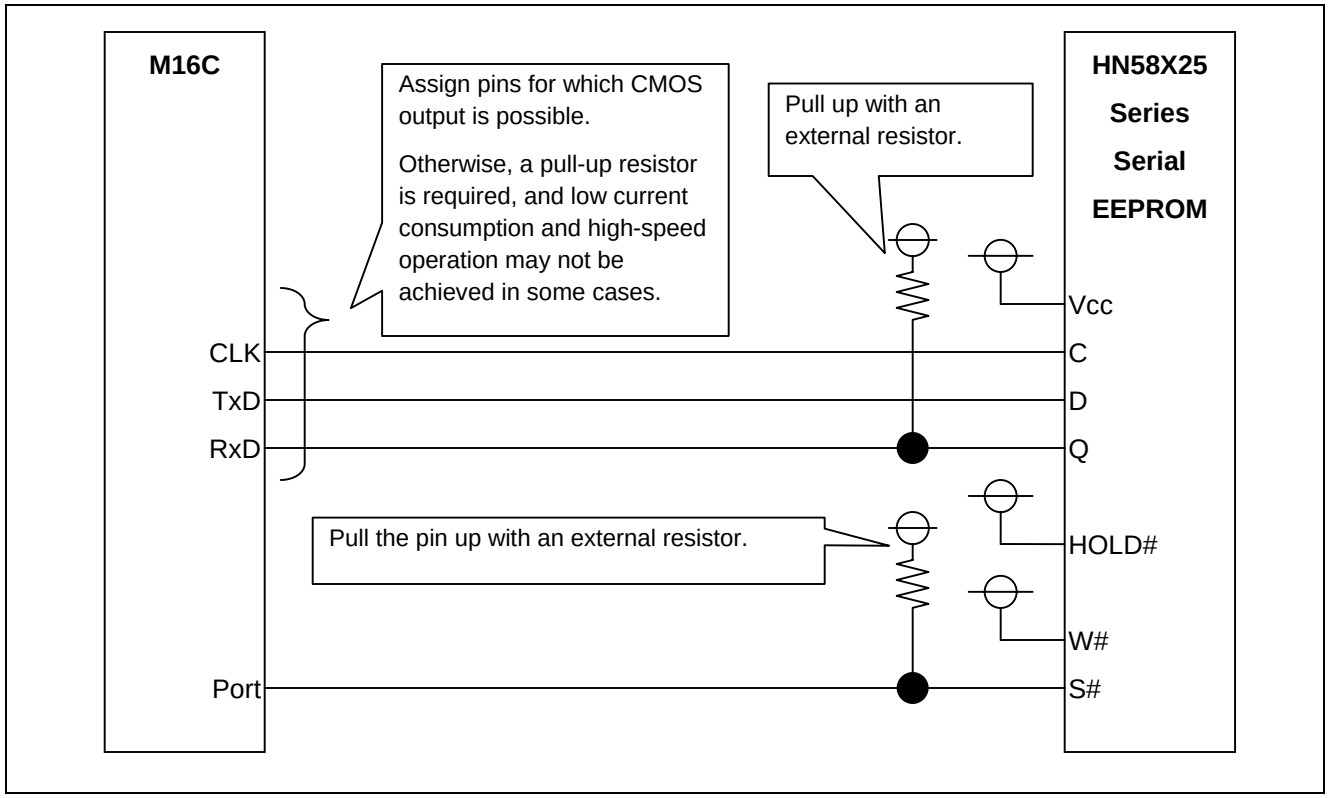
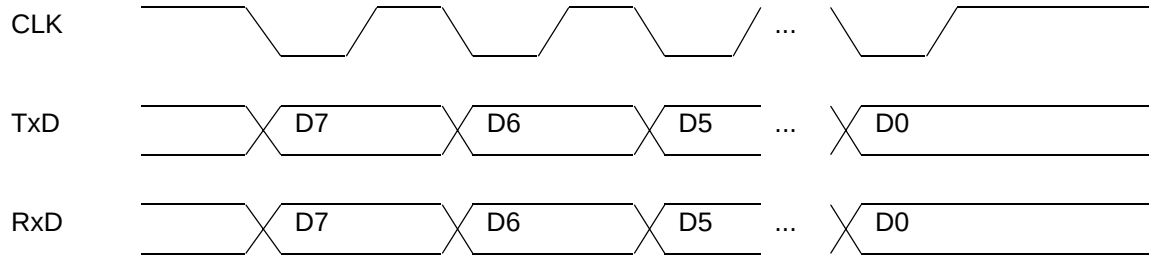


Figure 1.1 Serial EEPROM Connection Example

1.2 Signal Timing Generation of Clock Synchronous Serial I/O

Signals are generated at the following timing to satisfy the serial EEPROM timing.



- Transmission from MCU to serial EEPROM: Transmit data output at fall of transfer clock
- Reception from serial EEPROM to MCU: Receive data input at rise of transfer clock
- Transfer in MSB-first

The CLK pin level is high when transfer is not taking place.

Figure 1.2 Timing for Clock Synchronous Serial I/O of M16C

Check the data sheets of the MCU and serial EEPROM for the maximum clock frequency that can be used.

1.3 Control of S# Pin of Serial EEPROM

The S# pin of the serial EEPROM is connected to a M16C port and controlled using output of the M16C general port.

The period from the falling edge of the S# pin (port of M16C) of the serial EEPROM to the falling edge of the C pin (CLK of M16C) is controlled by inserting software wait cycles.

The period from the rising edge of the C pin (CLK of M16C) to the rising edge of the S# pin (port of M16C) is controlled by inserting software wait cycles.

Check the data sheet of the serial EEPROM and set the software wait time according to the system.

1.4 Processing after function operating

When function processing is begun, S# pin (Port of M16C) of EEPROM is set to high level first by setting the port function, and, next, C pin (CLK of M16C) of EEPROM is set to high level. Next, Serial I/O function is enabled and clock synchronous I/O mode is set. Command code etc. are output using serial I/O function after S# pin (Port of M16C) of EEPROM is set to low level.

After function processing is finished, S# pin (Port of M16C) of EEPROM is set to high level first and, next, Serial I/O function is disabled and changed to the function of general port, and next, Port/CLK/TxD/RxD pins are set to high level.

1.5 MCU Hardware Resources in Use

The hardware resources to be used are shown below.

In order to control the data transmission, the empty of transmit buffer is detected and interrupt is not used but transmit interrupt request bit is used.

Therefore the register setting related to interrupt is described below.

- Set the interrupt priority level to 000b (Level 0; Interrupt disable).
- Set the transmit interrupt cause select bit to 0 (No data present in transmit buffer).
  (Set the DMA request cause to UART transmit interrupt request if DMA is used.)

Table 1.1 Hardware Resources in Use

Resource in Use	Number of Used Resources
Clock synchronous serial I/O	One channel (essential)
Port (for control of the S# pin of serial EEPROM)	One port (essential)
DMAC	One channel (option)

The accessing mode between RAM and UART (transmit buffer or receive buffer) using DMAC is prepared as option.

1.6 M16C SFR (Peripheral Device Control Register) Setting - Clock Synchronous Serial I/O and Interrupt control Register

Set up the clock synchronous serial I/O as shown below to satisfy the serial EEPROM specifications/timing.

In order to control the data transmission, the empty of transmit buffer is detected and interrupt is not used but transmit interrupt request bit is used.

Therefore the register setting related to interrupt is described below.

- Set the interrupt priority level to 000b (Level 0; Interrupt disable).
- Set the transmit interrupt cause select bit to 0 (No data present in transmit buffer).
  (Set the DMA request cause to UART transmit interrupt request if DMA is used.)

1.6.1 M32C/87

An example of setting based on the register descriptions of (Table 17.2 Registers to Be Used and Setting in Clock Synchronous Serial I/O Mode) in the M32C/87 Group Hardware Manual Rev. 1.00 is shown in the table below.

Clock synchronous serial I/O other than UART2 (N channel open drain output) to be used are recommended.

Continuous receive mode should be disabled. The details please refer to the technical update TN-16C-A162A/J.

Table 1.2 Clock Synchronous Serial I/O Mode Settings

Register	Bit	Function and Setting
UiTB	7 to 0	Set the transmit data in these bits.
UiRB	7 to 0	The receive data is read from these bits.
	OER	Overrun error flag
UiBRG	7 to 0	Set the transfer speed in these bits. Clock frequency that can transfer data is different depending on the MCU.
UiMR	SMD2 to SMD0	Write 001b to these bits. (Clock synchronous serial I/O mode)
	CKDIR	Write 0 to this bit. (Internal clock) Set the clock frequency to UiBRG.
	IOPOL	Write 0 to this bit. (No reverse)
UiC0	CKS1, CKS0	Select the count source of UiBRG register in these bits.
	CRS	Write 0 to this bit. (This function is disabled because of CRD=1.)
	TXEPT	Transmit register empty flag (Read only)
	CRD	Write 1 to this bit. (CTS# and RTS# functions are disabled.)
	NCH	Write 0 to this bit. (CMOS output)
	CKPOL	Write 0 to this bit. Transmit data is output at falling edge of transfer clock and receive data is input at rising edge.
	UFORM	Write 1 to this bit. (MSB first)
	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	UiIRS	Write 0 to this bit at initialization. (No data present in UiTB register: TI=1)
	UiRRM	Write 0 to this bit. (Continuous receive mode is disabled)
	UiLCH	Write 0 to this bit. (Data logic is not reversed)
	SCLKSTPB	UiC1
UiSMR	7 to 0(Note 1)	Write 00 to these bits.
UiSMR2	7 to 0(Note 1)	Write 00 to these bits.
UiSMR3	7 to 0(Note 1)	Write 00 to these bits.
UiSMR4	7 to 0(Note 1)	Write 00 to these bits.

Note 1: Sample program doesn't set 00 data to these registers because initial values of these registers after reset are 00.

The setting example of interrupt control register is shown in the table bellow.

In order to control the data transmission, the empty of transmit buffer is detected and interrupt is not used but transmit interrupt request bit is used.

Table 1.3 Interrupt Control Register Settings

Register	Bit	Function and Setting
SiTIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

1.6.2 M16C/80

An example of setting based on the register descriptions in the M16C/80 Group Hardware Manual Rev. 1.00 is shown in the table below.

Clock synchronous serial I/O other than UART2 (N channel open drain output) to be used are recommended.

Continuous receive mode should be disabled. The details please refer to the technical update TN-16C-A162A/J.

Table 1.4 Clock Synchronous Serial I/O Mode Settings

Register	Bit	Function and Setting
UiTB	7 to 0	Set the transmit data in these bits.
UiRB	7 to 0	The receive data is read from these bits.
	OER	Overrun error flag
UiBRG	7 to 0	Set the transfer speed in these bits. Clock frequency that can transfer data is different depending on the MCU.
UiMR	SMD2 to SMD0	Write 001b to these bits. (Clock synchronous serial I/O mode)
	CKDIR	Write 0 to this bit. (Internal clock) Set the clock frequency to UiBRG.
	SLEP (U0MR, U1MR)	Write 0 to this bit.
	IOPOL (U2MR to U4MR)	Write 0 to this bit. (No reverse)
UiC0	CKS1, CKS0	Select the count source of UiBRG register in these bits.
	CRS	Write 0 to this bit. (This function is disabled because of CRD=1.)
	TXEPT	Transmit register empty flag (Read only)
	CRD	Write 1 to this bit. (CTS# and RTS# functions are disabled.)
	NCH	Write 0 to this bit. (CMOS output)
	CKPOL	Write 0 to this bit. Transmit data is output at falling edge of transfer clock and receive data is input at rising edge.
	UFORM	Write 1 to this bit. (MSB first)
U0C1, U1C1	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	7 to 4	These bits are always read as 0. The write value should always be 0.

U2C1 to U4C1	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	UiIRS (i; 2 to 4) (Note 1)	0 is written to this bit at initialization. (No data present in transmit buffer: TI=1)
	UiRRM (i; 2 to 4) (Note 1)	Write 0 to this bit. (Continuous receive mode is disabled.)
	UiLCH (i; 2 to 4)	Write 0 to this bit. (Data logic is not reversed.)
	UiERE (i; 2 to 4)	Write 0 to this bit. (Error signal output disabled)
UCON	U0IRS	Write it as follows when UART0 is used. Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U1IRS	Write it as follows when UART1 is used. Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U0RRM (Note 2)	Write 0 to this bit. (Continuous receive mode is disabled.)
	U1RRM (Note 2)	Write 0 to this bit. (Continuous receive mode is disabled.)
	5 to 4	The read data are invalid. The write value should always be 0.
	RCSP	Write 0 to this bit. (This function is disabled because of CRD are disabled.)
	7	The read data is invalid. The write value should always be 0.
UiSMR	7 to 0(Note 3)	Write 00 to these bits.
UiSMR2	7 to 0(Note 3)	Write 00 to these bits.
UiSMR3	7 to 0(Note 4)	Write 00 to these bits.

Note 1: Set it similarly to UCON (UART transmit and reception control register 2) as for UART0 and UART1.
Note 2: Set it similarly to UiC1 (UART transmit and reception control register 1) for UART2 to UART4.
Note 3: Sample program doesn't set 00 data to these registers because initial values of them after reset are 00.
Note 4: Sample program doesn't set 00 data to these registers other than U2SMR3 because initial values of them after reset are 00. Write 000b from DL2 to DL0 bits for U2SMR3.

The setting example of interrupt control register is shown in the table bellow.

In order to control the data transmission, the empty of transmit buffer is detected and interrupt is not used but transmit interrupt request bit is used.

Table 1.5 Interrupt Control Register Settings

Register	Bit	Function and Setting
SiTIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

1.6.3 M16C/62P

An example of setting based on the register descriptions of (Table 17.2 Registers to Be Used and Setting in Clock Synchronous Serial I/O Mode) in the M16C/62P Group Hardware Manual Rev. 2.41 is shown in the table below.

Clock synchronous serial I/O other than UART2 (N channel open drain output) to be used are recommended.

Don't use UART3 and UART4.

Table 1.6 Clock Synchronous Serial I/O Mode Settings

Register	Bit	Function and Setting
UiTB	7 to 0	Set the transmit data in these bits.
UiRB	7 to 0	The receive data is read from these bits.
	OER	Overrun error flag
UiBRG	7 to 0	Set the transfer speed in these bits. Clock frequency that can transfer data is different depending on the MCU.
UiMR	SMD2 to SMD0	Write 001b to these bits. (Clock synchronous serial I/O mode)
	CKDIR	Write 0 to this bit. (Internal clock) Set the clock frequency to UiBRG.
	IOPOL	Write 0 to this bit. (No reverse)
UiC0	CKS1, CKS0	Select the count source of UiBRG register in these bits.
	CRS	Write 0 to this bit. (This function is disabled because of CRD=1.)
	TXEPT	Transmit register empty flag (Read only)
	CRD	Write 1 to this bit. (CTS# and RTS# functions are disabled.)
	NCH	Write 0 to this bit. (CMOS output)
	CKPOL	Write 0 to this bit. Transmit data is output at falling edge of transfer clock and receive data is input at rising edge.
	UFORM	Write 1 to this bit. (MSB first)
U0C1, U1C1	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	5 to 4	The read data are invalid. The write value should always be 0.
	U0LCH/U1LCH	Write 0 to this bit. (Data logic is not reversed.)
	U0ERE/U1ERE	Write 0 to this bit. (Error signal output disabled.)

U2C1	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	U2IRS (Note1)	Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U2RRM (Note1)	Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UART2 continuous receive mode according to the usage.
	U2LCH	Write 0 to this bit. (Data logic is not reversed.)
	U2ERE	Write 0 to this bit. (Error signal output disabled)
UiSMR	7 to 0(Note 3)	Write 00 to these bits.
UiSMR2	7 to 0(Note 3)	Write 00 to these bits.
UiSMR3	7 to 0(Note 3)	Write 00 to these bits.
UiSMR4	7 to 0(Note 3)	Write 00 to these bits.
UCON	U0IRS	Set it as follows when UART0 is used. Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U1IRS	Set it as follows when UART1 is used. Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U0RRM (Note 2)	Set it as follows when UART0 is used. Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UART0 continuous receive mode according to the usage.
	U1RRM (Note 2)	Set it as follows when UART1 is used. Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UART1 continuous receive mode according to the usage.
	CLKMD0	Write 0 to this bit. (This function is disabled because of CLKMD1=1)
	CLKMD1	Write 0 to this bit. (CLK is output from only CLK1.)
	RCSP	Write 0 to this bit. (This function is disabled because of CRD are disabled.)
	7	The read data is invalid. The write value should always be 0.

Note 1: Set it similarly to UCON (UART transmit and reception control register 2) for UART0 and UART1.
Note 2: Set it similarly to U2C1 (UART transmit and reception control register 1) for UART2.
Note 3: Sample program doesn't set 00 data to these registers because initial values of them after reset are 00.

The setting example of interrupt control register is shown in the table bellow.

In order to control the data transmission, the empty of transmit buffer is detected and interrupt is not used but transmit interrupt request bit is used.

Table 1.7 Interrupt Control Register Settings

Register	Bit	Function and Setting
SiTIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

1.6.4 M16C/30P

An example of setting based on the register descriptions of (Table 15.2 Registers to Be Used and Setting in Clock Synchronous Serial I/O Mode) in the M16C/30P Group Hardware Manual Rev. 1.11 is shown in the table below.

Clock synchronous serial I/O other than UART2 (N channel open drain output) to be used are recommended.

Table 1.8 Clock Synchronous Serial I/O Mode Settings

Register	Bit	Function and Setting
UiTB	7 to 0	Set the transmit data in these bits.
UiRB	7 to 0	The receive data is read from these bits.
	OER	Overrun error flag
UiBRG	7 to 0	Set the transfer speed in these bits. Clock frequency that can transfer data is different depending on the MCU.
UiMR	SMD2 to SMD0	Write 001b to these bits. (Clock synchronous serial I/O mode)
	CKDIR	Write 0 to this bit. (Internal clock) Set the clock frequency to UiBRG.
	IOPOL	Write 0 to this bit. (No reverse)
UiC0	CLK1, CLK0	Select the count source of UiBRG register in these bits.
	CRS	Write 0 to this bit. (This function is disabled because of CRD=1.)
	TXEPT	Transmit register empty flag (Read only)
	CRD	Write 1 to this bit. (CTS# and RTS# functions are disabled.)
	NCH	Write 0 to this bit. (CMOS output)
	CKPOL	Write 0 to this bit. Transmit data is output at falling edge of transfer clock and receive data is input at rising edge.
	UFORM	Write 1 to this bit. (MSB first)
U0C1, U1C1	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	5 to 4	The read data are invalid. The write value should always be 0.
	U0LCH/U1LCH	Write 0 to this bit. (Data logic is not reversed.)
	U0ERE/U1ERE	Write 0 to this bit. (Error signal output disabled)

U2C1	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	U2IRS (Note1)	Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U2RRM (Note1)	Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UART2 continuous receive mode according to the usage.
	U2LCH	Write 0 to this bit. (Data logic is not reversed.)
	U2ERE	Write 0 to this bit. (Error signal output disabled)
UiSMR	7 to 0(Note 3)	Write 00 to these bits.
UiSMR2	7 to 0(Note 3)	Write 00 to these bits.
UiSMR3	7 to 0(Note 3)	Write 00 to these bits.
UiSMR4	7 to 0(Note 3)	Write 00 to these bits.
UCON	U0IRS	Set it as follows when UART0 is used. Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U1IRS	Set it as follows when UART1 is used. Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U0RRM (Note 2)	Set it as follows when UART0 is used. Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UART0 continuous receive mode according to the usage.
	U1RRM (Note 2)	Set it as follows when UART1 is used. Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UART1 continuous receive mode according to the usage.
	CLKMD0	Write 0 to this bit. (This function is disabled because of CLKMD1=1.)
	CLKMD1	Write 0 to this bit. (CLK is output from only CLK1.)
	RCSP	Write 0 to this bit. (This function is disabled because of CRD are disabled.)
	7	The read data is invalid. The write value should always be 0.

Note 1: Set it similarly to UCON (UART transmit and reception control register 2) for UART0 and UART1.
Note 2: Set it similarly to U2C1 (UART transmit and reception control register 1) for UART2.
Note 3: Sample program doesn't set 00 data to these registers because initial values of them after reset are 00.

The setting example of interrupt control register is shown in the table bellow.

In order to control the data transmission, the empty of transmit buffer is detected and interrupt is not used but transmit interrupt request bit is used.

Table 1.9 Interrupt Control Register Settings

Register	Bit	Function and Setting
SiTIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

1.6.5 M16C/29

An example of setting based on the register descriptions of (Table 14.2 Registers to Be Used and Setting in Clock Synchronous Serial I/O Mode) in the M16C/29 Group Hardware Manual Rev. 1.00 is shown in the table below.

Don't use UART3 and UART4.

Table 1.10 Clock Synchronous Serial I/O Mode Settings

Register	Bit	Function and Setting
UiTB	7 to 0	Set the transmit data in these bits.
UiRB	7 to 0	The receive data is read from these bits.
	OER	Overrun error flag
UiBRG	7 to 0	Set the transfer speed in these bits. Clock frequency that can transfer data is different depending on the MCU.
UiMR	SMD2 to SMD0	Write 001b to these bits. (Clock synchronous serial I/O mode)
	CKDIR	Write 0 to this bit. (Internal clock) Set the clock frequency to UiBRG.
	7	Write 0 to this bit.
UiC0	CKS1, CKS0	Select the count source of UiBRG register in these bits.
	CRS	Write 0 to this bit. (This function is disabled because of CRD=1.)
	TXEPT	Transmit register empty flag (Read only)
	CRD	Write 1 to this bit. (CTS# and RTS# functions are disabled.)
	NCH	Write 0 to this bit. (CMOS output)
	CKPOL	Write 0 to this bit. Transmit data is output at falling edge of transfer clock and receive data is input at rising edge.
	UFORM	Write 1 to this bit. (MSB first)
U0C1, U1C1	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	7 to 4	These bits are always read as 0. The write value should always be 0.
U2C1	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	U2IRS (Note 1)	Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U2RRM (Note 1)	Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UART2 continuous receive mode according to the usage.
	U2LCH	Write 0 to this bit. (Data logic is not reversed.)
	U2ERE	Write 0 to this bit. (Error signal output disabled.)

U2SMR	7 to 0(Note 3)	Write 00 to these bits.
U2SMR2	7 to 0(Note 3)	Write 00 to these bits.
U2SMR3	7 to 0(Note 3)	Write 00 to these bits.
U2SMR4	7 to 0(Note 3)	Write 00 to these bits.
UCON	U0IRS	Set it as follows when UART0 is used. Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U1IRS	Set it as follows when UART1 is used. Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	U0RRM (Note 2)	Set it as follows when UART0 is used. Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UART0 continuous receive mode according to the usage.
	U1RRM (Note 2)	Set it as follows when UART1 is used. Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UART1 continuous receive mode according to the usage.
	CLKMD0	Write 0 to this bit. (This function is disabled because of CLKMD1=1.)
	CLKMD1	Write 0 to this bit. (CLK is output from only CLK1).
	RCSP	Write 0 to this bit. (This function is disabled because of CRD are disabled.)
	7	The read data is invalid. The write value should always be 0.

Note 1: Set it similarly to UCON (UART transmit and reception control register 2) for UART0 and UART1.
Note 2: Set it similarly to U2C1 (UART transmit and reception control register 1) for UART2.
Note 3: Sample program doesn't set 00 data to these registers because initial values of them after reset are 00.

The setting example of interrupt control register is shown in the table bellow.

In order to control the data transmission, the empty of transmit buffer is detected and interrupt is not used but transmit interrupt request bit is used.

Table 1.11 Interrupt Control Register Settings

Register	Bit	Function and Setting
SiTIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

1.6.6 R8C/25

An example of setting based on the register descriptions of (Table 15.2 Registers to Be Used and Setting in Clock Synchronous Serial I/O Mode) in the R8C/25 Group Hardware Manual Rev. 2.00 is shown in the table below.

UART1can't be used, because it is not supported Clock synchronous.

Table 1.12 Clock Synchronous Serial I/O Mode Settings

Register	Bit	Function and Setting
UiTB	7 to 0	Set the transmit data in these bits.
UiRB	7 to 0	The receive data is read from these bits.
	OER	Overrun error flag
UiBRG	7 to 0	Set the transfer speed in these bits. Clock frequency that can transfer data is different depending on the MCU.
UiMR	SMD2 to SMD0	Write 001b to these bits. (Clock synchronous serial I/O mode)
	CKDIR	Write 0 to this bit. (Internal clock) Set the clock frequency to UiBRG.
	7	Write 0 to this bit.
UiC0	CKS1, CKS0	Select the count source of UiBRG register in these bits.
	2	Write 0 to this bit.
	TXEPT	Transmit register empty flag (Read only)
	4	This bit is always read as 0. The write value should always be 0.
	NCH	Write 0 to this bit. (CMOS output)
	CKPOL	Write 0 to this bit. Transmit data is output at falling edge of transfer clock and receive data is input at rising edge.
	UFORM	Write 1 to this bit. (MSB first)
UiC1	TE	0 is written to this bit at initialization. (Transmission disabled) Write 1 to this bit when transmission should be enabled.
	TI	Transmit buffer empty flag (Read only)
	RE	0 is written to this bit at initialization. (Reception disabled) Write 1 to this bit when reception should be enabled.
	RI	Receive complete flag (Read only)
	UiIRS	Write 0 to this bit at initialization. (No data present in transmit buffer: TI=1)
	UiRRM	Write 0 to this bit at initialization. (Continuous receive mode is disabled.) Select UARTi continuous receive mode according to the usage.
	7 to 6	These bits are always read as 0. The write value should always be 0.

The setting example of interrupt control register is shown in the table bellow.

In order to control the data transmission, the empty of transmit buffer is detected and interrupt is not used but transmit interrupt request bit is used.

Table 1.13 Interrupt Control Register Settings

Register	Bit	Function and Setting
SiTIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

1.7 M16C SFR (Peripheral Device Control Register) Setting - DMAC and Interrupt control Register

High-speed data transmission is possible using DMAC. The accessing mode between RAM and UART (transmit buffer or receive buffer) using DMAC is prepared as option.

1.7.1 M32C/87

An example of setting based on the register descriptions in the M32C/87 Group Hardware Manual Rev. 1.00 is shown in the table below.

The DMAC-related registers are CPU internal registers. Use LDC command when data are written to registers.

Table 1.14 DMAC Settings

Register	Bit	Function and Setting
UMiSL	DSEL4 to DSEL0	Select either UARTi transmit interrupt request or UARTi receive interrupt request according to the transfer mode. Change these bits while MDi0 and MDi1 bits are set to 00 (DMA inhibit). Write 1 to DRQ bit at the same time when settings are changed.
	DSR	Write 0 to this bit. Because software trigger is not used
	6	This bit is always read as 0. The write value should always be 0.
	DRQ	Don't write 0 to this bit.
DMD0	MD01 to MD00	Write 01b to these bits when DMA channel 0 is used. (Single transfer)
	BW0	Write 0 to this bit when DMA channel 0 is used. (8 bit)
	RW0	Set the value according to the transmission or reception when DMA channel 0 is used.
	MD11 to MD10	Write 01b to these bits when DMA channel 1 is used. (Single transfer)
	BW1	Write 0 to this bit when DMA channel 1 is used. (8 bit)
	RW1	Set the value according to the transmission or reception when DMA channel 1 is used.
DMD1	MD21 to MD20	Write 01b to these bits when DMA channel 2 is used. (Single transfer)
	BW2	Write 0 to this bit when DMA channel 2 is used. (8 bit)
	RW2	Set the value according to the transmission or reception when DMA channel 2 is used.
	MD31 to MD30	Write 01b to these bits when DMA channel 3 is used. (Single transfer)
	BW3	Write 0 to this bit when DMA channel 3 is used. (8 bit)
	RW3	Set the value according to the transmission or reception when DMA channel 3 is used.
DCTi	15 to 0	Set the number of transfer count of transfer counter.
DRCi	15 to 0	Reload value of transfer count register. Set the number of transfer count.
DMAi	23 to 0	Set the source address or destination address.
DSAi	23 to 0	Set the source address or destination address.
DRAi	23 to 0	Reload value of memory address register. Set the source address or destination address.

The setting example of interrupt control register is shown in the table bellow.

Table 1.15 Interrupt Control Register Settings

Register	Bit	Function and Setting
DMiIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

This sample program for M32C/87 disables DMA control.

1.7.2 M16C/80

An example of setting based on the register descriptions in the M16C/80 Group Hardware Manual Rev. 1.00 is shown in the table below.

The DMAC-related registers are CPU internal registers. Use LDC command when data are written to registers.

Table 1.16 DMAC Settings

Register	Bit	Function and Setting
UMiSL	DSEL4 to DSEL0	Select either UARTi transmit or UARTi receive according to the transfer mode. Change these bits while MDi0 and MDi1 bits are set to 00 (DMA inhibit). Write 1 to DRQ bit at the same time when settings are changed.
	DSR	Write 0 to this bit. Because software trigger is not used
	6	This bit is always read as 0. The write value should always be 0.
	DRQ	Don't write 0 to this bit.
DMD0	MD01 to MD00	Write 01b to these bits when DMA channel 0 is used. (Single transfer)
	BW0	Write 0 to this bit when DMA channel 0 is used. (8 bit)
	RW0	Set the value according to the transmission or reception when DMA channel 0 is used.
	MD11 to MD10	Write 01b to these bits when DMA channel 1 is used. (Single transfer)
	BW1	Write 0 to this bit when DMA channel 1 is used. (8 bit)
	RW1	Set the value according to the transmission or reception when DMA channel 1 is used.
DMD1	MD21 to MD20	Write 01b to these bits when DMA channel 2 is used. (Single transfer)
	BW2	Write 0 to this bit when DMA channel 2 is used. (8 bit)
	RW2	Set the value according to the transmission or reception when DMA channel 2 is used.
	MD31 to MD30	Write 01b to these bits when DMA channel 3 is used. (Single transfer)
	BW3	Write 0 to this bit when DMA channel 3 is used. (8 bit)
	RW3	Set the value according to the transmission or reception when DMA channel 3 is used.
DCTi	15 to 0	Set the number of transfer count of transfer counter.
DRCi	15 to 0	Reload value of transfer count register. Set the number of transfer count.
DMAi	23 to 0	Set the source address or destination address.
DSAi	23 to 0	Set the source address or destination address.
DRAi	23 to 0	Reload value of memory address register. Set the source address or destination address.

The setting example of interrupt control register is shown in the table bellow.

Table 1.17 Interrupt Control Register Settings

Register	Bit	Function and Setting
DMiIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

This sample program for M16C/80 disables DMA control.

1.7.3 M16C/62P

An example of setting based on the register descriptions in the M16C/62P Group Hardware Manual Rev. 2.41 is shown in the table below.

Table 1.18 DMAC Settings

Register	Bit	Function and Setting
UMiSL	DSEL3 to DSEL0	Select either UARTi transmit or UARTi receive according to the transfer mode. Write 0 to DMS bit because the factor is UART transmit or UART reception.
	5 to 4	These bits are always read as 0. The write value should always be 0.
	DMS	Write 0 to this bit because the factor is UART transmit or UART reception.
	DSR	Write 0 to this bit because software trigger is not used
DMiCON	DMBIT	Write 1 to this bit. (8 bit)
	DMASL	Write 0 to these bits. (Single transfer)
	DMAS	DMA request bit. Write 0 to this bit at initialization. (DMA Not requested)
	DMAE	Write 0 to this bit at initialization. (Disable) Write 1 to this bit when DMA is enabled
	DSD	0 is written to this bit at initialization. (Fixed) Select according to the source address
	DAD	0 is written to this bit at initialization. (Fixed) Select according to the destination address
	7 to 6	These bits are always read as 0. The write value should always be 0.
SARi	19 to 0	Set the source address of transfer.
	23 to 20	These bits are always read as 0. The write value should always be 0.
DARi	19 to0	Set the destination address of transfer.
	23 to 20	These bits are always read as 0. The write value should always be 0.
TCRi	15 to 0	Set the transfer count –1.

The setting example of interrupt control register is shown in the table bellow.

Table 1.19 Interrupt Control Register Settings

Register	Bit	Function and Setting
DMiIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disable.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

Note: UART1 is recommended not to use when DMA transfer is used.
When UART1 is in transmit state, DMA request factor select register is assigned to DMA0. When UART1 is in reception state, DMA request factor select register is assigned to DMA1. In order to DMA transfer is implemented, Both DMA0 and DMA1 have to be used and software has to be modified.

1.7.4 M16C/30P

An example of setting based on the register descriptions in the M16C/30P Group Hardware Manual Rev. 1.11 is shown in the table below.

Table 1.20 DMAC Settings

Register	Bit	Function and Setting
UMiSL	DSEL3 to DSEL0	Select either UARTi transmit or UARTi receive according to the transfer mode. Write 0 to DMS bit because the factor is UART transmit or UART reception.
	5 to 4	These bits are always read as 0. The write value should always be 0.
	DMS	Write 0 to this bit because the factor is UART transmit or UART reception.
	DSR	Write 0 to this bit because software trigger is not used
DMiCON	DMBIT	Write 1 to this bit. (8 bit)
	DMASL	Write 0 to these bits. (Single transfer)
	DMAS	DMA request bit. Write 0 to this bit at initialization. (DMA Not requested)
	DMAE	Write 0 to this bit at initialization. (Disable) Write 1 to this bit when DMA is enabled
	DSD	0 is written to this bit at initialization. (Fixed) Select according to the source address
	DAD	0 is written to this bit at initialization. (Fixed) Select according to the destination address
	7 to 6	These bits are always read as 0. The write value should always be 0.
SARi	19 to 0	Set the source address of transfer.
	23 to 20	These bits are always read as 0. The write value should always be 0.
DARi	19 to0	Set the destination address of transfer.
	23 to 20	These bits are always read as 0. The write value should always be 0.
TCRi	15 to 0	Set the transfer count –1.

The setting example of interrupt control register is shown in the table bellow.

Table 1.21 Interrupt Control Register Settings

Register	Bit	Function and Setting
DMiIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

Note: UART1 is recommended not to use when DMA transfer is used.
When UART1 is in transmit state, DMA request factor select register is assigned to DMA0. When UART1 is in reception state, DMA request factor select register is assigned to DMA1. In order to DMA transfer is implemented, Both DMA0 and DMA1 have to be used and software has to be modified.

1.7.5 M16C/29

An example of setting based on the register descriptions in the M16C/29 Group Hardware Manual Rev. 1.00 is shown in the table below.

Table 1.22 DMAC Settings

Register	Bit	Function and Setting
UMiSL	DSEL3 to DSEL0	Select either UARTi transmit or UARTi receive according to the transfer mode. Write 0 to DMS bit because the cause is UART transmit or UART reception.
	5 to 4	These bits are always read as 0. The write value should always be 0.
	DMS	Write 0 to this bit because the cause is UART transmit or UART reception.
	DSR	Write 0 to this bit because software trigger is not used
DMiCON	DMBIT	Write 1 to this bit. (8 bit)
	DMASL	Write 0 to these bits. (Single transfer)
	DMAS	DMA request bit. Write 0 to this bit at initialization. (DMA Not requested)
	DMAE	Write 0 to this bit at initialization. (Disable) Write 1 to this bit when DMA is enabled
	DSD	0 is written to this bit at initialization. (Fixed) Select according to the source address
	DAD	0 is written to this bit at initialization. (Fixed) Select according to the destination address
	7 to 6	These bits are always read as 0. The write value should always be 0.
SARi	19 to 0	Set the source address.
	23 to 20	These bits are always read as 0. The write value should always be 0.
DARi	19 to0	Set the destination address.
	23 to 20	These bits are always read as 0. The write value should always be 0.
TCRi	15 to 0	Set the transfer count –1.

The setting example of interrupt control register is shown in the table bellow.

Table 1.23 Interrupt Control Register Settings

Register	Bit	Function and Setting
DMiIC	ILVL2 to ILVL0	Write 000b to these bits. (Level 0: Interrupt is disabled.)
	IR	If this bit is 1, Interrupt is requested. Write 0 to this bit according to the needs.

Note 1: UART1 is recommended not to use when DMA transfer is used.
When UART1 is in transmit state, DMA request cause select register is assigned to DMA0. When UART1 is in reception state, DMA request cause select register is assigned to DMA1. In order to DMA transfer is implemented, Both DMA0 and DMA1 have to be used and software has to be modified.

1.7.6 R8C/25

There isn't any DMAC function.

2. Sample Programs

Two or more of the same devices can be connected to the serial bus and controlled.

The sample programs execute the following:

- Data read processing
- Data write processing
- Write-protection processing through software protection
- Status read processing

2.1 Overview of Software Operations

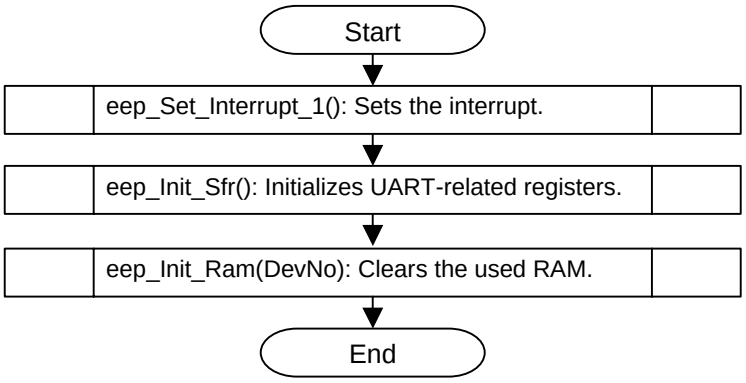
The operations roughly described below are performed.

(1) The driver initialization processing acquires the resources to be used by the driver and initializes them.
At this point, control signals (Port/CLK/TxD) connected to the serial EEPROM come to High.
(2) Function calls perform the following operations.
(a) The signals of pins connected to the serial EEPROM output to make serial EEPROM inactive state.
(b) Execute the processing of each function.
(c) Control signals (Port/CLK/TxD) connected to the serial EEPROM come to high.

2.2 Detailed Description of Functions

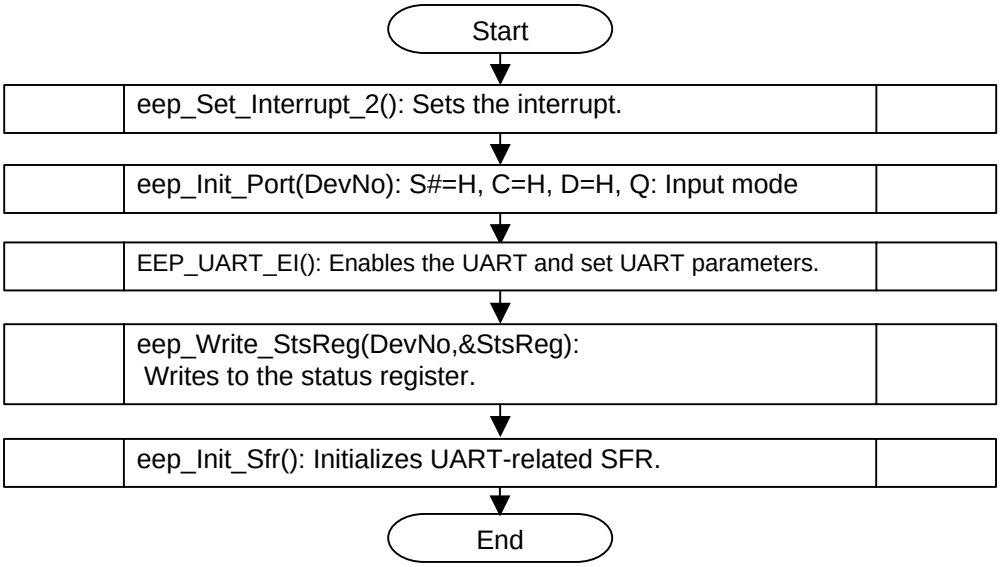
2.2.1 Driver Initialization Processing

Function Name
EEPROM driver initialization processing void eep_Init_Driver(void)
Arguments
None
Return Values
None
Operations
Initializes the EEPROM driver. Initializes the SFR for EEPROM control. Performs the following processing for each device. -Opens the EEPROM control ports. -Initializes the EEPROM control RAM. Call this function once at system activation.
Notes
None



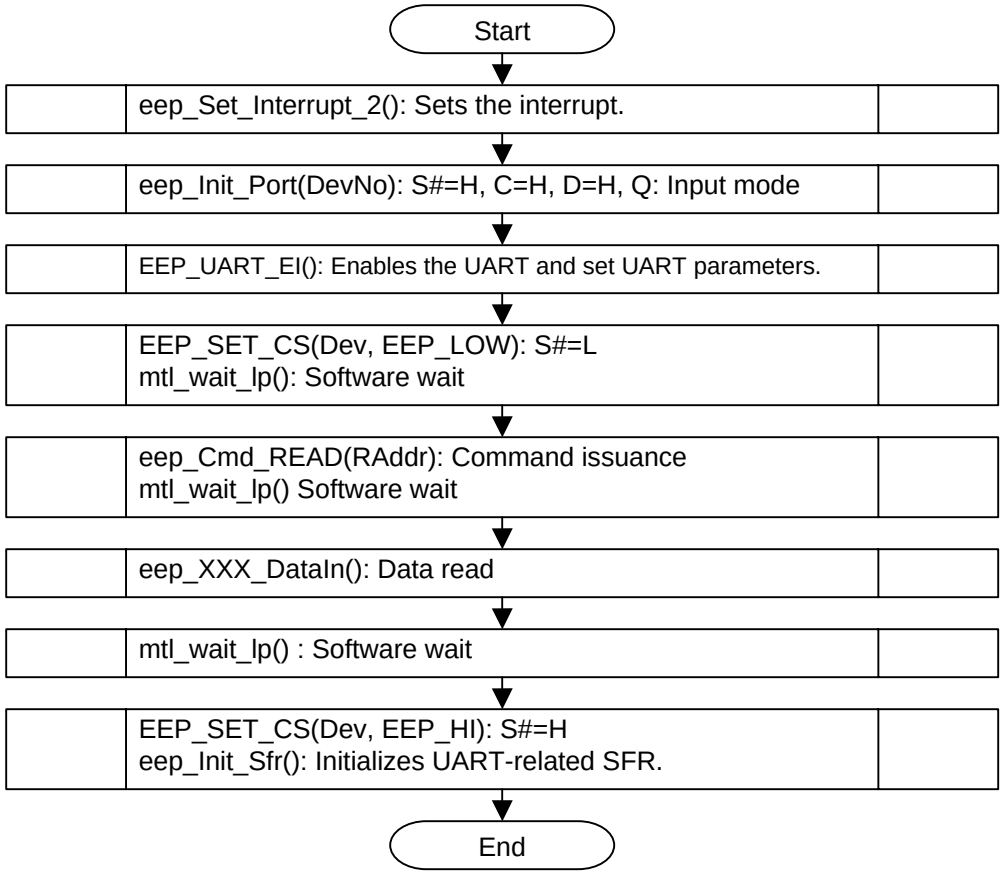
2.2.2 Write-Protection Setting Processing

Function Name			
Write-protection setting processing signed short eep_Write_Protect(unsigned char DevNo, unsigned char WpSts)			
Arguments			
unsigned char	DevNo	;	Device number
unsigned char	WpSts	;	Write-protection setting data
Return Values			
Returns the write-protection setting result.			
EEP_OK		;	Successful operation
EEP_ERR_PARAM		;	Parameter error
EEP_ERR_OTHER		;	Other error
Operations			
Makes the write-protection setting. Set the write-protection setting data (WpSts) as follows:			
EEP_WP_NONE		;	No protection
EEP_WP_UPPER_QUART		;	Upper-quarter protection setting
EEP_WP_UPPER_HALF		;	Upper-half protection setting
EEP_WP_WHOLE_MEM		;	Whole memory protection setting
Notes			
None			



2.2.3 Data Read Processing

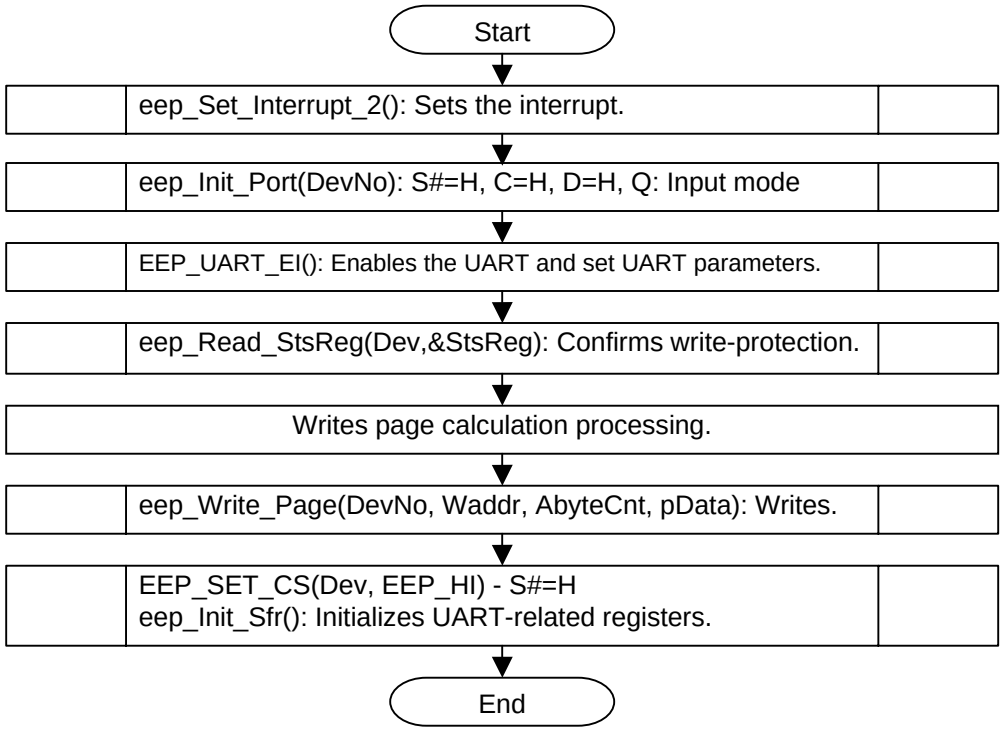
Function Name			
Data read processing signed short eep_Read_Data(unsigned char DevNo, unsigned short RAddr, unsigned short RCnt, unsigned char * pData)			
Arguments			
unsigned char	DevNo	;	Device number
unsigned short	RAddr	;	Read start address
unsigned short	RCnt	;	Number of bytes to be read
unsigned char FAR*	pData	;	Read data storage buffer pointer
Return Values			
Returns the read result.			
EEP_OK		;	Successful operation
EEP_ERR_PARAM		;	Parameter error
EEP_ERR_HARD		;	Hardware error
EEP_ERR_OTHER		;	Other error
Operations			
Reads data from EEPROM in bytes. Reads data from the specified address for the specified number of bytes.			
Notes			
The maximum write address is EEPROM size − 1.			



2.2.4 Data Write Processing

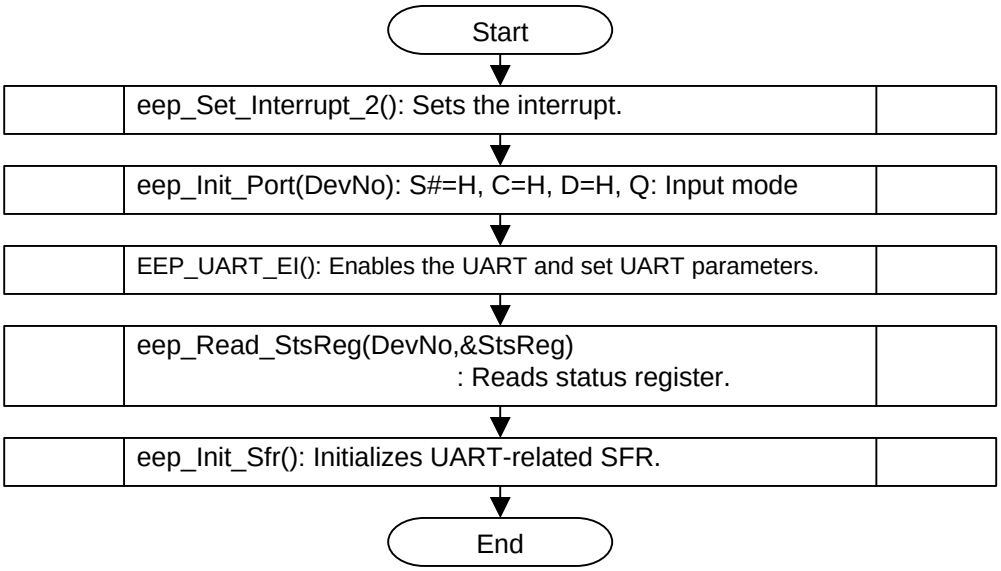
Function Name			
Data write processing signed short eep_Write_Data(unsigned char DevNo, unsigned short WAddr, unsigned short WCnt, unsigned char FAR* pData)			
Arguments			
unsigned char	DevNo	;	Device number
unsigned short	WAddr	;	Write start address
unsigned short	WCnt	;	Number of bytes to be written
unsigned char FAR*	pData	;	Write data storage buffer pointer
Return Values			
Returns the write result.			
EEP_OK		;	Successful operation
EEP_ERR_PARAM		;	Parameter error
EEP_ERR_HARD		;	Hardware error
EEP_ERR_WP		;	Write-protection error
EEP_ERR_OTHER		;	Other error
Operations			
Writes data to EEPROM in bytes. Writes data from the specified address for the specified number of bytes.			
Notes			
EEPROM can be written to only when write-protection has been canceled. The maximum write address is EEPROM size – 1.			

In a write to the serial EEPROM, address translation is performed and the page rewrite method is used.



2.2.5 Status Read Processing

Function Name			
Status read processing signed short eep_Read_Status(unsigned char DevNo, unsigned char * pStatus)			
Arguments			
unsigned char	DevNo	;	Device number
unsigned char FAR*	pStatus	;	Read status storage buffer
Return Values			
Returns the status register acquisition result.			
EEP_OK		;	Successful operation
EEP_ERR_PARAM		;	Parameter error
EEP_ERR_HARD		;	Hardware error
EEP_ERR_OTHER		;	Other error
Operations			
Reads the status. Reads from the status register. The following information is stored in the read status storage buffer (pStatus). Memory size ≤ 512 bytes Bits 7 to 4: Reserved (All 1) Bits 3, 2: BP1, BP0 00: No protection 01: Upper-quarter protection 10: Upper-half protection 11: Whole memory protection Bit 1: WEL 0: Write disabled 1: Write enabled Bit 0: WIP 1: During write operation Memory size > 512 bytes Bit 7: SRWD 0: Status register can be changed 1: Status register cannot be changed Bits 6 to 4: Reserved (All 0) Bits 3, 2: BP1, BP0 00: No protection 01: Upper-quarter protection 10: Upper-half protection 11: Whole memory protection Bit 1: WEL 0: Write disabled 1: Write enabled Bit 0: WIP 1: During write operation			
Notes			
None			



2.3 Return Value Definition

```
#define EEP_OK          (signed short)( 0)/* Successful operation    */
#define EEP_ERR_PARAM   (signed short)(-1)/* Parameter error         */
#define EEP_ERR_HARD    (signed short)(-2)/* Hardware error          */
#define EEP_ERR_WP      (signed short)(-3)/* Write-protection error  */
#define EEP_ERR_OTHER   (signed short)(-4)/* Other error             */
```

2.4 User Setting Examples

Setting examples when using the Renesas Technology MCU M16C/62P are shown below.

The location where a setting should be made is indicated by the comment of /** SET **/ in each file.

2.4.1 eep.h

(1) Definition of the number of devices used and device numbers

Specify the number of devices to be used and assign a number for each device.
In the example below, one device is used and 0 is assigned as the device number.
When using three or more, eep_io.h needs to be modified in addition to this file.

```
/*-------------------------------------------------------------------------------*/
/*  Define the number of the required serial EEPROM devices.(1 to N devices)     */
/*  Define the device number in accordance with the number of serial EEPROM devices */
/* to be connected.                                                              */
/*-------------------------------------------------------------------------------*/
/* Define number of devices */
#define EEP_DEV_NUM        1      /* 1 device                                    */

/* Define No. of slots */
#define EEP_DEV0           0      /* Device 0                                    */
#define EEP_DEV1           1      /* Device 1                                    */
```

(2) Definition of device used

Specify the device to be used.
In the example below, 4k bits device is used.

```
/*-------------------------------------------------------------------------- */
/*  Define the serial EEPROM device.                                         */
/*-------------------------------------------------------------------------- */
//#define EEP_SIZE_002K       /*   2kbit  (256 Byte)     */
#define EEP_SIZE_004K         /*   4kbit  (512 Byte)     */
//#define EEP_SIZE_008K       /*   8kbit  (  1kByte)     */
//#define EEP_SIZE_016K       /*  16kbit  (  2kByte)     */
//#define EEP_SIZE_032K       /*  32kbit  (  4kByte)     */
//#define EEP_SIZE_064K       /*  64kbit  (  8kByte)     */
//#define EEP_SIZE_128K       /* 128kbit  ( 16kByte)     */
//#define EEP_SIZE_256K       /* 256kbit  ( 32kByte)     */
```

(3) Definitions the way of interrupt setting of UART or DMA

Define the way of transmit interrupt control process.

This software controls the transmission processing by disabling the Interrupt Priority Select Bits and utilizing Interrupt Request Bit (IR) in Interrupt Control Register of UART or DMA.

The method of the interrupt disabling can be selected by the following three ways.

Select one of them according to the system.

Case 1. Set in the upper system and not setting in the device driver.
#define EEP_IC_SETTING0 should be validated.

Case 2. Set when the device driver is initialized – in executing “eep_Init_Driver()”.
#define EEP_IC _SETTING1 should be validated.

Case 3. Set when SI/O transfer – in executing “eep_Read_Data()”, “eep_Write_Data()”.
#define EEP_IC _SETTING2 should be validated.

Case 2 and 3 can be validated at the same time.

Precaution

The followings are the interrupt setting sequence when the above Case 2 and/or 3 are selected:

1. Disable interrupt (DI)
2. Disable the Interrupt Priority Select Bits and clear the Interrupt Request Bit (IR) of Interrupt Control Register for UART or DMA.
3. Enable interrupt (EI)

Be careful when interrupts enable flag (I flag) is managed by a higher system.

```
/*-----------------------------------------------------------------------*/
/* The setting method of the interrupt when "EEP_IC_SETTING1" and
"EEP_IC_SETTING2" are   */
/*  selected is as follows.                                              */
/*  Interrupt disable (DI) -> interrupt setting -> interrupt enable (EI)   */
/*  When manage an interrupt enable flag (I flag) by a higher system, please
be careful.    */
/*  When interrupt it by a higher system and manage it, please choose
"EEP_IC_SETTING0".   */
/*-----------------------------------------------------------------------*/
#define EEP_IC_SETTING0       /* Doesn't set in this driver                */
//#define EEP_IC_SETTING1     /* When the driver is initialized, it sets   */
//#define EEP_IC_SETTING2     /* When the resource is used, it sets        */
```

2.4.2 eep_sfr.h

Rename from eep_sfr.h.xxx (the header corresponding to the MCU) to eep_sfr.h and use it.

In the example below, the M16C/62P is used.

The sample program shows a description example in which UART 0 is used as the resource of the clock synchronous serial I/O. When DMAC is used it shows a description example in which DMA 0 is used.

(1)UART resource

```
/*----------------- UART definitions -----------------*/
#define EEP_UART_STIC   s0tic /* UART TX interrupt control register        */

#define EEP_UART_TXBUF  u0tb  /* UART transmit buffer register             */
#define EEP_UART_TXBUFL u0tbl /* UART transmit buffer register(lower 8bit) */
#define EEP_UART_RXBUF  u0rb  /* UART receive buffer register              */
#define EEP_UART_BRG    u0brg /* UART bit rate generator                   */
#define EEP_UART_MR     u0mr  /* UART transmit/receive mode register       */
#define EEP_UART_C0     u0c0  /* UART transmit/receive control register 0  */
#define EEP_UART_C1     u0c1  /* UART transmit/receive control register 1  */

#define EEP_UART_TXEND  txept_u0c0  /* UART TX Reg. empty flag             */
#define EEP_UART_TXNEXT ir_s0tic /* UART TX complete flag                  */
#define EEP_UART_TI     ti_u0c1  /* UART TX complete flag                  */
#define EEP_UART_RXNEXT ri_u0c1  /* UART RX complete flag                  */
#define EEP_UART_IRS    u0irs /* UART transmit interrupt cause select flag */
#define EEP_UART_RRM    u0rrm /* UART continuous receive mode enable flag  */
```

If another resource is used, make additions or modify the above program. Accordingly, also make additions or modify the /* UART setting */ definition with reference to section 1.6, M16C SFR (Peripheral Device Control Register) Setting - Clock Synchronous serial I/O and Interrupt control Register

(2) DMAC resource

```
/*----------------- DMAC definitions -----------------*/
#ifdef EEP_DMA_ON
#define EEP_DMA_DMIC    dm0ic    /* DMA interrupt control register        */

#define EEP_DMA_SL      dm0sl    /* DMA request cause select register     */
#define EEP_DMA_CON     dm0con   /* DMA control register                  */
#define EEP_DMA_SAR     sar0     /* DMA source pointer                    */
#define EEP_DMA_DAR     dar0     /* DMA destination pointer               */
#define EEP_DMA_TCR     tcr0     /* DMA transfer counter                  */
#define EEP_DMA_END     ir_dm0ic /* DMA interrupt request flag            */
```

If another resource is used, make additions or modify the above program. Accordingly, also make additions or modify the /* DMA setting */ definition with reference to section 1.7, M16C SFR (Peripheral Device Control Register) Setting - DMAC and Interrupt control Register

2.4.3 eep_io.h

Rename from eep_io.h.xxx (the header corresponding to the MCU) to eep_io.h and use it.

(1)Definition of resources used by UART or DMA of MCU used

Specify the resources of the MCU to be used.

In the example below, the clock synchronous serial I/O is used.

```
/*-------------------------------------------------------------------------- */
/*  Define the combination of the MCU's resources.                           */
/*-------------------------------------------------------------------------- */
//#define EEP_OPTION_1           /* Low speed   */ /* UART     */
#define EEP_OPTION_2             /* High speed  */ /* UART + DMAC */
```

(2) Definition of control ports of MCU used

Specify the control ports of the MCU to be used.

In the example below, RxD, TxD, CLK, and S# of the clock synchronous serial I/O are assigned.

When two devices are connected, make a definition regarding CS1.

When using three or more, eep.h needs to be modified in addition to this file.

```
/*-------------------------------------------------------------------------- */
/*  Define the control port.                                                 */
/*-------------------------------------------------------------------------- */
#define EEP_P_DATAO     p6_3           /* EEPROM DataOut              */
#define EEP_P_DATAI     p6_2           /* EEPROM DataIn               */
#define EEP_P_CLK       p6_1           /* EEPROM CLK                  */
#define EEP_D_DATAO     pd6_3          /* EEPROM DataOut              */
#define EEP_D_DATAI     pd6_2          /* EEPROM DataIn               */
#define EEP_D_CLK       pd6_1          /* EEPROM CLK                  */

#define EEP_P_CS0       p10_5    /* EEPROM CS0 (Negative-true logic) */
#define EEP_D_CS0       pd10_5   /* EEPROM CS0 (Negative-true logic) */
#if (EEP_DEV_NUM > 1)
#define EEP_P_CS1       p10_1    /* EEPROM CS1 (Negative-true logic) */
#define EEP_D_CS1       pd10_1   /* EEPROM CS1 (Negative-true logic) */
#endif   /* #if (EEP_DEV_NUM > 1) */
```

2.4.4 mtl_com.h (Common Header File)

Rename from mtl_com.h.xxx (the header corresponding to the MCU) to mtl_com.h and use it.

In the example below, the M16C/62P is used.

(1)Definition of OS header file

This software is an OS-independent program.

In the example below, the OS is not used. (The system call of MR30 is not used.)

```
/* In order to use wai_sem/sig_sem/dly_tsk for microITRON (Real-Time OS)-
compatible, */
/* include the OS header file that contains the prototype declaration.
/* When not using the OS, put the following 'define' and 'include' as comments.
  */
//#define MTL_OS_USE                /* Use OS            */
//#include <RTOS.h>                 /* OS header file    */
//#include "mtl_os.h"
```

(2) Definition of header file specifying common access area

Includes the header file in which the MCU registers are defined.

This file needs to be included because it is mainly used by the device driver for controlling the ports.

In the example below, the M16C/62P header file is included. Include the header file in accordance with the MCU.

```
/* In order to use definitions of MCU SFR area,                    */
/* include the header file of MCU SFR definition.                  */
#include "sfr62p.h"                          /* definition of MCU SFR   */
```

(3) Definition of loop timer

Include the header file below if software timer is used.

It is mainly used as wait time of device driver.

When software timer is not used, the define statement below should be a comment.

In the example below, software timer is used.

```
/* When not using the loop timer, put the following 'include' as comments.  */
#include "mtl_tim.h"
```

(4) Definition of endian type

This is the setting of FAT file system library for M16C family.

Specify the little endian if M16C family is used.

```
/* When using M16C or SuperH for Little Endian setting, define it. */
/* When using other MCUs, put 'define' as a comment.               */
#define MTL_MCU_LITTLE                /* Little endian           */
```

(5) The fast processes of mtl_endi.c

When Little Endian is specified and it is defined, it performs the fast processes of mtl_endi.c.

```
/* When using M16C, define it.                                     */
/* It performs the fast processes of 'mtl_endi.c'.                 */
#define MTL_ENDI_HISPEED         /* Uses the high-speed function.  */
```

(6) Specification of standard library type used

Specify the standard library type used. When the processing below is used in the library provided with the compiler, the define statement below should be a comment.

The optimized library enabling high-speed processing is prepared.

The following example shows the standard library set with the compiler.

```
/* Specify the standard library type used.                              */
/* When the processing below is used in the library provided with the   */
/* compiler, the define statement below should be a comment.            */
/* memcmp() / memcpy() / memset() / strcat() / strcmp() / strcpy() / strlen()*/
//#define MTL_USER_LIB                    /* Optimized library usage          */
```

(7)Definition of RAM area accessed by processing group used

Define the RAM area to be accessed by the user process group.

Standard functions and efficient operations for processes are applied.

If neither of them is defined, error is output when software is compiled

M16C/62P and M16C/29 are possible to define either MTL_MEM_FAR or MTL_MEM_NEAR.

The following is a definition example of MTL_MEM_NEAR when M16C/60, M16C/30, M16C/20 or R8C is used.

```
/* Define the RAM area to be accessed by the user process.              */
/* Efficient operations for standard functions and processes are applied.   */
//#define MTL_MEM_FAR         /* Supports Far RAM area of M16C/60
#define MTL_MEM_NEAR       /* Supports Near RAM area.       (Others)       */
```

Set only the above define statement and do not make any other modifications.

2.4.5 mtl_tim.h

(1) Definition of software timer

Sets the internal software timer used.

The following reference values are obtained at 24-MHz operation without wait.

The setting should be made in accordance with the system.

```
/* Define the counter value for the timer.                              */
/* Specify according to the user MCU, clock and wait requirements.      */
/*  Setting for 24MHz no wait                                           */
#define MTL_T_1US                          1    /* loop Number of   1us    */
#define MTL_T_2US                          2    /* loop Number of   2us    */
#define MTL_T_4US                          5    /* loop Number of   4us    */
#define MTL_T_5US                          6    /* loop Number of   5us    */
#define MTL_T_10US                        13    /* loop Number of  10us    */
#define MTL_T_20US                        28    /* loop Number of  20us    */
#define MTL_T_30US                        43    /* loop Number of  30us    */
#define MTL_T_50US                        72    /* loop Number of  50us    */
#define MTL_T_100US                      145    /* loop Number of  100us   */
#define MTL_T_200US                      293    /* loop Number of  200us   */
#define MTL_T_300US                     439     /* loop Number of  300us   */
#define MTL_T_400US     ( MTL_T_200US  *  2 )   /* loop Number of  400us   */
#define MTL_T_1MS                       1471    /* loop Number of  1ms     */
```

2.5 Usage Notes

The sample programs show description example in which UART 0 is used as the resource of the clock synchronous serial I/O. When DMAC is used it shows a description example in which DMA 0 is used.

When using another resource, set the software in accordance with the hardware.

2.6 Notes at Embedment

To embed the sample programs, include eep.h.

2.7 Usage of Another M16C Family MCU

Usage of another M16C family MCU is supported easily.

The following files must be prepared.

(1) I/O module common definition equivalent of eep_io.h.xxx
Define the I/O pins to be used with reference to the SFR header of the MCU used.
(2) SFR common definition equivalent of eep_sfr.h.xxx
Define the UART/DMA to be used with reference to the SFR header of the MCU used.
(3) Header definition equivalent of mtl_com.h.xxx
Create and define a header for the MCU used.

Create the above files with reference to the provided programs.

In addition, specify the created header in eep_io.h, eep_sfr.h, and mtl_com.h.

2.8 File Configuration

\com	<DIR>		Directory for common functions
	mtl_com.c		Various definitions for common functions
	mtl_com.h.common		Common header file
	mtl_com.h.m16c26		Common header file M16C/26
	mtl_com.h.m16C29		Common header file M16C/29
	mtl_com.h.m16C30P		Common header file M16C/30P
	mtl_com.h.m16c62n		Common header file M16C/62N
	mtl_com.h.m16c62p		Common header file M16C/62P
	mtl_com.h.m16c80		Common header file M16C/80
	mtl_com.h.m30245		Common header file M16C/24(M30245)
	mtl_com.h.m32c87		Common header file M32C/87
	mtl_com.h.r8c23		Common header file R8C/23
	mtl_com.h.r8c25		Common header file R8C/25
	mtl_mem.c		Common function
	mtl_tim.c	mtl_tim.h	Common function
	mtl_tim.h.sample		Common header file (Reference)
\seep_spi	<DIR>		Serial EEPROM directory
	eep.h		Driver common definition
	eep_io.c		I/O module
	eep_io.h.m16c29		I/O module common definition M16C/29
	eep_io.h.m16c30p		I/O module common definition M16C/30P
	eep_io.h.m16c62n		I/O module common definition M16C/62N
	eep_io.h.m16c62p		I/O module common definition M16C/62P
	eep_io.h.m16c80		I/O module common definition M16C/80
	eep_io.h.m30245		I/O module common definition M16C/24(M30245)
	eep_io.h.m32c87		I/O module common definition M32C/87
	eep_io.h.r8c23		I/O module common definition R8C/23
	eep_io.h.r8c25		I/O module common definition R8C/25
	eep_sfr.h.m16c26		SFR common definition M16C/26
	eep_sfr.h.m16c29		SFR common definition M16C/29
	eep_sfr.h.m16c30p		SFR common definition M16C/30P
	eep_sfr.h.m16c62n		SFR common definition M16C/62N
	eep_sfr.h.m16c62p		SFR common definition M16C/62P
	eep_sfr.h.m16c80		SFR common definition M16C/80
	eep_sfr.h.m30245		SFR common definition M16C/24(M30245)
	eep_sfr.h.m32c87		SFR common definition M32C/87
	eep_sfr.h.r8c23		SFR common definition R8C/23
	eep_sfr.h.r8c25		SFR common definition R8C/25
	eep_usr.c		Driver user I/F module
\sample	<DIR>		Sample program directory
	testmain.c		Sample program for operation verification Use this for operation verification.
	common.c	common.h	Various definitions for common functions

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
2.01	Jan.22.08	—	First edition issued
2.02	Jan.28.08	1	Software Version added

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