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H8/300L SLP Series

Serial Data Reception in Synchronous Mode

Introduction

Four bytes of 8-bit data is received using the serial data transfer function in synchronous mode. Data is received in the LSB first format starting from the least significant bit of data.

Target Device

H8/38024

Contents

1. Specifications

1. As shown in figure 1.1, four bytes of 8-bit data is received using the serial data transfer function in synchronous mode.
2. An external clock is used as a transfer clock.
3. The data length of receive data is eight bits and data is received in the LSB first format starting from the least significant bit of data.

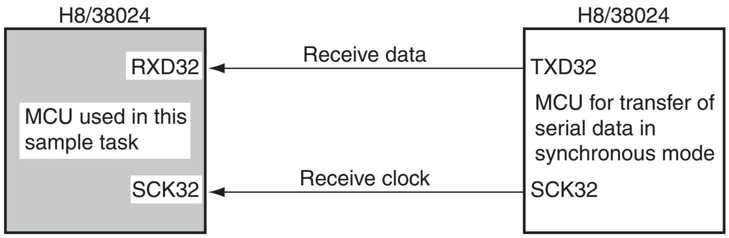
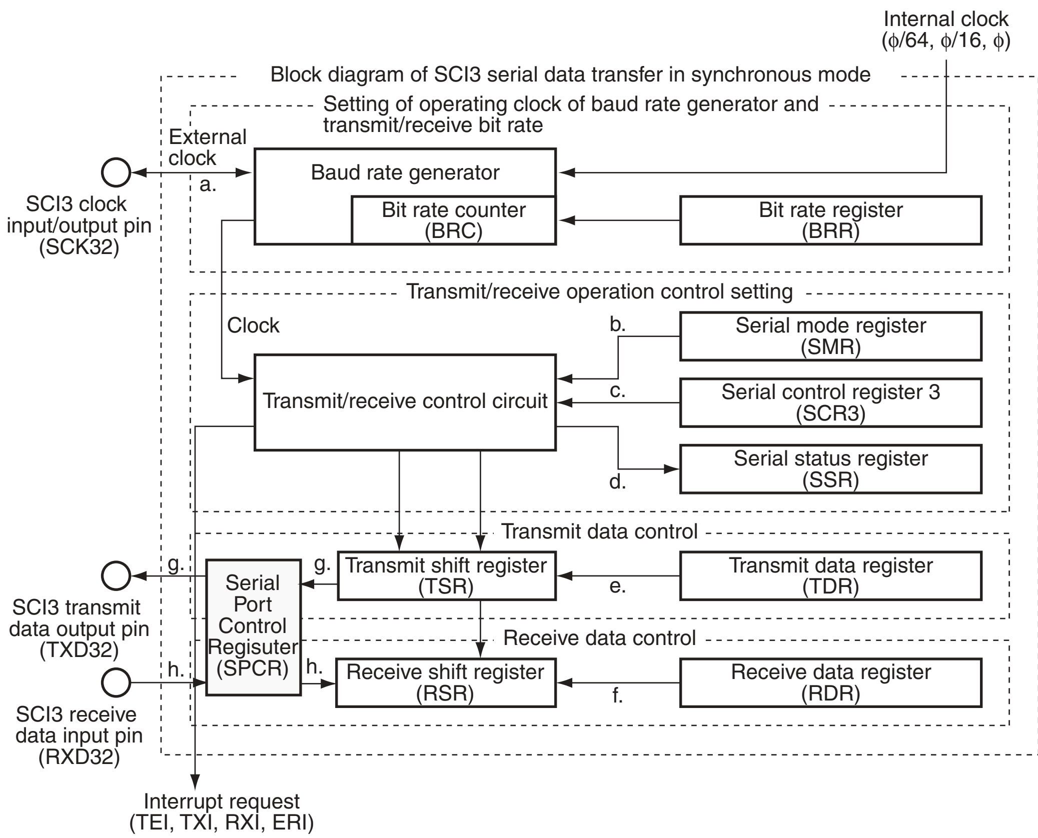


Figure 1.1 Serial Data Reception in Synchronous Mode

2. Description of Functions

1. In this sample task, serial data is received in synchronous mode using the Serial Communication Interface (SCI). Figure 2.1 shows a block diagram of serial data reception in synchronous mode which is described below.
   — Only overrun errors are detected as receive errors.
   — In synchronous mode, the data length is eight bits.
   — The receive shift register (RSR) is a register used to receive serial data. Serial data input to RSR from the RXD32 pin is set in the order in which it is received, starting from the LSB (bit 0), and converted to parallel data. When one byte of data is received, it is transferred to RDR automatically. RSR cannot be read from or written to directly by the CPU.
   — The receive data register (RDR) is an 8-bit register that stores received serial data. When reception of one byte of data is finished, the received data is transferred from RSR to RDR, and the receive operation is completed. RSR is then enabled for reception. RSR and RDR are double-buffered, allowing consecutive receive operations. RDR is a read-only register, and cannot be written to by the CPU.
   — The transmit shift register (TSR) is a register used to transmit serial data. Transmit data is first transferred from TDR to TSR, and serial data transmission is carried out by sending the data to the TXD32 pin in order, starting from the LSB (bit 0). When one byte of data is transmitted, the next byte of transmit data is automatically transferred from TDR to TSR, and transmission is started. Data transfer from TDR to TSR is not performed if no data has been written to TDR (if bit TDRE is set to 1). TSR cannot be read from or written to directly by the CPU.
   — The transmit data register (TDR) is an 8-bit register that stores transmit data. When TSR is found to be empty, the transmit data written in TDR is transferred to TSR, and serial data transmission is started. Continuous transmission is possible by writing the next transmit data to TDR during TSR serial data transmission. TDR can be read from or written to by the CPU at any time.
   — The serial mode register (SMR) is an 8-bit register used to set the serial data transfer format and to select the clock source for the internal baud rate generator.
   — Serial control register 3 (SCR3) is an 8-bit register for selecting transmit/receive operation and the transmit/receive clock source.
   — The serial status register (SSR) contains status flags that indicate the operational status of SCI3, and transmit/receive multiprocessor bits. Bits TDRE, RDRF, OER, PER, and FER can only be cleared to 0.
   — The transfer clock can be selected from a total of four clocks: three internal clocks and an external clock. When an internal clock is selected, the SCK32 pin functions as an output pin. When clock consecutive output mode is selected, the selected clock is consecutively output from the SCK32 pin. When an external clock is selected, the SCK32 pin functions as an input pin.
   — In this sample task, the source of the transfer clock is set to external clock.

— The serial port control register (SPCR) is used to switch P42/TXD32 pin function. In this sample task, P42/TXD32 pin is set to TXD32 output pin.
— As the SCI3 data transfer format, an 8-bit data can be selected, and data is transmitted in the LSB-first format, starting from the least significant bit. Transmit data is output from one falling edge to the next rising edge of the transfer clock. Receive data is latched at the rising edge of the transfer clock.
— In this sample task, the operation mode is set to an 8-bit mode, and 8-bit data is received.
— The SCI3 clock (SCK32) pin is the SCI3 clock I/O pin.
— The SCI3 receive data input (RXD32) pin is the input pin for SCI3 receive data.
— The serial port control register (SPCR) is an 8-bit register to control P42/TXD32 pin. In this sample task, RXD32 pin input data is set not to be inverted.



Notes: a. The external clock is received.
b. The serial data transfer format is set.
c. The transmit/receive operation and clock input pin in synchronous mode are selected.
d. The status flags (receive data register full, overrun error) indicate the operation status of SCI3.
e. Detecting that TSR is "empty", transmit data written in TDR is transferred to TSR.
f. The received data is transferred from RSR to RDR when receiving of one-byte data is completed.
g. Transmit data.
h. Receive data.

Figure 2.1 Block Diagram of Serial Data Reception in Synchronous Mode

2. Table 2.1 shows the assignment of functions in this sample task. Serial data is received in synchronous mode by assigning the functions as shown in table 2.1.

Table 2.1 Function Assignment

Function	Assignment
RSR	A register to receive serial data
RDR	A register to store receive data
SMR	Sets the serial data transfer format
SSR	Status flags to indicate operation status of SCI3
BRR	Sets receive bit rate
SCR3	Enables receive operation, sets RXD32 input pin, and sets SCK32 pin function as clock input pin
SCK32	SCI3 clock input pin
RXD32	SC13 receive data input pin

3. Principle of Operation

1. Figure 3.1 illustrates the principle of operation of this sample task. Serial data is received in synchronous mode by hardware and software processing of H8/38024 as shown in figure 3.1.

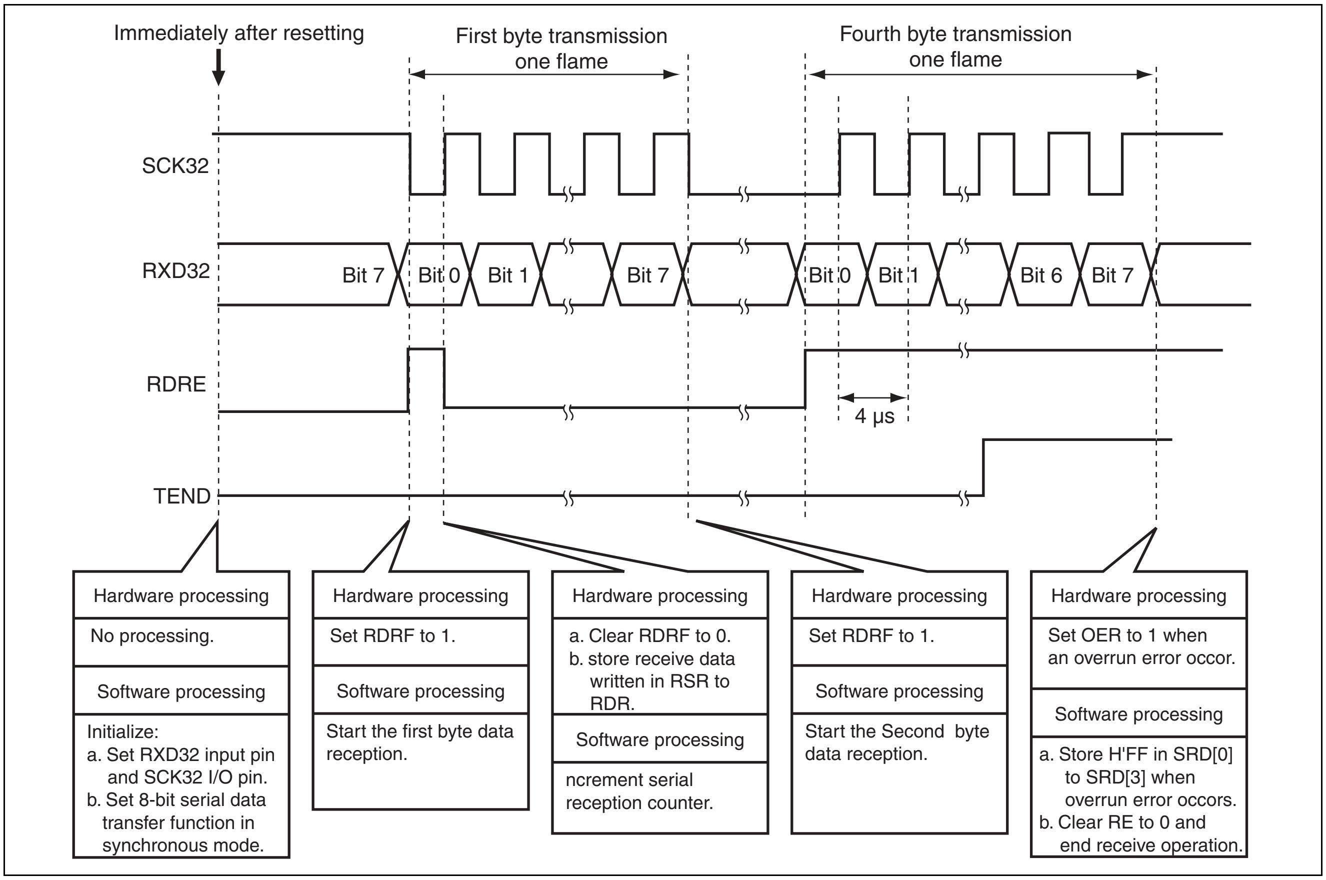


Figure 3.1 Operation Principle of Serial Data Reception in Synchronous mode

4. Description of Software

4.1 Modules

Table 4.1 describes the module in this sample task.

Table 4.1 Description of Modules

Module	Label	Function
Main Routine	main	Sets serial data reception in synchronous mode, stores H'FF in SRD[0] to SRD[3] when a receive error occurs, and ends operation when 4 byte data is received.

4.2 Arguments

Table 4.2 describes the arguments used in this sample task.

Table 4.2 Description of Arguments

Arguments	Function	Used in	Data Length	Input/ Output
SRD[0] to SRD[3]	Serial receive data in synchronous mode	Main Routine	1 byte	Output

4.3 Internal Registers

Table 4.3 describes the internal registers in this sample task.

Table 4.3 Description of Internal Registers

Register		Function	Address	Setting
SPCR	SCINV2	Serial Port Control Register (RXD32 Pin Input Data Inversion Switch) If SCINV2 = 0, RXD32 input data is not inverted. If SCINV2 = 1, RXD32 input data is inverted.	H'FF91 Bit 2	0
SMR	COM	Serial Mode Register (Communication Mode) If COM = 0, the communication mode is set to asynchronous mode. If COM = 1, the communication mode is set to synchronous mode.	H'FFA8 Bit 7	1
	MP	Serial Mode Register (Multi-Processor Mode) In synchronous mode, MP is set to 0.	H'FFA8 Bit 2	0
BRR		Bit Rate Register If BRR = H'04, the receive bit rate matched to the external operating clock is set to 250kbps.	H'FFA9	H'04
SCR3	RE	Serial Control Register 3 (Receive Enable) If RE = 0, receive operation is disabled. If RE = 1, receive operation is enabled.	H'FFAA Bit 4	1
	CKE1 CKE0	Serial Control Register 3 (Clock Enable 1, 0) If CKE1 = 1 and CKE0 = 0, the clock source is set to an external clock and SCK32 pin function to clock input pin	H'FFAA Bit 1 Bit 0	CKE1 = 1 CKE0 = 0

Register		Function	Address	Setting
SSR	RDRF	Serial Status Register (Receive Data Register Full) If RDRF = 0, receive data is not stored in RDR. If RDRF = 1, receive data is stored in RDR.	H'FFAC Bit 6	0
	OER	Serial Status Register (Overrun Error) If OER = 0, data reception is in progress or completed. If OER = 1, an overrun error has occurred during reception.	H'FFACB Bit 5	0
RDR		Receive Data Register An 8-bit register to store receive data.	H'FFAD	–

4.4 Description of RAM

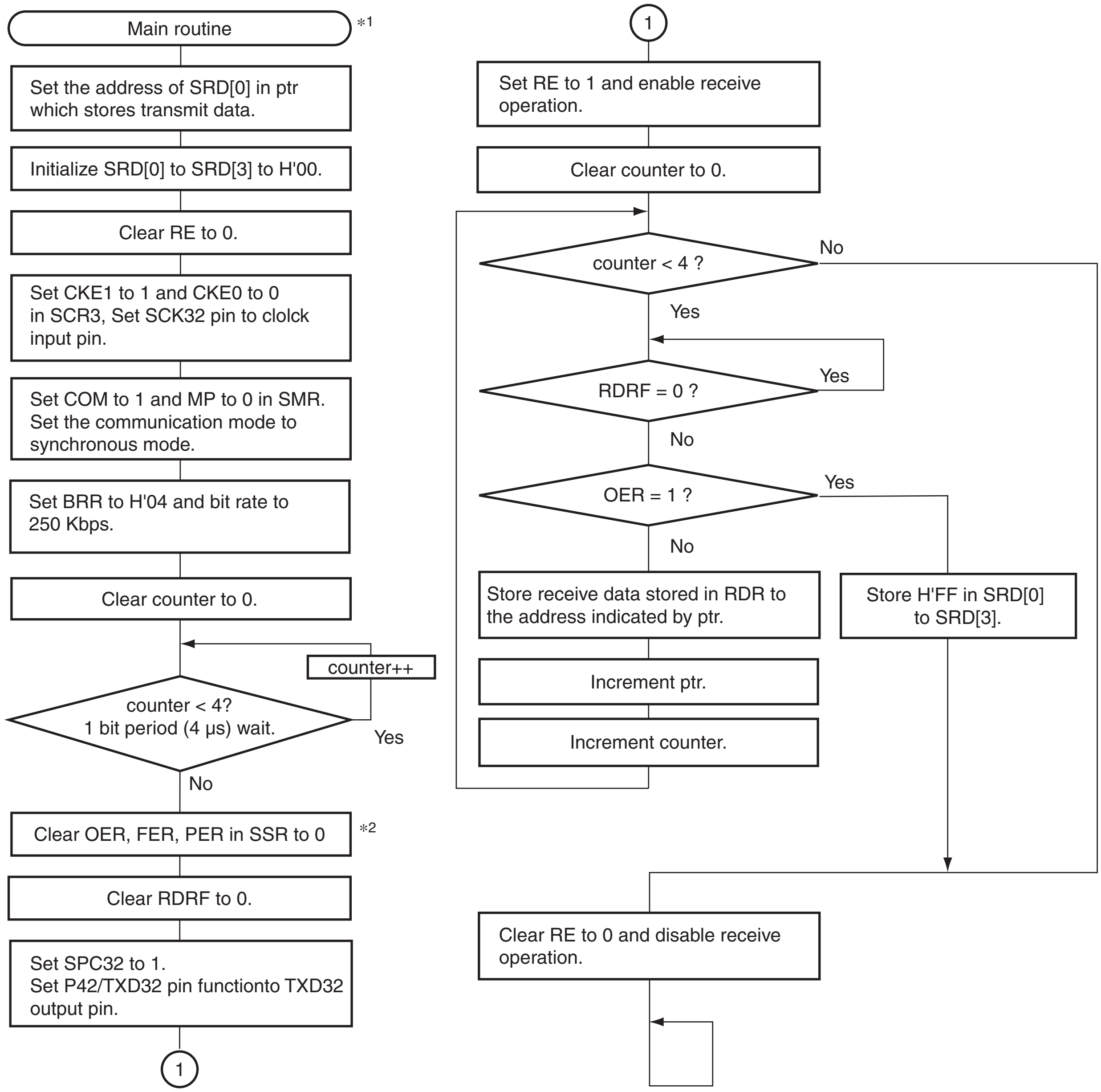
Table 4.4 describes the RAMs used in this sample task.

Table 4.4 Description of RAM

Label	Function	Address	Used in
SRD[0]	Stores the first byte of serial receive data in synchronous mode.	H'FB80	Main Routine
SRD[1]	Stores the second byte of serial receive data in synchronous mode.	H'FB81	Main Routine
SRD[2]	Stores the third byte of serial receive data in synchronous mode.	H'FB82	Main Routine
SRD[3]	Stores the fourth byte of clock synchronous data in synchronous mode serial receive data.	H'FB83	Main Routine

5. Flowchart

1. Main routine



Notes: 1. In this sample task, the stack pointer is set in INIT.SRC (assembly).
2. OER, FER, PER must be cleared to 0 in synchronous mode (reception).

6. Program Listing

INIT.SRC (Program listing)

```
     .EXPORT    _INIT
     .IMPORT    _main
 ;
     .SECTION  P,CODE
 _INIT:
     MOV.W      #H'FF80,R7
     LDC.B      #B'10000000,CCR
     JMP        @_main
 ;
     .END
```

```
/*************************************************************************************************/
/*                                                                                               */
/*  H8/300L Super Low Power Series                                                               */
/*      -H8/38024 Series-                                                                        */
/*  Application Note                                                                             */
/*                                                                                               */
/*  'Synchronous Serial Data Transmission'                                                       */
/*                                                                                               */
/*  Function                                                                                     */
/*  : Serial Communication Interface                                                             */
/*     Synchronous Serial Interface                                                              */
/*     -Transmitting                                                                             */
/*                                                                                               */
/*  External Clock : 10MHz                                                                       */
/*  Internal Clock : 5MHz                                                                        */
/*  Sub Clock      : 32.768kHz                                                                   */
/*                                                                                               */
/*************************************************************************************************/

#include    <machine.h>

/*************************************************************************************************/
/*  Symbol Definition                                                                            */
/*************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     SMR_BIT     (*(struct BIT *)0xFFA8)             /* Serial Mode Register              */
#define     COM         SMR_BIT.b7                          /* Communication Mode                */
#define     MP          SMR_BIT.b2                          /* Multiprocessor Mode               */
#define     CKS1        SMR_BIT.b1                          /* Clock Select 1                    */
#define     CKS0        SMR_BIT.b0                          /* Clock Select 0                    */
#define     BRR         *(volatile unsigned char *)0xFFA9   /* Bit Rate Register                 */
#define     SCR3_BIT    (*(struct BIT *)0xFFAA)             /* Serial Control Register 3         */
#define     TE          SCR3_BIT.b5                         /* Transmit Enable                   */
#define     RE          SCR3_BIT.b4                         /* Receive Enable                    */
```

```
#define     CKE1        SCR3_BIT.b1                         /* Clock Enable 1                       */
#define     CKE0        SCR3_BIT.b0                         /* Clock Enable 0                       */
#define     TDR         *(volatile unsigned char *)0xFFAB   /* Transmit Data Register               */
#define     SSR_BIT     (*(struct BIT *)0xFFAC)             /* Serial Status Register               */
#define     TDRE        SSR_BIT.b7                          /* Transmit Data Register Empty         */
#define     OER         SSR_BIT.b5                          /* Overrun Error                        */
#define     FER         SSR_BIT.b4                          /* Framing Error                        */
#define     PER         SSR_BIT.b3                          /* Parity Error                         */
#define     TEND        SSR_BIT.b2                          /* Transmit End                         */
#define     SPCR        *(volatile unsigned char *)0xFF91   /* Transmit Data Register               */
#define     SPCR_BIT    (*(struct BIT *)0xFF91)             /* Port Mode Register 1                 */
#define     SPC32       SPCR_BIT.b5                         /* TXD Output Terminal                  */

/********************************************************************************************/
/*  Function define                                                                         */
/********************************************************************************************/
extern void INIT ( void );                                  /* SP Set                               */
void        main ( void );

/********************************************************************************************/
/*  RAM define                                                                              */
/********************************************************************************************/
unsigned char   STD[4];

/********************************************************************************************/
/*  Vector Address                                                                          */
/********************************************************************************************/
#pragma section     V1                                      /* Vector Section Set                   */
void (*const VEC_TBL1[])(void) = {                          /* 0x0000 - 0x000F                      */
    INIT                                                    /* 0x0000 Reset Vector                  */
};

#pragma section                                             /* P                                    */
/********************************************************************************************/
/*  Main Program                                                                            */
/********************************************************************************************/
void main ( void )
{
    unsigned char   *ptr;
    unsigned char   counter;

    ptr = &STD[0];                                          /* Initialize Serial Transmitting       */
                                                            /*                         Data Address */
    STD[0] = 0x00;                                          /* Set Serial Transfer Data 0           */
    STD[1] = 0x55;                                          /* Set Serial Transfer Data 1           */
    STD[2] = 0xAA;                                          /* Set Serial Transfer Data 2           */
    STD[3] = 0xFF;                                          /* Set Serial Transfer Data 3           */

    CKE1 = 0;                                               /* Initialize Clock Enable 1            */
    CKE0 = 0;                                               /* Initialize Clock Enable 0            */

    COM = 1;                                                /* Initialize Communication Mode        */
    MP = 0;                                                 /* Initialize Multiprocessor Mode       */
    CKS1 = 0;                                               /* Initialize Clock Select 1 phi        */
    CKS0 = 0;                                               /* Initialize Clock Select 0 phi        */

    BRR = 4;                                                /* Initialize Bit Rate Register         */
    for(counter = 0 ; counter < 4; counter++);              /* BRR Counter 1 Loop                   */
```

```
    SPCR = 0xE0;                                      /* Initialize Output Port TXD            */

    OER = 0;                                          /* Clear OER                             */
    FER = 0;                                          /* Clear FER                             */
    PER = 0;                                          /* Clear PER                             */
    TDRE = 0;                                         /* Clear TDRE                            */

    TE = 1;                                           /* Start Serial Transmitting             */
    RE = 0;
    for(counter = 0 ; counter < 4 ; counter++){       /* Serial Transmitting Data Counter 4 Loop  */

        TDR = *ptr;                                   /* Write Serial Transmit Data to TDR     */
        ptr++;                                        /* Increment Serial Transmitting         */
                                                      /*                          Data Address */
        while(TDRE != 1){                             /* TDRE = 1 ?
*/
            ;
        }
    }

    while(TEND != 1){                                 /* End Serial Transmitting               */
        ;
    }

    SPC32 = 0;
    TE = 0;                                           /* Clear TE                              */

    while(1){
        ;
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
P	H'0100
B	H'FB80

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.03	—	First edition issued

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