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Renesas Electronics Corporation

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H8/300L SLP Series

Serial Data Reception in Asynchronous Mode

Introduction

Using the serial data transfer function in asynchronous mode, four bytes of 8-bit data are received. The data transfer format for transmit data is set to eight bits for data length, an odd parity and one bit for the stop bit length. Data is transmitted at the bit rate of 31250 bps. Data receiving is completed when four bytes of data is received.

Target Device

H8/38024

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1. Specifications

1. Using the serial data transfer function in asynchronous mode four bytes of 8-bit data are received as shown in figure 1.1.
2. The data transfer format for transmit data is set to eight bits for data length, an odd parity and one bit for the stop bit length.
3. Data is transmitted at the bit rate of 31250 bps. Data receiving is completed when four bytes of data is received.

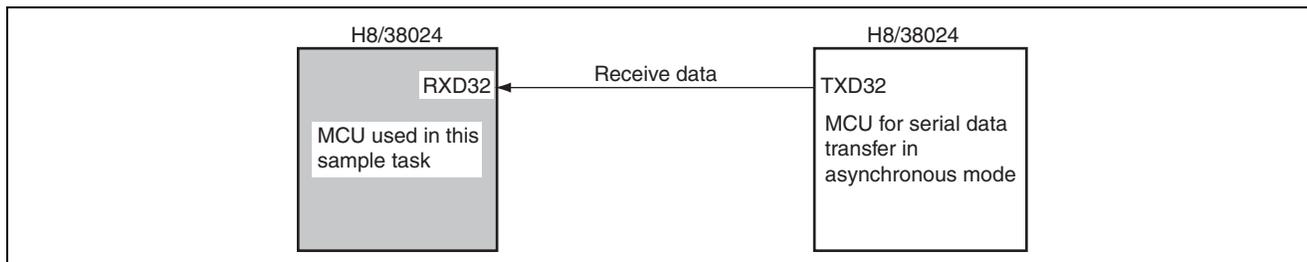


Figure 1.1 Serial Data Reception in Asynchronous Mode

2. Description of Functions

1. In this sample task, a Serial Communication Interface (SCI) is used for serial data reception in asynchronous mode. Figure 2.1 shows a block diagram of serial data reception in asynchronous mode which is described below.
 - In asynchronous mode, serial data communication is performed asynchronously, with synchronization provided character by character.
 - Serial data can be communicated with standard asynchronous communication LSIs such as Universal Asynchronous Receiver/Transmitter (UART) and Asynchronous Communication Interface Adapter (ACIA).
 - A multi-processor communication function is provided to enable serial data communications with multiple processors.
 - A desired transfer format can be selected from 16 format types.
 - The transmitter and receiver are independent, enabling simultaneous transmission and reception. Both the transmitter and receiver have a double-buffer architecture to achieve continuous transmission and reception.
 - Any desired bit rate can be selected using the on-chip baud rate generator.
 - The transmit and receive clock source can be selected from internal or external clocks.
 - There are six interrupt factors, namely, transmit complete, transmit data empty, receive data full, overrun error, framing error and parity error.
 - The Receive Shift Register (RSR) is a register to receive serial data. Serial data input from RXD32 pin is set in RSR in the receiving order that is starting from the LSB, and is converted into parallel data. When one-byte data is received, it is transferred automatically to RDR. RSR cannot be read from or written to directly by the CPU.
 - The Receive Data Register (RDR) is an 8-bit register to store received serial data. Receiving one-byte data, the received data is transferred from RSR to RDR to complete receive operation. RSR is then ready to receive data. RSR and RDR have a double buffer, enabling continuous receive operations. RDR is a receive-only register and cannot be written to by the CPU.
 - The Transmission Shift Register (TSR) is a register to transmit serial data. Transmit data is temporarily transferred from TDR to TSR and is sent to TXD32 pin starting from LSB (Bit 0) for serial data transmission. Transmitting one-byte data, the next transmit data is transferred automatically from TDR to TSR to start transmitting. If data is not written in TDR (1 is set in TDRE), data is not transferred from TDR to TSR. TSR cannot be read from or written to directly by the CPU.
 - The Transmit Data Register (TDR) is an 8-bit register to store transmit data. Detecting that TSR is "empty", transmit data written in TDR is transferred to TSR to start serial data transmission. By writing next transmit data in TDR during TSR serial data transmission, continuous transmission is possible. TDR can always be read from or written to by the CPU.

- The Serial Mode Register (SMR) is an 8-bit register for setting of a serial data transfer format and selecting a clock source for the baud rate generator. SMR can always be read from or written to by the CPU.
- The Serial Control Register 3 (SCR3) is an 8-bit register for selecting transmit/receive operations, clock output in asynchronous mode, interrupt request enable/disable, and transmit/receive clock source. SCR3 can always be read from or written to by the CPU.

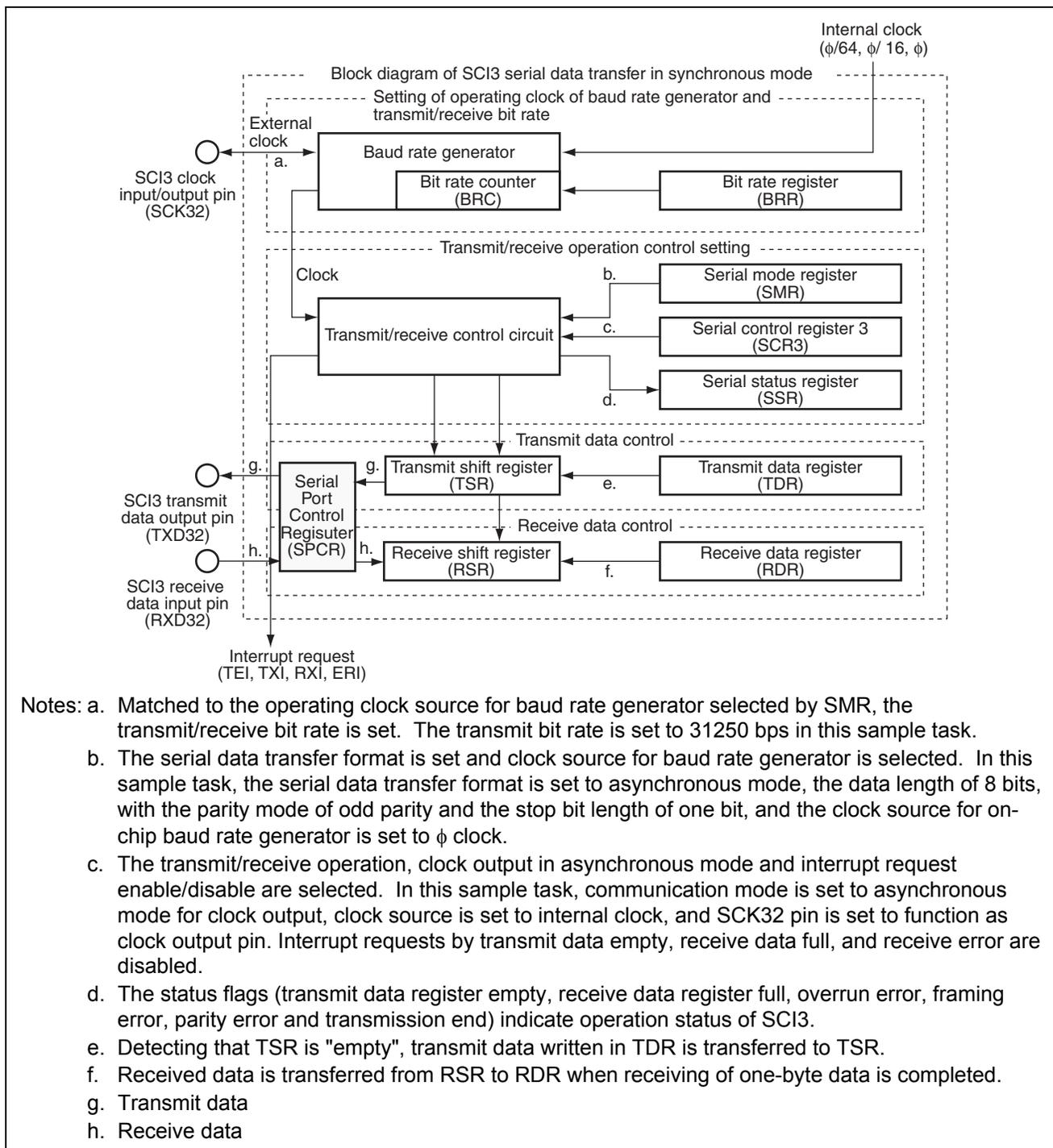


Figure 2.1 Block Diagram of Serial Data Reception in Asynchronous Mode

- The Serial Status Register (SSR) is an 8-bit register with on-chip status flags indicating operation status of SCI3 and on-chip multi-processor bits. SSR can always be read from or written to by the CPU, except 1 cannot be written in TDRE, RDRF, OER, PER or FER. 1 must be read in advance to clear them by writing 0. TEND and MPBR are for read only and data cannot be written in them.
- The Bit Rate Register (BRR) is an 8-bit register to set a transmit/receive bit rate matched to the operating clock for the baud rate generator selected by CSK1 and CKS0 in SMR. BRR can always be read from or written to by the CPU.
- Table 2.1 shows an example of BRR setting in asynchronous mode. Table 2.1 shows values in the active mode when OSC is 10 MHz.

Table 2.1 Example of BRR Settings for Bit Rates (Asynchronous Mode)

R Bit Rate (Bps)	110	150	200	250	1200	2400	31250
n		2	2	2	2	0	0
N		88	64	48	38	129	64
Error (%)		-0.25	+0.16	-0.35	+0.16	+0.16	+0.16

Notes: 1. Set errors to be less than 1%.

2. BRR set values can be calculated as follows:

$$N = \frac{OSC}{64 \times 2^{2n} \times B} \times 10^6 - 1$$

B: Bit rate (bps)

N: Set value of baud rate generator BRR ($0 \leq N \leq 255$)

OSC: Value of ϕ_{OSC} (MHz) = 10 MHz or subclock $\phi_w = 32.768$ KHz

n: Value set in CKS1 and CKS0 in SMR ($0 \leq n \leq 3$)

(See Table 2 for the relation between n and clock.)

Table 2.2 Relation between n and Clock

n	Clock	Set Value of SMR	
		CKS1	CKS0
0	ϕ	0	0
1	$\phi_w / 4, \phi_w$	0	1
2	$\phi/16$	1	0
3	$\phi/64$	1	1

3. The error shown in Table 1 is given by the following equation.
(rounded off to two decimals)

$$\text{Error (\%)} = \left\{ \frac{\phi \times 10^6}{(N+1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

4. When OSC is 10 MHz, the maximum bit rate (asynchronous mode) is 31250 bps, provided n=0 and N=4 are set.

- In asynchronous mode, serial communication is performed with synchronization provided character by character, transmitting and receiving characters added with a start bit indicating the start of communication and a stop bit indicating the end of communication.
- The transmitter and receiver are independent inside SCI3 and full duplex communications are possible. Both the transmitter and receiver have a double-buffer architecture, therefore it is possible to perform data writing during transmission and data reading during reception, and continuous transmission and reception is then possible.
- Figure 2.2 shows data format of asynchronous communications. In asynchronous communications, the communication line is normally maintained in the mark state ("High" level). SCI3 monitors communication line and starts serial communications when it detects the place which has become a space ("Low" level) to serve as a start bit.
- One character in communication data consists of the start bit ("Low" level), followed by transmit/receive data (LSB first, starting from the least significant bit), parity bit ("High" or "Low" level) and stop bit ("High" level) at the end.
- In asynchronous mode, synchronization is achieved by the falling edge of the start bit during reception. Data is sampled on the eighth clock of a frequency obtained by multiplying 16 times the one bit period and communication data is fetched in the center of each bit.

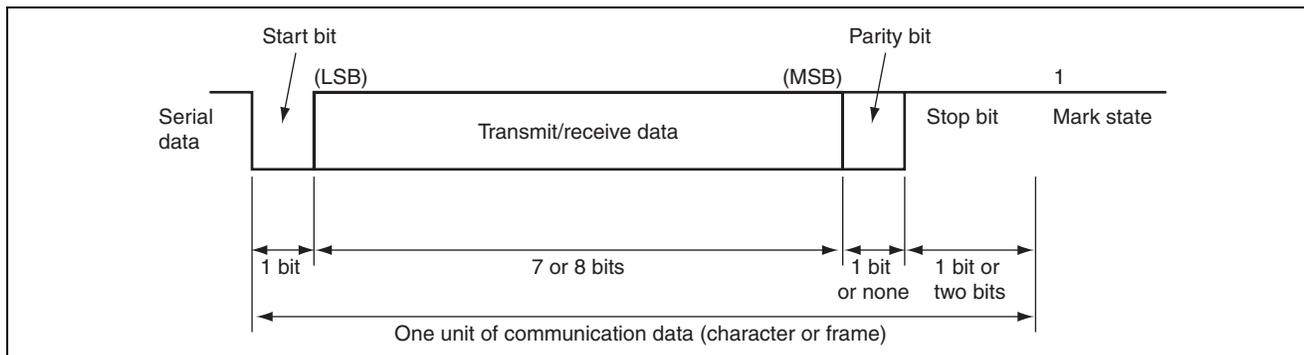


Figure 2.2 Data Format in Asynchronous Communications

- SCI3 clock (SCK32) is a clock input/output pin of SCI3.
- SCI3 receive data input (RXD32) is a receive data input pin of SCI3.
- SCI3 transmit data output (TXD32) is a transmit data output pin of SCI3.
- SCI3 interrupt factors total six, transmit complete, transmit data empty, receive data full and three receive errors (overrun error, framing error and parity error). Common vector address is assigned to them.
- Each interrupt request can be enabled/disabled by TIE and RIE in SCR3.
- If TDRE in SSR is set to 1, TXI is generated. If TEND in SSR is set to 1, TEI is generated. These two interrupts are generated during transmission.
- The initial value of TDRE in SSR is 1. Therefore, by setting TIE in SCR3 to 1 and by enabling a transmit data empty interrupt request (TXI) before transferring transmit data to TDR, TXI is generated even when transmit data is not ready.
- The initial value of TEND in SSR is 1. Therefore, by setting TEIE in SCR3 to 1 and by enabling a transmit end interrupt request (TEI) before transferring transmit data to TDR, TEI is generated even when transmit data is not sent.
- By processing which transfers transmit data to TDR within the interrupt handling routine, these interrupts can be utilized effectively. To prevent these interrupt requests (TXI and TEI), the enable bits (TIE and TEIE) interacting to these interrupt requests should be set to 1 after the transmit data has been transferred to TDR.
- RXI is generated when RDRF in SSR is set to 1. ERI is generated when OER, PER or FER is set to 1. These two interrupt requests are generated during reception.

2. Table 2.3 shows assignment of functions in this sample task. Serial data transmission in asynchronous mode is performed by assigning the functions as shown in table 2.3.

Table 2.3 Assignment of Functions

Function	Assignment
RSR	A register to receive serial data
RDR	A register to store receive data
SMR	Sets the serial data transfer format and clock source for the baud rate generator
SSR	Status flags to indicate operation status of SCI3
BRR	Sets transmit/receive bit rate
SCR3	Enables receive operation and sets RXD32 input pin
RXD32	SCI3 receive data input pin

3. Principle of Operation

1. Figure 3.1 illustrates the principle of operation of this sample task. Serial data is received in asynchronous mode by hardware and software processing as shown in figure 3.1.

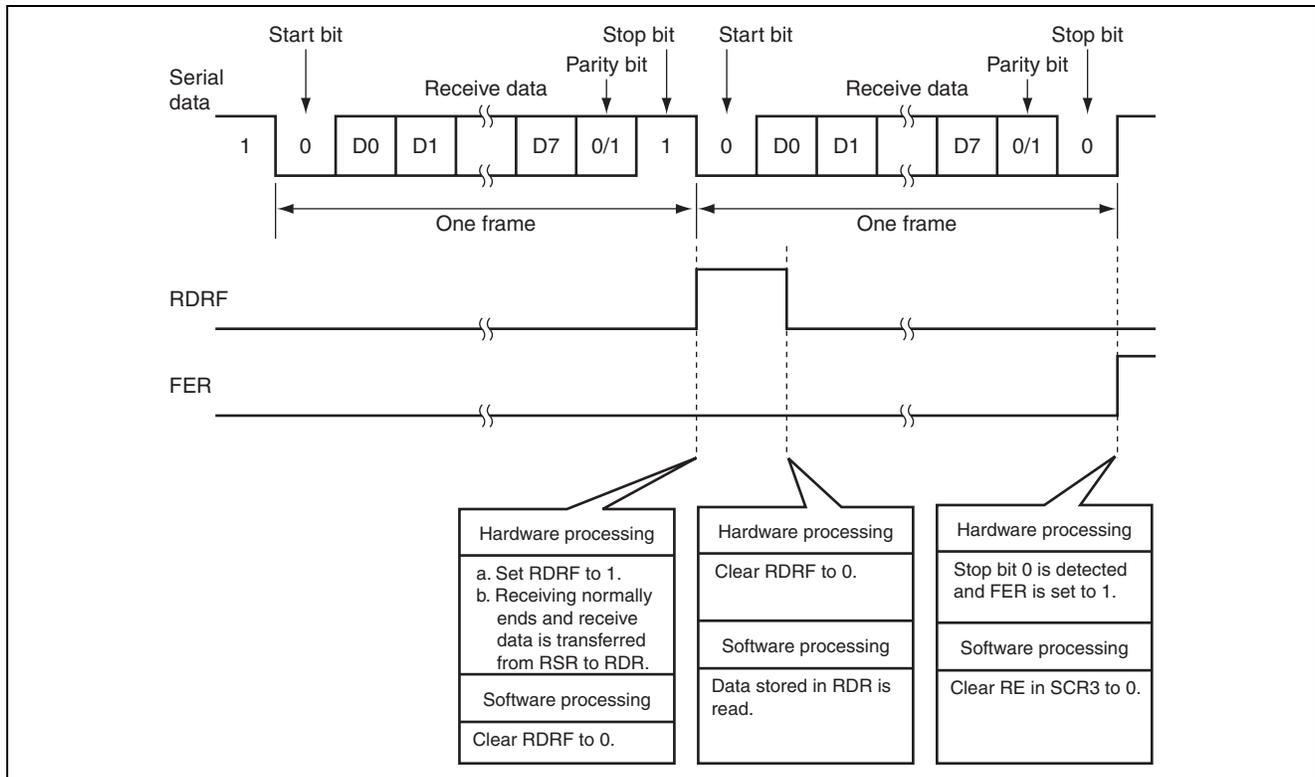


Figure 3.1 Operation Principle of Serial Data Reception in Asynchronous Mode

4. Description of Software

4.1 Modules

Table 4.1 describes the module in this sample task.

Table 4.1 Description of Modules

Module	Label	Function
Main Routine	main	Serial data reception in asynchronous mode setting, setting SRD[0] to SRD[3] to H'FF if receive error occurs, and ending operation when 4-byte data is received.

4.2 Arguments

Table 4.2 describes the arguments used in this sample task.

Table 4.2 Description of Arguments

Arguments	Function	Used in	Data Length	Input/Output
SRD[0] to SRD[3]	Serial receive data in asynchronous mode.	Main Routine	1 byte	Output

4.3 Internal Registers

Table 4.3 describes the internal registers in this sample task.

Table 4.3 Description of Internal Registers

Register	Function	Address	Setting
SMR	COM Serial mode register (Communication mode) If COM = 0, the communication mode is set to asynchronous mode. If COM = 1, the communication mode is set to synchronous mode.	H'FFA8 Bit 7	0
	CHR Serial mode register (Character length) If CHR = 0, the data length in asynchronous mode is set to 8-bit data. If CHR = 1, the data length in asynchronous mode is set to 7-bit data.	H'FFA8 Bit 6	0
	PE Serial mode register (Parity enable) If PE = 0, parity bit addition and check are disabled during transmission in asynchronous mode. If PE = 1, parity bit addition and check are enabled during transmission in asynchronous mode.	H'FFA8 Bit 5	1
	PM Serial mode register (Parity mode) If PM = 0, parity addition and check are set to even parity. If PM = 1, parity addition and check are set to odd parity.	H'FFA8 Bit 4	1

Register	Function	Address	Setting
SMR	STOP Serial mode register (Stop bit length) If STOP = 0, the stop bit length in asynchronous mode is set to one bit. If STOP = 1, the stop bit length in asynchronous mode is set to two bits.	H'FFA8 Bit 3	0
	MP Serial mode register (Multi-processor mode) If MP = 0, the multi-processor communication function is disabled. If MP = 1, the multi-processor communication function is enabled.	H'FFA8 Bit 2	0
	CKS1 Serial mode register (Clock select 1, 0)	H'FFA8	CKS1 = 0
	CKS0 If CKS1 = 0 and CKS0 = 0, the clock source for the on-chip baud rate generator is set to ϕ clock.	Bit 1 Bit 0	CKS0 = 0
BRR	Bit rate register If BRR = H'04, the transmit bit rate matched to the operating clock for the baud rate generator selected by CKS1 and CKS0 in SMR is set to 31250 bps.	H'FFA9	H'04
SCR3	RE Serial control register 3 (Receive enable) If RE = 0, reception operation is disabled. If RE = 1, reception operation is enabled.	H'FFAA Bit 4	0
	CKE1 Serial control register 3 (Clock enable 1, 0)	H'FFAA	CKE1 = 0
	CKE0 If CKE1 = 0 and CKE0 = 0, the clock source is set to an internal clock and SCK32 pin function to input/output port in asynchronous mode.	Bit 1 Bit 0	CKE0 = 0
SSR	RDRF Serial status register (Receive data register full) If RDRF = 0, no receive data is stored in RDR. If RDRF = 1, receive data is stored in RDR.	H'FFAC Bit 6	1
	OER Serial status register (Overrun error) If OER = 0, data is being received or reception has been completed. If OER = 1, an overrun error has occurred during data reception.	H'FFAC Bit 5	0
	FER Serial status register (Framing error) If FER = 0, data is being received or reception has been completed. If FER = 1, a framing error has occurred during data reception.	H'FFAC Bit 4	0
	PER Serial status register (Parity error) If PER = 0, data is being received or reception has been completed. If PER = 1, a parity error has occurred during data reception.	H'FFAC Bit 3	0
RDR	Receive data register An 8-bit register to store receive data.	H'FFAD	–
SPCR	SCINV2 Serial port control register (RXD32 pin input data inversion switch) If SCINV2 = 0, RXD32 input data is not inverted. If SCINV2 = 1, RXD32 input data is inverted.	H'FF91 Bit 2	0

4.4 Description of RAM

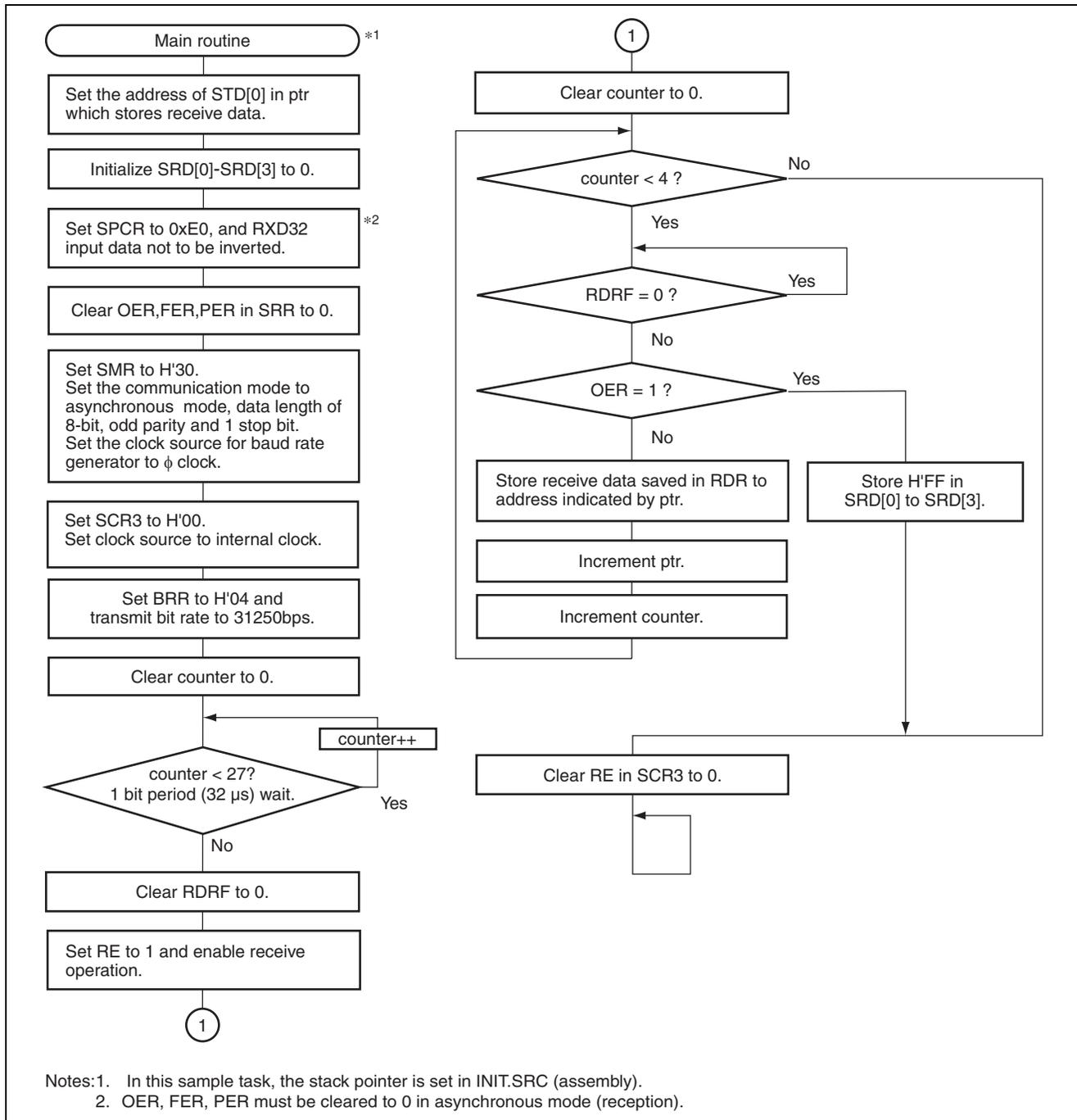
Table 4.4 describes the RAMs used in this sample task.

Table 4.4 Description of RAM

Label	Function	Address	Used in
SRD[0]	Stores the first byte of serial receive data in asynchronous mode.	H'FB80	Main Routine
SRD[1]	Stores the second byte of serial receive data in asynchronous mode.	H'FB81	Main Routine
SRD[2]	Stores the third byte of serial receive data in asynchronous mode.	H'FB82	Main Routine
SRD[3]	Stores the fourth byte of serial receive data in asynchronous mode.	H'FB83	Main Routine

5. Flowchart

1. Main routine



6. Program Listing

INIT.SRC (Program listing)

```

.EXPORT  _INIT
.IMPORT  _main
;
.SECTION P, CODE
_INIT:
MOV.W   #H'FF80, R7
LDC.B   #B'10000000, CCR
JMP     @_main
;
.END

/*****
/*
/* H8/300L Super Low Power Series
/* -H8/38024 Series-
/* Application Note
/*
/* 'Asynchronous Serial Data Reception'
/*
/* Function
/* : Serial Communication Interface
/*   Asynchronous Serial Interface
/*   -Receiving
/*
/* External Clock : 10MHz
/* Internal Clock : 5MHz
/* Sub Clock      : 32.768kHz
/*
*****/

#include <machine.h>

/*****
/* Symbol Definition
*****/
struct BIT {
    unsigned char  b7:1;    /* bit7 */
    unsigned char  b6:1;    /* bit6 */
    unsigned char  b5:1;    /* bit5 */
    unsigned char  b4:1;    /* bit4 */
    unsigned char  b3:1;    /* bit3 */
    unsigned char  b2:1;    /* bit2 */
    unsigned char  b1:1;    /* bit1 */
    unsigned char  b0:1;    /* bit0 */
};

#define SMR      *(volatile unsigned char *)0xFFA8    /* Serial Mode Register */
#define SMR_BIT  (*(struct BIT *)0xFFA8)             /* Serial Mode Register */
#define COM      SMR_BIT.b7                          /* Communication Mode */
#define CHR      SMR_BIT.b6                          /* Character Length */
#define PE       SMR_BIT.b5                          /* Parity Enable */
#define PM       SMR_BIT.b4                          /* Parity Mode */
#define STOP     SMR_BIT.b3                          /* Stop Bit Length */
#define MP       SMR_BIT.b2                          /* Multiprocessor Mode */
#define CKS1     SMR_BIT.b1                          /* Clock Select 1 */

```

```

#define CKS0      SMR_BIT.b0          /* Clock Select 0          */
#define BRR      *(volatile unsigned char *)0xFFA9 /* Bit Rate Register      */
#define SCR3     *(volatile unsigned char *)0xFFAA /* Serial Control Register 3 */
#define SCR3_BIT (*(struct BIT *)0xFFAA) /* Serial Control Register 3 */
#define TIE     SCR3_BIT.b7          /* Transmit Interrupt Enable */
#define RIE     SCR3_BIT.b6          /* Receive Interrupt Enable  */
#define TE      SCR3_BIT.b5          /* Transmit Enable          */
#define RE      SCR3_BIT.b4          /* Receive Enable           */
#define MPIE    SCR3_BIT.b3          /* Multiprocessor Interrupt Enable */
#define TEIE    SCR3_BIT.b2          /* Transmit End Interrupt Enable */
#define CKE1    SCR3_BIT.b1          /* Clock Enable 1          */
#define CKE0    SCR3_BIT.b0          /* Clock Enable 0          */
#define TDR     *(volatile unsigned char *)0xFFAB /* Transmit Data Register   */
#define SSR     *(volatile unsigned char *)0xFFAC /* Serial Status Register   */
#define SSR_BIT (*(struct BIT *)0xFFAC) /* Serial Status Register   */
#define TDRE    SSR_BIT.b7          /* Transmit Data Register Empty */
#define RDRF    SSR_BIT.b6          /* Receive Data Register Full  */
#define OER     SSR_BIT.b5          /* Overrun Error            */
#define FER     SSR_BIT.b4          /* Framing Error            */
#define PER     SSR_BIT.b3          /* Parity Error             */
#define TEND    SSR_BIT.b2          /* Transmit End             */
#define MPBR    SSR_BIT.b1          /* Multiprocessor Bit Receive */
#define MPBT    SSR_BIT.b0          /* Multiprocessor Bit Transfer */
#define RDR     *(volatile unsigned char *)0xFFAD /* Receive data Register    */
#define SPCR    *(volatile unsigned char *)0xFF91 /* Transmit Data Register   */
#define SPCR_BIT (*(struct BIT *)0xFF91) /* Port Mode Register 1     */
#define SPC32   SPCR_BIT.b5          /* TXD Output Terminal      */

/*****
/* Function define
/*****
extern void INIT ( void ); /* SP Set
void main ( void );

/*****
/* RAM define
/*****
unsigned char SRD[4];

/*****
/* Vector Address
/*****
#pragma section V1 /* Vector Section Set
void (*const VEC_TBL1[])(void) = { /* 0x0000 - 0x000F
INIT /* 0x0000 Reset Vector
};

#pragma section /* P

```

```

/*****
/* Main Program
*****/
void main ( void )
{
    unsigned char *ptr;
    unsigned char counter;

    ptr = &SRD[0]; /* Initialize Serial Receiving Data Address */

    SRD[0] = 0x00; /* Initialize Serial Receiving Data 0 */
    SRD[1] = 0x00; /* Initialize Serial Receiving Data 1 */
    SRD[2] = 0x00; /* Initialize Serial Receiving Data 2 */
    SRD[3] = 0x00; /* Initialize Serial Receiving Data 3 */

    SPCR = 0xE0; /* Initialize Output Port TXD */

    OER = 0; /* Clear OER */
    FER = 0; /* Clear FER */
    PER = 0; /* Clear PER */

    SMR = 0x30; /* Initialize Serial Mode Register */

    SCR3 = 0x00; /* Initialize Serial Control Register 3 */

    BRR = 4; /* Initialize Bit Rate Register */
    for(counter = 0; counter < 27; counter++); /* dummy wait */

    RDRF = 0; /* Clear RDRF */

    RE = 1; /* Start Serial Receiving */

    counter = 0; /* Clear counter */

    while(counter < 4){ /* Serial Receiving Data Counter 4 Loop */

        while(RDRF == 0){ /* End Serial Receiving */

            ;

        }

        if (OER == 1){ /* Overrun Error Flag = 1 ? */

            SRD[0] = 0xFF; /* Overrun Error 0 */
            SRD[1] = 0xFF; /* Overrun Error 1 */
            SRD[2] = 0xFF; /* Overrun Error 2 */
            SRD[3] = 0xFF; /* Overrun Error 3 */
            break;

        }

        else{

            *ptr = RDR; /* Save Serial Receiving Data */
            ptr++; /* Increment Serial Receiving Data Address */
            counter++; /* Increment counter */

        }

    }

}

```

```
RE = 0; /* Initialize Receiving Enable */  
  
while(1){  
    ;  
}  
}
```

Link address specifications

Section Name	Address
CV1	H'0000
P	H'0100
B	H'FB80

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.03	—	First edition issued

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