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H8/300H Super Low Power Series

Sensor Connection with Low Supply Current Using Comparator and A/D Converter

Introduction

This application note describes a method of sensor connection with low supply current, which is reduced by using the comparator function incorporated in the H8/38602R

Target Device

H8/38602R Group

Contents

1. Overview

The output voltage of the sensor is compared by the comparator, and when it exceeds a certain threshold, A/D conversion is performed. One of the advantages of this method is that execution of A/D conversion can be suppressed for voltage levels below a threshold by using a comparator, which only requires a small current, to compare the input voltage. This reduces the number of times A/D conversion is performed, allowing for a system with low supply current.

Figure 1 shows a conceptual drawing showing the difference in supply current between an earlier product, which does not use a comparator, and an H8/38602R Group product, which uses a comparator.

- H8/38602R Group product using a comparator (right figure)
  A/D conversion is performed when the analog input signal exceeds the threshold set in the comparator.
- Earlier product not using a comparator (left figure)
  A/D conversion is performed at constant timing, regardless of the input voltage level.

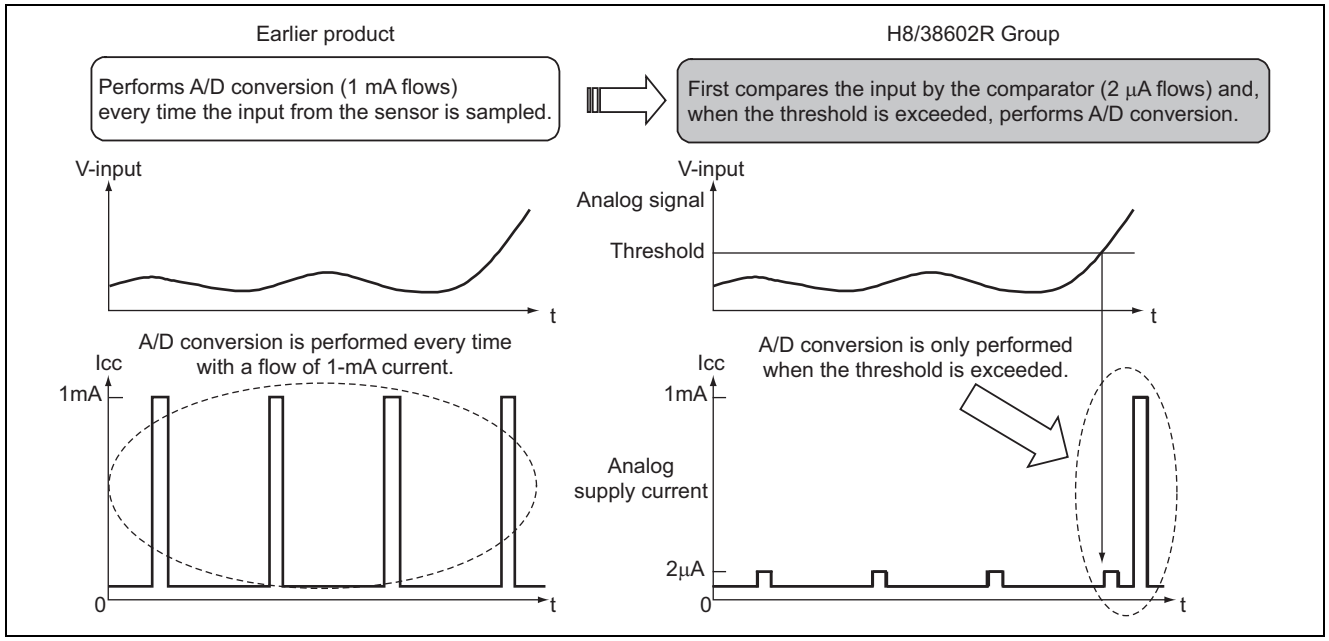


Figure 1 Conceptual Drawing about Supply Current

2. Specifications

1. The H8/38602R initializes the modules for use, then enters watch mode.
2. Upon a 0.25-second periodic interrupt generated by the realtime clock (RTC), the chip recovers from watch mode to enter sub-active mode.
3. In the RTC interrupt exception handling, the sensor voltage input to the COMP0 pin is compared with the reference voltage by the comparator function.
4. The H8/38602R performs A/D conversion when the sensor voltage exceeds the reference voltage. Otherwise, it enters watch mode.
5. After the A/D conversion has ended, the chip enters watch mode.
6. The sensor connected to the H8/38602R is the precision, Centigrade temperature sensor IC (LM35DZ) from National Semiconductor.
7. Figure 2 is a connection diagram of this application, and table 1 shows supply currents.

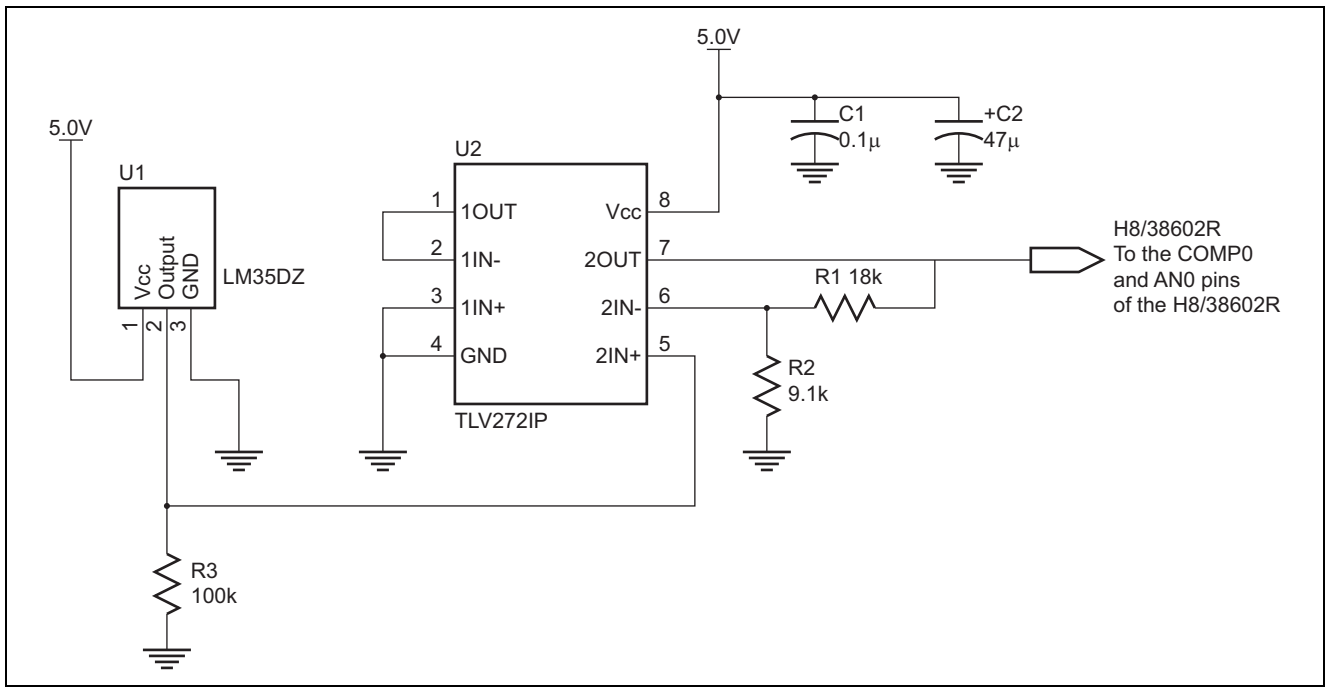


Figure 2 Connection Diagram

Table 1 Supply Currents

Case	Measurement Condition	Measured Value	Unit
CPU is stopped	Vcc = 3.3 V A 32.768-kHz crystal resonator is used. Operating mode: Watch mode Operating modules: RTC, comparator, flash memory	5.6	µA
Comparator is operating	Vcc = 3.3 V A 32.768-kHz crystal resonator is used. Operating mode: Sub-active mode Operating modules: RTC, comparator, flash memory	94.5	
A/D conversion is performed	Vcc = 3.3 V A 32.768-kHz crystal resonator is used. Operating mode: Sub-active mode Operating modules: RTC, A/D converter, comparator, flash memory	828.7	

3. Description of Functions Used

3.1 Comparator Function

3.1.1 Description of Comparator Function

The H8/38602R has on-chip comparators that compare the input voltage with the reference voltage. Figure 3 shows a block diagram of the comparator function.

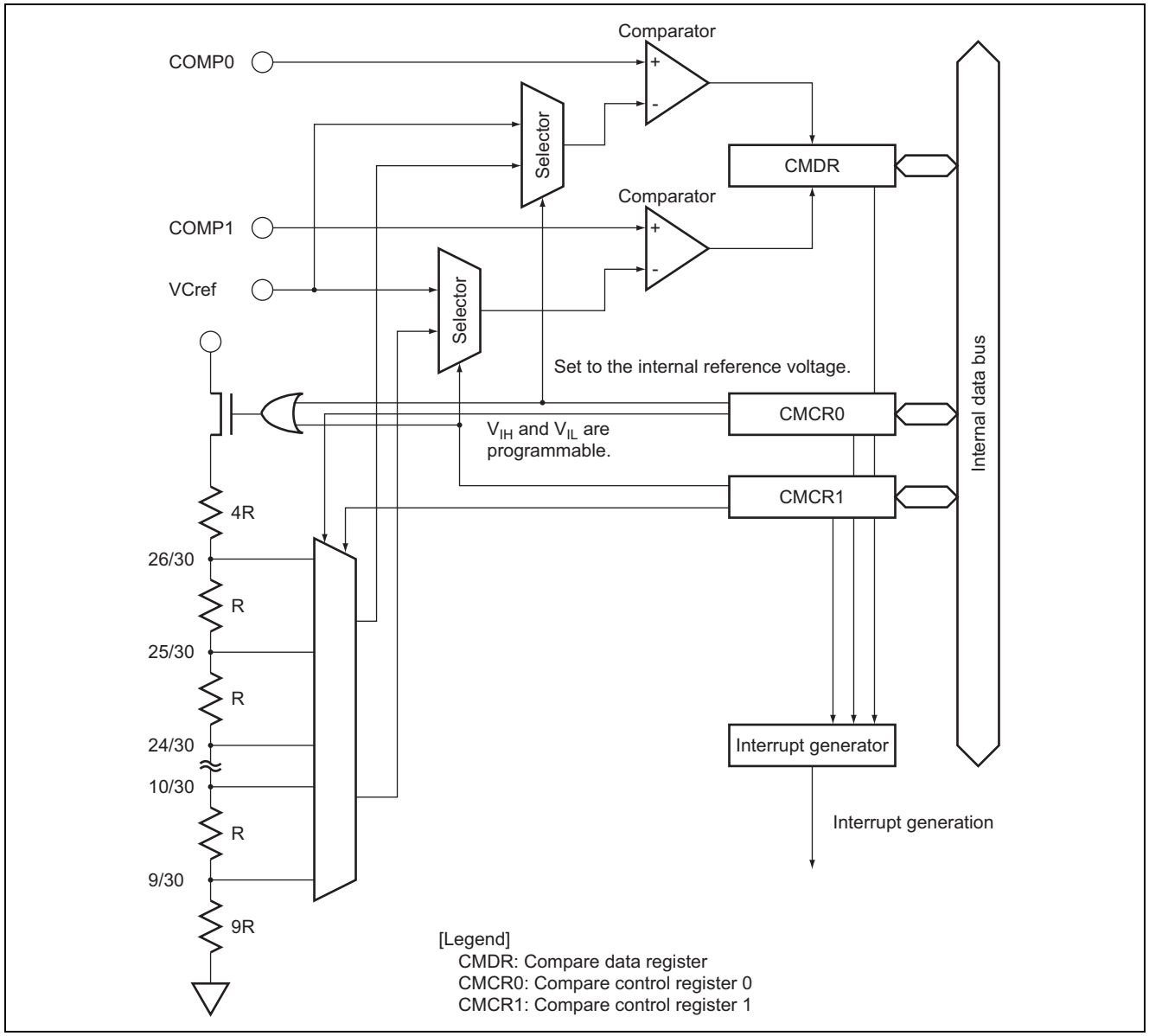


Figure 3 Comparator Block Diagram

- Compare Control Registers 0 and 1 (CMCR0 and CMCR1)
  CMCR0 and CMCR1 are registers for controlling the respective comparators.
- Compare Data Register (CMDR)
  CMDR is a register for storing the results of comparing the signal on the analog input pin with the reference voltage.

3.1.2 Hysteresis Characteristics of the Comparator

Figure 4 shows the relationship between the voltage input from the COMP pin and the state of CDR when hysteresis is selected and not selected by the CMLS bit in CMCR. For CDR, the result of comparison by the comparator, hysteresis characteristics can be selected by the CMLS bit as shown in the figure.

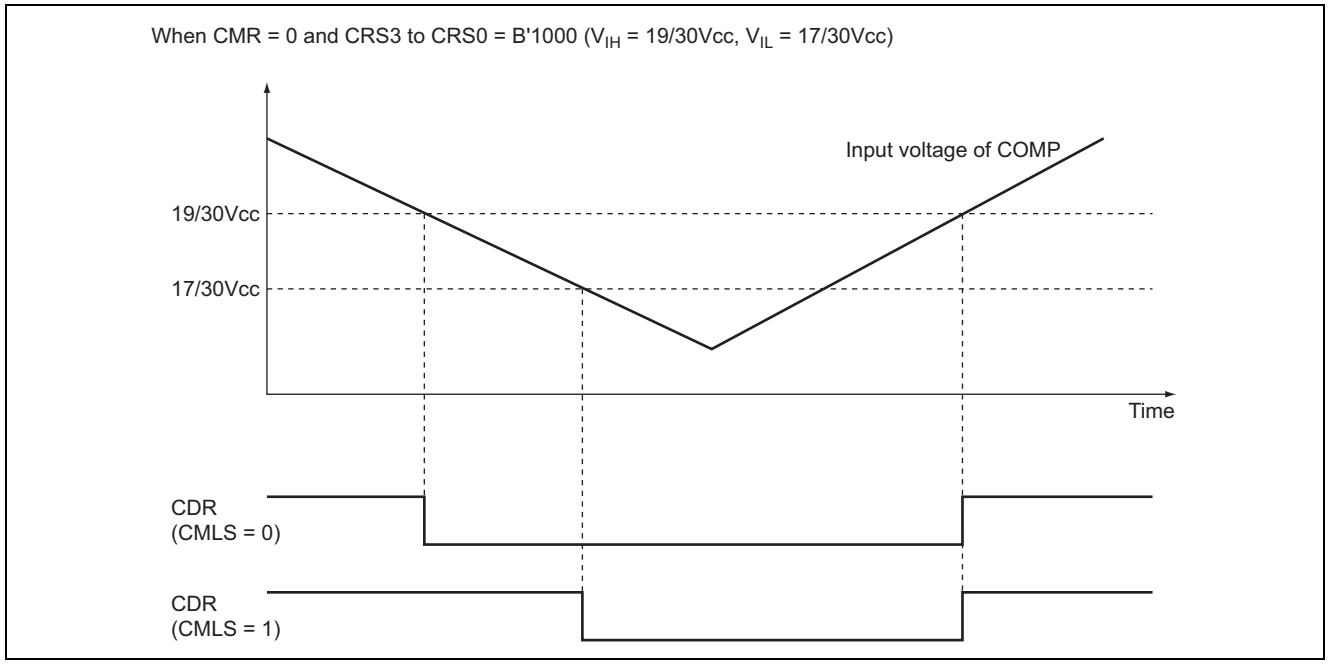


Figure 4 CDR When Hysteresis is Selected/Not Selected

3.2 A/D Converter Function

This is a 10-bit A/D converter with a successive approximation method, and can convert analog inputs on six channels.

- A/D result register (ADRR)
  ADRR is a 16-bit read-only register for storing A/D conversion results. Data is stored in the ten higher-order bits of ADRR. ADRR is always readable by the CPU. The ADRR value during A/D conversion is undefined, and after A/D conversion, ten bits of A/D-converted data are stored and held until the next conversion is started. The initial value of ADRR is undefined. This register should be read in a word unit.

- A/D mode register (AMR)
  AMR sets the conversion time for the A/D converter, selects an external trigger, and specifies an analog input pin.

- A/D start register (ADSR)
  ADSR starts or stops A/D conversion.

3.3 Realtime Clock (RTC) Function

The realtime clock (RTC) is a timer capable of counting time from one second to one week. It can generate interrupts at intervals of 0.25 second to one week.

- RTC Control Register 1 (RTCCR1)
  RTCCR1 controls the start/stop and reset of the clock timer.
- RTC Control Register 2 (RTCCR2)
  RTCCR2 controls weekly, daily, hourly, minute, 1-second, 0.5-second, and 0.25-second periodic interrupts. When any one of weekly, daily, hourly, minute, 1-second, 0.5-second, and 0.25-second interrupts is enabled and such an interrupt is generated, the corresponding flag of the RTC interrupt flag register (RTCFLG) is set to 1. While the RTC is operating as a free-running counter, this register controls the overflow interrupt of the free-running counter.
- Clock Source Select Register (RTCCSR)
  RTCCSR selects a clock source. Selecting a clock other than a 32.768-kHz clock disables the realtime clock function, and the RTC module operates as an 8-bit free-running counter.

3.4 Power-Down Mode Function

The operating modes after a reset is released include normal active (high-speed) mode and seven power-down modes in which power consumption is reduced considerably. In addition, a module standby function is provided whereby the operation of on-chip modules can be selectively stopped to reduce power consumption.

- System Control Register 1 (SYSCR1)
  SYSCR1 controls power-down mode together with the SYSCR2 register.
- System Control Register 2 (SYSCR2)
  SYSCR2 controls power-down mode together with the SYSCR1 register.
- Clock Stop Registers 1 and 2 (CKSTPR1 and CKSTPR2)
  CKSTPR1 and CKSTPR2 place on-chip peripheral modules in standby mode, on a module-by-module basis.

3.4.1 Watch Mode

In watch mode, the system clock oscillator and the CPU stop operating, and the on-chip peripheral functions other than the WDT, RTC, timer B1, asynchronous event counter, and comparators stop operating. As long as a prescribed voltage is supplied, the contents of the internal registers of the CPU and some of the on-chip peripheral modules, as well as the contents of on-chip RAM, are retained, and I/O ports retain their states before watch mode is entered.

Watch mode is exited with an interrupt. When an interrupt request is generated, watch mode is exited and interrupt exception handling starts. The mode after the exit is one of active (high-speed), active (medium-speed), and sub-active modes depending on the combination of LSON of SYSCR1 and MSON of SYSCR2. When watch mode shifts to active mode, interrupt exception handling starts after the time set in STS2 to STS0 of SYSCR1 has elapsed. When the I bit of CCR is 1 or when acceptance of the interrupt is disabled by the interrupt enable register, watch mode cannot be exited.

In watch mode, driving the $\overline{\text{RES}}$ pin low causes the system clock oscillator to start. At the same time as the start of system clock oscillation, the system clock is supplied to the entire LSI. Make sure that the $\overline{\text{RES}}$ pin is held low until system clock oscillation has become stable. Driving the $\overline{\text{RES}}$ pin high after the elapse of oscillation stabilization time causes the CPU to start reset exception handling. Table 2 shows the LSI state in watch mode. Figure 5 shows a diagram of transition from active mode to watch mode.

3.4.2 Sub-Active Mode

In sub-active mode, the system clock oscillator stops operating, and the on-chip peripheral modules other than IIC2 operate. As long as a prescribed voltage is supplied, the contents of the internal registers of some of the on-chip peripheral modules are retained. Sub-active mode is exited when a SLEEP instruction is executed. The mode after exit is one of sub-sleep, active, and watch modes depending on the combination of SSBY, LSON, and TMA3 of SYSCR1 and MSON and DTON of SYSCR2. When the I bit of CCR is 1 or when acceptance of the interrupt is disabled with the interrupt enable register, sub-active mode cannot be exited.

In sub-active mode, driving the $\overline{\text{RES}}$ pin low causes the system clock oscillator to start. At the same time as the start of system clock oscillation, the system clock is supplied to the entire LSI. Make sure that the $\overline{\text{RES}}$ pin is held low until system clock oscillation has become stable. Driving the $\overline{\text{RES}}$ pin high after the elapse of oscillation stabilization time causes the CPU to start reset exception handling.

It is possible to select an operating frequency in sub-active mode from among the watch clock (ϕ_W) and the watch clock divided by 2, 4, or 8, using SA1 and SA0 of SYSCR2. After execution of the SLEEP instruction, the operating frequency is switched to the frequency set before the execution of the SLEEP instruction. Table 2 shows the LSI state in sub-active mode. Figure 5 shows a diagram of transition from sub-active mode to watch mode.

Table 2 LSI State

Function		Active (high-speed)	Watch	Sub-active
System clock oscillator		Operating	Stopped	Stopped
Sub-clock oscillator		Operating/stopped	Operating	Operating
CPU	Instruction	Operating	Stopped	Operating
	RAM	Operating	Retained	Operating
	Register	Operating	Retained	Operating
	I/O	Operating	Retained	Operating
External interrupt	NMI	Operating	Operating	Operating
	IRQ0	Operating	Operating	Operating
	IRQ1	Operating	Operating	Operating
	IRQAEC	Operating	Operating	Operating
Peripheral module	Timer B1	Operating	Operating/retained*1	Operating/retained*1
	Timer W	Operating	Retained	Operating/retained*2
	WDT	Operating	Operating/retained*3	Operating/retained*3
	RTC	Operating	Operating/retained*4	Operating/retained*4
	Asynchronous event counter	Operating	Operating	Operating
	SCI3/IrDA	Operating	Reset	Operating/retained*5
	IIC2	Operating	Retained	Retained
	SSU	Operating	Retained	Operating/retained*6
	A/D converter	Operating	Retained	Operating/retained*7
	Comparator	Operating	Operating	Operating

Notes: *1. Operating when ϕ_W/256 or ϕ_W/1024 is selected as an internal clock; otherwise, stopped and retained.

*2. Operating when ϕ_W, ϕ_W/4 or ϕ_W/16 is selected as an internal clock; otherwise, stopped and retained.

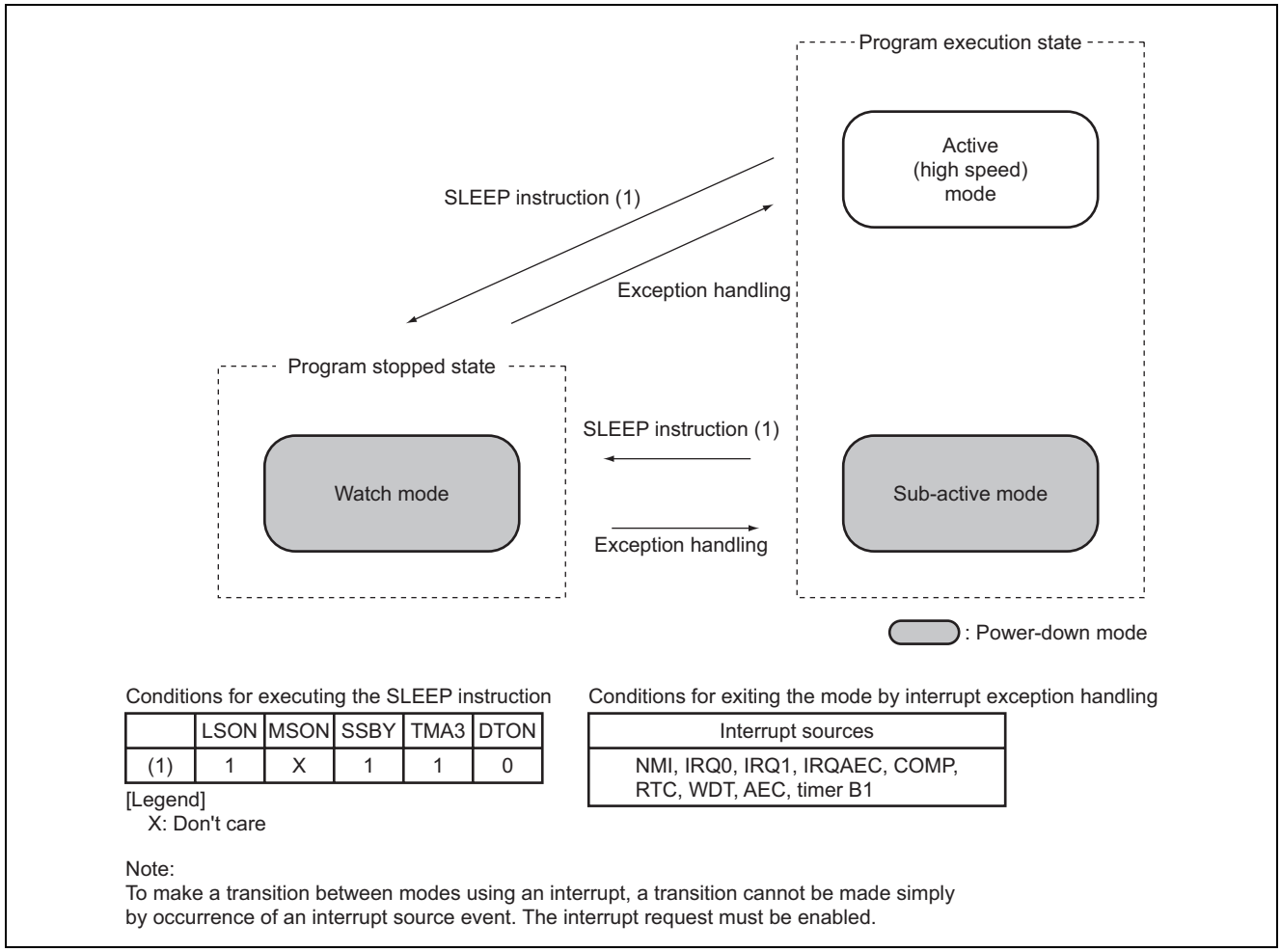
*3. Operating when the on-chip oscillator or ϕ_W/16 or ϕ_W/256 is selected as an internal clock; otherwise, stopped and retained.

*4. Operating when ϕ_W/4 is selected as an internal clock; otherwise, stopped and retained.

*5. Operating when ϕ_W is selected an internal clock; otherwise, stopped and retained.

*6. Operating when ϕ_{SUB}/2 is selected as an internal clock; otherwise, stopped and retained.

*7. Operating when ϕ_W/2 is selected as an internal clock; otherwise, stopped and retained.



Conditions for executing the SLEEP instruction

	LSON	MSON	SSBY	TMA3	DTON
(1)	1	X	1	1	0

[Legend]
X: Don't care

Conditions for exiting the mode by interrupt exception handling

Interrupt sources
NMI, IRQ0, IRQ1, IRQAEC, COMP, RTC, WDT, AEC, timer B1

Note:
To make a transition between modes using an interrupt, a transition cannot be made simply by occurrence of an interrupt source event. The interrupt request must be enabled.

Figure 5 Mode Transition Diagram

- Transition from active (high-speed) mode to watch mode
  1. Set the SSBY and LSON bit of SYSCR1 to 1 and clear the TMA3 bit to 0.
  2. Clear DTON of SYSCR2 to 0.
  3. Execute the SLEEP instruction.

- Exit from watch mode
  1. In watch mode, accept NMI, IRQ0, IRQ1, IRQAEC, COMP, RTC, WDT, AEC, or timer B1 interrupt request.
  2. Execute interrupt handling. (In this application, the LSI recovers to sub-active mode.)

- Transition from sub-active mode to watch mode
  1. Set the SSBY and LSON bit of SYSCR1 to 1 and clear the TMA3 bit to 0.
  2. Clear the DTON bit of SYSCR2 to 0.
  3. Execute the SLEEP instruction.

3.4.3 Module Standby Mode

The module standby function can be set for all peripheral modules. When placed in the module standby state, a module has its clock supply stopped, entering the power-down state. A module is placed in the module standby state by setting the bit of CKSTPR1 or CKSTPR2 that corresponds to that module to 0, and is released from the state by setting it to 1.

3.5 Watchdog Timer Function

The H8/38602R has an internal watchdog timer (WDT). After a reset, the WDT is turned on. The WDT is an 8-bit timer, and resets the inside of the H8/38602 when the CPU is unable to change a counter value, causing an overflow to occur, due to a fault such as a system runaway. Because this application note does not use the watchdog timer function, the watchdog timer function is stopped.

- The timer control/status register WD1 (TCSRWD1)
  The timer control/status register WD1 (TCSRWD1) controls writing to TCSRWD1 itself and to TCWD. TCSRWD1 also controls the operation of the watchdog timer and indicates its operating status. To rewrite this register, use the MOVE instruction. Bit manipulation instructions cannot be used to change its setting.

3.6 Interrupt Controller

The H8/38602R uses an interrupt controller to control interrupts.

- Interrupt Enable Register 1 (IENR1)
  IENR1 enables RTC, IRQAEC, IRQ1, and IRQ0 interrupt requests.

3.7 LM35DZ Precision, Centigrade Temperature Sensor IC

The temperature sensor IC used in this application note is described below. The LM35DZ is a precision IC temperature sensor whose output voltage is linearly proportional to Centigrade (°C) temperature. The operating voltage ranges from 4 to 30 V, and the temperature coefficient is linear, +10 mV/°C. For detailed data sheets and other information, visit the website (http://www.national.com/) of National Semiconductor Corporation.

3.8 Assignment of Functions

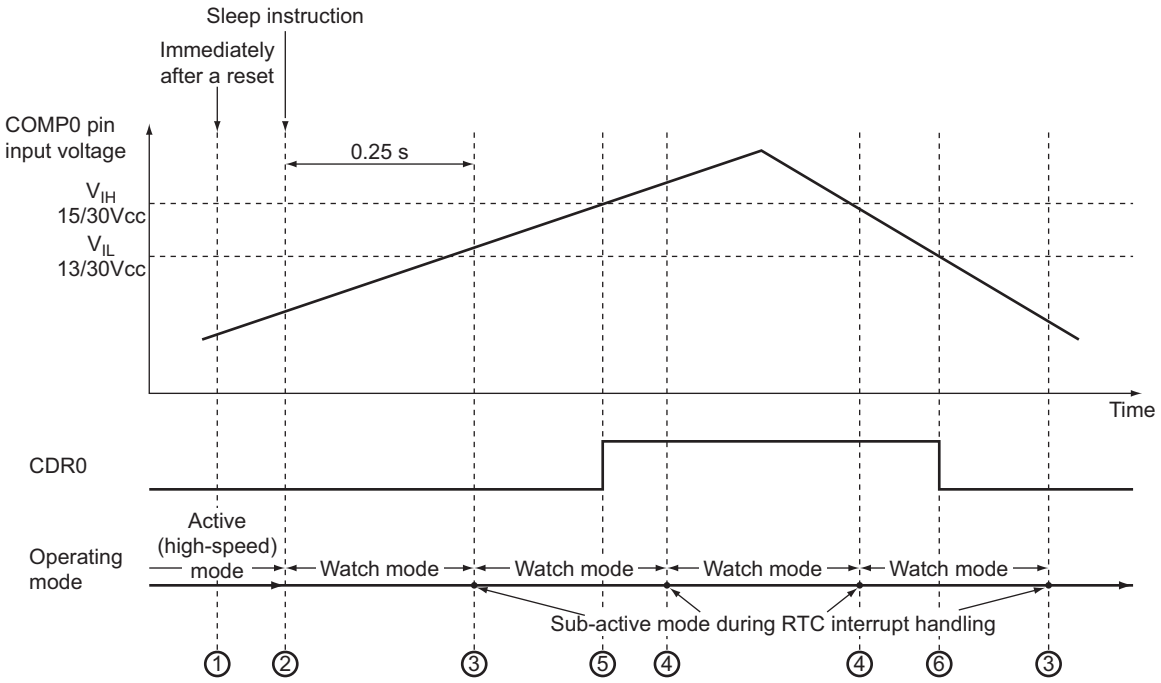
The function assignment of this sample task is given in table 3. Functions are assigned as shown in the table to make a sensor connection with low supply current using the comparator and the A/D converter.

Table 3 Assignment of Functions

Function	Assignment of Function
CMCR0	Controls comparator operation and selects a reference voltage.
CMDR	Stores the results of comparison by the comparator.
ADRR	Stores the A/D-converted result.
AMR	Selects a clock for A/D conversion and selects AN0 as the analog channel.
ADSF	Controls the start/stop of A/D conversion.
RTCCR1	Controls the operation and reset of the RTC.
RTCCR2	Controls RTC periodic interrupts.
RTCCSR	Selects a clock source for the RTC.
SYSCR1	Controls mode transition together with SYSCR2.
SYSCR2	Controls mode transition together with SYSCR1.
CKSTPR1	Controls module standby state together with CKSTPR2.
CKSTPR2	Controls module standby state together with CKSTPR1.
IENR1	Controls RTC periodic interrupts.
TCRWD1	Stops the watchdog timer.

4. Principles of Operation

The method of connecting a sensor with a low supply current using the comparator and the A/D converter is shown in figure 6. Through the hardware processing and software processing shown in figure 6, a sensor is connected with low supply current using the comparator and the A/D converter.



① Hardware processing

None

Software processing

a. Set power-down mode.
b. Set the module standby state.
c. Configure the comparator.
d. Configure the A/D converter.
e. Configure the RTC.
f. Stop the WDT.
g. Enable interrupts.
h. Start comparator operation.

② Hardware processing

Enter watch mode.

Software processing

a. Start the RTC.
b. Enter watch mode by Sleep instruction.

③ Hardware processing

a. Set 025SEIFG to 1.
b. Recover to sub-active mode.
c. Enter watch mode.

Software processing

a. Start RTC 0.25-second interrupt handling.
b. Clear 025SEIF to 0.
c. Dummy-read the CDR0 bit.
d. Check the CDR0 bit.
e. Enter watch mode by sleep instruction.

④ Hardware processing

a. Set 025SEIFG to 1.
b. Recover to sub-active mode.
c. Enter watch mode.

Software processing

a. Start RTC 0.25-second interrupt handling.
b. Clear 025SEIF to 0.
c. Dummy-read the CDR0 bit.
d. Check the CDR0 bit.
e. Start A/D conversion.
f. Enter watch mode by sleep instruction.

⑤ Hardware processing

Set the CDR0 bit to 1.

⑥ Hardware processing

Clear the CDR0 bit to 0.

Figure 6 Connecting a Sensor with Low Supply Current Using Comparator and A/D Converter

5. Description of Software

5.1 Modules

Table 4 lists the modules of this sample task.

Table 4 Description of Modules

Module Name	Label Name	Description
Main routine	main	Configures the comparator, A/D converter and RTC, sets the mode to enter by the sleep instruction, makes settings for power-down modes and the module standby function, initializes the RAM area for use, stops the WDT, and enables interrupts.
RTC interrupt	rtc_int	Performs comparison by the comparator and A/D conversion.

5.2 Arguments

This sample task does not use arguments.

5.3 Internal Registers Used

This section describes the internal registers used in this sample task.

- Compare Control Register 0 (CMCR0) Address: H'F0DC

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	CME0	0	0/1	R/W	Comparator Enable 0: The comparator is stopped. 1: The comparator operates.
6	CMIE0	0	0	R/W	Comparator Interrupt Enable 0: Comparator interrupts are disabled. 1: Comparator interrupts are enabled.
5	CMR0	0	0	R/W	Comparator Reference Voltage Select 0: Internal power supply voltage is selected as the reference voltage. 1: Reference voltage is input from the VCref pin. For information on the combinations of the CMR and CMLS bits, see table 5.
4	CMLS0	0	1	R/W	Comparator Hysteresis Select 0: Hysteresis is deselected. 1: Hysteresis is selected. When CMR = 1, clear this bit to 0. For information on the combinations of the CMR and CMLS bits, see table 5.
3	CRS3	0	0	R/W	Internal Reference Voltage Select When CMR = 0 and CMLS = 0, the electric potential of V_{IH} is selected as the internal power-supply voltage. When CMR = 0 and CMLS = 1, V_{IL} will be as below according to the settings of bits CRS3 to CRS0. When CMR = 1, the settings of bits CRS3 to CRS0 are invalid. 0100: V_{IH} 15/30 Vcc, V_{IL} 13/30 Vcc
2	CRS2	0	1	R/W	
1	CRS1	0	0	R/W	
0	CRS0	0	0	R/W	

Table 5 Combinations of CMR and CMLS Bits

CMR	CMLS	Description
0	0	Compares the internal power-supply voltage (V_{IH} voltage set by bits CRS3 to CRS0) and the potential on the COMP pin. No hysteresis involved.
	1	Compares the internal power-supply voltage and the potential on the COMP pin. Hysteresis involved. V_{IH} and V_{IL} are set by bits CRS3 to CRS0.
1	0	Compares VCref with the potential on the COMP pin. No hysteresis involved.
	1	Setting prohibited

- Compare Data Register (CMDR) Address: H'F0DE

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
0	CDR0	—*	0/1	R	[Setting condition] • COMP0 pin potential > Reference voltage [Clearing condition] • COMP0 pin potential ≤ Reference voltage

Note: * Determined from the pin state and the reference voltage.

- A/D Result Register (ADRR) Address: H'FFBC

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
15	ADR9	Undefined	Undefined	R	ADRR is a 16-bit read-only register for storing A/D conversion results. Data is stored in the ten higher-order bits of ADRR. ADRR is always readable by the CPU. The ADRR value during A/D conversion is undefined, and after A/D conversion, ten bits of A/D-converted data are stored and held until the next conversion is started. The initial value of ADRR is undefined. This register should be read in a word unit.
14	ADR8	Undefined	Undefined	R	
13	ADR7	Undefined	Undefined	R	
12	ADR6	Undefined	Undefined	R	
11	ADR5	Undefined	Undefined	R	
10	ADR4	Undefined	Undefined	R	
9	ADR3	Undefined	Undefined	R	
8	ADR2	Undefined	Undefined	R	
7	ADR1	Undefined	Undefined	R	
6	ADR0	Undefined	Undefined	R	
5	—	—	—	—	
4	—	—	—	—	
3	—	—	—	—	
2	—	—	—	—	
1	—	—	—	—	
0	—	—	—	—	

- A/D Mode Register (AMR) Address: H'FFBE

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
6	TRGE	0	0	R/W	External Trigger Select Enables or disables starting of A/D conversion by external trigger input. 0: Starting of A/D conversion by an external trigger is disabled. 1: A/D conversion is started on a rising or falling edge of the $\overline{\text{ADTRG}}$ pin. Which edge of the $\overline{\text{ADTRG}}$ to select can be specified with the ADTRGNEG bit of IEGR.
5	CKS1	0	1	R/W	Clock Select
4	CKS0	0	1	R/W	Select a clock source for A/D conversion. 00: ϕ/8 (Conversion time = 124 states (max) (when reference clock = ϕ)) 01: ϕ/4 (Conversion time = 62 states (max) (when reference clock = ϕ)) 10: ϕ/2 (Conversion time = 31 states (max) (when reference clock = ϕ)) 11: ϕ_W/2 (Conversion time = 31 states (max) (when reference clock = ϕ_{SUB})) When the setting is 11 and the mode is sub-active or sub-sleep mode, the A/D converter is operational only when the CPU operating clock is ϕ_W.
3	CH3	0	0	R/W	Channel Select 3 to 0
2	CH2	0	1	R/W	Select an analog input channel.
1	CH1	0	0	R/W	00xx: No selection
0	CH0	0	0	R/W	0100: AN0 0101: AN1 0110: AN2 0111: AN3 1000: AN4 1001: AN5 101x: No selection 11xx: No selection To switch channels, ADSF must be cleared to 0.

Legend:
x: Don't care

- A/D Start Register (ADSR) Address: H'FFBF

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	ADSF	0	0/1	R/W	Setting this bit to 1 causes A/D conversion to start. After the conversion has ended, the converted data is set in ADRR and this bit is cleared to 0 at the same time. A/D conversion can be forcibly terminated by writing 0 to this bit.

- RTC Control Register 1 (RTCCR1) Address: H'F06C

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	RUN	—/(0)*	0/1	R/W	RTC Operation Start 0: The RTC stops operation. 1: The RTC starts operation.
4	RST	0	1/0	R/W	Reset 0: Normal operation 1: All registers and the control circuit of the RTC are reset except for RTCCSR and this bit. Note that after setting this bit to 1, be sure to clear it to 0.

Note: * Initial value after the RTC is reset with the RST bit of RTCCR1.

- RTC Control Register 2 (RTCCR2) Address: H'F06D

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
0	025SEIE	—/(0)*	0/1	R/W	0.25-second Periodic Interrupt Enable 0: 0.25-second periodic interrupts are disabled. 1: 0.25-second periodic interrupts are enabled.

Note: * Initial value after the RTC is reset with the RST bit of RTCCR1.

- Clock Source Select Register (RTCCSR) Address: H'F06F

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
3	RCS3	1	1	R/W	Clock Source Select
2	RCS2	0	0	R/W	0000: ϕ/8 (Free-running counter operation)
1	RCS1	0	0	R/W	0001: ϕ/32 (Free-running counter operation)
0	RCS0	0	0	R/W	0010: ϕ/128 (Free-running counter operation) 0011: ϕ/256 (Free-running counter operation) 0100: ϕ/512 (Free-running counter operation) 0101: ϕ/2048 (Free-running counter operation) 0110: ϕ/4096 (Free-running counter operation) 0111: ϕ/8192 (Free-running counter operation) 1000: RTC operation at 32.768 kHz 1001 to 1111: Setting prohibited

- RTC Interrupt Flag Register (RTCFLG) Address: H'F067

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
0	025SEIFG	—/(0)*2	0/1	R/W*1	[Setting condition] • A 0.25-second periodic interrupt is generated. [Clearing condition] • When 025SEIFG is 1, 0 is written to 025SEIFG.

Note: *1 Only 0 can be written to clear the flag.
*2 Initial value after the RTC is reset with the RST bit of RTCCR1.

- System Control Register 1 (SYSCR1) Address: H'FFF0

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	SSBY	0	1	R/W	Software Standby Selects the mode to enter after the SLEEP instruction is executed. 0: Sleep mode or sub-sleep mode 1: Standby mode or watch mode
6	STS2	0	1	R/W	Standby Timer Select 2 to 0 When a transition is to be made from standby mode, sub-active mode, or watch mode to active mode or sleep mode, these bits set the number of states to wait from the start of the oscillation of the system clock oscillator until clock pulses are supplied. Set the number so that the waiting time is equal to or greater than oscillation stabilization time in accordance with the operating frequency. When the on-chip oscillator is used, the minimum (STS2 = 1, STS1 = 1, and STS0 = 1) is recommended. With a setting other than the recommended value, operation may start before the waiting time has elapsed.
5	STS1	0	1	R/W	
4	STS0	0	0	R/W	
3	LSON	0	1	R/W	Selects whether to use the system clock (ϕ) or the subclock (ϕ_{SUB}) as the CPU operating clock when watch mode is exited. 0: Uses the system clock (ϕ) as the CPU operating clock. 1: Uses the sub-clock (ϕ_{SUB}) as the CPU operating clock.
2	TMA3	0	1	R/W	This bit selects the mode to enter after the SLEEP instruction is executed in combination with SSBY and LSON of SYSCR1 and DTON and MSON of SYSCR2.
1	MA1	1	0	R/W	Active Mode Clock Select 1 and 0
0	MA0	1	0	R/W	Select the operating clock in active (medium-speed) and sleep (medium-speed) mode. Write to the MA1 and MA0 bits only in active (high-speed) mode or sub-active mode. 00: $\phi_{OSC}/8$ 01: $\phi_{OSC}/16$ 10: $\phi_{OSC}/32$ 11: $\phi_{OSC}/64$

- System Control Register 2 (SYSCR2) Address: H'FFF1

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
3	DTOM	0	1	R/W	Direct Transfer On Flag This bit selects the mode to enter after the SLEEP instruction is executed together with SYSCR1's SSBY, TMA3, LSON bits, and SYSCR2's MSON bit.
2	MSON	0	0	R/W	Middle Speed On Flag This bit selects whether to enter active (high-speed) mode or active (middle-speed) mode after standby mode, watch mode, or sleep mode is exited. 0: Active (high-speed) mode 1: Active (middle-speed) mode
1	SA1	0	1	R/W	Sub-active Mode Clock Select 1 and 0
0	SA0	0	1	R/W	Select a sub-active and sub-sleep mode operating clock. A switch to the selected clock is made after the SLEEP instruction is executed. 00: $\phi_W/8$ 01: $\phi_W/4$ 10: $\phi_W/2$ 11: ϕ_W

- Clock Stop Register 1 (CKSTPR1) Address: H'FFFA

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	—	0	—	—	Reserved bit This bit is always read as 0 and cannot be modified.
6	S3CKSTP	0	0	R/W	SCI3 Module Standby*[1] When this bit is cleared to 0, SCI3 enters standby mode.
5	—	0	—	—	Reserved bit This bit is always read as 0 and cannot be modified.
4	ADCKSTP	0	1	R/W	A/D Converter Module Standby When this bit is cleared to 0, the A/D converter enters standby mode.
3	—	0	—	—	Reserved bit This bit is always read as 0 and cannot be modified.
2	TB1CKSTP	0	0	R/W	Timer B1 Module Standby When this bit is cleared to 0, timer B1 enters standby mode.
1	FROMCKSTP*[2]	1	1	R/W	Flash Memory Module Standby When this bit is cleared to 0, the flash memory enters standby mode.
0	RTCCKSTP	1	1	R/W	RTC Module Standby When this bit is cleared to 0, the RTC enters standby mode.

Note: *1 When SCI3 is placed in module standby mode, all the registers of SCI3 are reset.
*2 Be sure to set this bit to 1 when using an on-chip emulator.

- Clock Stop Register 2 (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	—	0	—	—	Reserved bit This bit is always read as 0 and cannot be modified.
6	TWCKSTP	0	0	R/W	Timer W Module Standby When this bit is cleared to 0, timer W enters standby mode.
5	IICCKSTP	0	0	R/W	IIC2 Module Standby When this bit is cleared to 0, IIC2 enters standby mode.
4	SSUCKSTP	0	0	R/W	SSU Module Standby When this bit is cleared to 0, the SSU enters standby mode.
3	AECCKSTP	0	0	R/W	Asynchronous Event Counter Module Standby When this bit is cleared to 0, the asynchronous event counter enters standby mode.
2	WDCKSTP	0	0	R/W*	Watchdog Timer Module Standby When this bit is cleared to 0, the watchdog timer enters standby mode.
1	COMPCKSTP	0	1	R/W	Comparator Module Standby When this bit is cleared to 0, the comparator enters standby mode.
0	—	0	—	—	Reserved bit This bit is always read as 0 and cannot be modified.

Note: * WDCKSTP is valid when the WDON bit in TCSRW is 0. When WDCKSTP is set to 0 while WDON is 1 (WDT is operating), WDCKSTP is cleared to 0 but the WDT does not enter module standby mode continuing the watchdog function. At the same time when the WDON bit is set to 0 by software, the WDCKSTP bit becomes valid and the WDT enters module standby mode.

- Interrupt Enable Register 1 (IENR1) Address: H'FFF3

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	IENRTC	0	1	R/W	RTC Interrupt Enable Setting this bit to 1 enables RTC interrupt requests.

- Timer Control/Status Register WD1 (TCSRWD1) Address: H'FFB1

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	B6WI	1	1	R/W	Bit 6 Write Disable Writing to bit 6 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
6	TCWE	0	0	R/W	Timer Counter W Write Enable Writing to TCWD is enabled when this bit is set to 1. When writing to this bit, 0 must be written to bit 7.
5	B4WI	1	*	R/W	Bit 4 Write Disable Writing to bit 4 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
4	TCSRWE	0	*	R/W	Timer Control/Status Register W Write Enable Writing to bits 2 and 0 of this register is enabled when this bit is set to 1. When writing to this bit, 0 must be written to bit 5.
3	B2WI	1	*	R/W	Bit 2 Write Disable Writing to bit 2 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
2	WDON	1	*	R/W	Watchdog Timer On Setting this bit to 1 causes TCWD to start counting up. Clearing it to 0 causes TCWD to stop counting up. [Clearing condition] • 0 is written to B2WI and WDON while TCSRWE is 1. [Setting conditions] • A reset is made. • 0 is written to B2WI and 1 is written to WDON while TCSRWE is 1.
1	B0WI	1	1	R/W	Bit 0 Write Disable Writing to bit 0 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
0	WRST	0	0	R/W	Watchdog Timer Reset [Clearing conditions] • A reset is made with the $\overline{\text{RES}}$ pin. • 0 is written to B0WI and WRST while TCSRWE is 1. [Setting condition] • TCWD overflows and an internal reset signal is generated.

Note: * These bits are manipulated so as to stop the watchdog timer. See the flowchart for the main routine.

5.4 RAM Usage

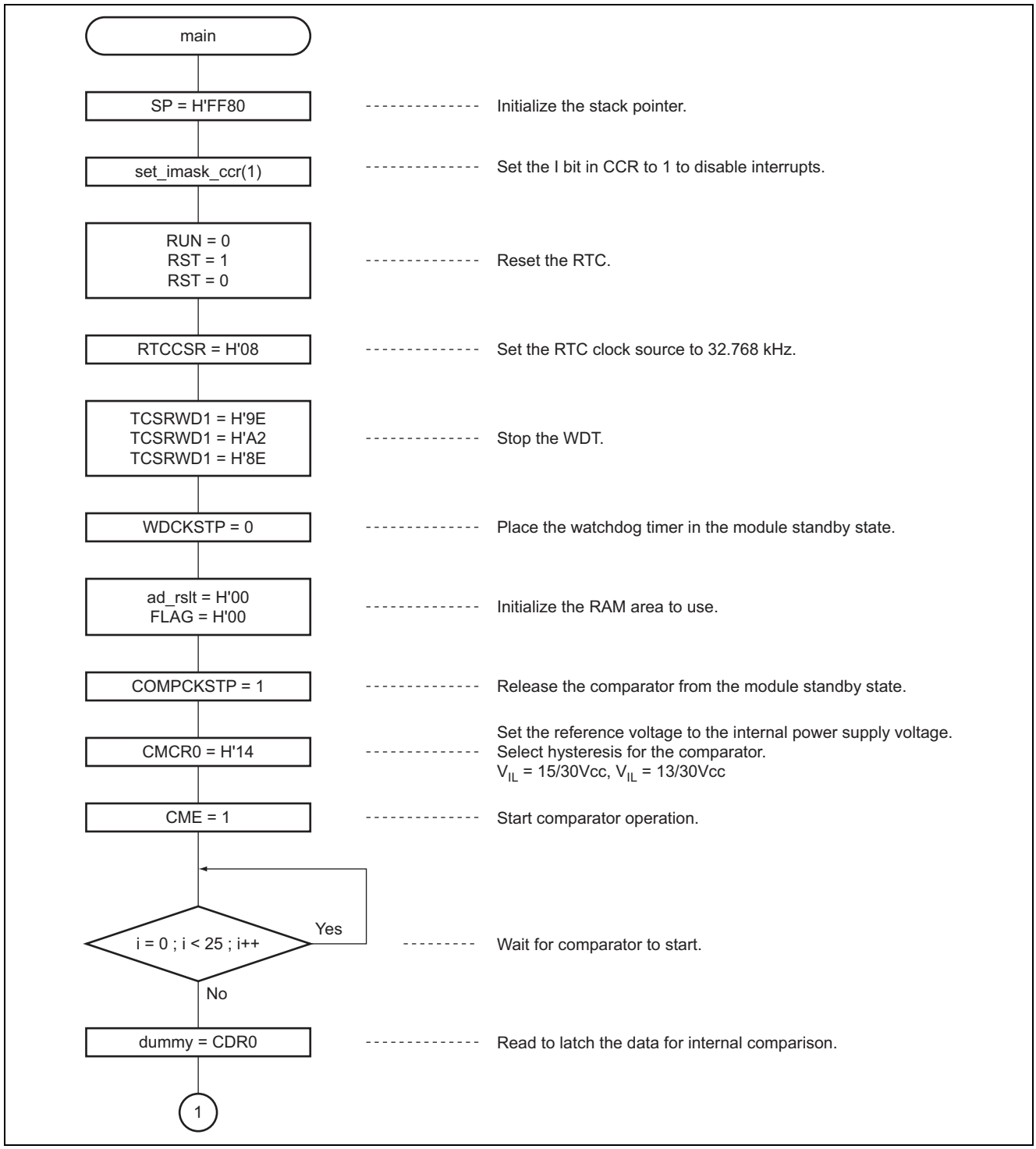
The RAM usage in this sample task is given below.

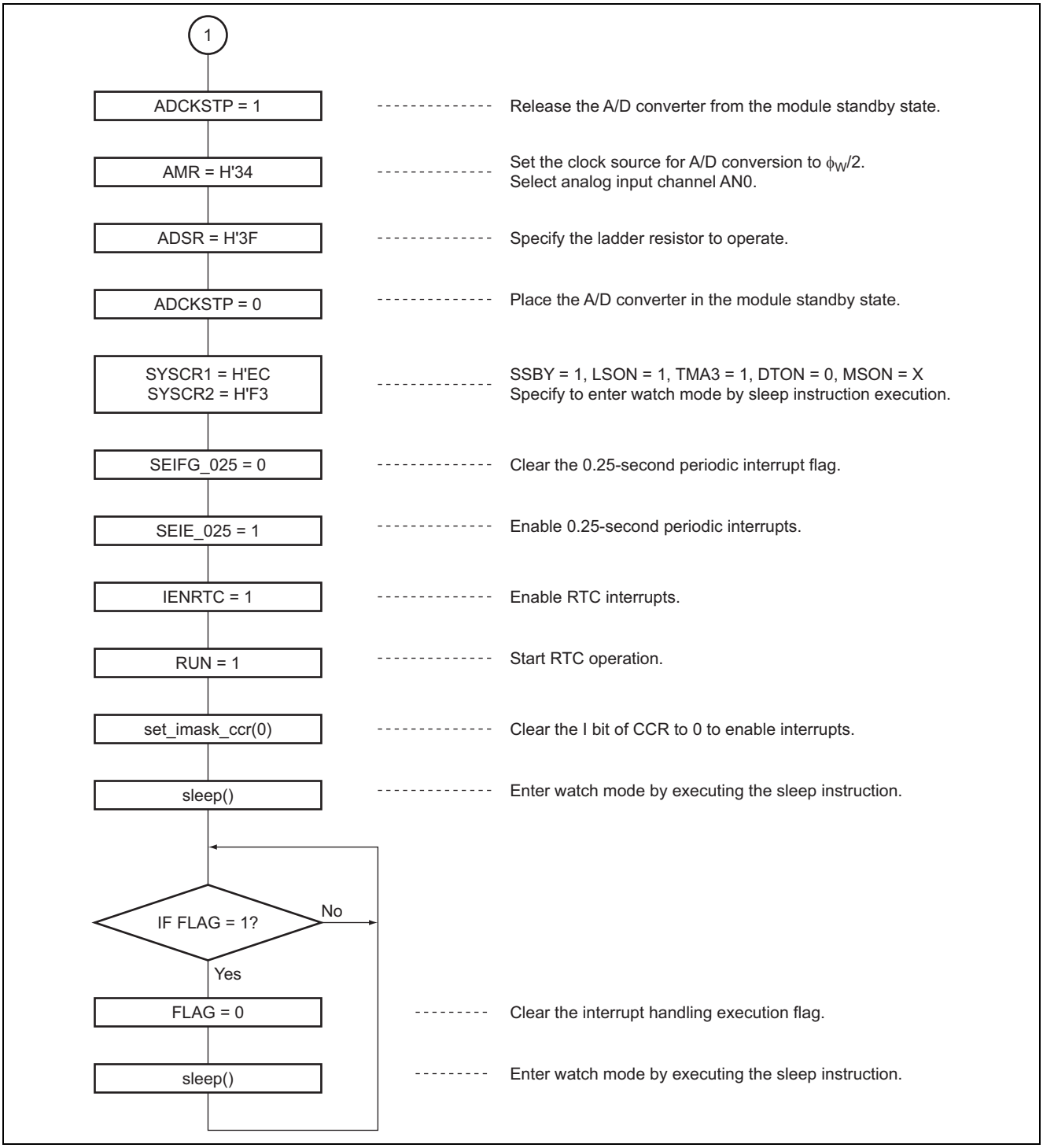
Table 6 RAM Usage

Type	Label Name	Description	Used in
unsigned short	ad_rslt	Stores A/D conversion results.	main, rtc_int
unsigned char	FLAG	Flag indicating the execution of interrupt handling. 0: Interrupt handling is not yet executed. 1: Interrupt handling is being executed.	main, rtc_int

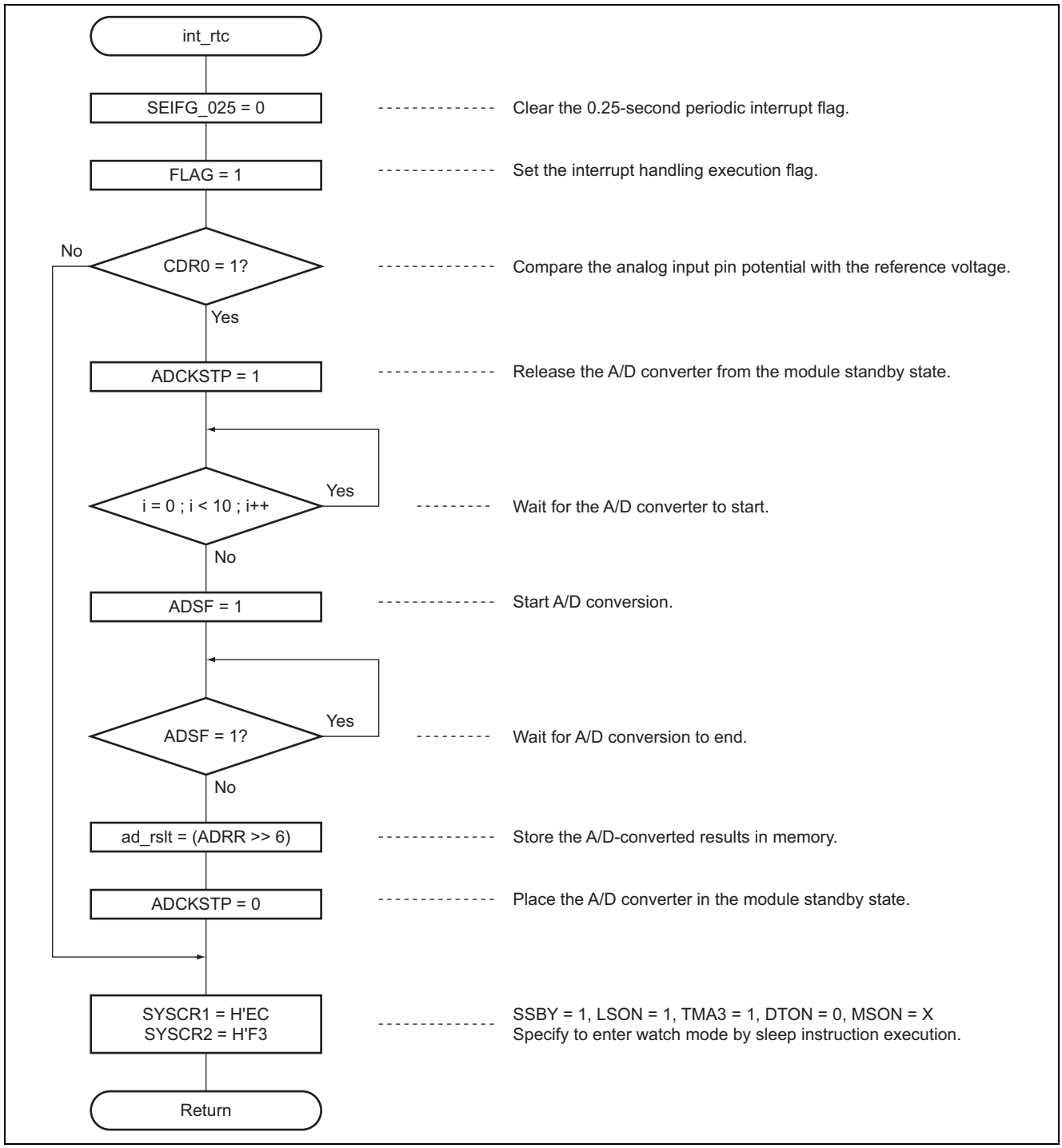
6. Flowcharts

6.1 main Function




1
ADCKSTP = 1
Release the A/D converter from the module standby state.
AMR = H'34
Set the clock source for A/D conversion to φW/2.
Select analog input channel AN0.
ADSR = H'3F
Specify the ladder resistor to operate.
ADCKSTP = 0
Place the A/D converter in the module standby state.
SYSCR1 = H'EC
SYSCR2 = H'F3
SSBY = 1, LSON = 1, TMA3 = 1, DTON = 0, MSON = X
Specify to enter watch mode by sleep instruction execution.
SEIFG_025 = 0
Clear the 0.25-second periodic interrupt flag.
SEIE_025 = 1
Enable 0.25-second periodic interrupts.
IENRTC = 1
Enable RTC interrupts.
RUN = 1
Start RTC operation.
set_imask_ccr(0)
Clear the I bit of CCR to 0 to enable interrupts.
sleep()
Enter watch mode by executing the sleep instruction.
IF FLAG = 1?
No
Yes
FLAG = 0
Clear the interrupt handling execution flag.
sleep()
Enter watch mode by executing the sleep instruction.

6.2 int_rtc Function



7. Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F380

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		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.15.07	—	First edition issued

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