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SH7080 Group

SCIF Asynchronous Serial Data Transfer Function Using the DTC

Introduction

This application note describes data transmission and reception that uses the internal SCIF (Serial Communication Interface with FIFO) for asynchronous serial transfer and a data transfer function that uses the internal DTC (Data Transfer Controller). You can use this application note as reference information for designing user software.

Target Device

SH7085 (R5F7085)

Contents

1. Specifications

This sample application uses an asynchronous serial transfer function with FIFO and a data transfer function that uses the DTC to transmit and receive 32-byte data.

Applicable Conditions:

- Microcomputer: SH7085 (R5F7085)
- Operating frequency: Internal clock 80 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
  MTU2 clock 40 MHz
  MTU2S clock 80 MHz
- C compiler V.9.00.02 manufactured by Renesas Technology Corp.

- The communication format of transmit/receive data is a data length of 8 bits, no parity, and 1 stop bit.
- Data is transmitted and received at 9600 bits/s.
- The transmit trigger number is set to 8, and 32-byte data is transmitted using a transmit-FIFO-data-empty interrupt source.
- The receive trigger number is set to 8, and 32-byte data is received using a receive-data-full interrupt source.

Figure 1 shows the operations in this sample task.

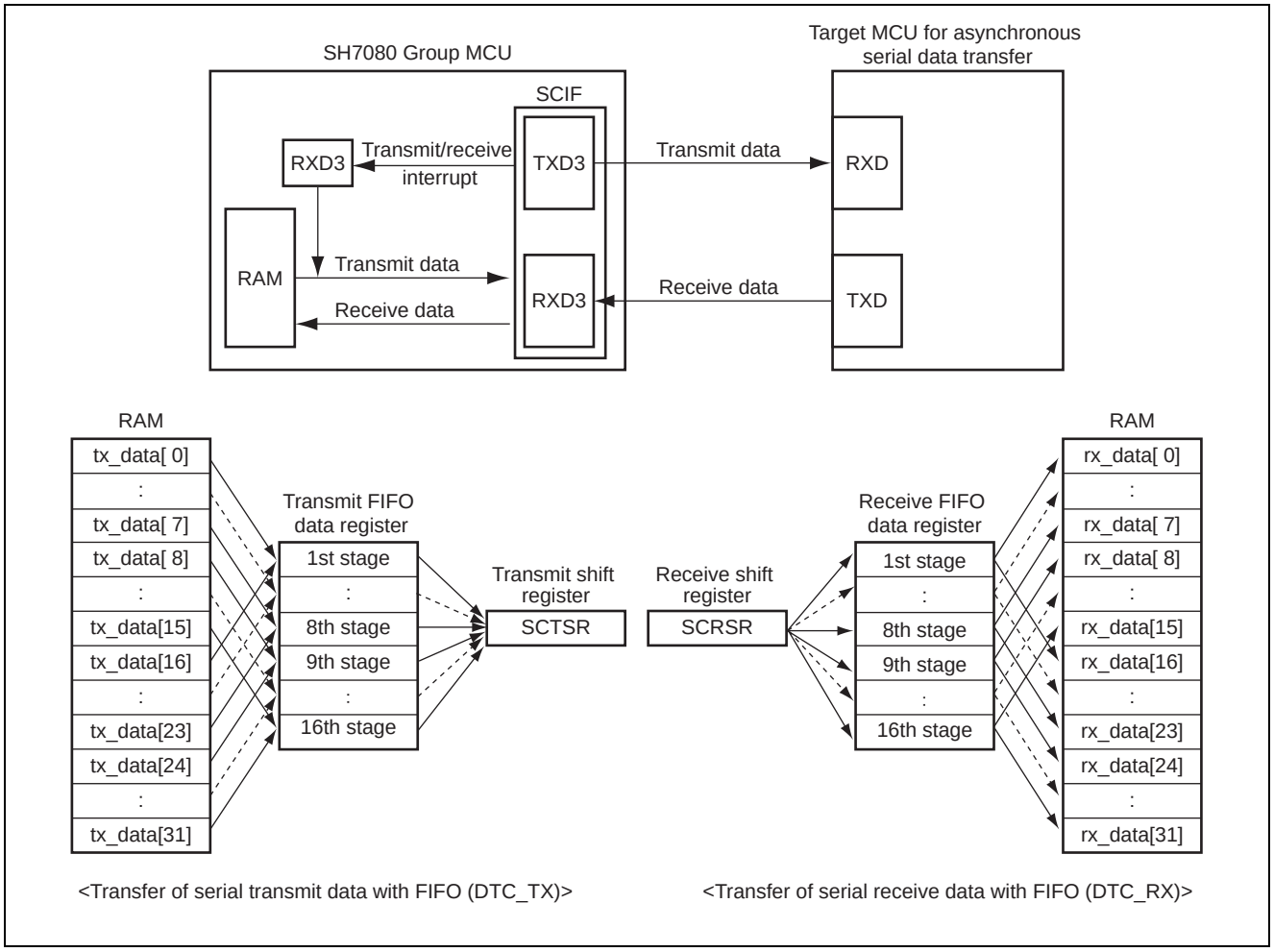


Figure 1 Asynchronous Serial Data Transmission/Reception Using FIFO and the DTC

Table 1 is a list of DTC transfer conditions.

Table 1 DTC Transfer Conditions

Condition	DTC Transfer Condition on SCIF Transmit Side (DTC_TX)	DTC Transfer Condition on SCIF Receive Side (DTC_RX)
Transfer mode	Normal mode	Normal mode
Number of transfer operations	32	32
Transfer size	Bytes	Bytes
Transfer source	Internal RAM	Receive FIFO data register
Transfer destination	Transmit FIFO data register	Internal RAM
Address of transfer source	The transfer source address is incremented after transfer.	Fixed transfer source
Address of transfer destination	Fixed transfer destination	The transfer destination address is incremented after transfer.
Activation source	SCIF transmit-FIFO-data-empty interrupt	SCIF receive-data-full interrupt
Interrupt processing	After completion of the specified data transfer, interrupts are enabled for the CPU.	After completion of the specified data transfer, interrupts are enabled for the CPU.

2. Operational Overview of Functions Used

This sample task uses the Serial Communication Interface with FIFO (SCIF) and the Data Transfer Controller (DTC) to perform asynchronous serial data transmission and reception.

2.1 SCIF Asynchronous Serial Data Transfer

A block diagram of SCIF asynchronous serial data transmission and reception is shown in figure 2.

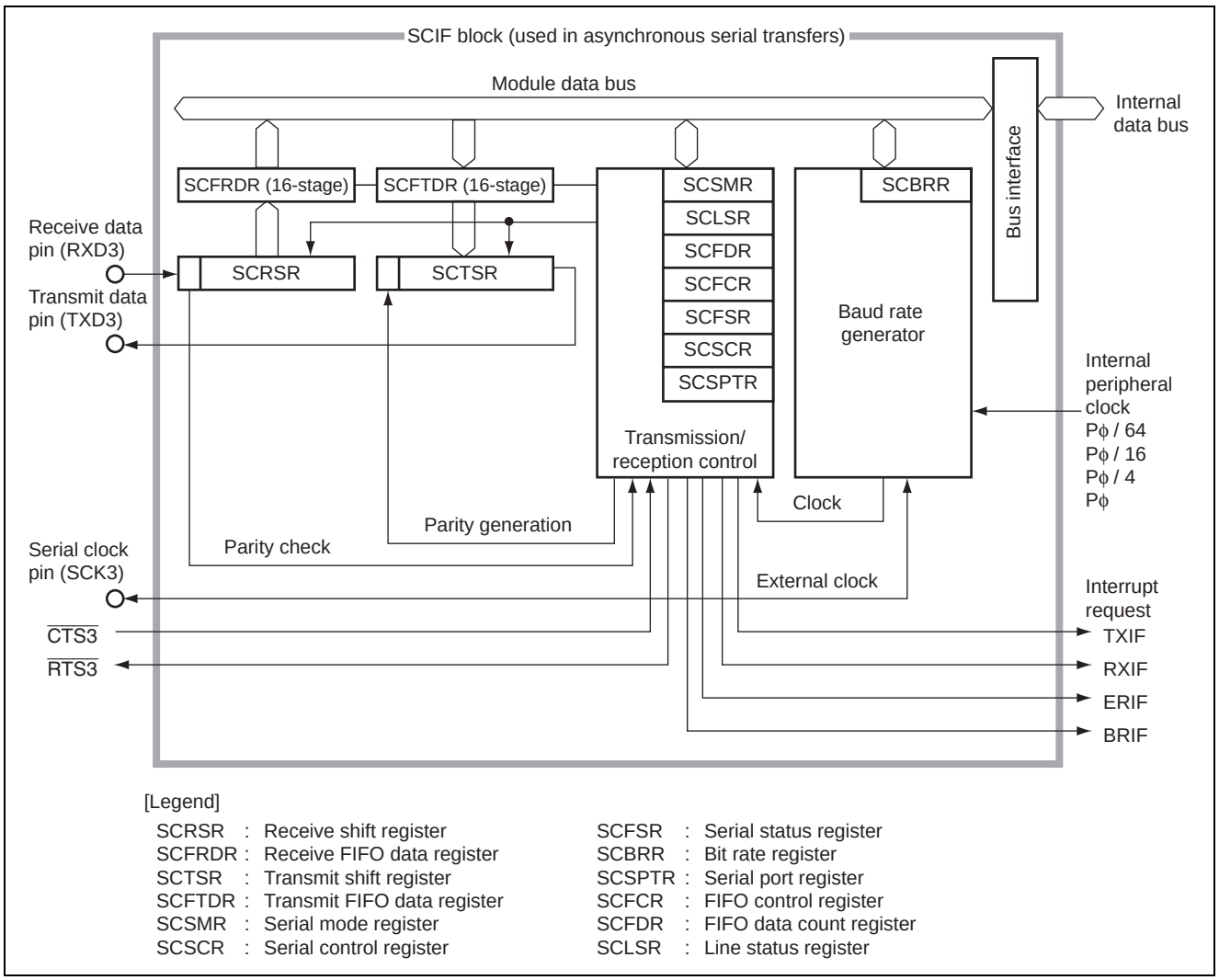


Figure 2 Block Diagram of SCIF (Serial Communication Interface with FIFO)

- Separate 16-stage FIFO registers each for transmission and reception provide efficient, high-speed serial communication.
- Serial data communication is performed by start-stop in character units. The SCIF can communicate with a universal asynchronous receiver/transmitter (UART), an asynchronous communication interface adapter (ACIA), or any other communications chip that employs a standard asynchronous serial system.
- The Receive Shift Register (SCRSR) is used to receive serial data. The SCIF sets serial data input from the RDX pin in SCRSR in the order received starting with the LSB (bit 0) and converts the data to parallel data. When 1 byte of data has been received, the data is transferred automatically to the Receive FIFO Data Register (SCFRDR). The CPU can neither read data from nor write data to SCRSR directly.
- The Receive FIFO Data Register (SCFRDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold received serial data. When 1 byte of serial data has been received, the received serial data is transferred from the Receive Shift Register (SCRSR) to SCFRDR for storage, completing the receive operation. Receive operations can be performed successively until 16 bytes of data are stored in the register. The CPU can read data from SCFRDR, but it cannot write data to SCFRDR. If a read from the Receive FIFO Data Register is attempted when there is no receive data in the register, the value read is undefined. When the register has become full with receive data, any subsequently received serial data is lost.
- The Transmit Shift Register (SCTSR) is used to transmit serial data. The SCIF transfers transmits data from the Transmit FIFO Data Register (SCFTDR) to SCTSR, and performs serial data transmission by sending the data to the TXD pin in order starting with the LSB (bit 0). When 1 byte of data has been transmitted, the next transmit data is transferred automatically from SCFTDR to SCTSR to start transmission. The CPU can neither read data from nor write data to SCTSR directly.
- The Transmit FIFO Data Register (SCFTDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold data that is to be transmitted serially. When the SCIF detects that the Transmit Shift Register (SCTSR) is empty, the SCIF starts serial transmission by transferring the transmit data written in SCFTDR to SCTSR. Serial transmission can be performed as long as data remains in SCFTDR. The CPU can write data to SCFTDR at any time. When SCFTDR becomes full with transmit data (16 bytes), no more data can be written. If an attempt is made to write more data, the data is ignored.
- The Serial Mode Register (SCSMR) is a 16-bit register used to set the SCIF serial communication format and select the clock source of the baud rate generator. The CPU can read data from and write data to SCSMR at any time.
- The Serial Control Register (SCSCR) is a 16-bit register used to enable and disable SCIF transmit and receive operations and interrupt requests and to select the clock source for transmit and receive operations. The CPU can read data from and write data to SCSCR at any time.
- The Serial Status Register (SCFSR) is a 16-bit register. The upper 8 bits indicate the number of receive errors in the data in the Receive FIFO Data Register, and the lower 8 bits consist of status flags indicating the SCIF operating state. The CPU can read data from and write data to SCFSR at any time. However, 1 cannot be written in the ER, TEND, TDFE, BRK, RDF, and DR status flags. Before these flags can be cleared to 0, they must first be read as 1. The FER and PER flags are read-only flags, and no data can be written to them.
- The Bit Rate Register (SCBRR) is an 8-bit register that sets the serial transmit/receive bit rate together with the baud rate generator clock source selected by the CKS1 and CKS0 bits of the Serial Mode Register (SCSMR). The CPU can read data from and write data to SCBRR at any time. SCBRR is initialized to H'FF by a power-on reset.
- The FIFO Control Register (SCFCR) is a 16-bit register used to reset the data count and set the trigger data number for the Transmit FIFO Data Register and the Receive FIFO Data Register. The register also contains a loopback test enable bit. The CPU can read data from and write data to SCFCR at any time.
- The FIFO Data Count Register (SCFDR) is a 16-bit register that indicates the number of data bytes stored in the Transmit FIFO Data Register (SCFTDR) and in the Receive FIFO Data Register (SCFRDR). The upper 8 bits indicate the number of transmit data bytes in SCFTDR, and the lower 8 bits indicate the number of receive data bytes in SCFRDR. The CPU can read data from SCFDR at any time.
- The Line Status Register (SCLSR) is a 16-bit register that the CPU can read from and write to at any time. However, 1 cannot be written to the ORER status flag. Before the ORER status flag can be cleared to 0, they must first be read as 1.

2.2 Operational Overview of Data Transfer Using the DTC

A block diagram of data transfer using the DTC is shown in figure 3.

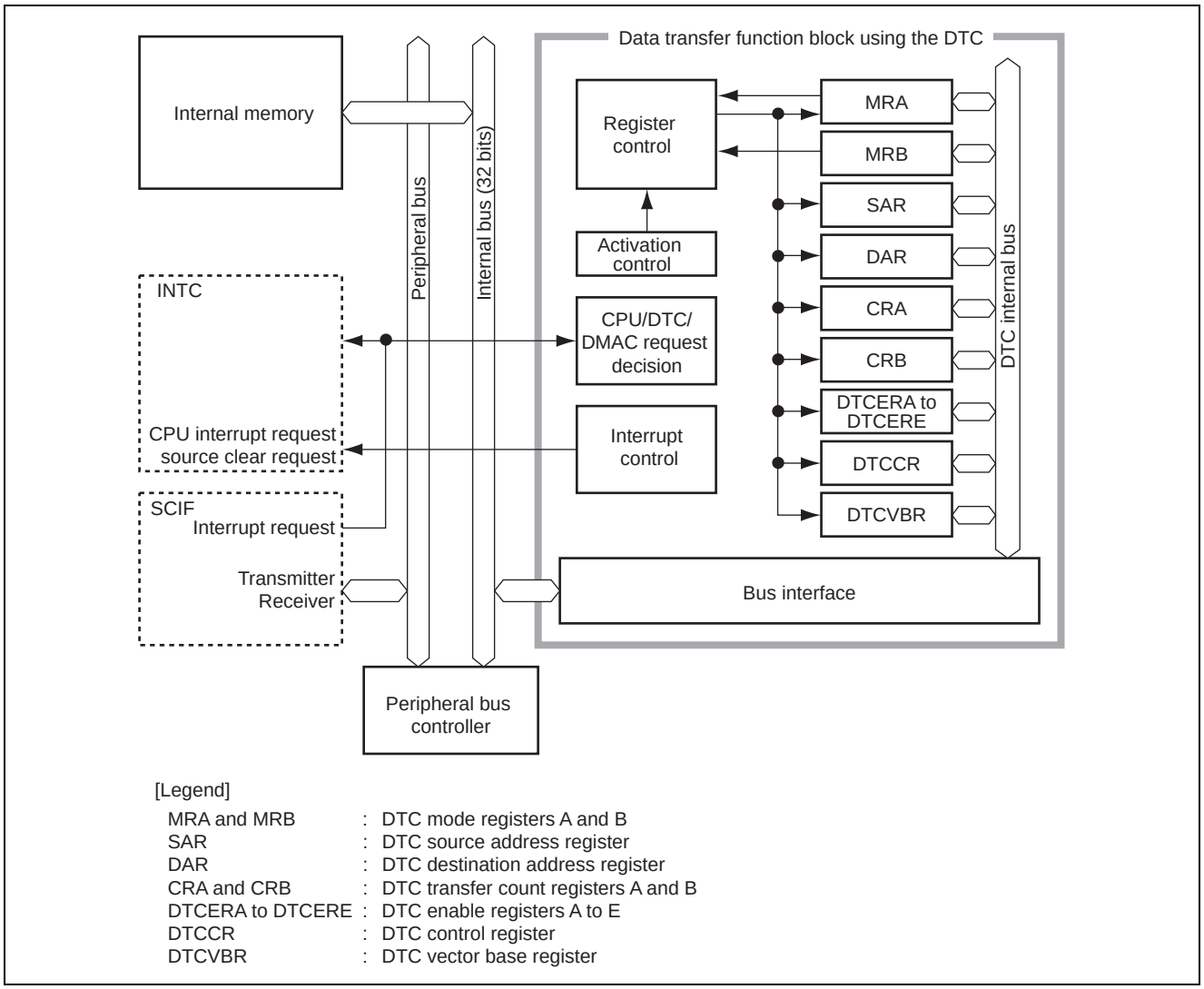


Figure 3 Block Diagram of DTC Used for Data Transfer

- DTC Mode Register A (MRA) selects the DTC operating mode. This register cannot be accessed directly by the CPU.
- DTC Mode Register B (MRB) selects the DTC operating mode. This register cannot be accessed directly by the CPU.
- The DTC Source Address Register (SAR) is a 32-bit register that specifies the address of the transfer source of the data to be transferred by the DTC. This register cannot be accessed directly by the CPU.
- The DTC Destination Address Register (DAR) is a 32-bit register that specifies the address of the transfer destination of the data to be transferred by the DTC. This register cannot be accessed directly by the CPU.
- DTC Transfer Count Register A (CRA) is a 16-bit register that specifies the number of DTC data transfer operations.
  In the normal transfer mode, the entire register functions as a 16-bit transfer counter (1 to 65,536). Each time a data transfer operation is performed, the counter value is decremented by one. When the counter value is set to H'0000, the DTCEn bit (n = 15 to 0) corresponding to the activation source is cleared, and an interrupt request is issued to the CPU. H'0001 set in the counter indicates one transfer operation, H'FFFF indicates 65,535 transfer operations, and H'0000 indicates 65,536 transfer operations.
  In the repeat transfer mode, this register is divided into two parts: CRAH (the upper 8 bits) and CRAL (the lower 8 bits). CRAH holds the number of transfer operations, and CRAL functions as an 8-bit transfer counter (1 to 256). Each time a data transfer is performed, CRAL is decremented by one. When the counter value reaches H'00, the CRAH contents are transferred. If CRAH and CRAL are both set to H'01, the number of transfer operations is 1. If CRAH and CRAL are both set to H'FF, the number of transfer operations is 255. If CRAH and CRAL are both set to H'00, the number of transfer operations is 256.
  In the block transfer mode, this register is divided into two parts: CRAH (the upper 8 bits) and CRAL (the lower 8 bits). CRAH indicates the block size, and CRAL functions as an 8-bit block size counter (1 to 256 bytes, 1 to 256 words, or 1 to 256 longwords). Each time a data transfer operation is performed, CRAL is decremented by one byte (or word or longword). When the counter value reaches H'00, the CRAH contents are transferred. If CRAH and CRAL are both set to H'01, the block size is 1 byte (or 1 word or 1 longword). If CRAH and CRAL are both set to H'FF, the block size is 255 bytes (or 255 words or 255 longwords). If CRAH and CRAL are both set to H'00, the block size is 256 bytes (or 256 words or 256 longwords). This register cannot be accessed directly by the CPU.
- DTC Transfer Count Register B (CRB) is a 16-bit register that specifies the number of the DTC block data transfer operations when the block transfer mode is set. The register functions as a 16-bit counter for counting the number of transfer operations (1 to 65,536). Each time a data transfer operation is performed, the counter is decremented by one. When the counter value reaches H'0000, the DTCEn bit (n = 15 to 0) corresponding to the activation source is cleared, and an interrupt request is issued to the CPU. H'0001 set in the counter indicates one transfer operation, H'FFFF indicates 65,535 transfer operations, and H'0000 indicates 65,536 transfer operations. In the normal transfer mode and the repeat transfer mode, CRB is not used. CRB cannot be accessed directly by the CPU.
- DTC Enable Registers A to E (DTCERA to DTCERE) are used to select an interrupt source that activates the DTC.
- The DTC Control Register (DTCCR) sets skipping of reading of transfer information.
- The DTC Vector Base Register (DTCVBR) is a 32-bit register used to set the base address for vector table address calculation.

3. Principles of Operation

The principles of operation for this sample task are illustrated in figure 4. The software and hardware processing is described in tables 2 and 3.

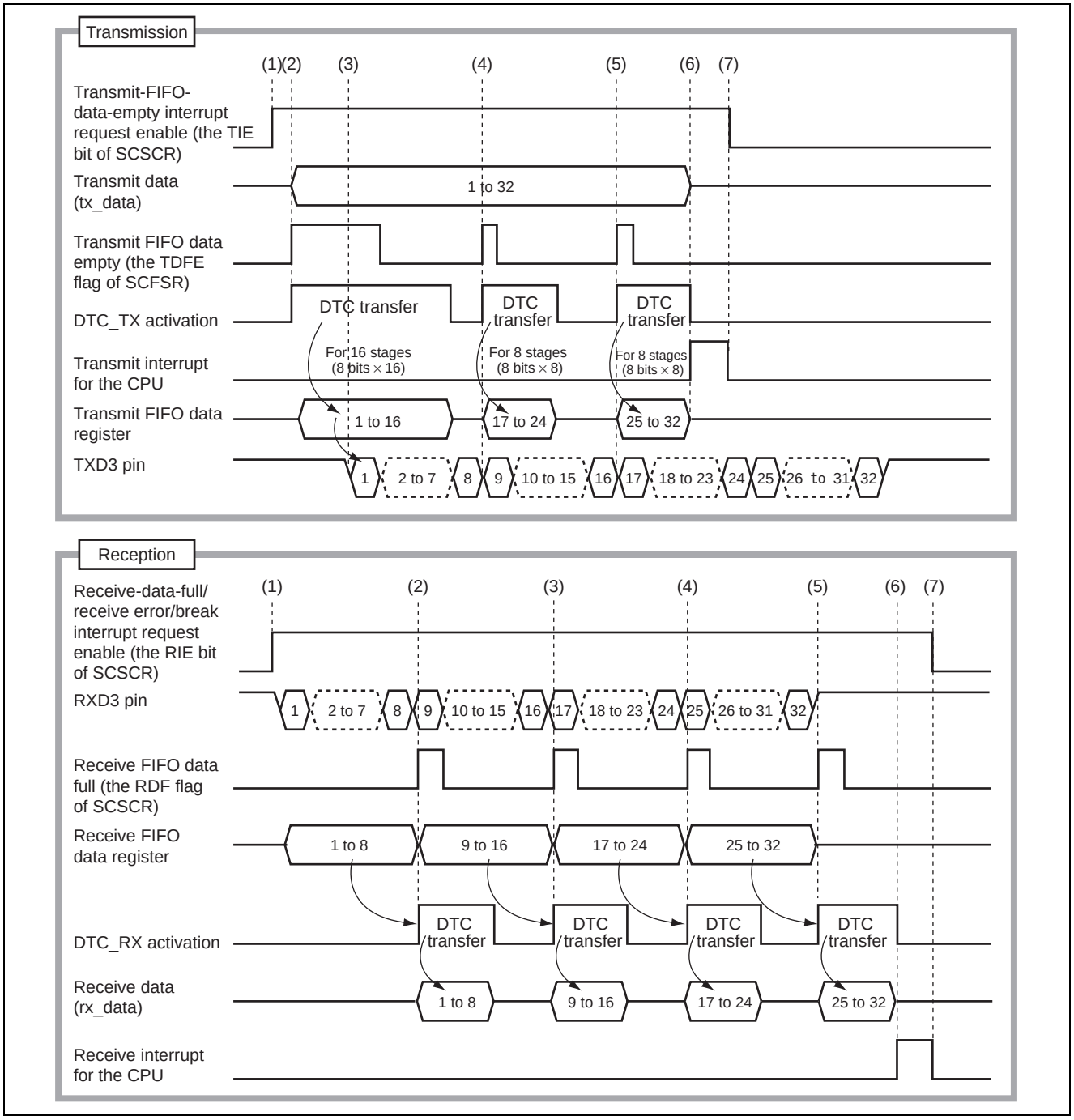


Figure 4 Principles of Operation

Table 2 Description of Software and Hardware Processing (Transmission)

Step	Software Processing	Hardware Processing
(1)	• Enable transmit-data-empty interrupt requests(the TIE bit of SCSCR) and transmit operation (the TE bit of SCSCR).	—
(2)	—	• Activate DTC_TX with a transmit-FIFO-data-empty interrupt. • Transfer transmit data from RAM to the Transmit FIFO Data Register.
(3)	—	• Transmit the 8 bytes of data in the Transmit FIFO Data Register.
(4)	• Same as (2)	• Same as (2)
(5)	• Same as (3)	• Same as (3)
(6)	—	• Transmit the 8 bytes of data in the Transmit FIFO Data Register. • Generate a transmit interrupt for the CPU.
(7)	• Clear Transmit-FIFO-Data-Empty Interrupt Request Enable (the TIE bit of SCSCR) to 0 to disable interrupts.	—

Table 3 Description of Software and Hardware Processing (Reception)

Step	Software Processing	Hardware Processing
(1)	• Enable receive-data-full interrupt requests, receive error interrupt requests, and break interrupt requests (the RIE bit of SCSCR), and enable receive operation (the RE bit of SCSCR).	—
(2)	—	• Activate DTC_RX with a receive-data-full interrupt. • Transfer receive data from the Receive FIFO Data Register to RAM.
(3)	• Same as (2)	• Same as (2)
(4)	• Same as (2)	• Same as (2)
(5)	• Same as (2)	• Same as (2)
(6)	—	• Generate a receive interrupt for the CPU.
(7)	• Read 1 from Receive-Data-Full Interrupt Request/Receive Error Interrupt Request/Break Interrupt Request Enable (the RIE bit of SCSCR) and from Receive Enable (the RE bit of SCSCR), and then clear these bits to 0.	—

4. Description of Software

4.1 Description of Modules

The modules of this sample task are described in table 4.

Table 4 Modules

Module Name	Label Name	Description
Main routine	main()	Sets the DTC, makes the initial settings for the SCIF, and enables transmit and receive operations.
SCIF receive-data-full interrupt routine	int_scif_rxif ()	SCIF receive-data-full interrupts
SCIF receive error interrupt routine	int_scif_erif()	SCIF receive error interrupts
SCIF break interrupt routine	int_scif_brif()	SCIF break interrupts
SCIF transmit-FIFO-data-empty interrupt routine	int_scif_txif()	SCIF transmit-FIFO-data-empty interrupts

4.2 Variables Used

The variables used in this sample task are described in table 5.

Table 5 Variables

Variable, Label Name	Description	Used In
volatile unsigned char tx_data[32]	Transmit data storage area	main ()
volatile unsigned char rx_data[32]	Receive data storage area	main ()

4.3 Setting the Registers

This section describes the setting of registers used in this sample application. Note that the settings shown below are used in the sample task and are not initial values.

4.3.1 Register for Setting the Clock Pulse Generator (CPG)

(1) Frequency Control Register (FRQCR)

The Frequency Control Register specifies the division ratio of the operating frequency.

Setting value: H'0241

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	IFC[2:0]	000	Division ratio of the internal clock (Iϕ) frequency 000: × 1, 80 MHz when the input clock is 10 MHz
11-9	BFC[2:0]	001	Division ratio of the bus clock (Bϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz
8-6	PFC[2:0]	001	Division ratio of the peripheral clock (Pϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz
5-3	MIFC[2:0]	000	Division ratio of the MTU2S clock (MIϕ) frequency 000: × 1, 80 MHz when the input clock is 10 MHz
2-0	MPFC[2:0]	001	Division ratio of the MTU2 clock (MPϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz

4.3.2 Registers for Setting the Power-Down Mode

(1) Standby Control Register 2 (STBCR2)

This register controls the operation of each module in power-down mode.

Setting value: H'28

Bit	Bit Name	Setting Value	Function
7	MSTP7	0	0: RAM in operation.
6	MSTP6	0	0: ROM in operation.
5	—	1	Reserved
4	MSTP4	0	0: DTC in operation.
3	MSTP3	1	1: Stops clock supply to DMAC module.
2-0	—	000	Reserved

(2) Standby Control Register 3 (STBCR3)

This register controls the operation of each module in power-down mode.

Setting value: H'BF

Bit	Bit Name	Setting Value	Function
7	MSTP15	1	1: Stops clock supply to I^2C2 module.
6	MSTP14	0	0: SCIF operates
5	MSTP13	1	1: Stops clock supply to SCI_2 module.
4	MSTP12	1	1: Stops clock supply to SCI_1 module.
3	MSTP11	1	1: Stops clock supply to SCI_0 module.
2	MSTP10	1	1: Stops clock supply to the SSU module.
1-0	—	11	Reserved

4.3.3 Registers for Setting the Data Transfer Controller (DTC)

(1) DTC Control Register (DTCCR)

This register sets skipping of reading the transfer information.

Setting value: H'10

Bit	Bit Name	Setting Value	Function
7-5	—	000	Reserved
4	RRS	1	0: Does not skip reading of the transfer information. 1: Skips reading of the transfer information when the vector number values match.
3	RCHNE	0	0: Disables chain transfer after a repeated transfer.
2-1	—	00	Reserved
0	ERR	0	0: No interrupt requests

(2) Setting transfer information (MRA, MRB, SAR, DAR, CRA, and CRB) for SCIF transmission

- DTC Mode Register A (MRA)

This register selects the DTC operating mode (transfer information for SCIF transmission).

Setting value: H'08

Bit	Bit Name	Setting Value	Function
7-6	MD[1:0]	00	00: Normal transfer
5-4	Sz[1:0]	00	00: Byte transfer
3-2	SM[1:0]	10	10: Increments SAR after a transfer. (SAR is incremented by 1 if B'00 is set to Sz1 and Sz0, by 2 if B'01 is set to Sz0 and Sz1, or by 4 if B'10 is set to Sz0 and Sz1.)
1-0	—	00	Reserved

- DTC Mode Register B (MRB)
  This register selects the DTC operating mode (transfer information for SCIF transmission).
  Setting value: H'00

Bit	Bit Name	Setting Value	Function
7	CHNE	0	0: Disables chain transfer.
6	CHNS	0	0: Performs chain transfer sequentially.
5	DISEL	0	0: Generates an interrupt request for the CPU only when the specified data transfer has been completed.
4	DTS	0	0: The destination side is a repeat area or block area.
3-2	DM[1:0]	00	0x: DAR is fixed.
1-0	—	00	Reserved

- DTC Source Address Register (SAR)
  This register specifies the address of the transfer source of the data to be transferred by the DTC.
  Setting value: &tx_data[0]
- DTC Destination Address Register (DAR)
  This register specifies the address of the transfer destination of the data to be transferred by the DTC.
  Setting value: &SCIF.SCFTDR
- DTC Transfer Count Register A (CRA)
  This register specifies the number of times that the DTC transfers data.
  Setting value: 32
- DTC Transfer Count Register B (CRB)
  This register specifies the number of times that the DTC transfers block data in block transfer mode.
  Setting value: 0

(3) Setting transfer information (MRA, MRB, SAR, DAR, CRA, and CRB) for SCIF reception

- DTC Mode Register A (MRA)
  This register selects the DTC operating mode.
  Setting value: H'00

Bit	Bit Name	Setting Value	Function
7-6	MD[1:0]	00	00: Normal transfer
5-4	Sz[1:0]	00	00: Byte transfer
3-2	SM[1:0]	00	0x: SAR is fixed.
1-0	—	00	Reserved

- DTC Mode Register B (MRB)
  This register selects the DTC operating mode.
  Setting value: H'08

Bit	Bit Name	Setting Value	Function
7	CHNE	0	0: Disables chain transfer.
6	CHNS	0	0: Performs chain transfer sequentially.
5	DISEL	0	0: Generates an interrupt request for the CPU only when the specified data transfer has been completed.
4	DTS	0	0: The destination side is a repeat area or block area.
3-2	DM[1:0]	10	10: Increments DAR after a transfer. (DAR is incremented by 1 if B'00 is set to Sz1 and Sz0, by 2 if B'01 is set to Sz1 and Sz0, or by 4 if B'10 is set to Sz1 and Sz0.)
1-0	—	00	Reserved

- DTC Source Address Register (SAR)
  This register specifies the address of the transfer source of the data to be transferred by the DTC.
  Setting value: &SCIF.SCFRDR

- DTC Destination Address Register (DAR)
  This register specifies the address of the transfer destination of the data to be transferred by the DTC.
  Setting value: &rx_data[0]

- DTC Transfer Count Register A (CRA)
  This register specifies the number of times that the DTC transfers data.
  Setting value: 32

- DTC Transfer Count Register B (CRB)
  This register specifies the number of times that the DTC transfers block data in block transfer mode.
  Setting value: 0

(4) DTC Vector Base Register (DTCVBR)
This register specifies the base address for vector table address calculation.
Setting value: H'00000000

(5) DTC Enable Register E (DTCERE)

This register selects an interrupt source for activating the DTC.

Setting value: H'0300

Bit	Bit Name	Setting Value	Function
15	DTCE15	0	0: No corresponding interrupt source
14	DTCE14	0	0: No corresponding interrupt source
13	DTCE13	0	0: No corresponding interrupt source
12	DTCE12	0	0: No corresponding interrupt source
11	DTCE11	0	0: No corresponding interrupt source
10	DTCE10	0	0: No corresponding interrupt source
9	DTCE9	1	Generation source of the activation source: SCIF, activation source: RXIF
8	DTCE8	1	Generation source of the activation source: SCIF, activation source: TXIF
7	DTCE7	0	0: No corresponding interrupt source
6	DTCE6	0	0: No corresponding interrupt source
5	DTCE5	0	0: No corresponding interrupt source
4	DTCE4	0	0: No corresponding interrupt source
3	DTCE3	0	0: No corresponding interrupt source
2	DTCE2	0	0: No corresponding interrupt source
1	DTCE1	0	0: No corresponding interrupt source
0	DTCE0	0	0: No corresponding interrupt source

4.3.4 Registers for Setting the Serial Communication Interface with FIFO (SCIF)

(1) Serial Control Register (SCSCR)

This register enables or disables transmit and receive operations and interrupt requests, and selects the clock source for transmit and receive operations.

Setting value: H'00F0

Bit	Bit Name	Setting Value	Function
15-8	—	00000000	Reserved
7	TIE	1	0: Disables transmit-FIFO-data-empty interrupt (TXIF) requests. 1: Enables transmit-FIFO-data-empty interrupt (TXIF) requests.
6	RIE	1	0: Disables receive-data-full interrupt (RXIF) requests, receive error interrupt (ERIF) requests, and break interrupt (BRIF) requests. 1: Enables receive-data-full interrupt (RXIF) requests, receive error interrupt (ERIF) requests, and break interrupt (BRIF) requests
5	TE	1	0: Disables transmit operations. 1: Enables transmit operations.
4	RE	1	0: Disables receive operations. 1: Enables receive operations.
3	REIE	0	0: Disables receive error interrupt (ERIF) requests and break interrupt (BRIF) requests.
2	—	0	Reserved
1-0	CKE[1:0]	00	00: The internal clock/SCK pin functions as an input pin (the input signal is ignored).

(2) FIFO Control Register (SCFCR)

This register resets the data count and sets the trigger data number for the Transmit FIFO Data Register and the Receive FIFO Data Register.

Setting value: H'0080

Bit	Bit Name	Setting Value	Function
15-11	—	00000	Reserved
10-8	RSTRG[2:0]	000	000: $\overline{\text{RTS}}$ output active trigger. Invalid because modem signals are not allowed.
7-6	RTRG[1:0]	10	10: Receive FIFO data trigger number = 8
5-4	TTRG[1:0]	00	00: Transmit FIFO data trigger number = 8
3	MCE	0	0: Disables modem signals.
2	TFRST	0	0: Disables resetting of the Transmit FIFO Data Register. 1: Enables resetting of the Transmit FIFO Data Register.
1	RFRST	0	0: Disables resetting of the Receive FIFO Data Register. 1: Enables resetting of the Receive FIFO Data Register.
0	LOOP	0	0: Disables the loopback test.

(3) Serial Status Register (SCFSR)

The upper 8 bits of this register indicate the number of receive errors, and the lower 8 bits indicate the SCIF operating state.

Setting value: H'0000

Bit	Bit Name	Setting Value	Function
15-12	PER[3:0]	0000	Number of parity errors
11-8	FER[3:0]	0000	Number of framing errors
7	ER	0	Receive error
6	TEND	0	0: Transmission is in progress. 1: Transmission has ended.
5	TDFE	0	0: The number of transmit data items written in SCFTDR is greater than the specified transmit trigger number. 1: The number of transmit data items written in SCFTDR is smaller than the specified transmit trigger number.
4	BRK	0	0: No break signal
3	FER	0	0: No framing error
2	PER	0	0: No parity error
1	RDF	0	0: The number of SCFRDR receive data items is smaller than the specified receive trigger number.
0	DR	0	0: Reception is in progress, or there is no receive data left in SCFRDR after normal reception.

(4) Serial Mode Register (SCSMR)

This register sets the communication format and selects the clock source of the baud rate generator.

Setting value: H'0000

Bit	Bit Name	Setting Value	Function
15-8	—	00000000	Reserved
7	C/$\overline{A}$	0	0: Asynchronous mode
6	CHR	0	0: 8-bit data
5	PE	0	0: Disables parity bit addition and checking.
4	O/$\overline{E}$	0	0: Ignores the O/$\overline{E}$ bit specification because PE = 0.
3	STOP	0	0: 1 stop bit
2	—	0	Reserved
1-0	CKS[1:0]	00	00: Pϕ clock

(5) Bit Rate Register (SCBRR)

This register sets the bit rate for serial transmission and reception.

Setting value: H'81

Bit	Bit Name	Setting Value	Function
7-0	—	1000 0001	Bit rate for serial transmission/reception

4.3.5 Registers for Setting the Pin Function Controller (PFC)

(1) Port E IO Register L (PEIORL)

This register selects the input directions of the pins in port E.

Setting value: H'0020

Bit	Bit Name	Setting Value	Function
15	PE15IOR	0	0: PE15 input
14	PE14IOR	0	0: PE14 input
13	PE13IOR	0	0: PE13 input
12	PE12IOR	0	0: PE12 input
11	PE11IOR	0	0: PE11 input. RXD3 input pin
10	PE10IOR	0	0: PE10 input
9	PE9IOR	0	0: PE9 input
8	PE8IOR	0	0: PE8 input
7	PE7IOR	0	0: PE7 input
6	PE6IOR	0	0: PE6 input
5	PE5IOR	1	1: PE5 output. TXD3 output pin
4	PE4IOR	0	0: PE4 input
3	PE3IOR	0	0: PE3 input
2	PE2IOR	0	0: PE2 input
1	PE1IOR	0	0: PE1 input
0	PE0IOR	0	0: PE0 input

(2) Port E Control Register L2 (PECRL2)

This register selects the functions of multiplexed pins in port E.

Setting value: H'0020

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PE7MD[2:0]	000	000: PE7 input/output (port)
11	—	0	Reserved
10-8	PE6MD[2:0]	000	000: PE6 input/output (port)
7	—	0	Reserved
6-4	PE5MD[2:0]	010	010: TXD3 output (SCIF)
3	—	0	Reserved
2-0	PE4MD[2:0]	000	000: PE4 input/output (port)

(3) Port E Control Register L3 (PECRL3)

This register selects the functions of multiplexed pins in port E.

Setting value: H'3000

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PE11MD[2:0]	011	011: RXD3 input (SCIF)
11	—	0	Reserved
10-8	PE10MD[2:0]	000	000: PE10 input/output (port)
7	—	0	Reserved
6-4	PE9MD[2:0]	000	000: PE9 input/output (port)
3	—	0	Reserved
2-0	PE8MD[2:0]	000	000: PE8 input/output (port)

4.3.6 Register for Setting the Interrupt Controller (INTC)

(1) Interrupt Priority Register L (IPRL)

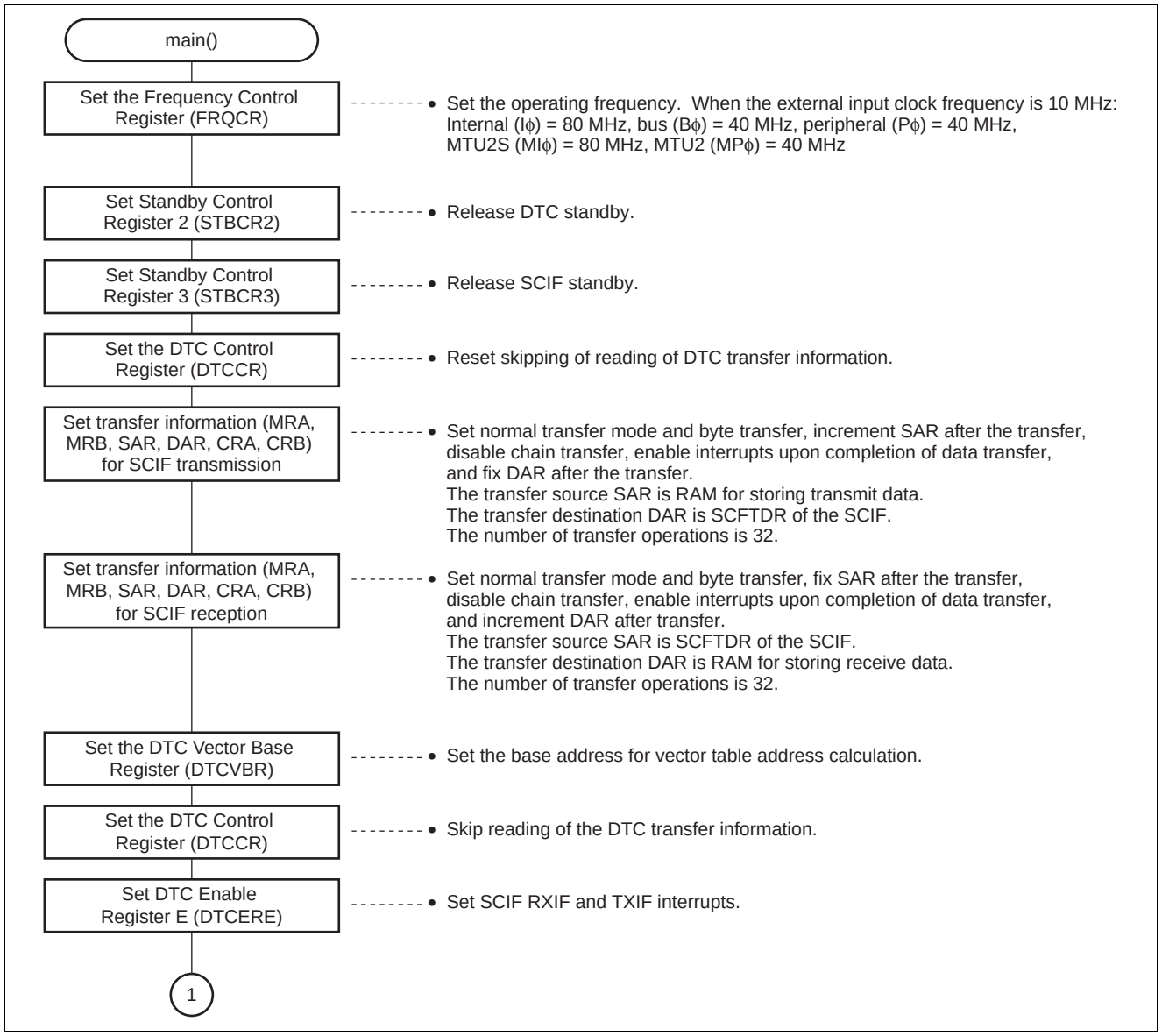
This register determines the priority levels of the corresponding interrupt requests.

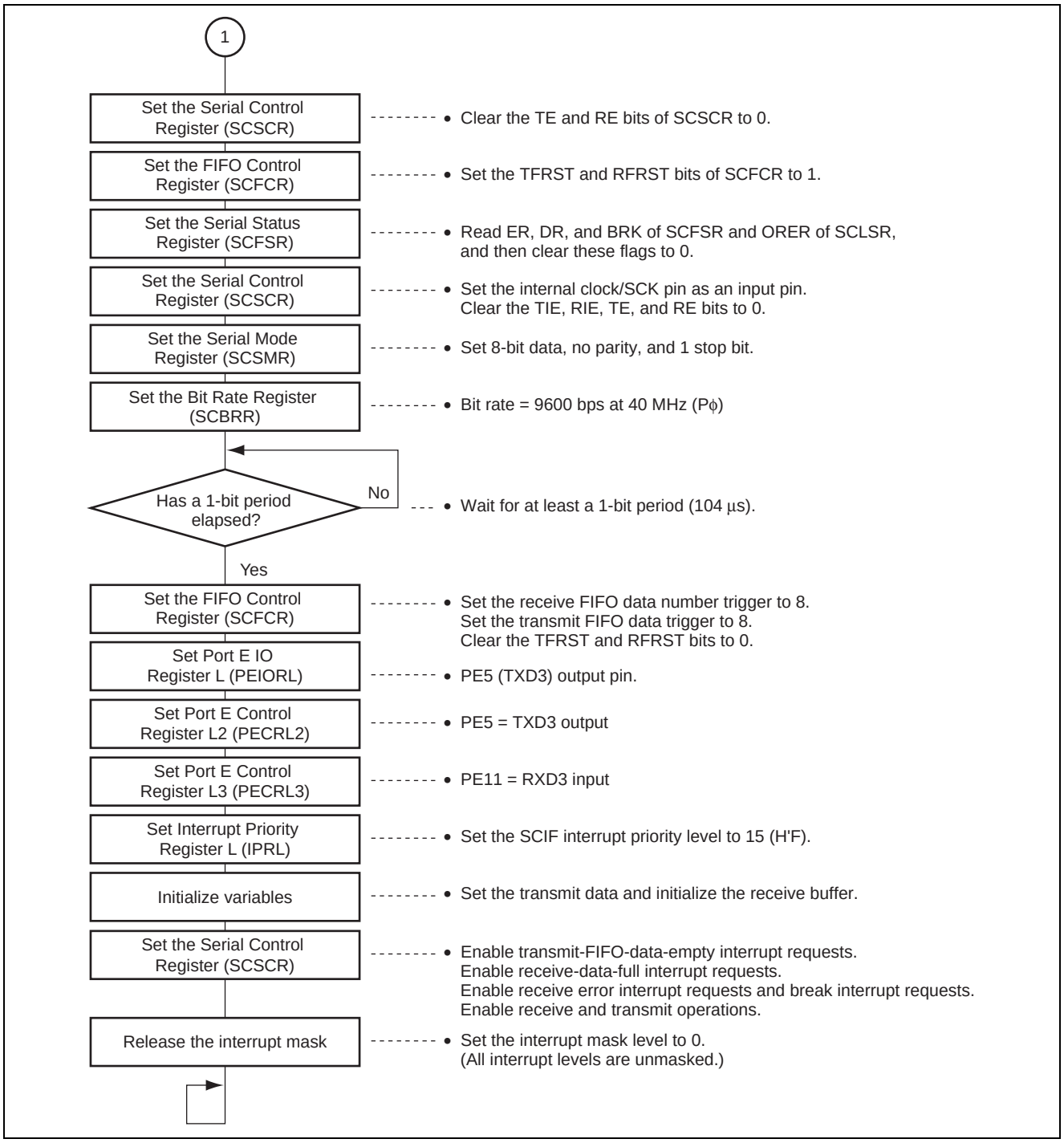
Setting value: H'000F

Bit	Bit Name	Setting Value	Function
15-12	IPR[15:12]	0000	Priority level 0
11-8	IPR[11:8]	0000	Priority level 0
7-4	IPR[7:4]	0000	Priority level 0
3-0	IPR[3:0]	1111	Priority level 15, SCIF interrupts

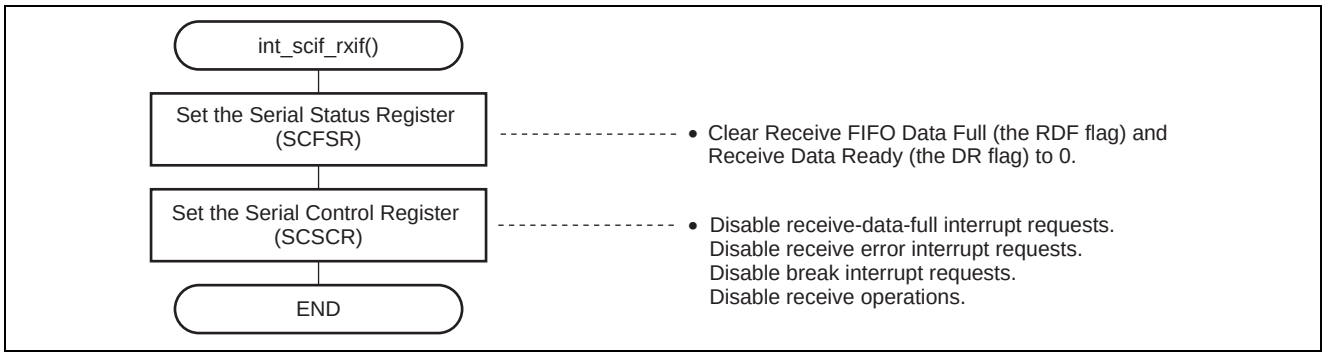
5. Flowcharts

5.1 Main Routine

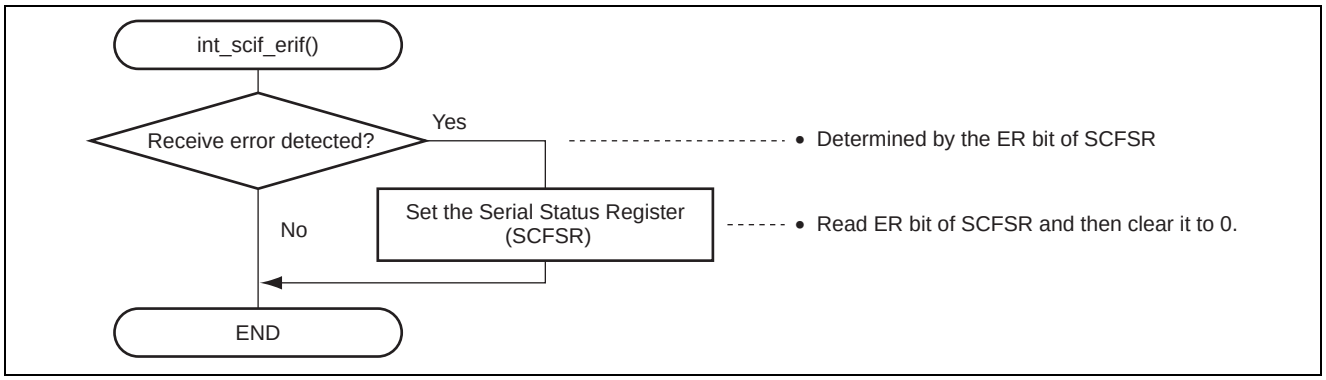



1
Set the Serial Control Register (SCSCR)
• Clear the TE and RE bits of SCSCR to 0.
Set the FIFO Control Register (SCFCR)
• Set the TFRST and RFRST bits of SCFCR to 1.
Set the Serial Status Register (SCFSR)
• Read ER, DR, and BRK of SCFSR and ORER of SCLSR, and then clear these flags to 0.
Set the Serial Control Register (SCSCR)
• Set the internal clock/SCK pin as an input pin. Clear the TIE, RIE, TE, and RE bits to 0.
Set the Serial Mode Register (SCSMR)
• Set 8-bit data, no parity, and 1 stop bit.
Set the Bit Rate Register (SCBRR)
• Bit rate = 9600 bps at 40 MHz (Pϕ)
Has a 1-bit period elapsed?
No
• Wait for at least a 1-bit period (104 µs).
Yes
Set the FIFO Control Register (SCFCR)
• Set the receive FIFO data number trigger to 8. Set the transmit FIFO data trigger to 8. Clear the TFRST and RFRST bits to 0.
Set Port E IO Register L (PEIORL)
• PE5 (TXD3) output pin.
Set Port E Control Register L2 (PECRL2)
• PE5 = TXD3 output
Set Port E Control Register L3 (PECRL3)
• PE11 = RXD3 input
Set Interrupt Priority Register L (IPRL)
• Set the SCIF interrupt priority level to 15 (H'F).
Initialize variables
• Set the transmit data and initialize the receive buffer.
Set the Serial Control Register (SCSCR)
• Enable transmit-FIFO-data-empty interrupt requests. Enable receive-data-full interrupt requests. Enable receive error interrupt requests and break interrupt requests. Enable receive and transmit operations.
Release the interrupt mask
• Set the interrupt mask level to 0. (All interrupt levels are unmasked.)

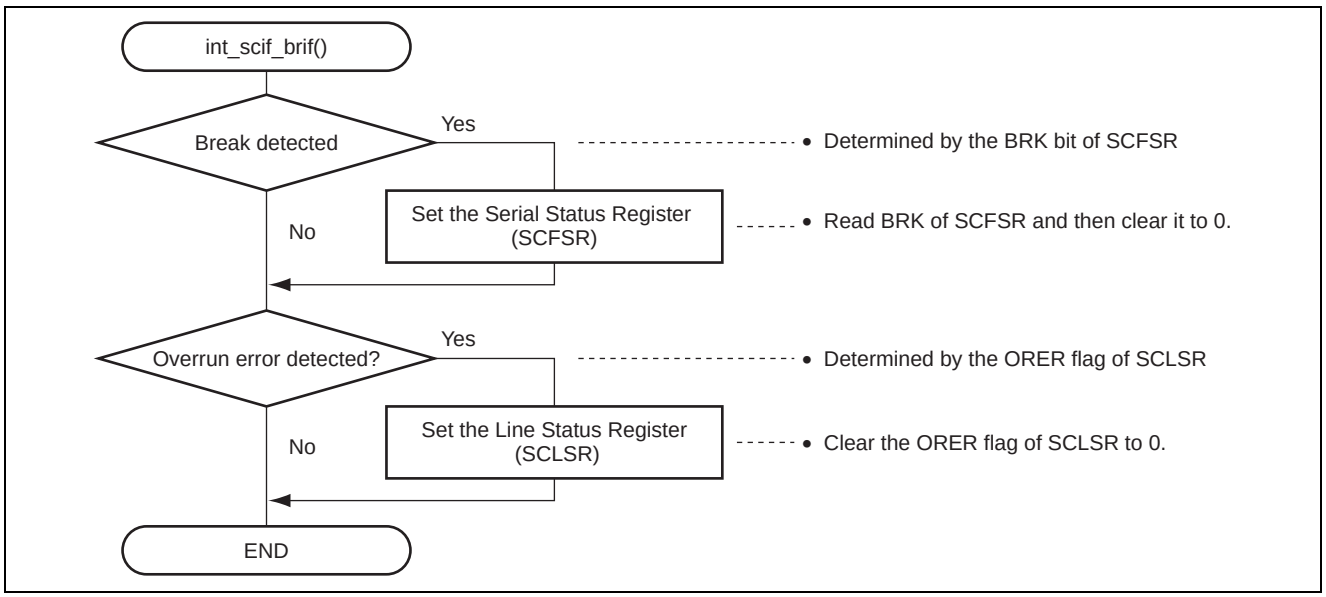
5.2 SCIF Receive-Data-Full Interrupt Routine



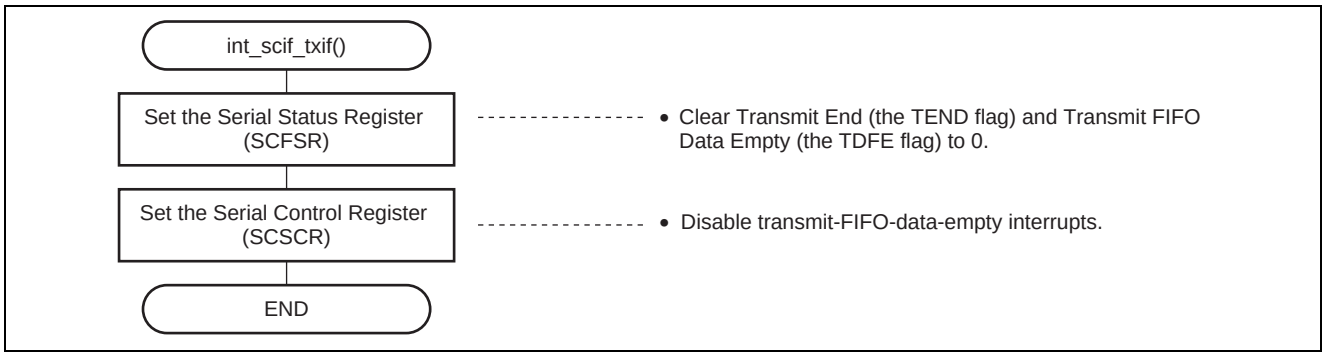
5.3 SCIF Receive Error Interrupt Routine



5.4 SCIF Break Interrupt Routine



5.5 SCIF Transmit-FIFO-Data-Empty Interrupt Routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.14.05	—	First edition issued

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