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SH7211 Group

SCIF Asynchronous Serial Data Reception Function

Introduction

This application note describes the serial data reception function that uses the receive-FIFO-data-full interrupt source of the Serial Communication Interface with FIFO (SCIF).

Target Device

SH7211

Contents

1. Preface

1.1 Specifications

This sample application uses an asynchronous serial transfer function with FIFO to receive 20-byte data. Figure 1 shows the configuration.

- SCIF1 is used.
- The communication format of receive data is a data length of 8 bits, no parity, and 1 stop bit.
- Data is received at a bit rate of 9600 bits/s.
- The receive trigger number is set to 8, and 20-byte data is received using a receive-data-full interrupt source with FIFO.
- Once 20 bytes of data have been received, operation for reception is halted.

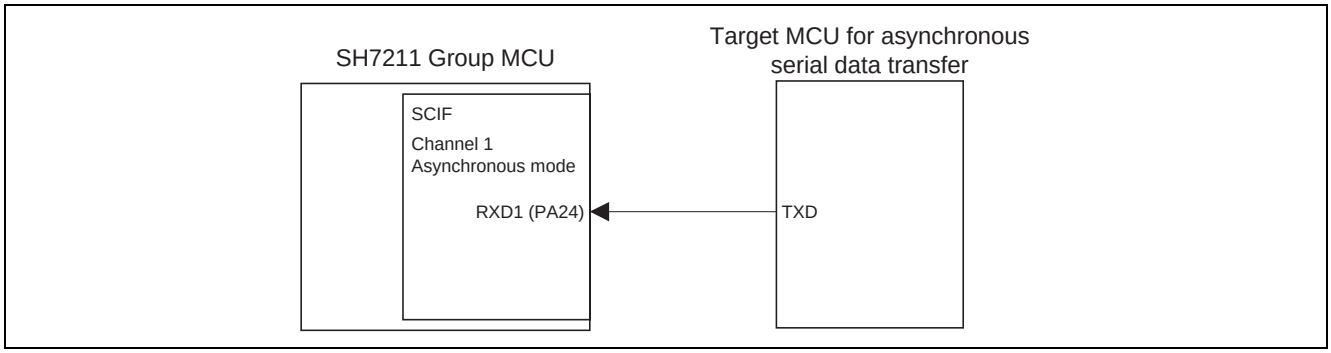


Figure 1 Asynchronous Serial Data Reception with FIFO

1.2 Module Used

- Serial communications interface with FIFO (SCIF1)

1.3 Applicable Conditions

- MCU: SH7211
- Operating frequency:
  - Internal clock: Iϕ = 160 MHz
  - Bus clock: Bϕ = 40 MHz
  - Peripheral clock: Pϕ = 40 MHz
  - MTU2S clock: Mϕ = 80 MHz
  - AD clock: Aϕ = 40 MHz
- MCU operating mode: Single chip mode
- Integrated development environment:
  High-performance Embedded Workshop Ver.4.05.01.001
  (from Renesas Technology Corp.)
- C compiler: SuperH RISC Engine Family C/C++ Compiler Package Ver.9.03 Release00
  from Renesas Technology Corp.
- Compiler options: Default settings of the High-performance Embedded Workshop
  (-cpu=sh2a -include="$(WORKSPDIR)\inc"
  -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto –chgincpath
  -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0
  -struct_alloc=1 -nologo)

2. Overview

This sample application uses the receive-data-full interrupt sources of the Serial Communication Interface with FIFO (SCIF) to receive asynchronous serial data.

2.1 Operational Overview of Module Used

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communications is synchronized in character units. The transmitting and receiving sections of the SCIF are independent, so operations for transmission and reception can proceed simultaneously. Both the transmitter and receiver have a 16-stage FIFO buffered structure so that data can be read or written during transmission or reception, which enables high-speed continuous data transfer.

In asynchronous serial communications, the communication line is normally held in the mark (high) state. The SCIF monitors the line and starts serial communications when the line goes to the space (low) state, indicating a start bit.

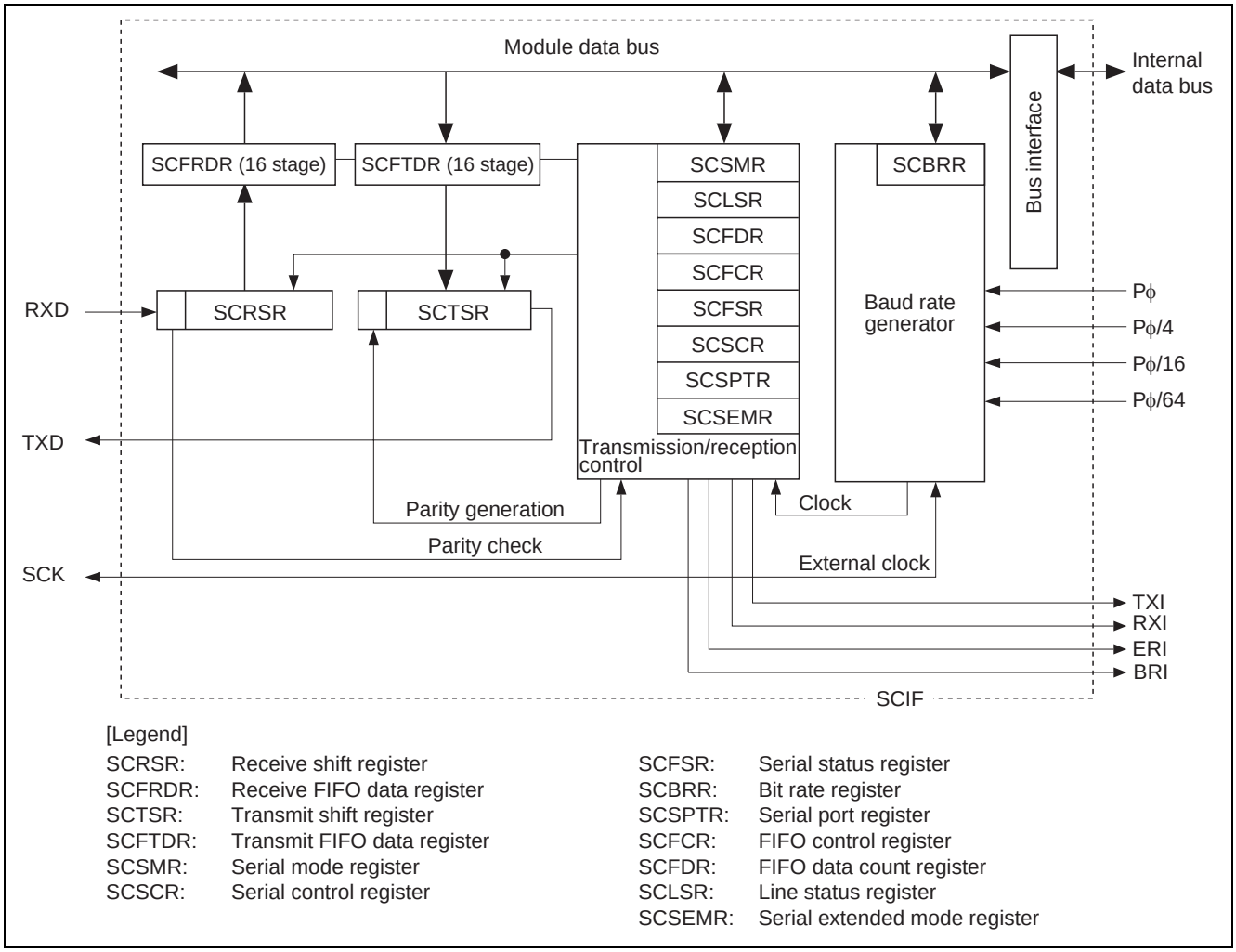
One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in this order.

For details on the SCIF, please refer to the section on Serial Communication Interface with FIFO (SCIF) in the *SH7211 Group Hardware Manual* (REJ09B0344).

Table 1 gives an overview of Serial Communication Interface with FIFO (SCIF). Figure 2 shows a block diagram of the SCIF.

Table 1 Overview of Serial Communication Interface with FIFO (SCIF)

Item	Description
Number of interfaces	3 (0 to 3)
Clock sources	Internal and external clocks are selectable For internal clock: The clock from the baud-rate generator is used to operate. For external clock: Input of a clock signal at 16 times the frequency of the bit rate is required.
Data format	Transfer data length: 7 or 8 bits Selects the parity bit addition Stop bit: 1 or 2 bits
Bit rate	For internal clock: 110 bps to 1.25 Mbps (Pϕ = 40 MHz) For external clock: up to 625 kbps (Pϕ = 40 MHz, external input clock of 10.0000 MHz)
Error detection	Framing, parity and overrun errors
Interrupt requests	Transmit-FIFO-data-empty interrupt (TXI) Receive-FIFO-data-full interrupt (RXI) Receive error interrupt (ERI) Break interrupt (BRI)



[Legend]

SCRSR:	Receive shift register	SCFSR:	Serial status register
SCFRDR:	Receive FIFO data register	SCBRR:	Bit rate register
SCTSR:	Transmit shift register	SCSPTR:	Serial port register
SCFTDR:	Transmit FIFO data register	SCFCR:	FIFO control register
SCSMR:	Serial mode register	SCFDR:	FIFO data count register
SCSCR:	Serial control register	SCLSR:	Line status register
		SCSEMR:	Serial extended mode register

Figure 2 Block Diagram of the SCIF

The Serial Communication Interface with FIFO (SCIF) has the following registers.

- The Receive Shift Register (SCRSR) is used to receive serial data. The SCIF sets serial data input from the RDX pin in SCRSR in the order received starting with the LSB (bit 0) and converts the data to parallel data. When 1 byte of data has been received, the data is transferred automatically to the Receive FIFO Data Register (SCFRDR). The CPU can neither read data from nor write data to SCRSR directly.
- The Receive FIFO Data Register (SCFRDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold received serial data. When 1 byte of data has been received, the received serial data is transferred from the Receive Shift Register (SCRSR) to SCFRDR for storage, completing the receive operation. Receive operations can be performed successively until 16 bytes of data are stored in the register. The CPU can read data from SCFRDR, but it cannot write data to SCFRDR. If a read from the Receive FIFO Data Register is attempted when there is no receive data in the register, the value read is undefined. When the register becomes full with receive data, any subsequently received serial data is lost.
- The Transmit Shift Register (SCTSR) is used to transmit serial data. The SCIF transfers transmit data from the Transmit FIFO Data Register (SCFTDR) to SCTSR, and then performs serial data transmission by sending the data to the TXD pin in order starting with the LSB (bit 0). When 1 byte of data has been transmitted, the next transmit data is transferred automatically from SCFTDR to SCTSR to start transmission. The CPU can neither read data from nor write data to SCTSR directly.
- The Transmit FIFO Data Register (SCFTDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold data that is to be transmitted serially. When the SCIF detects that the Transmit Shift Register (SCTSR) is empty, the SCIF starts serial transmission by transferring the transmit data written in SCFTDR to SCTSR. Serial transmission can be performed as long as data remains in SCFTDR. The CPU can write data to SCFTDR at any time. When SCFTDR becomes full with transmit data (16 bytes), no more data can be written. If an attempt is made to write more data, the data is ignored.
- The Serial Mode Register (SCSMR) is a 16-bit register used to set the SCIF serial communication format and select the clock source of the baud rate generator. The CPU can read data from and write data to SCSMR at any time.
- The Serial Control Register (SCSCR) is a 16-bit register used to enable or disable SCIF transmit and receive operations and interrupt requests and to select the transmit/receive clock source. The CPU can read data from and write data to SCSCR at any time.
- The Serial Status Register (SCFSR) is a 16-bit register. The upper 8 bits indicate the number of receive errors in the data in the Receive FIFO Data Register, and the lower 8 bits consist of status flags indicating the SCIF operating state. The CPU can read data from and write data to SCFSR at any time. However, 1 cannot be written in the ER, TEND, TDFE, BRK, RDF, and DR status flags. Before these flags can be cleared to 0, they must first be read as 1. The FER and PER flags are read-only flags, and data cannot be written to them.
- The Bit Rate Register (SCBRR) is an 8-bit register that sets the serial transmit/receive bit rate together with the baud rate generator clock source selected by the CKS1 and CKS0 bits of the Serial Mode Register (SCSMR). The CPU can read data from and write data to SCBRR at any time. SCBRR is initialized to H'FF by a power-on reset.
- The FIFO Control Register (SCFCR) is a 16-bit register that resets the number of data and sets the trigger data number for the Transmit FIFO Data Register and the Receive FIFO Data Register. The register also contains a loopback test enable bit. The CPU can read data from and write data to SCFCR at any time.
- The FIFO Data Count Register (SCFDR) is a 16-bit register that indicates the number of data bytes stored in the Transmit FIFO Data Register (SCFTDR) and in the Receive FIFO Data Register (SCFRDR). The upper 8 bits indicate the number of transmit data bytes in SCFTDR, and the lower 8 bits indicate the number of receive data bytes in SCFRDR. The CPU can read data from SCFDR at any time.
- The Line Status Register (SCLSR) is a 16-bit register that the CPU can read from and write to at any time. However, 1 cannot be written to the ORER status flag. Before the ORER status flag can be cleared, it must first be read as 1.

2.2 Operation of the Sample Program

Table 2 lists setting conditions of receive operation in asynchronous mode.

Table 2 Setting Conditions of Receive Operation in Asynchronous Mode

Item	Description
Channels in use	SCIF1
Used pin	RXD1 (PA24): Receive data input pin
Transfer mode	Asynchronous mode
Transfer rate	9600 bps
Receive data	20 bytes
Data length	8 bits (LSB first)
Parity bit	None
Stop bit	1 bit
Receive trigger	8
Interrupts	Receive-FIFO-data-full interrupt (RXI) Receive error interrupt (ERI) Break interrupt (BRI)

Figure 3 shows operations for reception. The reference program handles storage of twenty bytes of received data in the reception buffer. Reception operations end once the 20 bytes have been received.

Serial data received via the RXD1 pin are converted to parallel data by the receive shift register (SCRSR) and transferred one byte at a time to the receive FIFO data register (SCFRDR). The receive data full interrupt is generated when the SCFRDR holds eight bytes of data. Processing for this interrupt transfers received data from the SCFRDR to the reception buffer.

Furthermore, even if the SCFRDR holds fewer than eight bytes of received data, the receive data ready interrupt is generated after an interval of 15 etu has elapsed following the stop bit for the final byte. At this time the remaining received data in the SCFRDR are stored in the reception buffer.

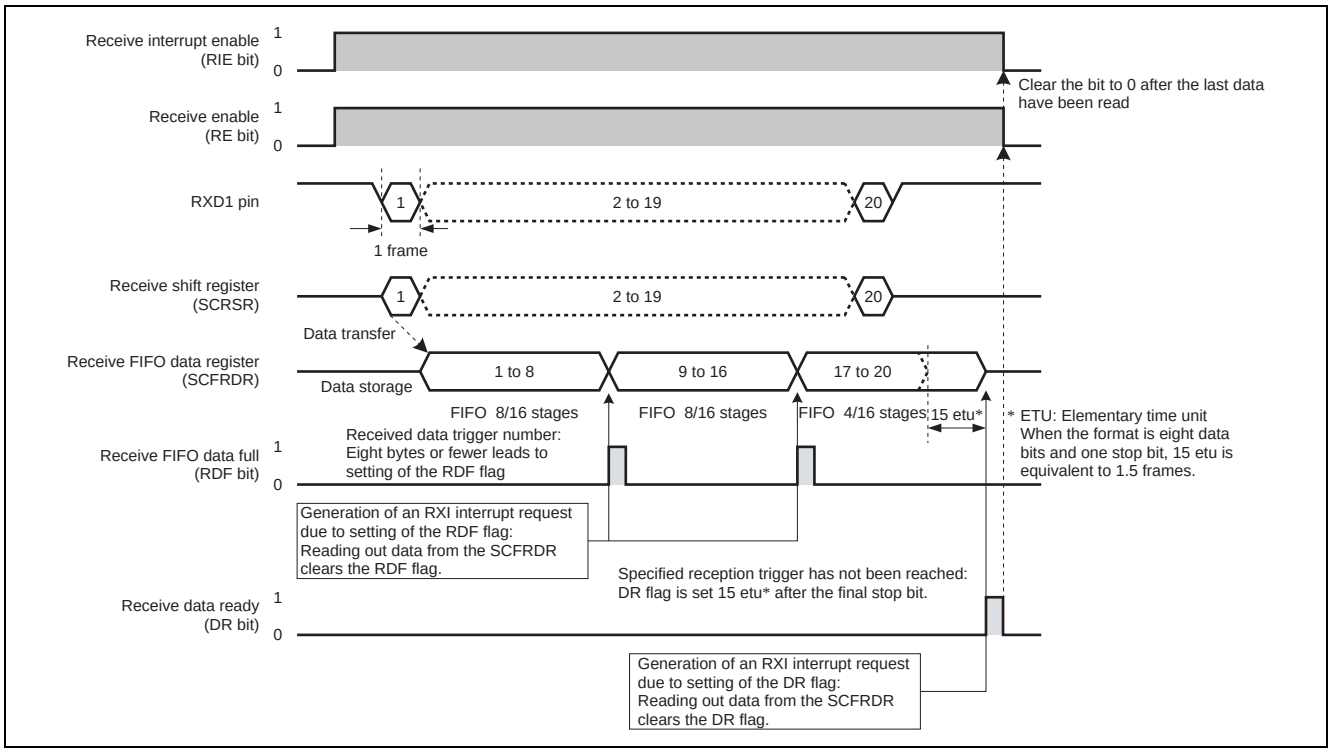


Figure 3 Receive Operation

2.3 Configuration of the Sample Program

2.3.1 Description of Functions

Table 3 lists functions used in this sample program.

Table 3 Functions Used

Function Name	Label	Description
Main	main ()	• Initializes other modules • Initialized Serial Communication Interface with FIFO (SCIF) • SCIF receiver enabled
Standby setting	stbcr_init ()	• Makes setting to release SCIF from standby
Initialization of PFC	pfc_init ()	• Initialized Pin Function Controller (PFC) • Pin function of the SCIF is set.
Initialization of SCIF	scif_init()	• Initialized SCIF
SCIF receive-FIFO-data-full interrupt	Int_scif_rxif ()	• Handles SCIF receive-FIFO-data-full interrupts.
SCIF receive error interrupt	Int_scif_erif ()	• Handles SCIF receive error interrupts.
SCIF break interrupt	Int_scif_brif ()	• Handles SCIF break interrupts.

2.3.2 Variable Usage

Table 4 gives a list of variables used in the sample program.

Table 4 Variable Usage

Label Name	Description	Name of Employing Module
unsigned char Rcv_Data[20]	Receive buffer	Int_scif_rxif ()
unsigned long Rcv_Count	Number of receive data items	
unsigned long Rxif_Count	Receive-FIFO-data-full interrupt count	
unsigned long Erif_Count	Receive error interrupt count	Int_scif_erif ()
unsigned long Brif_Count	Break interrupt count	Int_scif_brif ()

2.4 Procedure for Setting Module Used

The following subsections describe the flow of processing by the sample program.

2.4.1 main Function

Figure 4 shows the flow of processing by the main function.

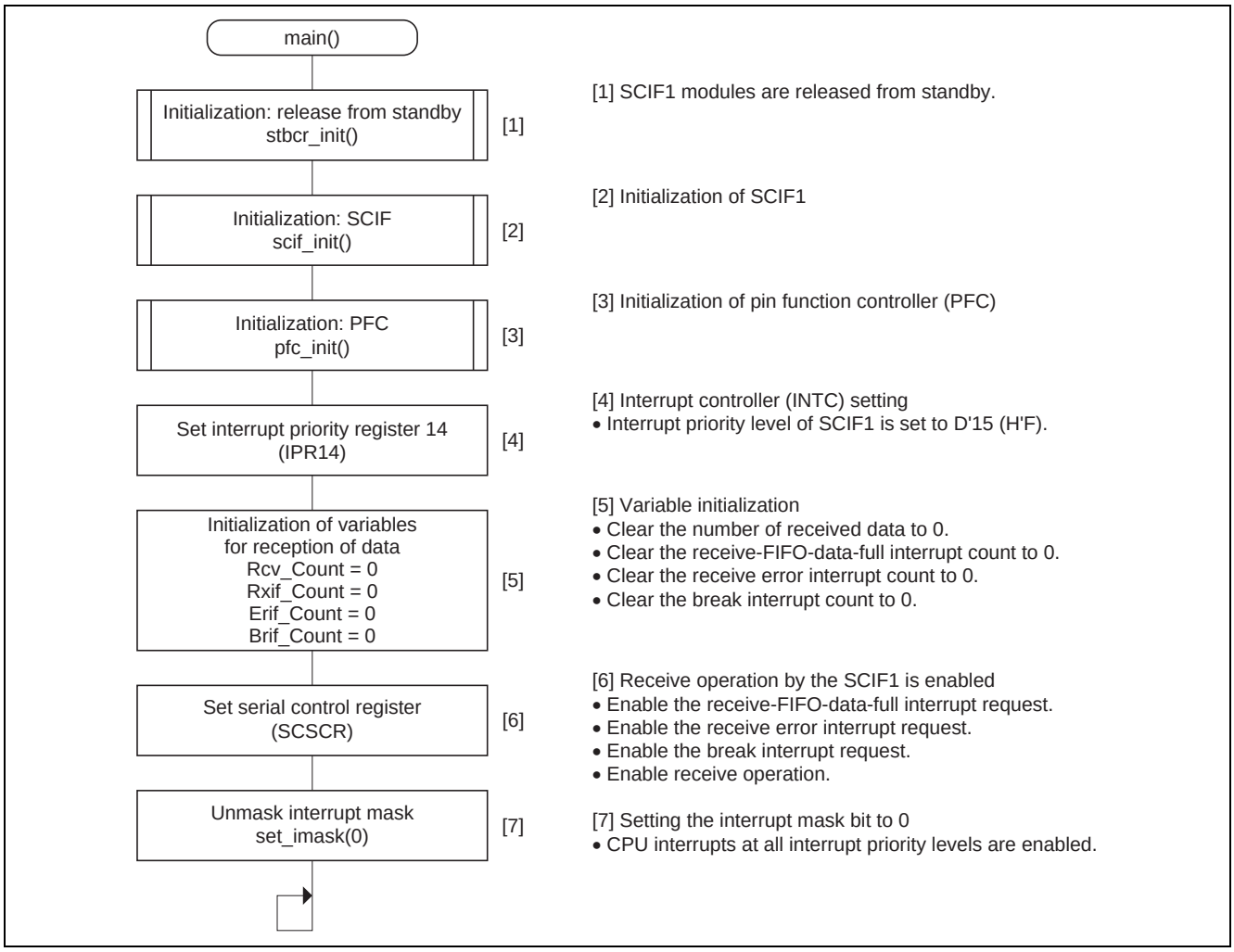


Figure 4 Flow of Processing by the main Function

2.4.2 Initialization of the Standby

Figure 5 shows the flow for initialization of the standby.

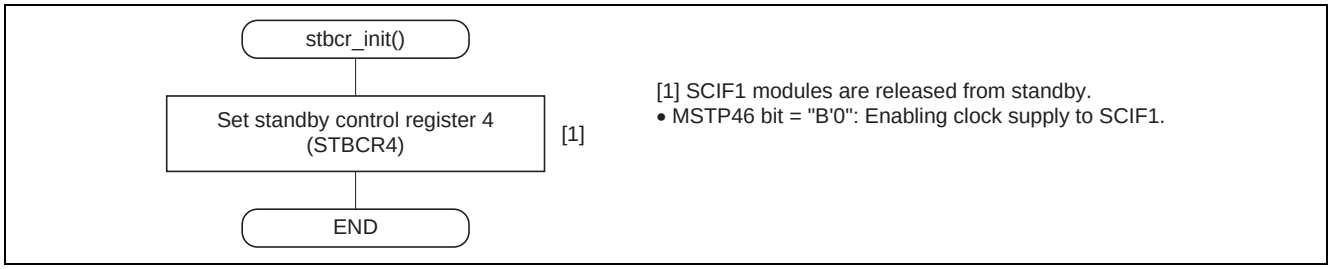


Figure 5 Flow for Initialization of the Standby

2.4.3 Initialization of Pin Function Controller (PFC)

Figure 6 shows the flow for initialization of the PFC.

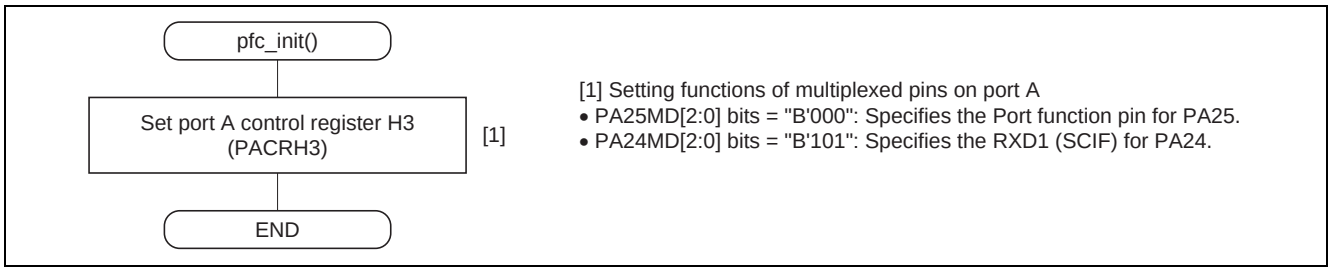


Figure 6 Flow for Initialization of the PFC

2.4.4 Initialization of Serial Communication Interface with FIFO (SCIF)

Figure 7 shows the flow for initialization of the SCIF.

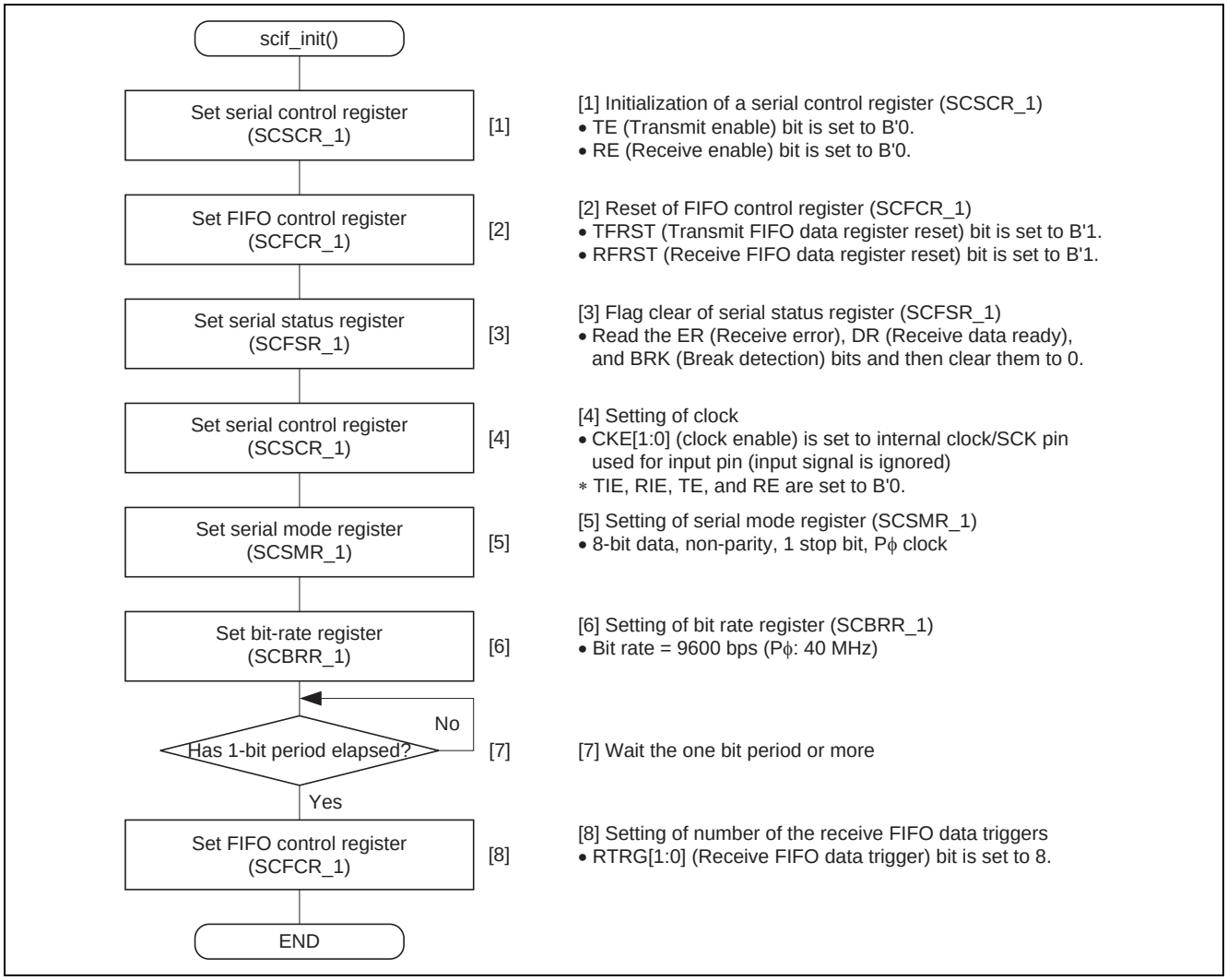


Figure 7 Flow for Initialization of the SCIF

2.4.5 SCIF Receive-FIFO-Data-Full Interrupt Function

Figure 8 shows the flow for SCIF receive-FIFO-data-full interrupt function.

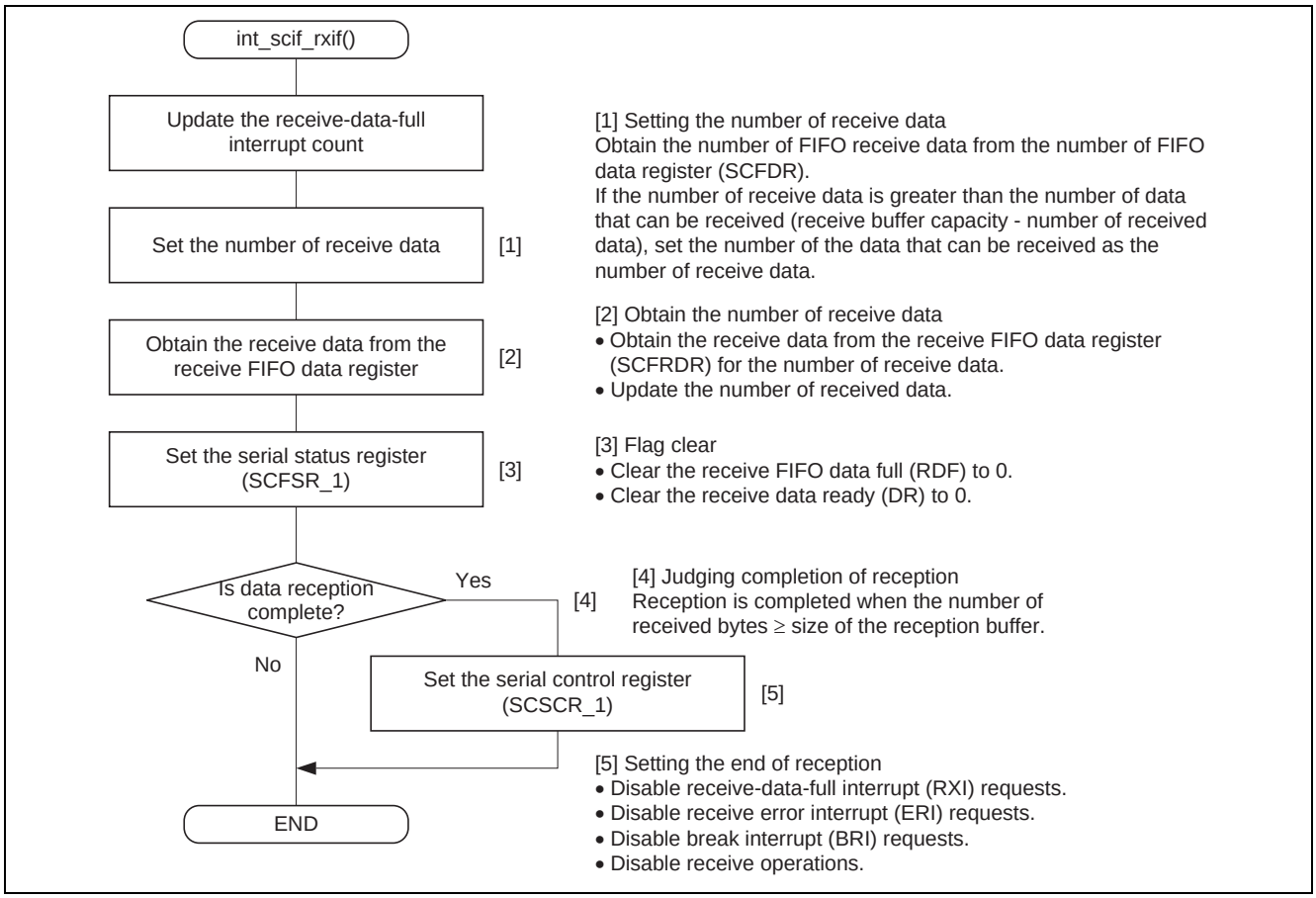


Figure 8 Flow for SCIF Receive-FIFO-Data-Full Interrupt Function

2.4.6 SCIF Receive Error Interrupt Function

Figure 9 shows the flow for SCIF receive error interrupt function.

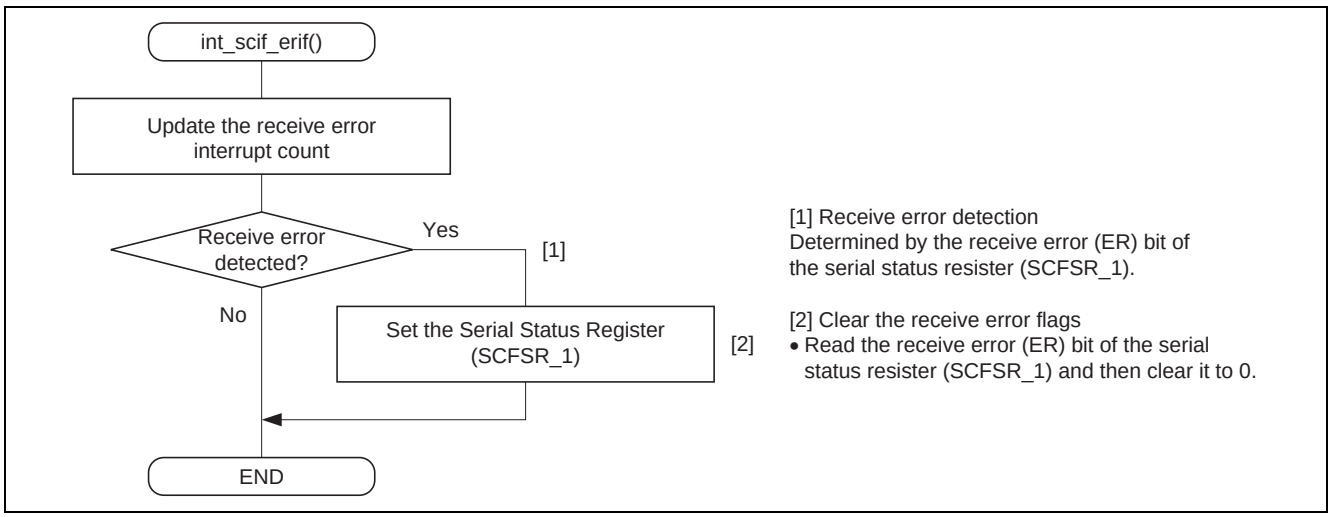


Figure 9 Flow for SCIF Receive Error Interrupt Function

2.4.7 SCIF Break Interrupt Function

Figure 10 shows the flow for SCIF break interrupt function.

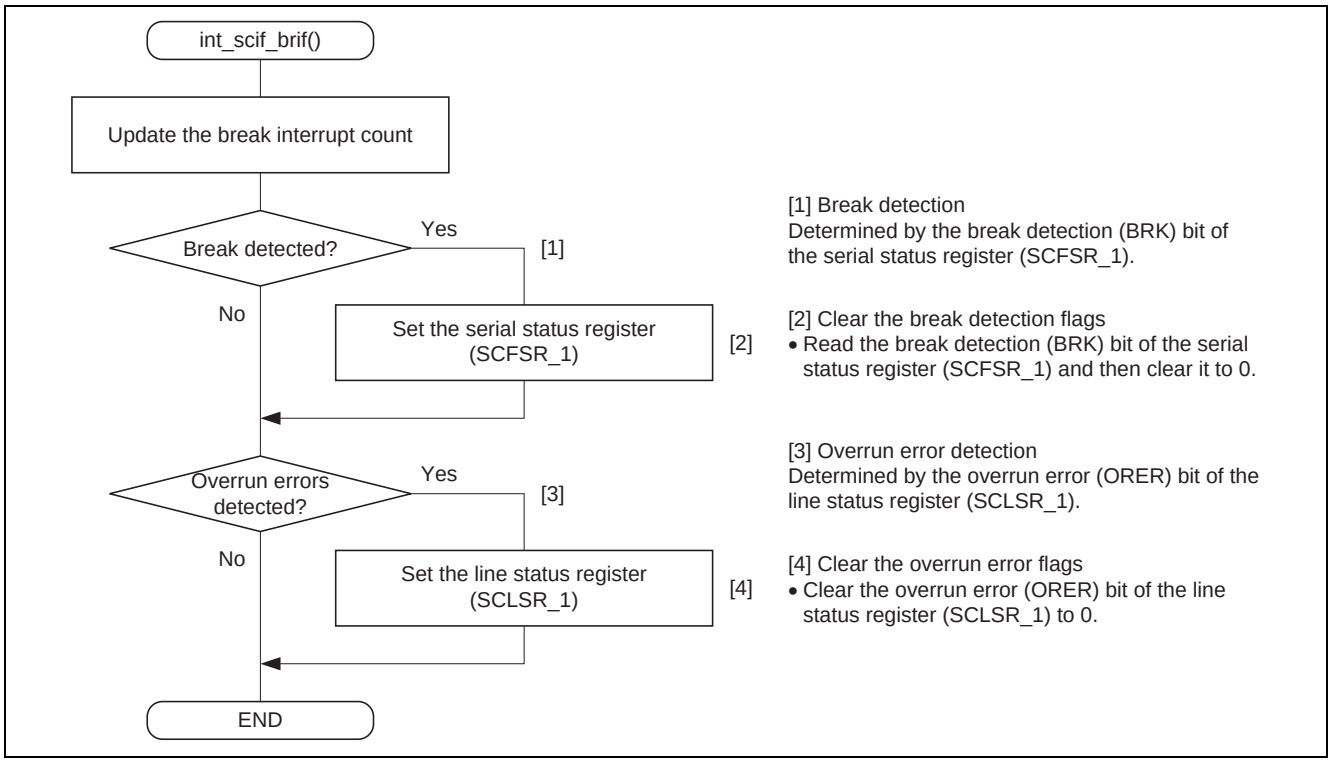


Figure 10 Flow for SCIF Break Interrupt Function

2.5 Settings of Registers in the Sample Program

The following describes the settings of registers used in the sample program.

2.5.1 Clock Pulse Generator (CPG)

Table 5 gives a list of settings for registers for the clock pulse generator (CPG).

Table 5 Clock Pulse Generator (CPG)

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE0010	H'1303	Specifies division ratios for clock output setting and operating frequency • CKOEN = "B'1": Fix the CK pin low • STC[1:0] = "B'11": ×2, PLL circuit 1 • IFC[2:0] = "B'000": ×1, internal clock (Iϕ) • RNGS = "B'0": High frequency mode • PFC[2:0] = "B'011": ×1/4, peripheral clock (Pϕ)

2.5.2 Power-Down Modes

Table 6 gives register settings related to low-power modes.

Table 6 Power-Down Modes

Register Name	Address	Setting	Description
Standby control register 4 (STBCR4)	H'FFFE040C	H'B6	Settings for the operation of various modules • MSTP47 = "B'1": Clock supply to SCIF0 halted. • MSTP46 = "B'0": SCIF1 runs. • MSTP45 = "B'1": Clock supply to SCIF2 halted. • MSTP44 = "B'1": Clock supply to SCIF3 halted. • MSTP42 = "B'1": Clock supply to CMT halted. • MSTP41 = "B'1": Clock supply to WAVEIF halted.

2.5.3 Serial Communication Interface with FIFO (SCIF)

Table 7 gives a list of settings for registers of Serial Communication Interface with FIFO (SCIF).

Table 7 Serial Communication Interface with FIFO (SCIF)

Register Name	Address	Setting	Description
Serial mode register_1 (SCSMR_1)	H'FFFE8800	H'0000	Sets SCIF_1 mode • C/A = "B'0": Asynchronous mode • CHR = "B'0": 8-bit data • PE = "B'0": Disables adding and checking of parity bits • STOP = "B'0": 1 stop bit • CKS[1:0] = "B'00": Pϕ clock
Bit rate register_1 (SCBRR_1)	H'FFFE8804	H'81	Bit rate: 9600 bps
Serial control register_1 (SCSCR_1)	H'FFFE8808	H'0050	Initialization • RIE = "B'1": Enables receive-FIFO-data-full interrupt (RXI), receive-error-interrupt (ERI), break interrupt (BRI) requests • TE = "B'0": Disables transmission of data • RE = "B'1": Enables reception of data • REIE = "B'0": Disables receive-error-interrupt (ERI), break interrupt (BRI) requests • CKE[1:0] = "B'00": Internal clock, SCK pin is used as an input pin (input signal is ignored)
Serial status register_1 (SCFSR_1)	H'FFFE8810	H'0060	• PER[3:0] = Number of parity errors • FER[3:0] = Number of framing errors • ER = "B'0": Reception is in progress or has been completed normally. • BRK = "B'0": No break signal • FER = "B'0": No framing error • PER = "B'0": No parity error • RDF = "B'1": The number of SCFRDR receive data items is greater than the specified receive trigger number. • DR = "B'0": Reception is in progress, or there is no receive data left in SCFRDR after normal reception.
FIFO control register_1 (SCFCR_1)	H'FFFE8818	H'0080	• RTRG[1:0] = "B'10": Receive FIFO data trigger number = 8 • TFRST = "B'0": Disables resetting of the transmit FIFO data register. • RFRST = "B'0": Disables resetting of the receive FIFO data register. • LOOP = "B'0": Disables loopback test

2.5.4 Interrupt Controller (INTC)

Table 8 gives a list of settings for registers of Interrupt Controller (INTC).

Table 8 Interrupt Controller (INTC)

Register Name	Address	Setting	Description
Interrupt priority register 14 (IPR14)	H'FFFE0C10	H'0F00	Selects interrupt priority (levels 0 to 15). • Bit 15-12 = "B'0000": SCIF_0 interrupt level = 0 • Bit 11-8 = "B'1111": SCIF_1 interrupt level = 15 • Bit 7-4 = "B'0000": SCIF_2 interrupt level = 0 • Bit 3-0 = "B'0000": SCIF_3 interrupt level = 0

2.5.5 Pin Function Controller (PFC)

Table 9 gives a list of settings for registers of Pin Function Controller (PFC).

Table 9 Pin Function Controller (PFC)

Register Name	Address	Setting	Description
Port A control register H3 (PACRH3)	H'FFFE380A	H'0005	Specifies functions of multiplexed pins on port A. • PA25MD[2:0] = "B'000": Specifies the PA25 I/O (port) for PA25. • PA24MD[2:0] = "B'101": Specifies the RXD1 input (SCIF) for PA24.

3. Documents for Reference

- Hardware Manual
  SH7211 Group Hardware Manual (REJ09B0344)
  (The most up-to-date version of this document is available on the Renesas Technology Website.)
- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
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