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SH7080 Group

SCIF Asynchronous Serial Data Reception Function

Introduction

This application note describes the serial data reception function that uses the receive-data-full interrupt source of the SCIF (Serial Communication Interface with FIFO). You can use this application note as reference information for designing user software.

Target Device

SH7085 (R5F7085)

Contents

1. Specifications

This sample application uses an asynchronous serial transfer function with FIFO to receive 20-byte data. Figure 1 shows the operations in this sample task.

Applicable Conditions:

- Microcomputer: SH7085 (R5F7085)
- Operating frequency: Internal clock 80 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
  MTU2 clock 40 MHz
  MTU2S clock 80 MHz
- C compiler: V.8.00.04 manufactured by Renesas Technology Corp.

- The communication format of receive data is a data length of 8 bits, no parity, and 1 stop bit.
- Data is received at a bit rate of 9600 bits/s.
- The receive trigger number is set to 8, and 20-byte data is received using a receive-data-full interrupt source.

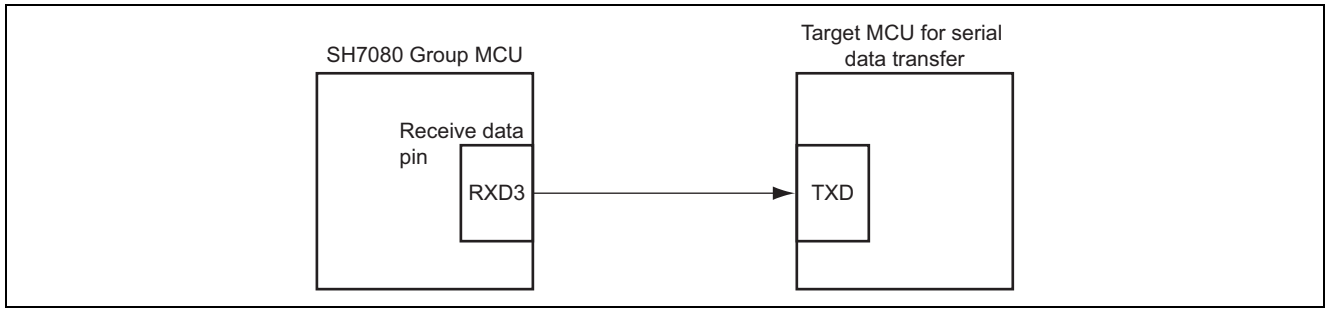


Figure 1 Asynchronous Serial Data Reception with FIFO

2. Operational Overview of Functions Used

This sample application uses the receive-data-full interrupt sources of the SCIF (Serial Communication Interface with FIFO) to receive asynchronous serial data. A block diagram of the SCIF is illustrated in figure 2.

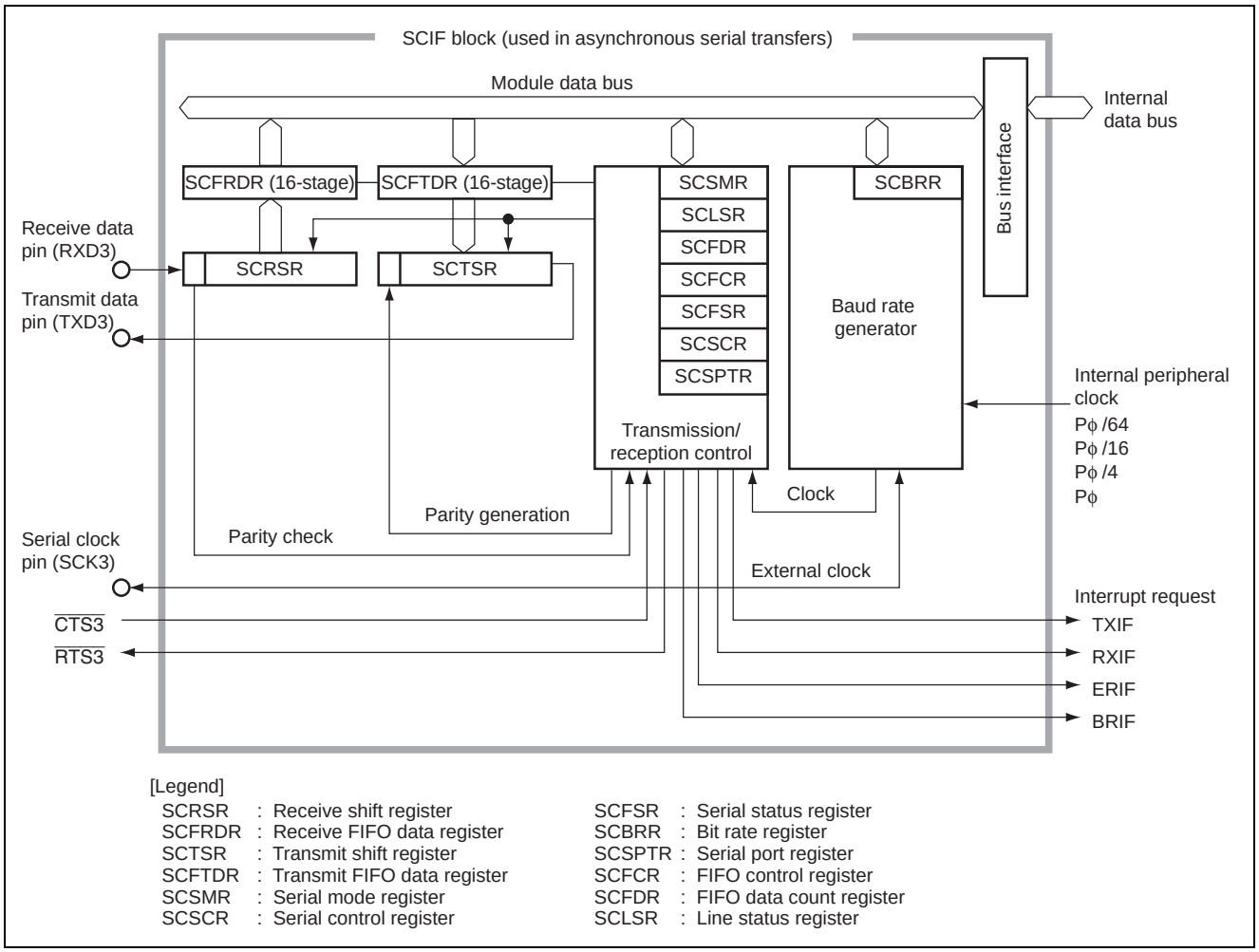


Figure 2 Block Diagram of SCIF (Serial Communication Interface with FIFO)

- Separate 16-stage FIFO registers each for transmission and reception enable efficient, high-speed serial communication.
- Serial data communication is performed by start-stop in character units. The SCIF can communicate with a universal asynchronous receiver/transmitter (UART), an asynchronous communication interface adapter (ACIA), or any other communications chip that employs a standard asynchronous serial system.
- The Receive Shift Register (SCRSR) is used to receive serial data. The SCIF sets serial data input from the RDX pin in SCRSR in the order received starting with the LSB (bit 0) and converts the data to parallel data. When 1 byte of data has been received, the data is transferred automatically to the Receive FIFO Data Register (SCFRDR). The CPU can neither read data from nor write data to SCRSR directly.

- The Receive FIFO Data Register (SCFRDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold received serial data. When 1 byte of data has been received, the received serial data is transferred from the Receive Shift Register (SCRSR) to SCFRDR for storage, completing the receive operation. Receive operations can be performed successively until 16 bytes of data are stored in the register. The CPU can read data from SCFRDR, but it cannot write data to SCFRDR. If a read from the Receive FIFO Data Register is attempted when there is no receive data in the register, the value read is undefined. When the register becomes full with receive data, any subsequently received serial data is lost.
- The Transmit Shift Register (SCTSR) is used to transmit serial data. The SCIF transfers transmit data from the Transmit FIFO Data Register (SCFTDR) to SCTSR, and then performs serial data transmission by sending the data to the TXD pin in order starting with the LSB (bit 0). When 1 byte of data has been transmitted, the next transmit data is transferred automatically from SCFTDR to SCTSR to start transmission. The CPU can neither read data from nor write data to SCTSR directly.
- The Transmit FIFO Data Register (SCFTDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold data that is to be transmitted serially. When the SCIF detects that the Transmit Shift Register (SCTSR) is empty, the SCIF starts serial transmission by transferring the transmit data written in SCFTDR to SCTSR. Serial transmission can be performed as long as data remains in SCFTDR. The CPU can write data to SCFTDR at any time. When SCFTDR becomes full with transmit data (16 bytes), no more data can be written. If an attempt is made to write more data, the data is ignored.
- The Serial Mode Register (SCSMR) is a 16-bit register used to set the SCIF serial communication format and select the clock source of the baud rate generator. The CPU can read data from and write data to SCSMR at any time.
- The Serial Control Register (SCSCR) is a 16-bit register used to enable or disable SCIF transmit and receive operations and interrupt requests and to select the transmit/receive clock source. The CPU can read data from and write data to SCSCR at any time.
- The Serial Status Register (SCFSR) is a 16-bit register. The upper 8 bits indicate the number of receive errors in the data in the Receive FIFO Data Register, and the lower 8 bits consist of status flags indicating the SCIF operating state. The CPU can read data from and write data to SCFSR at any time. However, 1 cannot be written in the ER, TEND, TDFE, BRK, RDF, and DR status flags. Before these flags can be cleared to 0, they must first be read as 1. The FER and PER flags are read-only flags, and data cannot be written to them.
- The Bit Rate Register (SCBRR) is an 8-bit register that sets the serial transmit/receive bit rate together with the baud rate generator clock source selected by the CKS1 and CKS0 bits of the Serial Mode Register (SCSMR). The CPU can read data from and write data to SCBRR at any time. SCBRR is initialized to H'FF by a power-on reset.
- The FIFO Control Register (SCFCR) is a 16-bit register that resets the number of data and sets the trigger data number for the Transmit FIFO Data Register and the Receive FIFO Data Register. The register also contains a loopback test enable bit. The CPU can read data from and write data to SCFCR at any time.
- The FIFO Data Count Register (SCFDR) is a 16-bit register that indicates the number of data bytes stored in the Transmit FIFO Data Register (SCFTDR) and in the Receive FIFO Data Register (SCFRDR). The upper 8 bits indicate the number of transmit data bytes in SCFTDR, and the lower 8 bits indicate the number of receive data bytes in SCFRDR. The CPU can read data from SCFDR at any time.
- The Line Status Register (SCLSR) is a 16-bit register that the CPU can read from and write to at any time. However, 1 cannot be written to the ORER status flag. Before the ORER status flag can be cleared, it must first be read as 1.

3. Principles of Operation

The principles of operation for this sample task are illustrated in figure 3. The software and hardware processing is described in table 1.

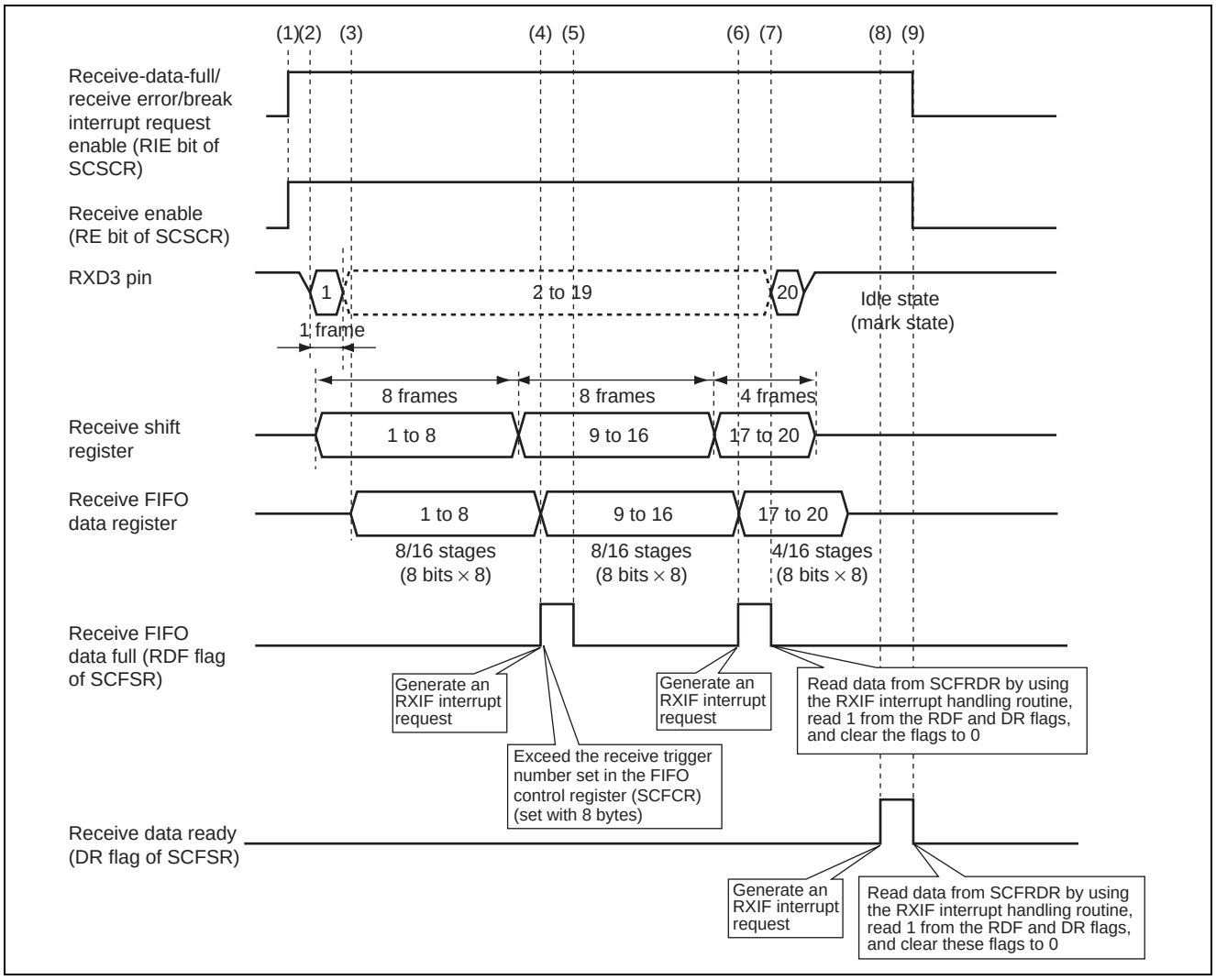


Figure 3 Principles of Operation

Table 1 Description of Software and Hardware Processing

Step	Software Processing	Hardware Processing
(1)	• Enable receive-data-full interrupt requests, receive error interrupt requests, and break interrupt requests (the RIE bit of SCSCR), and enable receive operation (the RE bit of SCSCR).	—
(2)	—	• Detect the start bit (0) and start receive operation.
(3)	—	• Transfer data one frame a time from the Receive Shift Register to the Receive FIFO Data Register.
(4)	• Read the appropriate number of receive data bytes from the Receive FIFO Data Register into the receive buffer.	• Generate a receive-data-full interrupt.
(5)	• Read 1 from Receive FIFO Data Full (the RDF bit of SCFSR) and Receive Data Ready (the DR bit of SCFSR) and then clear these bits to 0.	—
(6)	• Read the appropriate number of receive data bytes from the Receive FIFO Data Register into the receive buffer.	• Generate a receive-data-full interrupt.
(7)	• Read 1 from Receive FIFO Data Full (the RDF bit of SCFSR) and Receive Data Ready (the DR bit of SCFSR) and then clear these bits to 0.	—
(8)	• Read the appropriate number of receive data bytes from the Receive FIFO Data Register into the receive buffer.	• The Receive Data Ready (the DR bit of SCFSR) is set to 1, generating a receive-data-full interrupt.
(9)	• Read 1 from Receive FIFO Data Full (the RDF bit of SCFSR) and Receive Data Ready (the DR bit of SCFSR) and then clear these bits to 0. • When the data has been received, read 1 from Receive-Data-Full Interrupt Request/Receive Error Interrupt Request/Break Interrupt Request Enable (the RIE bit of SCFSR) and from Receive Enable (the RE bit of SCFSR), and then clear these bits to 0.	—

4. Description of Software

4.1 Description of Modules

The modules of this sample task are described in table 2.

Table 2 Modules

Module Name	Label Name	Description
Main routine	main()	Makes initial settings for the SCIF and enables receive operations.
SCIF receive-data-full interrupt routine	int_scif_rxif ()	Handles SCIF receive-data-full interrupts.
SCIF receive error interrupt routine	int_scif_erif ()	Handles SCIF receive error interrupts.
SCIF break interrupt routine	int_scif_brif ()	Handles SCIF break interrupts.

4.2 Variables Used

The variables used in this sample task are described in table 3.

Table 3 Variables

Variable, Label Name	Description	Used In
unsigned char Rcv_Data[20]	Receive buffer	int_scif_rxif ()
unsigned long Rcv_Count	Number of receive data items	int_scif_rxif ()
unsigned long Rxif_Count	Receive-data-full interrupt count	int_scif_rxif ()
unsigned long Erif_Count	Receive error interrupt count	int_scif_erif ()
unsigned long Brif_Count	Break interrupt count	int_scif_brif ()

4.3 Setting the Registers

This section describes the setting of registers used in this sample task. Note that the settings shown below are used in the sample task and are not initial values.

4.3.1 Register for Setting the Clock Pulse Generator (CPG)

(1) Frequency Control Register (FRQCR)

The Frequency Control Register specifies the division ratio of the operating frequency.

Setting: H'0241

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	IFC[2:0]	000	Division ratio of the internal clock (Iϕ) frequency 000: × 1, 80 MHz when the input clock is 10 MHz
11-9	BFC[2:0]	001	Division ratio of the bus clock (Bϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz
8-6	PFC[2:0]	001	Division ratio of the peripheral clock (Pϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz
5-3	MIFC[2:0]	000	Division ratio of the MTU2S clock (MIϕ) frequency 000: × 1, 80 MHz when the input clock is 10 MHz
2-0	MPFC[2:0]	001	Division ratio of the MTU2 clock (MPϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz

4.3.2 Register for Setting the Power-Down Mode

(1) Standby Control Register 3 (STBCR3)

This register controls the operation of each module in the power-down mode.

Setting: H'BF

Bit	Bit Name	Setting Value	Function
7	MSTP15	1	1: Stops clock supply to I^2C2 module.
6	MSTP14	0	0: SCIF in operation.
5	MSTP13	1	1: Stops clock supply to SCI_2 module.
4	MSTP12	1	1: Stops clock supply to SCI_1 module.
3	MSTP11	1	1: Stops clock supply to SCI_0 module.
2	MSTP10	1	1: Stops clock supply to the SSU module.
1-0	—	11	Reserved

4.3.3 Register for Setting the Serial Communication Interface with FIFO (SCIF)

(1) Serial Control Register (SCSCR)

This register enables and disables transmit and receive operations and interrupt requests, and selects the clock source for transmit and receive operations.

Setting: H'0050

Bit	Bit Name	Setting Value	Function
15-8	—	0000 0000	Reserved
7	TIE	0	0: Disables transmit-FIFO-data-empty interrupt (TXIF) requests.
6	RIE	1	0: Disables receive-data-full interrupt (RXIF) request, receive error interrupt (ERIF) requests, and break interrupt (BRIF) requests. 1: Enables receive-data-full interrupt (RXIF) requests, receive error interrupt (ERIF) requests, and break interrupt (BRIF) requests.
5	TE	0	0: Disables transmit operations.
4	RE	1	0: Disables receive operations. 1: Enables receive operations.
3	REIE	0	0: Disables receive error interrupt (ERIF) requests and break interrupt (BRIF) requests.
2	—	0	Reserved
1-0	CKE[1:0]	00	00: The internal clock/SCK pin functions as an input pin (the input signal is ignored).

(2) FIFO Control Register (SCFCR)

This register resets the data count and sets the trigger data number for the Transmit FIFO Data Register and the Receive FIFO Data Register.

Setting: H'0080

Bit	Bit Name	Setting Value	Function
15-11	—	00000	Reserved
10-8	RSTRG[2:0]	000	000: $\overline{\text{RTS}}$ output active trigger. Invalid because modem signals are not allowed.
7-6	RTRG[1:0]	10	10: Receive FIFO data trigger number = 8
5-4	TTRG[1:0]	00	00: Transmit FIFO data trigger number = 8
3	MCE	0	0: Disables modem signals.
2	TFRST	0	0: Disables resetting of the Transmit FIFO Data Register. 1: Enables resetting of the Transmit FIFO Data Register.
1	RFRST	0	0: Disables resetting of the Receive FIFO Data Register. 1: Enables resetting of the Receive FIFO Data Register.
0	LOOP	0	0: Disables loopback test.

(3) Serial Status Register (SCFSR)

The upper 8 bits of this register indicate the number of receive errors, and the lower 8 bits indicate the SCIF operating state.

Setting: H'0000

Bit	Bit Name	Setting Value	Function
15-12	PER[3:0]	0000	Number of parity errors
11-8	FER[3:0]	0000	Number of framing errors
7	ER	0	0: Reception is in progress or has been completed normally.
6	TEND	0	0: Transmission is in progress. 1: Transmission has ended.
5	TDFE	0	0: The number of transmit data items written in SCFTDR is greater than the specified transmit trigger number. 1: The number of transmit data items written in SCFTDR is smaller than the specified transmit trigger number.
4	BRK	0	0: No break signal
3	FER	0	0: No framing error
2	PER	0	0: No parity error
1	RDF	0	0: The number of SCFRDR receive data items is smaller than the specified receive trigger number.
0	DR	0	0: Reception is in progress, or there is no receive data left in SCFRDR after normal reception.

(4) Serial Mode Register (SCSMR)

This register sets the communication format and selects the clock source of the baud rate generator.

Setting: H'0000

Bit	Bit Name	Setting Value	Function
15-8	—	0000 0000	Reserved
7	C/$\overline{A}$	0	0: Asynchronous mode
6	CHR	0	0: 8-bit data
5	PE	0	0: Disables parity bit addition and checking.
4	O/$\overline{E}$	0	0: Ignores the O/$\overline{E}$ bit specification because PE = 0.
3	STOP	0	0: 1 stop bit
2	—	0	Reserved
1-0	CKS[1:0]	00	00: Pϕ clock

(5) Bit Rate Register (SCBRR)

This register sets the bit rate for serial transmission and reception.

Setting: H'81

Bit	Bit Name	Setting Value	Function
7-0	—	1000 0001	Bit rate for serial transmission/reception

4.3.4 Register for Setting the Pin Function Controller (PFC)

(1) Port E Control Register L3 (PECRL3)

This register selects the functions of multiplexed pins in port E.

Setting: H'3000

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PE11MD[2:0]	011	011: RXD3 input (SCIF)
11	—	0	Reserved
10-8	PE10MD[2:0]	000	000: PE10 input/output (port)
7	—	0	Reserved
6-4	PE9MD[2:0]	000	000: PE9 input/output (port)
3	—	0	Reserved
2-0	PE8MD[2:0]	000	000: PE8 input/output (port)

4.3.5 Register for Setting the Interrupt Controller (INTC)

(1) Interrupt priority register L (IPRL)

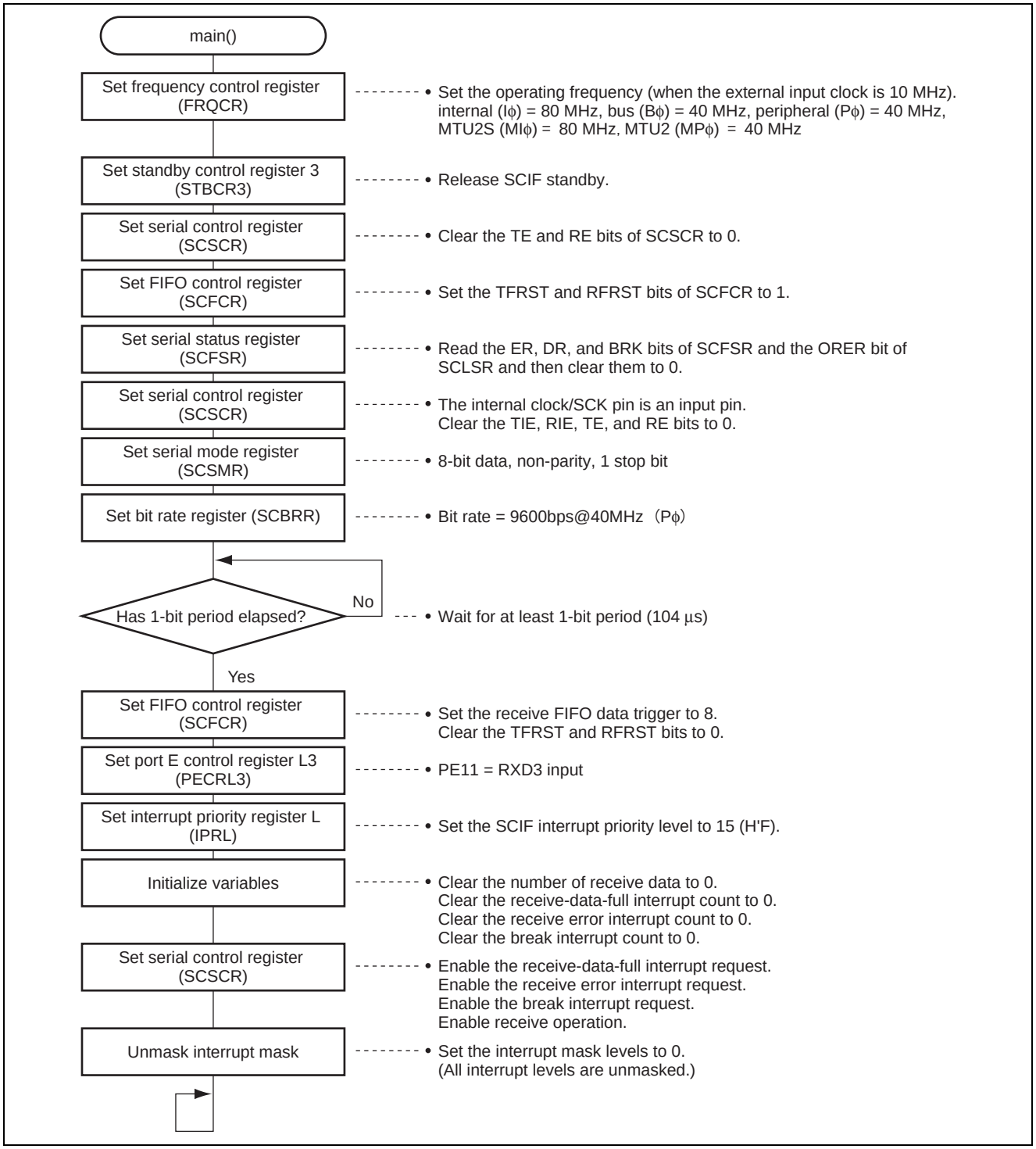
This register determines the priority levels of the corresponding interrupt requests.

Setting: H'000F

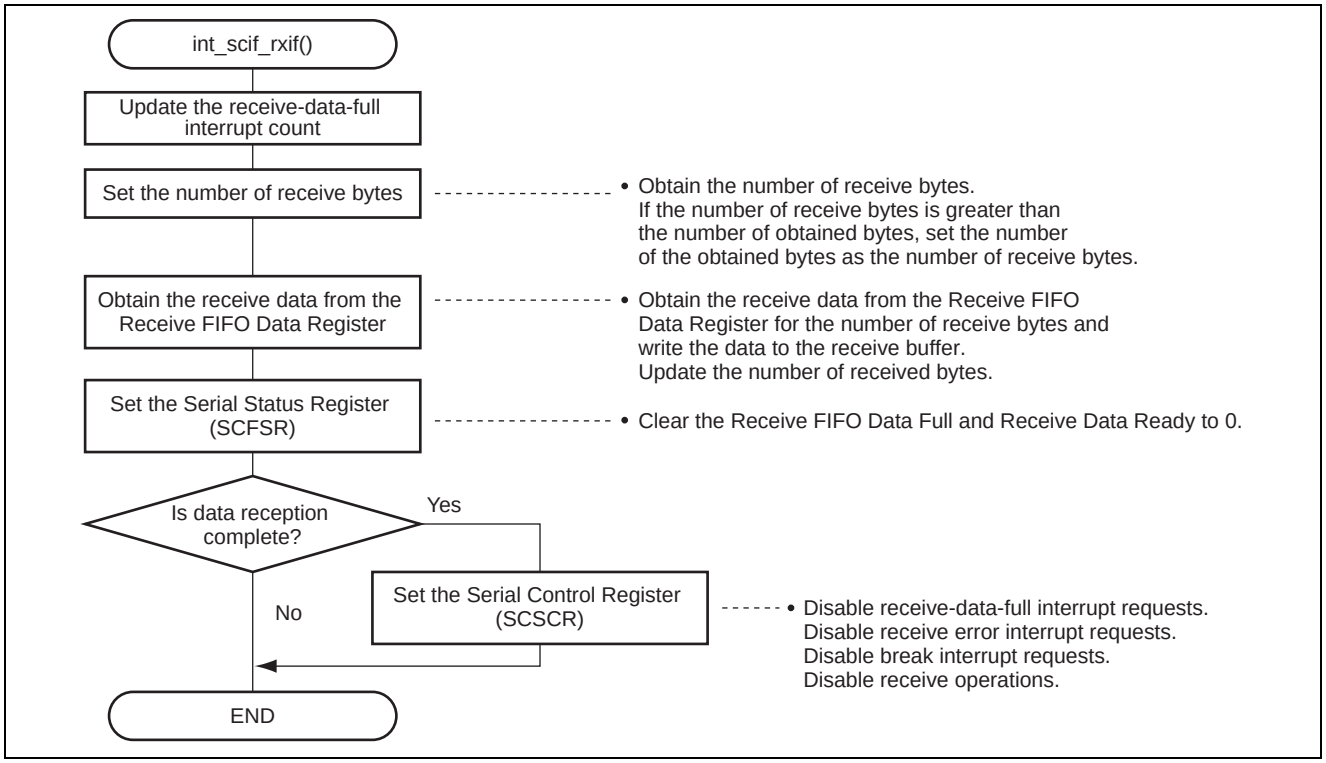
Bit	Bit Name	Setting Value	Function
15-12	IPR[15:12]	0000	Priority level 0
11-8	IPR[11: 8]	0000	Priority level 0
7-4	IPR[7:4]	0000	Priority level 0
3-0	IPR[3: 0]	1111	Priority level 15, SCIF interrupts

5. Flowcharts

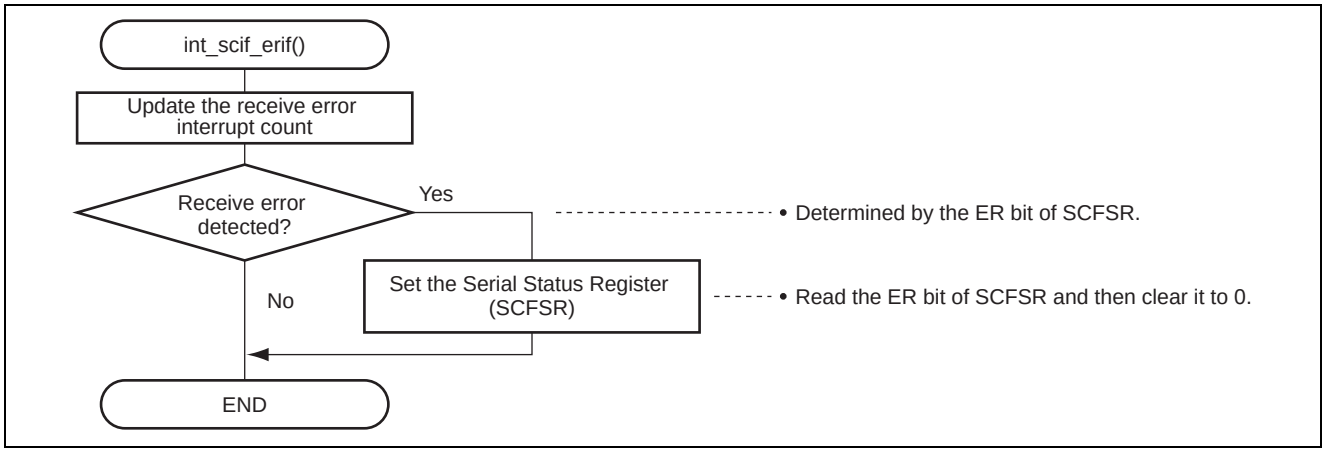
5.1 Main Routine



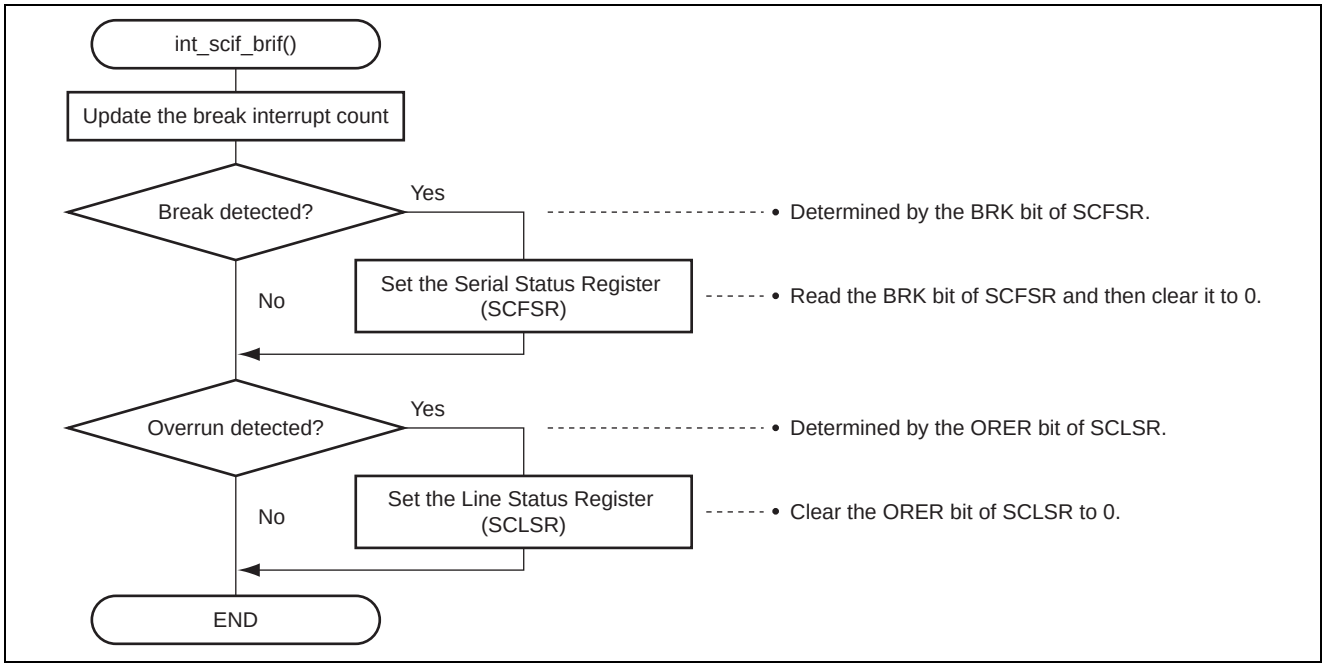
5.2 SCIF Receive-Data-Full Interrupt Routine



5.3 SCIF Receive Error Interrupt Routine



5.4 SCIF Break Interrupt Routine



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Rev.	Date	Description	
		Page	Summary
1.00	Sep.14.05	—	First edition issued

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