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April 1st, 2010
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Introduction
This application note describes the controller area network module (RCAN-ET) and provides an example of its application to data frame reception.

Target Devices
SH7137

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2. Description of the Sample Application....................................................................... 3
3. Listing of the Sample Program.................................................................................. 10
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1. Preface

1.1 Specifications

- Transfer rate: 500 kbps
- Mailbox for transmission: Mailbox 0
- Received data frame is as follows.
  - ID: 0 (standard format), data length code (DLC): 2, and data: H'C1C2

1.2 Module Used

- Controller area network (RCAN-ET)

1.3 Applicable Conditions

- MCU: SH7137
- Operating frequency:
  - Internal clock: 80 MHz
  - Bus clock: 40 MHz
  - Peripheral clock: 40 MHz
- C compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01 Release01 from Renesas Technology
- Compiler options: Default settings of the High-performance Embedded Workshop (-cpu = sh2 -debug -gbr = auto -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0 -struct_alloc = 1)

1.4 Related Application Note

None
2. Description of the Sample Application

This sample program employs the RCAN-ET module to receive a data frame in standard format (ID: 0).

2.1 Overview of Operations by the Module Used

The SH7137 CPU has an internal RCAN-ET module that support CAN2.0B and comply with ISO-11898.

The RCAN-ET module has 15 programmable transmit/receive mailboxes and one receive-only mailbox, each supporting a programmable reception filter mask, providing for highly flexible communications. Figure 1 shows the structure of the RCAN-ET module. For details on the module, refer to the section on the controller area network in the SH7137 Group Hardware Manual.

![Figure 1 Structure of the RCAN-ET Module](image-url)
2.2 Procedure for Setting the Module Used

This section describes initial settings for the reception of data frames by the RCAN-ET module.

Initial settings of the module are made in reset mode (configuration mode). On subsequent release from reset mode, the RCAN-ET module participates in CAN-bus activity. In initial settings in this sample program, one mailbox is set for transmission and reception respectively. Figures 2 and 3 show examples of the flow of initialization for the RCAN-ET module. For details on the settings made to individual registers, refer to the SH7137 Group Hardware Manual.

![Flowchart]

**Figure 2 Example of Initialization Flow for the RCAN-ET Module (1)**
Clearing the RAM area of mailbox 0

Setting message control (MB[0].CONTROL) (for reception).

- Setting message control (MB[0].CONTROL)
  MBC[2:0] (mailbox configuration) is set to B'010.
  [Function] Reception of remote/data frame is enabled.
  IDE (identifier extension bit) is cleared to 0.
  [Function] Standard format
  RTR (remote transmission request bit) is cleared to 0.
  [Function] Data frame
  STDID[10:0] (standard identifier) is cleared to 0.
  [Function] ID = 0

- Setting local acceptance filter mask (LAFM)
  LAFM is set to H'0000 0000.
  [Function] Mask is not set.

Clearing the RAM area of mailbox 0

Setting message control (MB[1].CONTROL) *1

- Setting message control (MB[1].CONTROL) *1
  MBC[2:0] (mailbox configuration) is set to B'000.
  [Function] Transmission of remote/data frame is enabled.
  DLC[3:0] (Data length code) is set to B'010.
  [Function] Data length = 2 bytes
  IDE (Identifier extension bit) is cleared to 0.
  [Function] Standard format
  RTR (Remote transmission request bit) is cleared to 0.
  [Function] Data frame
  STDID[10:0] (Standard identifier) is cleared to 0.
  [Function] ID = 0

Clearing the RAM area of mailbox 1 *1

Setting bit configuration register 0 (BCR0)

- Setting bit configuration register 0 (BCR0)
  BRP[7:0] (Baud rate pre-scale) is set to B'0000 0011.
  [Function] One time quantum is set as 8 cycles of the peripheral bus clock.
  Given TSG1 and TSG2 as indicated above, the transfer rate is
  500 kbps (refer to 2.3, Bit Configuration and Transfer Rate).

Setting bit configuration register 1 (BCR1)

- Setting bit configuration register 1 (BCR1)
  TSG1[3:0] (Time segment 1) is set to B'00101 (6 time quanta).
  TSG2[2:0] (Time segment 2) is set to B'010 (3 time quanta).
  SJW[1:0] (Resynchronization jump width) is set to B'00 (1 time quantum).
  [Function] Prevention of substantial misalignment of the sampling points
  Set BSP (Bit sample point).
  [Function] Selects sampling at a single point or determination of each sample value
  from the majority value of three points.

Setting master control register (MCR)

- Setting master control register (MCR)
  MCR0 (reset request) is cleared.
  [Function] Reset mode request is cleared.
  MCR1 (halt request) is cleared.
  [Function] Halt mode request is cleared.

Setting interrupt request register (IRR)

- Clearing interrupt request register (IRR)
  IRR0 to IRR15 are cleared.
  [Function] All interrupt flags are cleared.

Release from reset state? (GSR3 = 0?)

- Release from reset state? (GSR3 = 0?)
  Yes
  No

Note: 1. This processing is not required for reception alone,
  but descriptions in this sample program are on the
  assumption that both transmission and reception are performed.

Figure 3  Example of Initialization Flow for the RCAN-ET Module (2)
2.3 Bit Configuration and Transfer Rate

One-bit time for the CAN module has the four segments indicated below.

1) Synchronization segment (SS)
2) Propagation time segment (PRSEG)
3) Phase buffer segment 1 (PHSEG1)
4) Phase buffer segment 2 (PHSEG2)

Furthermore, the individual segments are structured in units of a base time called the time quantum (Tq). Figure 4 shows an example of the configuration of a bit in the case where SS = 1Tq, PRSEG = 3Tq, PHSEG1 = 3Tq, and PHSEG2 = 3Tq.

![Figure 4 Configuration of One-Bit Time](image)

In the RCAN-ET, the Tq of PRSEG + PHSEG1 is set to TSEG1[3:0] in bit configuration register 1 (BCR1) and the Tq of PHSEG2 is set to TSEG2[2:0] (Tq = set value + 1). Additionally, the number of cycles of the peripheral-bus clock corresponding to 1Tq is set in BRP[7:0] of bit configuration register 0 (BCR0).

In the following description, BRP[7:0], TSEG1[3:0] and TSEG2[2:0] indicate the register settings, and BRP, TSEG1, TSEG2, and SJW indicate the values that correspond to these register settings. For the values corresponding to the values set in registers, refer to the section on the controller area network in the SH7137 Group Hardware Manual.

By definition, Tq for the RCAN-ET module is $1Tq = 2 \times \frac{\text{peripheral bus clock}}{(BRP[7:0] + 1) \times \text{the number of Tq in 1-bit time}}$.

The following restrictions apply to settings of the bit-configuration registers.

$TSEG1 \text{ (Min)} > TSEG2 \geq SJW \text{ (Max)}$  
(SJW = 1 to 4)

SJW: Jump width for resynchronization. This segment is used to correct phase errors by extending phase buffer segment 1 or shortening phase buffer segment 2.

$8 \leq TSEG1 + TSEG2 + 1 \leq 25 \text{ time quanta}$

$TSEG2 \geq 2$

Since the settings in this sample program are as follows: peripheral bus clock = 40 MHz, BRP = 3, TSEG1 = 5, TSEG2 = 2, the transfer rate is calculated with the following formula.

Transfer rate (bps) = 40 M $(2 \times (3 + 1) \times ((5 + 1) + (2 + 1) + 1)) = 500 k$
2.4 Operation of the Sample Program

In this sample program, a data frame in standard format (ID: 0) is received in mailbox 0 at a transfer rate of 500 kbps. Figure 5 shows waveforms for data frame reception.

Figure 5 Waveform for Data Frame Reception by the RCAN-ET
### 2.5 Procedure of Processing by the Sample Program

Table 1 gives an example of the settings for the controller area network (RCAN-ET). Figure 6 shows an example of the flow of processing by this sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby control register 3</td>
<td>H’FFFF E806</td>
<td>H’F6</td>
<td>• MSTP8 = 0: RCAN-ET runs</td>
</tr>
<tr>
<td>Master control register (MCR)</td>
<td>H’FFFF D800</td>
<td>H’0001</td>
<td>• MCR0 = 1: Reset mode transition request</td>
</tr>
<tr>
<td></td>
<td></td>
<td>H’1001</td>
<td>• MCR15 = 1: RCAN-ET is not the same as HCAN2</td>
</tr>
<tr>
<td>Intercept mask register (IMR)</td>
<td>H’FFFF D80A</td>
<td>H’FFFF</td>
<td>• Disables all interrupts of RCAN</td>
</tr>
<tr>
<td>Bit configuration register 1</td>
<td>H’FFFF D804</td>
<td>H’5200</td>
<td>• TSG1[3:0] = 0101: PRSEG + PHSEG1 = 6 Tq</td>
</tr>
<tr>
<td>(BCR1)</td>
<td></td>
<td></td>
<td>• TSG2[2:0] = 010: PHSEG2 = 3 Tq</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• SJW[1:0] = 00: SJW = 1 Tq</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• BSP = 0: Bit sampling at one point</td>
</tr>
<tr>
<td>Bit configuration register 0</td>
<td>H’FFFF D806</td>
<td>H’0003</td>
<td>• BRP[7:0] = 3: 1 Tq = 8 × Pψ</td>
</tr>
<tr>
<td>(BCR0)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Message control field (MB[0].CONTROL1H)</td>
<td>H’FFFF D910</td>
<td>H’0200</td>
<td>• MBC[2:0] = 010: Enables reception of data frames and remote frames</td>
</tr>
<tr>
<td>Message control field (MB[1].CONTROL1H)</td>
<td>H’FFFF D930</td>
<td>H’0002</td>
<td>• MBC[2:0] = 000: Enables transmission of data frames and remote frames</td>
</tr>
<tr>
<td>Message control field (MB[1].CONTROL0H)</td>
<td>H’FFFF D920</td>
<td>H’0000 0000</td>
<td>• IDE = 0: Standard format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• RTR = 0: Data frame</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• STDID[10:0] = 0: Standard ID = 0</td>
</tr>
<tr>
<td>Local acceptance filter mask</td>
<td>H’FFFF D904</td>
<td>H’0000 0000</td>
<td>• Clear: MASK is not set</td>
</tr>
<tr>
<td>(MB[0].LAFMH)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Message data field (MB[0].MSG_DATA_0)</td>
<td>H’FFFF D908</td>
<td>H’0000</td>
<td>• Data field clear (RAM area is cleared)</td>
</tr>
<tr>
<td>Data frame receive pending</td>
<td>H’FFFF D842</td>
<td>H’0001</td>
<td>• RXPR[31:0] = H’0001: Clears the reception-completed flag</td>
</tr>
<tr>
<td>register 0 (RXPR0)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
main function

Set pin function controller (PFC): io_init_pfc();

Initialize controller area network (RCAN-ET): io_init_can();

Reception of data frame: io_data_receive();

Reception of data frame

Clear the data-frame reception completed flag (in RXPR0)

Confirm received data

END

END

Yes

No

Reception completed (RXPR0 = 1)?

Setting of pin function controller

Set the port-B control register L2 (Set to CRx0 and CTx0)

Figure 6   Example of Flow of Processing by the Sample Program
3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```c
/* FILE COMMENT */
* System Name : SH7137 Sample Program
* File Name : main.c
* Contents : CAN Module Application (Data Frame Receive)
* Version : 1.00.00
* Model : M3A-HS37
* CPU : SH7137
* Compiler : SHC9.1.1.0
* note : CAN bus speed 500 kbps
* <Caution>
* This sample program is for reference
* and its operation is not guaranteed.
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* history : 2008.03.24 ver.1.00.00
*/

#include "iodefine.h" /* SH7137 iodefine */

/* ---- prototype declaration ---- */
void main(void);
void io_init_pfc(void);
void io_init_can(void);
void io_data_receive(void);

/* ---- symbol definition ---- */
#define CAN_GSR3 0x0008
#define CAN_IRR0 0x0001
#define CAN_MB0 0x0001

/* ---- RAM allocation variable declaration ---- */
unsigned char nIDE = 0; /* ide */
unsigned char nRTR = 0; /* rtr */
unsigned char nDLC = 0; /* dlc */
unsigned int nSID = 0; /* sid */
unsigned int nEID = 0; /* eid */
unsigned char gRcv_data[8]; /* data of message */
```
2. Sample Program Listing: main.c (2)

```c
/*""FUNC COMMENT"*******************************************************
* Outline     : Sample program main
*-----------------------------------------------------------------------
* Include     : non
*-----------------------------------------------------------------------
* Declaration : void main(void);
*-----------------------------------------------------------------------
* Function    : Sample program main
*-----------------------------------------------------------------------
* Argument    : void
*-----------------------------------------------------------------------
* Return Value: void
*-----------------------------------------------------------------------
* Notice      : non
""FUNC COMMENT END"***************************************************/
void main(void)
{
    /* ==== Setting of PFC ==== */
    io_init_pfc();
    /* ==== Initializing CAN module ==== */
    io_init_can();
    /* ==== CAN data frame reception ==== */
    io_data_receive();
    while(1){
        /* loop */
    }
}

/*""FUNC COMMENT"*******************************************************
* Outline     : PFC setting
*-----------------------------------------------------------------------
* Include     : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration : void io_init_pfc(void);
*-----------------------------------------------------------------------
* Function    : Pin function CTRLler (PFC) setting
*-----------------------------------------------------------------------
* Argument    : void
*-----------------------------------------------------------------------
* Return Value: void
*-----------------------------------------------------------------------
* Notice      : non
""FUNC COMMENT END"***************************************************/
void io_init_pfc(void)
{
    /* ==== Setting of PFC ==== */
    /* ---- Port B CTRL register L2 ---- */
    PFC.PBCRL2.BIT.PB7MD = 0x6; /* Set CRx0 */
    PFC.PBCRL2.BIT.PB6MD = 0x6; /* Set CTx0 */
    PFC.PBIORL.BIT.B7    = 0;  /* PB7(CRX0) input */
    PFC.PBIORL.BIT.B6    = 1;  /* PB6(CTX0) output */
}
```
3. Sample Program Listing: main.c (3)

```c
/* ***FUNC COMMENT***
Outline     : RCAN setting
-----------------------------------------------------------------------
Include     : #include "iodefine.h"
-----------------------------------------------------------------------
Declaration : void io_init_can(void);
-----------------------------------------------------------------------
Function    : Controller area network (RCAN) set
-----------------------------------------------------------------------
Argument    : void
-----------------------------------------------------------------------
Return Value: void
-----------------------------------------------------------------------
Notice      : non
***FUNC COMMENT END***
*/
void io_init_can(void)
{
    int i;
    /* ---- Setting of power down mode(RCAN) ---- */
    STB.CR3.BYTE = 0xf6;   /* Module Standby Clear */
    /* RCAN */
    /* ---- Initializing CAN module ---- */
    RCANET.MCR.WORD |= 0x0001;   /* CAN Interface reset mode */
    while((RCANET.IRR.WORD & CAN_IRR0) != CAN_IRR0){
        /* Reset state waiting */
    }
    /* ---- IRR = 1, GSR = 1 (Auto SET) ---- */
    /* ---- Clear IRR0 ---- */
    RCANET.IRR.WORD = 0x0001;
    /* ---- RCAN mode selection(MCR15) ---- */
    RCANET.MCR.WORD |= 0x8000;   /* RCAN-ET is not same as HCAN2 */
    /* ---- Disable all can interrupt ---- */
    RCANET.IMR.WORD  = 0xffff;   /*---- Config mailbox0 as reception slot ---- */
    RCANET.MB[0].CTRL1.WORD = 0x0200;  /* can receive data and remote frame */
    RCANET.MB[0].CTRL0.LONG = 0x00000000; /* Initialize the Message Control Field */
    RCANET.MB[0].LAFM.LONG = 0x00000000;
    for(i = 0; i < 8; i++){   /* data clear */
        RCANET.MB[0].MSG_DATA[i] =  0x00;
    }
    /* ---- Config mailbox1 as transmission slot ---- */
    RCANET.MB[1].CTRL1.WORD = 0x0002;  /* Can send data or remote frame, dlc=2 */
    RCANET.MB[1].CTRL0.LONG = 0x00000000; /* standard data frame, id=0x000 */
    RCANET.MB[1].LAFM.LONG = 0x00000000;
    for(i = 0; i < 8; i++){   /* data clear */
        RCANET.MB[1].MSG_DATA[i] =  0x00;
    }
    /* ---- Config baudrate ---- */
    RCANET.BCR1.WORD = 0x5200;   /* tsg1=5(6 bit),tsg2=2(3 bit),sjw=0(1 bit),bsp=0 */
    RCANET.BCR0.WORD = 0x0003;   /* 500 Kbps */
    // RCANET.BCR0.WORD = 0x0007;   /* 250 Kbps */
    // RCANET.BCR0.WORD = 0x000f;   /* 125 Kbps */
    /* ---- Clear interrupt flags ---- */
    RCANET.IRR.WORD = 0xffffff;
```

void io_init_can(void)
/* ---- Clear reset and halt ---- */
RCANET.MCR.WORD &= 0xf8fc;  /* MCR0,MCR1 clear */
while( (RCANET.GSR.WORD & CAN_GSR3) != 0x0000 ){
    /* reset state is end */
}

/*"FUNC COMMENT"*******************************************************
* Outline : Data frame receive
*-----------------------------------------------------------------------
* Include : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration : void io_data_receive(void);
*-----------------------------------------------------------------------
* Function : Receives the data frame by using RCANET
*-----------------------------------------------------------------------
* Argument : void
*-----------------------------------------------------------------------
* Return Value : void
*-----------------------------------------------------------------------
* Notice : non
***"FUNC COMMENT END"***************************************************/
void io_data_receive(void)
{
    int i;

    /* ---- Reception completion waiting ---- */
    while((RCANET.RXPR0.WORD & CAN_MB0) != CAN_MB0){
    }

    /* ---- Receive data storage ---- */
    nIDE = RCANET.MB[0].CTRL0.BIT.IDE;
    nRTR = RCANET.MB[0].CTRL0.BIT.RTR;
    nDLC = RCANET.MB[0].CTRL1.BIT.DLC;
    nSID = RCANET.MB[0].CTRL0.BIT.STDID;
    nEID = RCANET.MB[0].CTRL0.BIT.EXDID;
    if(nDLC > 8){
        nDLC = 8;
    }
    for(i = 0; i < nDLC; i++){
        gRcv_data[i] = RCANET.MB[0].MSG_DATA[i];
    }

    /* ---- Reception completion flag clear ---- */
    RCANET.RXPR0.WORD = CAN_MB0;
}

/* End of File */
4. Documents for Reference

- Software Manual
  SH-1/SH2/SH-DSP Software Manual (REJ09B0171)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manuals
  SH7137 Group Hardware Manual (REJ09B0402)
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