Renesas Synergy™ Platform

S7G2 Parity Error Workaround

Introduction

Renesas has identified an issue with the S7G2 MCU, where spurious parity error interrupts are generated for a specific SRAM address range when the ICLK frequency is above 120 MHz and parity checking is enabled.

The S7G2 has 640 KB of contiguous SRAM, and the 216-KB region that is impacted by this issue is in the middle of the SRAM range (0x20008000 to 0x2003DFFF). A workaround for this issue is to exclude the SRAM at this address range by masking off the region with a constant buffer of 216 KB so that this region is not used by the user application, thereby avoiding the spurious parity error interrupts.

Target Device

S7G2

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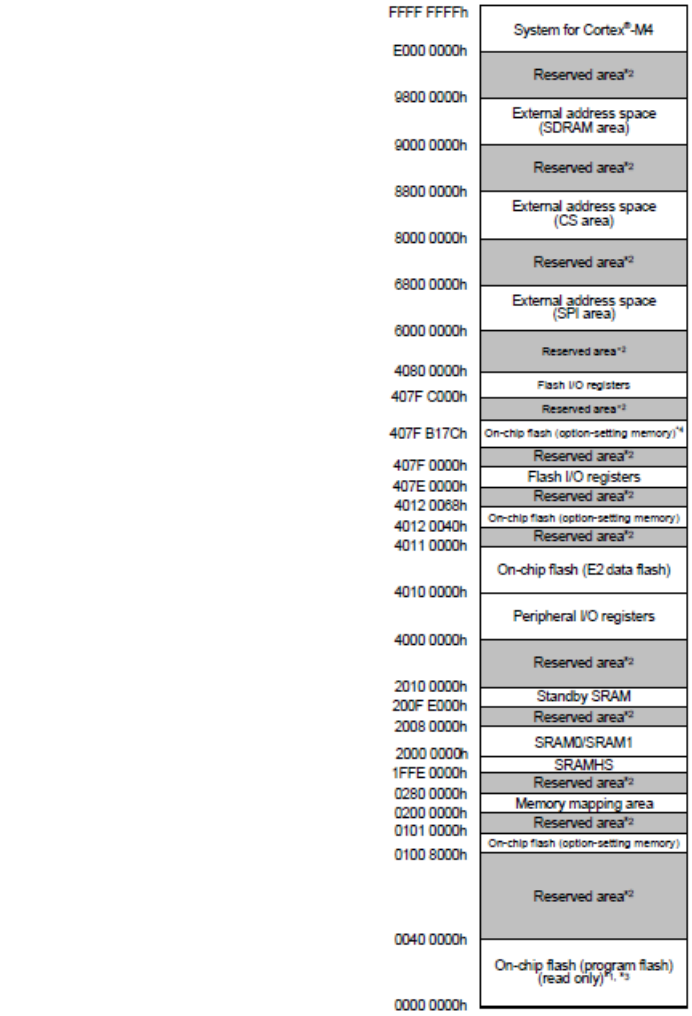
1. Memory Organization and the SRAM address range for S7G2

1.1 Memory map of S7G2 MCU



Note 1. The capacity of the flash differs depending on the products:

Product	Address
4-MB product	0000 0000h to 003F FFFFh
3-MB product	0000 0000h to 002F FFFFh

Note 2. Do not access reserved areas.

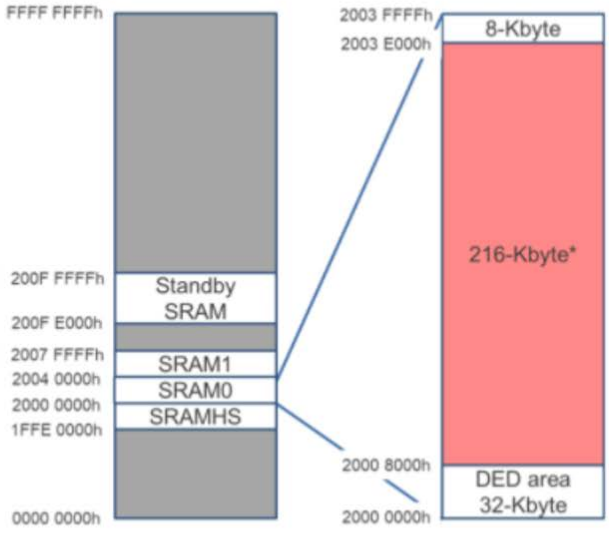
Figure 1. S7G2 Memory Map

- Contiguous SRAM region of 640 KB spans the 1FFE0000H to 20080000H address range.
- The MCU provides on-chip, high-speed SRAM modules with optional parity-bit checking or DED (double-bit error detection). The first 32 KB of SRAM0 supports DED. Parity checking is performed on other areas.

1.2 Observed error

The address region 0x20008000-0x2003DFFF is subject to spurious parity interrupts when the MCU is operated at ICLK greater than 120 MHz and when parity error interrupts or resets are enabled. Under these conditions an invalid interrupt or reset may occur.

- SRAM data can be correctly read and written up to ICLK = 240 MHz even when the parity error flag shows the wrong value.



Memory map

*Parity circuit works correctly up to ICLK 120MHz in this 216-Kbyte area

Parity circuit works correctly up to 240MHz in all the rest of the area.

Figure 2. Memory Map of Affected Area

2. Linker Script Workaround for the IAR Toolchain

As a workaround, the address range 0x20008000-0x2003DFFF can be masked off by declaring a constant buffer of 216 KB in the IAR linker script using following steps.

2.1 Define symbols for addresses of start and end of region in the linker script

Define symbols for the start and end addresses for the region to be masked as a reserved region in the linker script `S7G2.icf`

```
s7g2.icf | hal_entry.c | s7g2_iar_test.map | startup_S7G2.c | main.c | hal_entry.c | startup
14  define symbol region_FLASH_end      = 0x003FFFFF;
15  define symbol region_RAM_start      = 0x1FFE0000;
16  define symbol region_RAM_end        = 0x2007FFFF;
17  define symbol region_reserved_start = 0x20008000;
18  define symbol region_reserved_end   = 0x2003DFFF;
19  define symbol region_DF_start       = 0x40100000;
20  define symbol region_DF_end         = 0x4010FFFF;
```

Figure 3. Start and End Regions

2.2 Define the reserved region in the linker script

```
s7g2.icf
34  define region FLASH_region      = mem:[from region_FLASH_start   to region_FLASH_end];
35  define region RAM_region        = mem:[from region_RAM_start     to region_RAM_end];
36  define region DF_region         = mem:[from region_DF_start      to region_DF_end];
37  define region SDRAM_region      = mem:[from region_SDRAM_start   to region_SDRAM_end];
38  define region QSPI_region       = mem:[from region_QSPI_start    to region_QSPI_end];
39
40  define region ID_CODE_region    = mem:[from region_ID_CODES_start   to region_ID_CODES_end];
41
42  define region reserved_region     = mem:[from region_reserved_start   to region_reserved_end];
43
44  initialize manually { readwrite };
```

Figure 4. Reserved Region

2.3 Declare the placeholder for the buffer in the linker script

This will reserve the 216-KB address space as `reserved_region` starting from 0x20008000-0x2003DFFF

```
s7g2.icf
93                              rw section .data,
94                              block HW_LOCK,
95                              rw section HEAP,
96                              rw section .stack,
97                              block RAM_CODE };
98
99          place in reserved_region  {rw section BUFFER};
100
101         place in DF_region      { ro section .data_flash };
102         place in SDRAM_region   { rw section .sdram, rw section .frame };
103         place in QSPI_region    { section .qspi_flash  };
```

Figure 5. Placeholder

2.4 Place a constant buffer in the reserved region in the application code/hal_entry.c

This will place a constant buffer of 216-KB at the defined location, hence masking the region off.

```
1   /* HAL-only entry function */
2   #include "hal_data.h"

    #if defined(__ICCARM__)
    #pragma location="BUFFER"
    __root uint8_t buffer[216*1024]={0};
    #endif
```

Figure 6. Buffer in Reserved Region

3. Linker Script Workaround for the GCC Toolchain

As a workaround, the address range 0x20008000-0x2003DFFF can be masked off by declaring a const buffer of 216 KB and using the GCC linker script to place it at the desired address using following steps.

3.1 Define memory region in the linker script

Define `reserved_section` as a region in memory with start address 0x20008000 in the RAM section and define a section in this region as .buffer in the linker script file (`s7g2.ld`).

Ensure the following when placing the buffer in the GCC linker script to use all 160 KB available before address 0x20008000:

1. Make sure the buffer is placed after the stack area so as to use as much of the 160-KB memory region available before address 0x20008000 as possible.

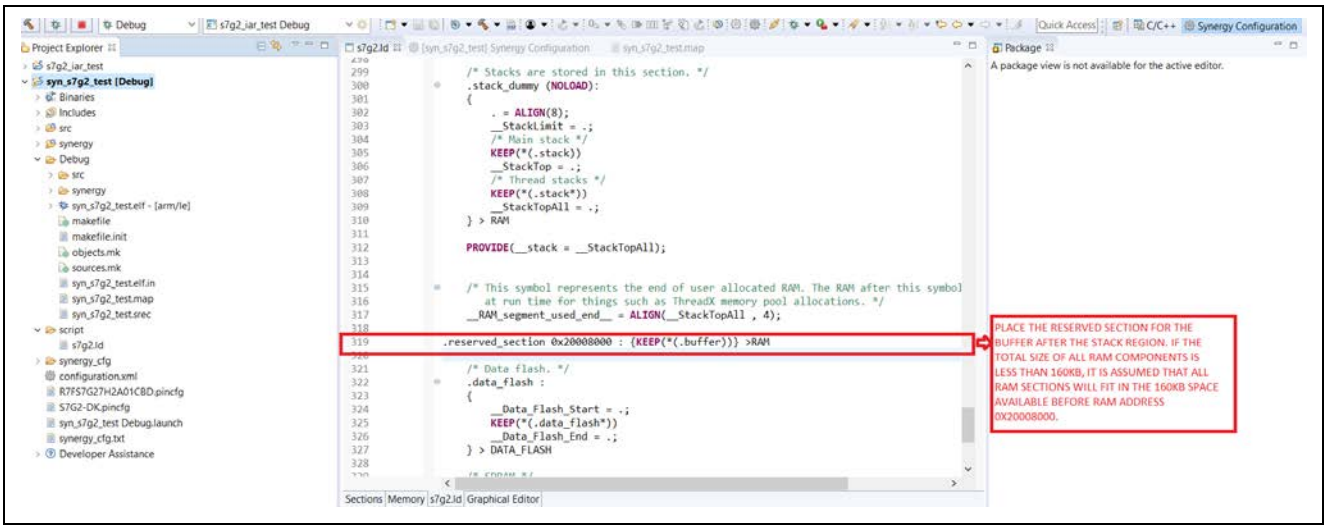


Figure 7. Define and place reserved_section

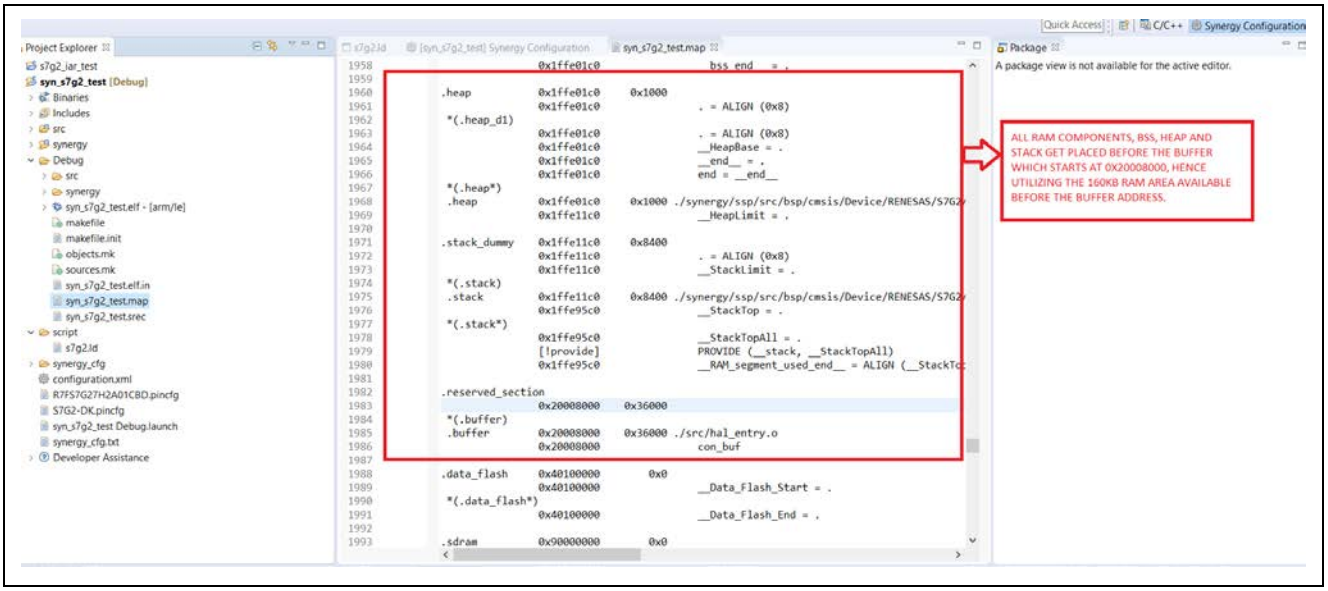


Figure 7. Map file showing the placement of the buffer and RAM sections before the buffer.

2. If any region overflows into the buffer and the linker throws an overlapping regions error, move the buffer before the region until the overflow no longer occurs. If the addition of RAM regions exceeds 160 KB, move the buffer before the region that stops the overlap error.

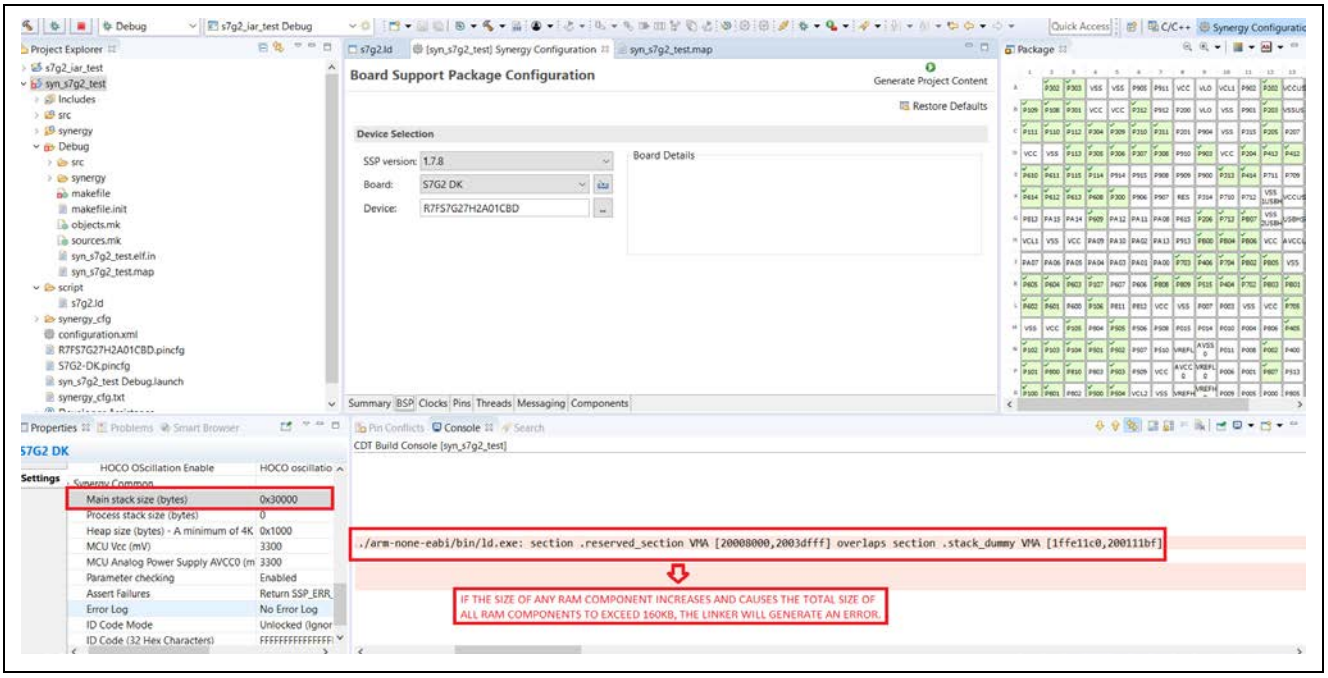


Figure 8. Stack region is increased so that it overflows into buffer and the linking error is generated

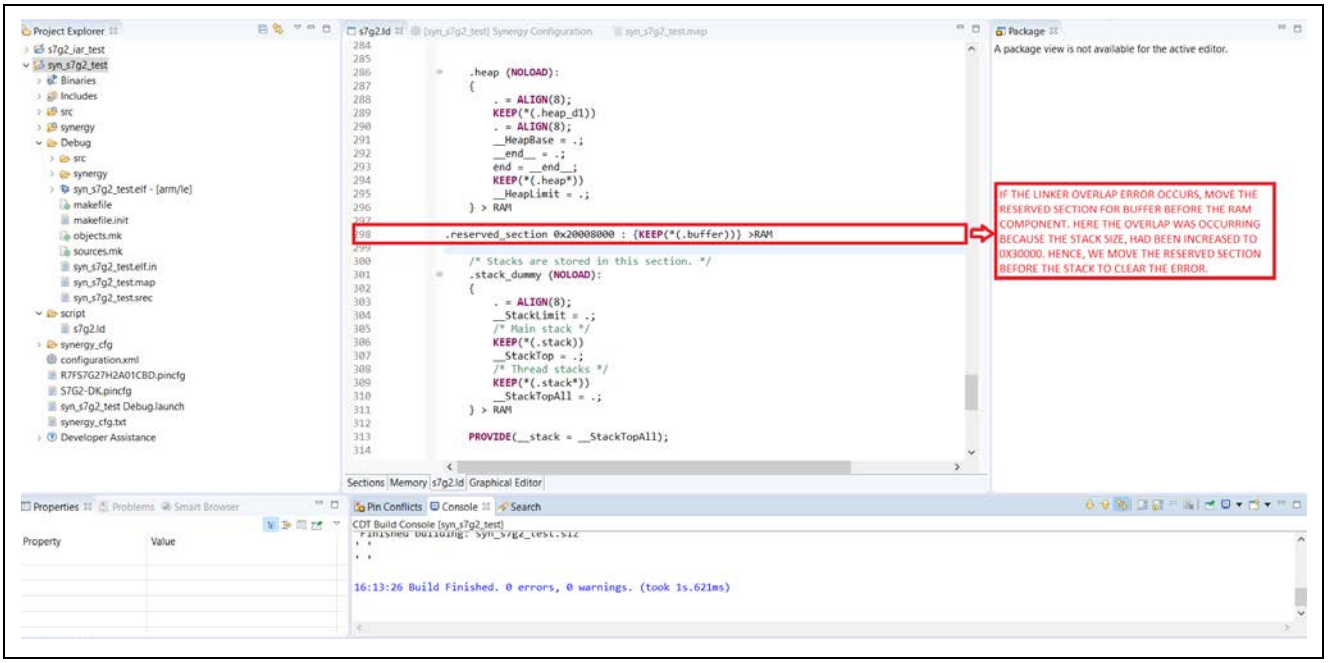


Figure 9. Buffer is moved before the stack region so that the linker error is cleared

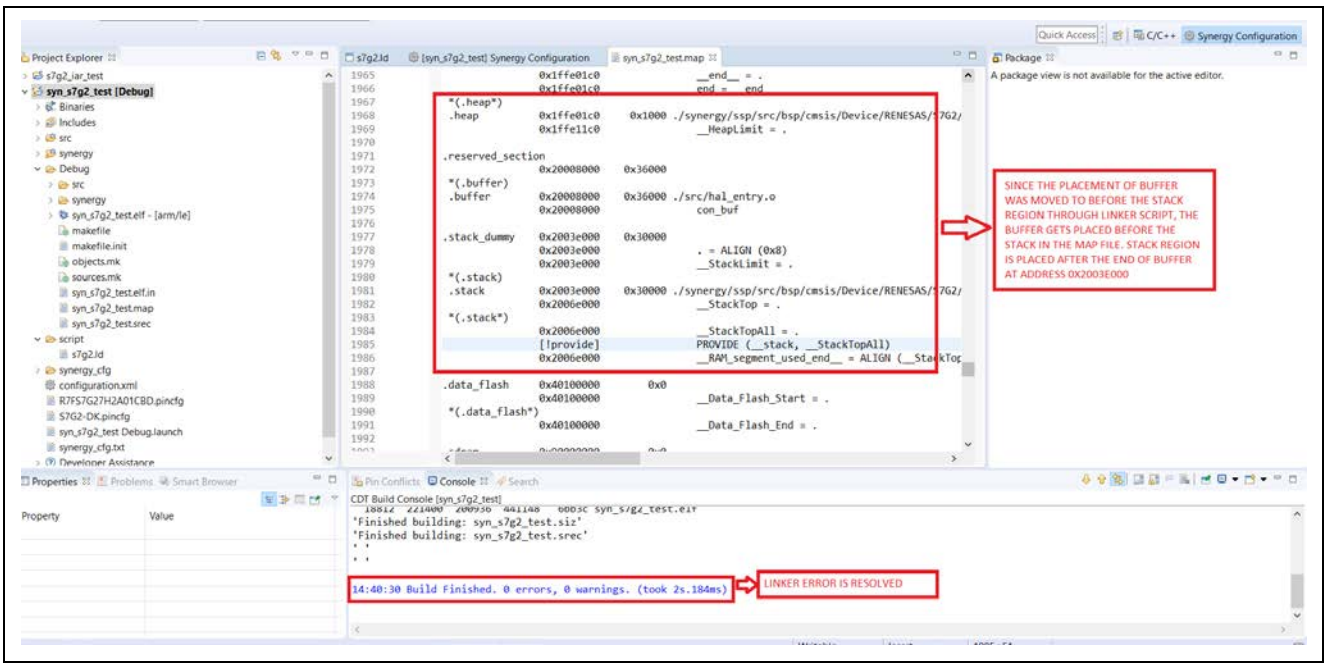


Figure 10. Buffer is placed before the stack since it was placed before the stack in the linker script

Note: The user is responsible for changing the placement of the buffer as needed. The buffer needs to be located at the right place for optimum usage of available memory before address 0x20008000.

3.2 Place a constant buffer in the reserved region in the application code/hal_entry.c

This will place a const buffer of 216 KB at the defined location, masking the region off.

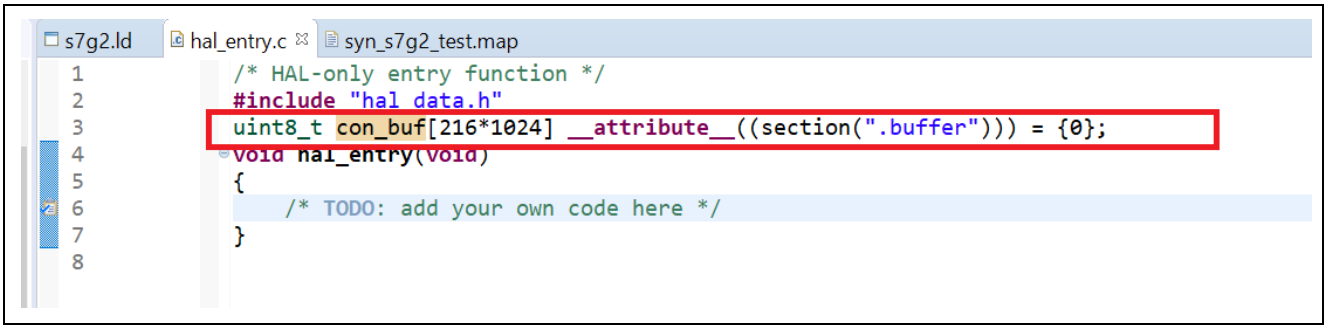


Figure 11. Place Buffer in Reserved Region

4. Expected output and memory allocation

4.1 .map file with IAR linking

Region BUFFER is placed at 0x20008000 from the application code (`hal_entry`) and a 216-KB space is reserved in the RAM as seen in the `.map` file

```
"P5":                                      0x36000
  P5 s0                          0x20008000  0x36000  <Init block>
    BUFFER               inited  0x20008000  0x36000  hal_entry.o [1]
                       - 0x2003e000  0x36000
```

Figure 12. Buffer .map File

4.2 .map file with GCC linking

The section .buffer of length 216KB is placed in the .reserved_section in memory at address 0x20008000 as seen in the .map file

```
.reserved_section
                0x20008000    0x36000
 *(.buffer)
 .buffer        0x20008000    0x36000 ./src/hal_entry.o
                0x20008000                con_buf
```

Figure 13. .buffer in .reserved_section

5. Notes

1. The workaround mentioned above will decrease the available RAM by 216 KB.
2. This workaround splits the SRAM into two non-contiguous memory sections, but the linker is able to seamlessly allocate and assign data to these two sections without developer intervention.
3. Other workarounds :
   a. Do not use SRAM parity error interrupts (or reset). Set PARIOAD.OAD = 0 and NMIER.RPEEN = 0. These are the default settings for the MCU in the Synergy Software Package (SSP). These settings disable parity error interrupts and resets.
   b. Do not use SRAM0 2000_8000h-2003_DFFFh (216 KB)
      # Normal use space: 424 KB (=640 – 216 KB)
   c. If parity error interrupts or resets are enabled and ICLK is greater than 120 MHz, avoid any read access to the 216-KB SRAM0 address (2000 8000h – 2003 DFFFh) (from CPU, DMAC/DTC, EDMAC, JPEG, DRW, LCDC).
   d. Use an ICLK frequency less than 120MHz (ICLK ≦ 120MHz)

6. References

List of the reference documents and links.

- https://gcc.gnu.org/onlinedocs/gcc-4.8.2/gcc/Variable-Attributes.html
- https://www.iar.com/support/tech-notes/linker/how-do-i-place-a-group-of-functions-or-variables-in-a-specific-section/

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec.8.2020	—	First release of document

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(Rev.4.0-1 November 2017)

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