RZ/T1 Group

ΔΣ Interface (DSMIF) Sample Program

R01AN3158EJ0120
Rev.1.20
Jun. 07, 2018

Summary

This application note describes how to configure the on-chip ΔΣ interface of RZ/T1 group products.

Target Devices

RZ/T1 group

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications of the target microcomputer and extensively evaluate and test the modified program.

Table of Contents

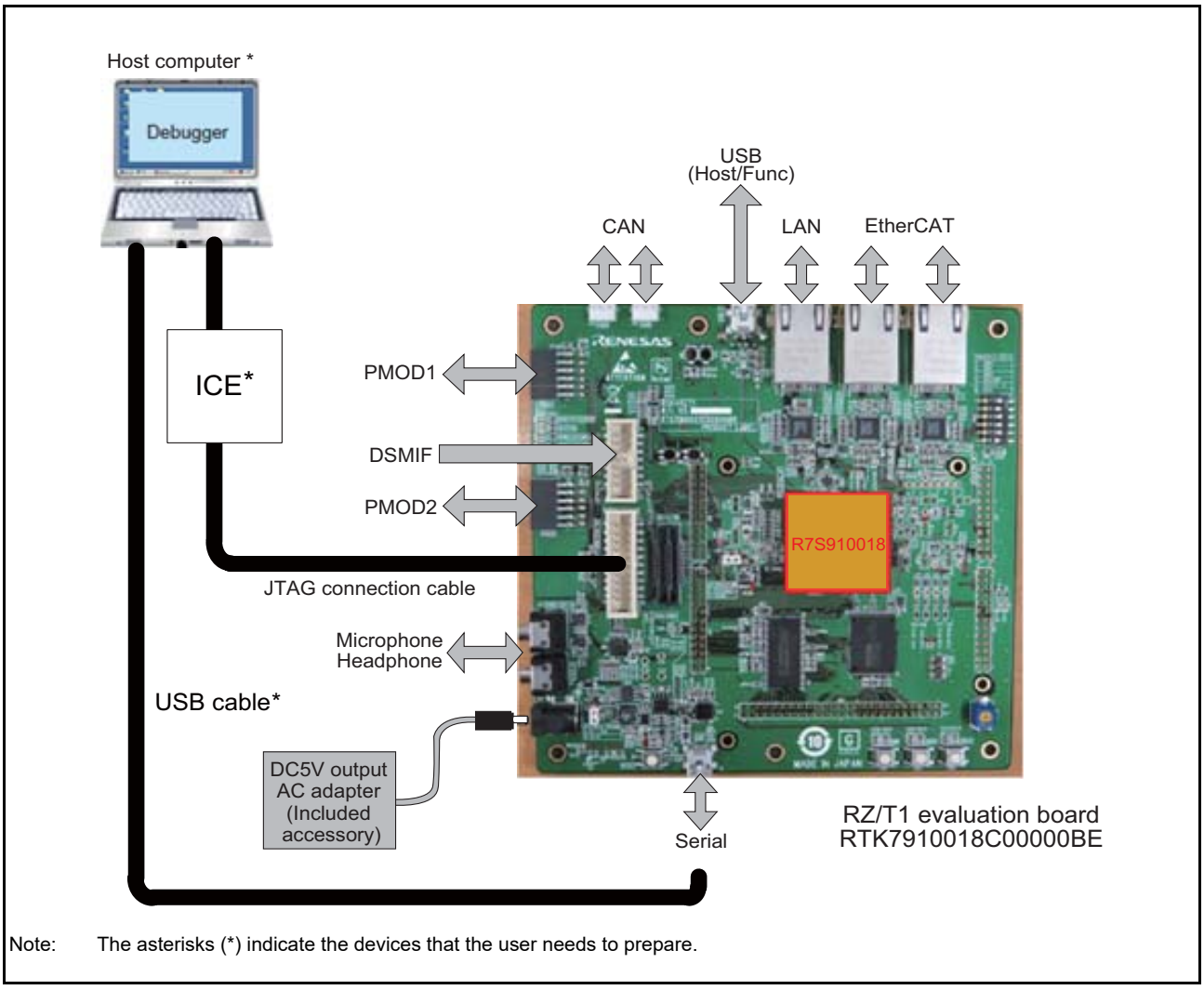
1. Specifications

RZ/T1 microcontrollers have two ΔΣ interface (DSMIF) units for a total of four channels, three for unit 0 (channels U, V, W) and one for unit 1 (channel X), which are connected to up to four external delta-sigma modulators. The interfaces filter 1-bit delta-sigma modulated data and convert it to 16-bit data.

The major peripheral modules and their applications are listed in Table 1.1. The operating environment is shown in Figure 1.1.

Table 1.1 Major Functions and Applications

Peripheral Module	Application
Clock generator (CPG)	CPU clock and low-speed on-chip oscillator
Serial communication interface with FIFO (SCIFA)	Asynchronous communications of the SCIFA is used for COM port communications by using an RS-232C interface
ΔΣ interface (DSMIF for channel X in unit 1)	Filter 1-bit digital data from an external delta-sigma modulator and convert this into 16-bit data.
Error control module (ECM)	Error sources 30 and 31 (X overcurrent abnormality detection error and X short-circuit abnormality detection error) are used
Compare match timer W (CMTW in unit 0)	Used as the timer in monitoring of the 16-bit digital data converted through the DSMIF
Interrupt controller (ICUA)	Error detection, compare match interrupt, and reception FIFO data full interrupt are used



Note: The asterisks (*) indicate the devices that the user needs to prepare.

Figure 1.1 Operating Environment

2. Operating Environment

The sample program covered in this application note is for the environment below.

Table 2.1 Operating Environment

Item	Description
Microcomputer	RZ/T1 group
Operating frequency	CPU clock (CPUCLK): 450 MHz
Operating voltage	Power supply voltage (I/O): 3.3 V
Integrated development environment	IAR Systems: Embedded Workbench® for Arm (version 8.20.2) Arm: Arm® integrated environment: Arm Development Studio 5 (DS-5™) (version 5.26.2) Renesas: e²studio (version 6.1.0)
Operating modes	SPI boot mode (serial flash) 16-bit-bus boot mode (Nor flash)
Settings for communication for the terminal software	• Transfer rate: 115200 bps • Data length: 8 bits • Parity: none • Stop bit length: 1 bit • Flow control: not supported • New line code (reception): CR • New line code (transmission): CR
Board	• RZ/T1 evaluation board (RTK7910018C00000BE) • PS9352A sub-board for the RZ/T1 evaluation board*1 (hereinafter “PS9352A sub-board”)
Devices (functions to be used on the board)	• Serial interface (USB-mini B connector J8) • NOR flash memory (connected to CS0 and CS1 spaces) Manufacturer: Macronix International Co., Ltd. Model: MX29GL512FLT2I-10Q • Serial flash memory Manufacturer: Macronix International Co., Ltd. Model: MX25L51245G • ΔΣ interface (DSMIF connector J12)
USB serial port driver for PC	• For RTK7910018C00000BE • For RTK7910022C00000BR

Note 1. The PS9352A sub-board includes a high-precision ΔΣ A/D converter. It is of the optical isolation type and converts variations in the analog input voltage into streams of 1-bit data.
Using the RZ/T1 evaluation board with the PS9352A sub-board enables checking the operation of the ΔΣ A/D converter in combination with a Sinc³ filter.

3. Related Application Notes

The application notes related to this application note are listed below for reference.

- RZ/T1 Group Application Note: Initial Settings (R01AN2554EJ)
- RZ/T1 Group Application Note: FIFO Integrated Serial Communication Interface (SCIFA) (R01AN2577EJ)
- RZ/T1 Group Application Note: CMTW & ELC Sample Program (R01AN2600EJ)

Note: Settings for registers of the microcontroller which are not stated in this application note are as described in the above application notes.

4. Peripheral Modules

The basics of the operating mode, clock generator (CPG), serial communication interface with FIFO (SCIFA), ΔΣ interfaces (DSMIF), error control module (ECM), compare match timer W (CMTW), interrupt controller (ICUA), reset, and general purpose I/O ports are found in *RZ/T1 Group User's Manual Hardware*.

5. Hardware

5.1 Pins

Table 5.1 lists the pins used and their functions.

Table 5.1 Pins and Functions

Pin	I/O	Content
MD0	Input	Operating mode selection
MD1	Input	MD0 = L and MD1 = L and MD2 = L (for SPI boot mode)
MD2	Input	MD0 = L and MD1 = H and MD2 = L (for 16-bit bus boot mode)
MCLK0 to MCLK3	I/O	Clock I/O pin
MDAT0 to MDAT3	Input	Data input pin

5.2 Reference Circuit

Figure 5.1 shows a block diagram of the ΔΣ interface.

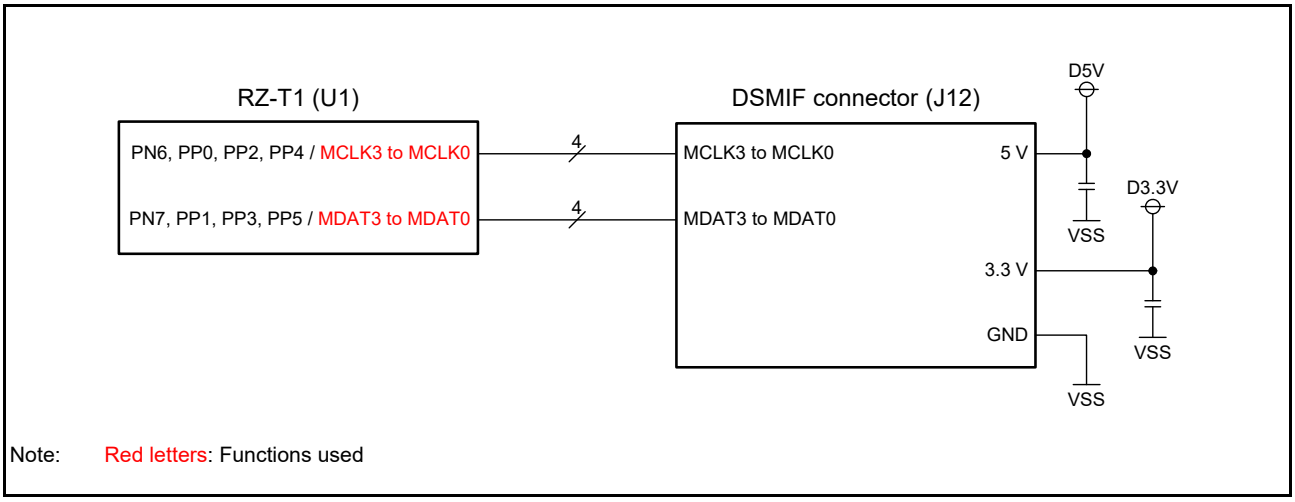


Figure 5.1 ΔΣ Interface Block Diagram

5.3 Connecting the PS9352A Sub-board

Figure 5.2 shows the connection of the PS9352A sub-board to J12 connector of the RZ/T1 evaluation board (RTK7910018C00000BE).

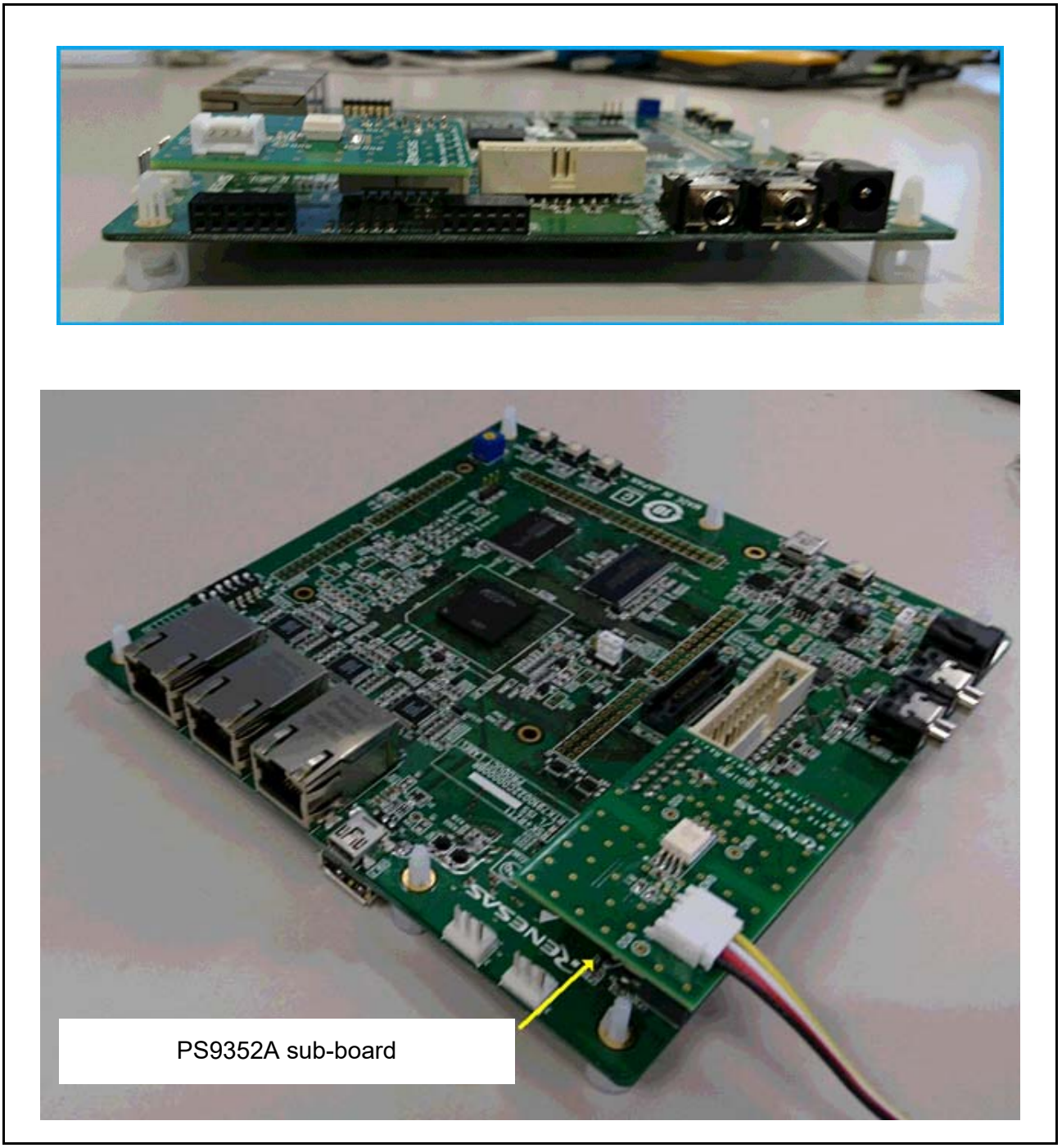


Figure 5.2 Connecting the PS9352A Sub-board

6. Software

The software includes a driver for the ΔΣ interface (DSMIF) and the API functions needed for reading the delta-sigma converted data.

6.1 Functional Overview

The software monitors the delta-sigma modulated current values through terminal software on a host PC. The communications are synchronous and through an RS-232C interface (COM port) on the PC and through SCIFA (serial communication interface). Overcurrent abnormality detection errors and short-circuit abnormality detection errors (both on channel x) are monitored.

Users can make preferred settings of the filters to apply in monitoring of the currents from a menu of the sample program. The filters are used in the combinations (0 to 14) listed in Table 6.1.

Table 6.1 Allowed Combinations of Filters

Combination Number	SINC Filter Stage (Filter Name)	Value of WORD1GEN[2:0] or WORD2GEN[2:0]	MSB	Value of BITSHIFT1[3:0] or BITSHIFT2[3:0]	Resolution
0	3 (sinc3)	010b	Bit 8	1000b	9 bits
1		011b	Bit 11	0110b	12 bits
2		100b	Bit 14	0100b	15 bits
3		101b	Bit 17	0010b	16 bits
4		110b	Bit 20	0001b	16 bits
5		111b	Bit 23	0000b	16 bits
6	2 (sinc2)	011b	Bit 7	1001b	8 bits
7		100b	Bit 9	0111b	10 bits
8		101b	Bit 11	0110b	12 bits
9		110b	Bit 13	0101b	14 bits
10		111b	Bit 15	0011b	16 bits
11	1 (sinc1)	100b	Bit 4	1100b	5 bits
12		101b	Bit 5	1011b	6 bits
13		110b	Bit 6	1010b	7 bits
14		111b	Bit 7	1001b	8 bits

Note: For the parameters for each filter, refer to section 41.3.5 Filter Setting of *RZ/T1 Group User's Manual: Hardware*.

6.2 Interrupts

The interrupts used in this sample program are listed below.

Table 6.2 Interrupts Used in the Sample Program

Interrupt (Source ID)	Priority Level	Processing Outline
Detection of ECM errors (maskable) (ERRD)	3	DSMIF error detection Scan operation is stopped on detection of the following errors: • X overcurrent abnormality detection error • X short-circuit abnormality detection error
CMTW unit 0 compare match interrupt_ch0 (CMWI0)	3	Compare match completion The value for current is read every time this interrupt is detected while scanning in the low-frequency scan mode.
SCIFA unit 2 reception FIFO data full (RXIF2)	3	Key input detection Scan operation is stopped when a key input is detected while scanning in the low-frequency scan mode.

6.3 Fixed-Width Integer

The fixed-width integers used in this sample program are listed below. These fixed-width integers are defined in the standard library.

Table 6.3 Fixed-Width Integers Used in the Sample Program

Symbol	Content
int8_t	8-bit signed integer
int16_t	16-bit signed integer
int32_t	32-bit signed integer
int64_t	64-bit signed integer
uint8_t	8-bit unsigned integer
uint16_t	16-bit unsigned integer
uint32_t	32-bit unsigned integer
uint64_t	64-bit unsigned integer

6.4 Structures

Table 6.4 to Table 6.6 are the structures used in this sample program.

Table 6.4 Structure for Storing X1DATA Filter Settings (st_dsmif_filter_cfg_x1_t)

Member		Content
uint8_t	sinc1sel	SINC filter stage for the X1DATA register: The number of the SINC filter stages to be applied to the X1DATA register is selected from the following: DSMIF_SINC_1: One stage DSMIF_SINC_2: Two stages DSMIF_SINC_3: Three stages The value specified in this member is set to SINC1SEL[1:0] of the XYZ control register (XYZCTL).
uint8_t	word1gen	Decimation clock for the X1DATA register: The decimation clock to be applied to the X1DATA register is selected from the following: DSMIF_DIV_MCLK_4: MCLK3/4 DSMIF_DIV_MCLK_8: MCLK3/8 DSMIF_DIV_MCLK_16: MCLK3/16 DSMIF_DIV_MCLK_32: MCLK3/32 DSMIF_DIV_MCLK_64: MCLK3/64 DSMIF_DIV_MCLK_128: MCLK3/128 DSMIF_DIV_MCLK_256: MCLK3/256 The value specified in this member is set to WORD1GEN[2:0] of the XYZ control register (XYZCTL).
uint8_t	bitshift1	Bit shift for the X1DATA register: The width of bit shifting to be applied to the X1DATA register is selected from the following (for 16 bits of the 24-bit results of decimation): DSMIF_BITSHIFT_0 to DSMIF_BITSHIFT_12 See Section 6.5, Constants for details of the setting values. The value specified in this member is set to BITSHIFT1[3:0] of the XYZ control register (XYZCTL).

Table 6.5 Structure for Storing X2DATA Filter Settings (st_dsmif_filter_cfg_x2_t)

Member		Content
uint8_t	sinc2sel	SINC filter stage for the X2DATA register: The number of the SINC filter stages to be applied to the X2DATA register is selected from the following: DSMIF_SINC_1: One stage DSMIF_SINC_2: Two stages DSMIF_SINC_3: Three stages The value specified in this member is set to SINC2SEL[1:0] of the XYZ control register (XYZCTL).
uint8_t	word2gen	Decimation clock for the X2DATA register: The decimation clock to be applied to the X2DATA register is selected from the following: DSMIF_DIV_MCLK_4: MCLK3/4 DSMIF_DIV_MCLK_8: MCLK3/8 DSMIF_DIV_MCLK_16: MCLK3/16 DSMIF_DIV_MCLK_32: MCLK3/32 DSMIF_DIV_MCLK_64: MCLK3/64 DSMIF_DIV_MCLK_128: MCLK3/128 DSMIF_DIV_MCLK_256: MCLK3/256 The value specified in this member is set to WORD2GEN[2:0] of the XYZ control register (XYZCTL).
uint8_t	bitshift2	Bit shift for the X2DATA register: The width of bit shifting to be applied to the X2DATA register is selected from the following (for 16 bits of the 24-bit results of decimation): DSMIF_BITSHIFT_0 to DSMIF_BITSHIFT_12 See Section 6.5, Constants for details of the setting values. The value specified in this member is set to BITSHIFT2[3:0] of the XYZ control register (XYZCTL).

Table 6.6 Structure for Storing DSMIF Error Status (st_dsmif_errorx_t)

Member		Content
uint8_t	erxi	X overcurrent abnormality detection error status Allowed values: 0: No error occurred 1: An error occurred
uint8_t	erxsc	X short-circuit abnormality detection error status Allowed values: 0: No error occurred 1: An error occurred
uint8_t	err_all	X overcurrent/short-circuit abnormality detection error status (both abnormalities are detected) Allowed values: 0: No error occurred 1: An error occurred

6.5 Constants

Table 6.7 and Table 6.8 list the constants used in this sample program.

Table 6.7 Constants for Registers Used for DSMIF (1 / 2)

Constant	Value	Description
DSMIF_CLEAR_ERR_XYZ	(0x00000170u)	Clear the error on channel X.
DSMIF_FILTER_SET_0 to DSMIF_FILTER_SET_14	(0u) to (14u)	Set the SINC filter, decimation clock, and bit shift in a batch by selecting the combination of settings. See Table 6.1 Allowed Combinations of Filters, for setting values.
DSMIF_SINC_1	(1u)	Setting of the SINC filter: sinc1 (one stage)
DSMIF_SINC_2	(2u)	Setting of the SINC filter: sinc2 (two stages)
DSMIF_SINC_3	(0u)	Setting of the SINC filter: sinc3 (three stages)
DSMIF_DIV_MCLK_4	(0u)	Setting of the decimation clock: MCLK3/4
DSMIF_DIV_MCLK_8	(2u)	Setting of the decimation clock: MCLK3/8
DSMIF_DIV_MCLK_16	(3u)	Setting of the decimation clock: MCLK3/16
DSMIF_DIV_MCLK_32	(4u)	Setting of the decimation clock: MCLK3/32
DSMIF_DIV_MCLK_64	(5u)	Setting of the decimation clock: MCLK3/64
DSMIF_DIV_MCLK_128	(6u)	Setting of the decimation clock: MCLK3/128
DSMIF_DIV_MCLK_256	(7u)	Setting of the decimation clock: MCLK3/256
DSMIF_BITSHIFT_0	(0u)	Setting of bit shifting: [23:8]
DSMIF_BITSHIFT_1	(1u)	Setting of bit shifting: [20:5]
DSMIF_BITSHIFT_2	(2u)	Setting of bit shifting: [17:2]
DSMIF_BITSHIFT_3	(3u)	Setting of bit shifting: [15:0]
DSMIF_BITSHIFT_4	(4u)	Setting of bit shifting: [14:0], 1’b0
DSMIF_BITSHIFT_5	(5u)	Setting of bit shifting: [13:0], 2’b00
DSMIF_BITSHIFT_6	(6u)	Setting of bit shifting: [11:0], 4’b000
DSMIF_BITSHIFT_7	(7u)	Setting of bit shifting: [9:0], 6’b00_0000
DSMIF_BITSHIFT_8	(8u)	Setting of bit shifting: [8:0], 7’b000_0000
DSMIF_BITSHIFT_9	(9u)	Setting of bit shifting: [7:0], 8’b0000_0000
DSMIF_BITSHIFT_10	(10u)	Setting of bit shifting: [6:0], 9’b0_0000_0000
DSMIF_BITSHIFT_11	(11u)	Setting of bit shifting: [5:0], 10’b00_0000_0000
DSMIF_BITSHIFT_12	(12u)	Setting of bit shifting: [4:0], 11’b000_0000_0000
DSMIF_READ_X1	(1u)	Select X1DATA to read the value for current from.
DSMIF_READ_X2	(2u)	Select X2DATA to read the value for current from.
DSMIF_ERR_ERIX	(1u)	Set an error status as X overcurrent abnormality detection error.
DSMIF_ERR_ERXSC	(2u)	Set an error status as X short-circuit abnormality detection error.
DSMIF_ERR_ALL	(3u)	Set an error status as X overcurrent/short-circuit abnormalities detection error.
DSMIF_MODE_HIGH	(0u)	Set to high-frequency scan mode.
DSMIF_MODE_LOW	(1u)	Set to low-frequency scan mode.
DSMIF_UPPER_LIMIT_5	(0xF800u)	Upper limit of the current when the filtering resolution is 5 bits
DSMIF_UPPER_LIMIT_6	(0xFC00u)	Upper limit of the current when the filtering resolution is 6 bits
DSMIF_UPPER_LIMIT_7	(0xFE00u)	Upper limit of the current when the filtering resolution is 7 bits
DSMIF_UPPER_LIMIT_8	(0xFF00u)	Upper limit of the current when the filtering resolution is 8 bits
DSMIF_UPPER_LIMIT_9	(0xFF80u)	Upper limit of the current when the filtering resolution is 9 bits
DSMIF_UPPER_LIMIT_10	(0xFFC0u)	Upper limit of the current when the filtering resolution is 10 bits
DSMIF_UPPER_LIMIT_12	(0xFFF0u)	Upper limit of the current when the filtering resolution is 12 bits
DSMIF_UPPER_LIMIT_14	(0xFFFCu)	Upper limit of the current when the filtering resolution is 14 bits

Table 6.7 Constants for Registers Used for DSMIF (2 / 2)

Constant	Value	Description
DSMIF_UPPER_LIMIT_15	(0xFFFEu)	Upper limit of the current when the filtering resolution is 15 bits
DSMIF_UPPER_LIMIT_16	(0xFFFFu)	Upper limit of the current when the filtering resolution is 16 bits
DSMIF_HVA_WRITE_DATA	(1u)	The value for the interrupt processing ending notification bit (HVA)
DSMIF_PIC_CLEAR_EDGE	(1u)	The value for clearing the edge detection state
ECM_ERROR_BIT_DSMIF_ALL	(0x7E000000u)	Mask ECM errors at initialization of the DSMIF (error sources 26 to 28, 30, 31 and the twenty-eight reserved bits).
ECM_ERROR_BIT_DSMIF_XYZ	(0x60000000u)	Mask, enable, or clear the X overcurrent/short-circuit abnormalities detection error (error sources 30 and 31).
MPC_PN6PFS_PSEL_MCLK3	(0x28u)	Specify the peripheral function assigned to the PN6 pin as MCLK3.
MPC_PN7PFS_PSEL_MDAT3	(0x28u)	Specify the peripheral function assigned to the PN7 pin as MDAT3.

Table 6.8 Constants Used in Configuration

Constant	Value	Description
DSMIF_XYZ_I_VALUE_MIN	(1u)	Set the lower limit for judging X overcurrent abnormality detection error.
DSMIF_XYZ_SHORT_CNT_1	(0x00001FFEu)	Set the threshold for the input of 0-value data for judging the detection of short-circuit abnormalities.
DSMIF_XYZ_SHORT_CNT_0	(0x00001FFEu)	Set the threshold for the input of 1-value data for judging the detection of short-circuit abnormalities.
DSMIF_ERROR_OFFSET	(1u)	Offset for setting the upper limit for judging the detection of X overcurrent abnormalities.
CMTW_CNT_MAX	(0x0047868Cu)	Set the timeout for compare match with the value of the timer counter (CMWCNT) in low-frequency scan mode.
CMTW_CNT_CAPTURE	(30u)	Set the interval for executing high-frequency scans.
BUFFER_CNT	(10000u)	Specify the size of the buffer which holds the values for current in high-frequency scanning.
SCIFA_HVA_WRITE_DATA	(0u)	The value for the interrupt processing ending notification bit (HVA)
STRING_SIZE	(1024)	Specify the size of the buffer (gbuff) which holds the data received from the terminal software.

6.6 Variables

The static type variables are listed in the table below.

Table 6.9 Static Type Variables

Type	Variable	Description
static char	gbuff[STRING_SIZE]	Data received from the terminal software
static uint8_t	scan_mode	Set the scan frequencies to high or low
static uint8_t	filter_set	Number of the specified filter stage (0 to 14)
static uint16_t	xdata_buf[BUFFER_CNT]	Buffer for storing the value for current to be read
static uint32_t	log_cnt	Counter for log data stored in the buffer
static bool	error_flag	DSMIF error flag
static bool	cmt_flag	Compare match completion flag
static bool	key_flag	Key input detection flag
static st_dsmif_filter_cfg_x1_t	filter_cfg_x1_t	Structure for storing the DSMIF filter setting of X1DATA: The filter setting of X1DATA is changed according to the setting stored in this structure.
static st_dsmif_filter_cfg_x2_t	filter_cfg_x2_t	Structure for storing the DSMIF filter setting of X2DATA: The filter setting of X2DATA is changed according to the setting stored in this structure.
static st_dsmif_errorx_t	dsmif_errx	Structure for storing the DSMIF error status: When an error occurred, the corresponding error status is stored in this structure.

6.7 Functions

The functions are listed in the table below.

Table 6.10 Functions

Type	Description
R_DSMIF_Init	Initial settings of the DSMIF
R_DSMIF_Start	Start filtering by the DSMIF.
R_DSMIF_Stop	Stop filtering by the DSMIF.
R_DSMIF_SetFilter	Change settings of the DSMIF filters.
R_DSMIF_ReadXData	Read the value for current from the DSMIF.
R_DSMIF_GetErrorStatus	Get the error source of the DSMIF.
scifa_set_intr_setting	Set the SCIFA interrupts.
scifa_enable_intr_reg	Enable the SCIFA interrupts.
scifa_disable_intr_reg	Disable the SCIFA interrupts.
main	Main function of the sample program

6.8 Function Specifications

Specifications of the functions used for the sample codes are described.

R_DSMIF_Init		
Synopsis	Initial settings of the DSMIF	
Declaration	void R_DSMIF_Init (void (*pcallback)(void));	
Description	This function makes the following initial settings of the DSMIF. Set the DSMIF to the slave mode Mask ECM error sources Release the DSMIF from the module-stop state Initialize the DSMIF registers Set ports to input or output	
Argument	void (*pcallback)(void)	A pointer to the DSMIF error callback function
Returned Value	None	
Remark	None	

R_DSMIF_Start	
Synopsis	Make necessary settings to start filtering by the DSMIF.
Declaration	void R_DSMIF_Start(void);
Description	This function makes the following settings necessary to start filtering (monitoring the value for current) by the DSMIF. Start filtering by the DSMIF Wait for the filter to start operating Set the DSMIF error conditions Enable ECM error interrupts
Argument	None
Returned Value	None
Remark	None

R_DSMIF_Stop	
Synopsis	Make necessary settings to stop filtering by the DSMIF.
Declaration	void R_DSMIF_Stop(void);
Description	This function makes the following settings necessary to stop filtering (monitoring the value for current) by the DSMIF. Disable ECM error interrupts Stop filtering by the DSMIF
Argument	None
Returned Value	None
Remark	None

R_DSMIF_SetFilter		
Synopsis	Change the DSMIF filter setting	
Declaration	void R_DSMIF_SetFilter(uint8_t x1_setting, uint8_t x2_setting);	
Description	This function is used to change the following settings of the DSMIF filter: SINC filter stage Decimation clock Bit shift	
Argument	uint8_t x1_setting	Select the filter setting to be applied to X1DATA: DSMIF_FILTER_SET_0 to DSMIF_FILTER_SET_14 See Table 6.1 Allowed Combinations of Filters for the setting values.
	uint8_t x2_setting	Select the filter setting to be applied to X2DATA: DSMIF_FILTER_SET_0 to DSMIF_FILTER_SET_14 See Table 6.1 Allowed Combinations of Filters for the setting values.
Returned Value	None	
Remark	If the values outside the predetermined range are specified in the arguments, DSMIF_FILTER_SET_0 is set instead. The same values are set in X1DATA and X2DATA in this sample program.	

R_DSMIF_ReadXData		
Synopsis	Read the value for current filtered through the DSMIF	
Declaration	uint16_t R_DSMIF_ReadXData(uint8_t data_reg);	
Description	This function reads the 16-bit digital data that were converted through the DSMIF filter from the specified register. The value for current is read from either of the following registers specified by the argument: Channel X current value register (X1DATA) Channel X current value register (X2DATA)	
Argument	uint8_t data_reg	Select the register to read the value for current from: DSMIF_READ_X1: X1DATA is selected DSMIF_READ_X2: X2DATA is selected
Returned Value	uint16_t read_data: The value for current that was read	
Remark	The returned value is undefined if the value outside the predetermined range is specified in the argument. X2DATA for judging detection of overcurrent abnormality error is selected in this sample program for error detection.	

R_DSMIF_GetErrorStatus	
Synopsis	Get the error source generated while the DSMIF is running.
Declaration	uint8_t R_DSMIF_GetErrorStatus(void);
Description	This function acquires the error source for the following errors occurred while the DSMIF is running: X overcurrent abnormality detection error X short-circuit abnormality detection error
Argument	None
Returned Value	Detected error source is returned. DSMIF_ERR_ERIX (1): X overcurrent abnormality detection error DSMIF_ERR_ERXSC (2): X short-circuit abnormality detection error
Remark	None

scifa_set_intr_setting		
Synopsis	Set the SCIFA interrupts.	
Declaration	void scifa_set_intr_setting (void (*pcallback)(void));	
Description	This function enables the SCIFA key input interrupts by the following settings: Register the interrupt callback functions Register the reception FIFO data full interrupt handler	
Argument	void (*pcallback)(void)	A pointer to the callback function for the SCIFA key input interrupt
Returned Value	None	
Remark	None	

scifa_enable_intr_reg	
Synopsis	Enables the SCIFA interrupt.
Declaration	void scifa_enable_intr_reg(void);
Description	This function enables reception FIFO data full interrupt
Argument	None
Returned Value	None
Remark	None

scifa_disable_intr_reg	
Synopsis	Disables the SCIFA interrupt.
Declaration	void scifa_disable_intr_reg(void);
Description	This function disables reception FIFO data full interrupt
Argument	None
Returned Value	None
Remark	None

main	
Synopsis	Main function of the sample program
Declaration	int main (void)
Description	This is the main function of the sample program.
Argument	None
Returned Value	None
Remark	None

6.9 Flowcharts of the Functions

6.9.1 Main Function

Figure 6.1 is a flowchart of the main function.

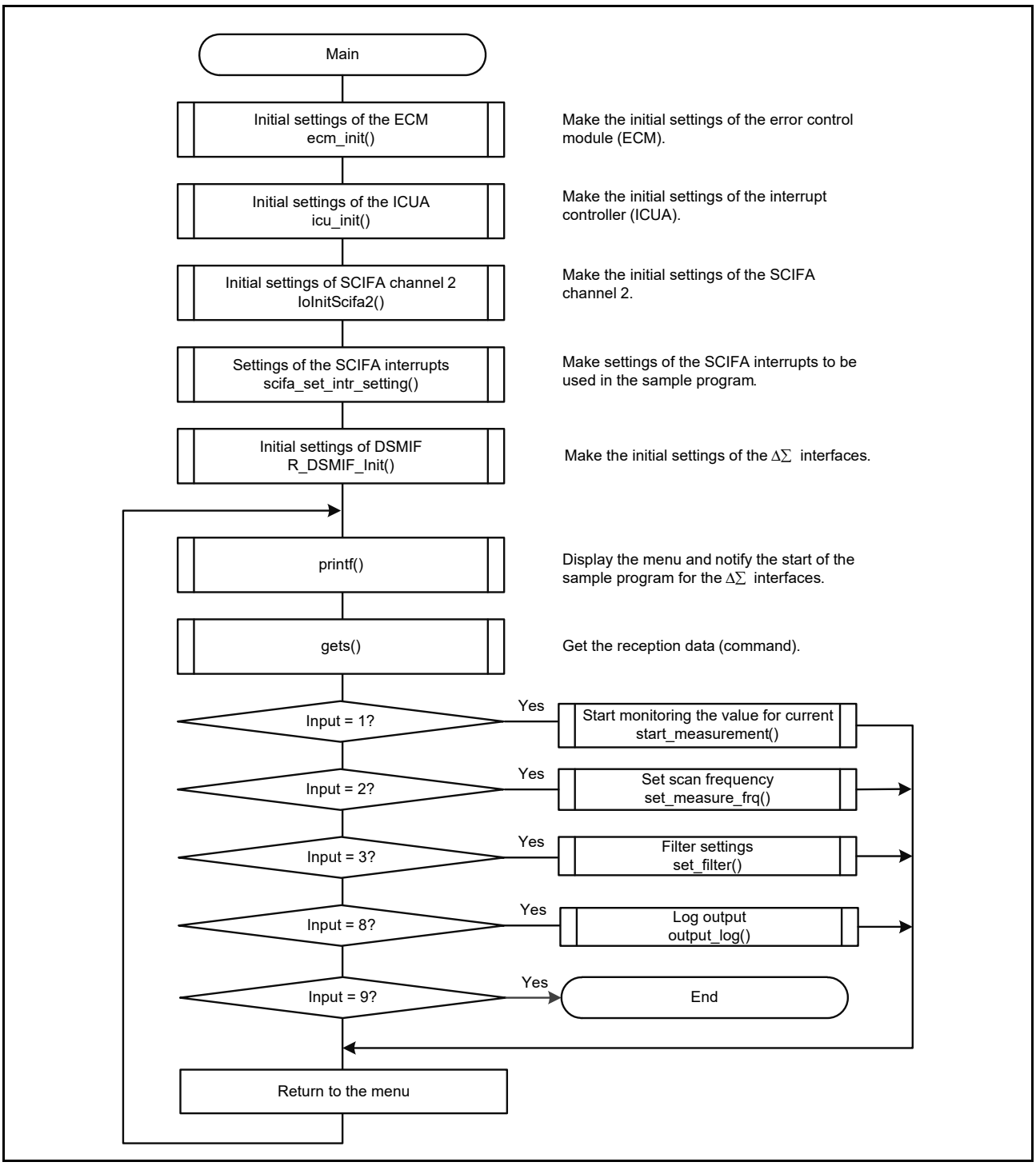


Figure 6.1 Flowchart of Main Function

6.10 Sample Program Operation

This section describes the operation of the sample program in a terminal software on a host PC.

6.10.1 Setting Projects

Details on configuration of the projects used in the development environments EWARM, DS-5, and e^{2}studio are described in *RZ/T1 Group Application Note: Initial Settings*.

Note: If this sample program is to be compiled as a project for the kptgcc compiler, the address where the .data section starts in NOR boot mode must be changed from 0x7F000 to 0x78000.

6.10.2 Connecting Boards

Demonstrations of this sample program require the PS9352A sub-board. Connect the PS9352A sub-board to the RZ/T1 evaluation board (RTK7910018C00000BE) as illustrated in Figure 5.2. Then, supply the following voltages to the PS9352A sub-board by referring to Figure 6.2.

VDD and GND pins:	Connect to the input power supply (5 V).
Vin+ pin:	Connect to the power supply of the device to be evaluated (0 V to 200 mV). (GND for evaluating load voltage.)
Vin- pin:	Connect to the GND of the device to be evaluated (0 V to 200 mV). (0 V to 200 mV for evaluating load voltage.)

Note: Supply voltages to these pins only after the power to the RZ/T1 evaluation board (RTK7910018C00000BE) has been supplied.

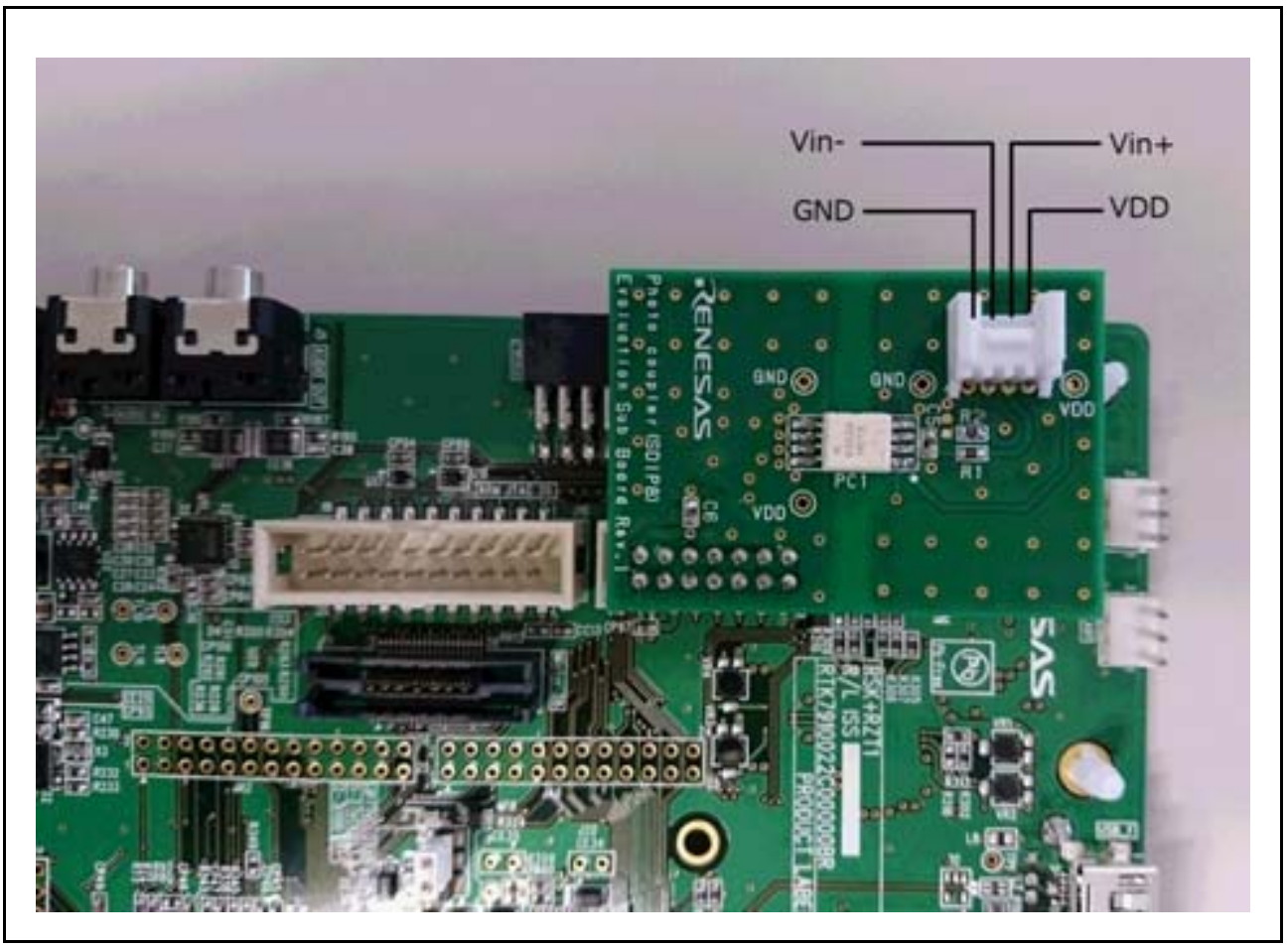


Figure 6.2 Voltages Input to PS9352A Sub-board

6.10.3 Preparation

The sample program requires communications with a host PC. Preparation for this is described below with TeraTerm as the terminal program.

(1) Startup the terminal software on the host PC. Configure the serial port as shown below. When COM3 is used for Tera Term:

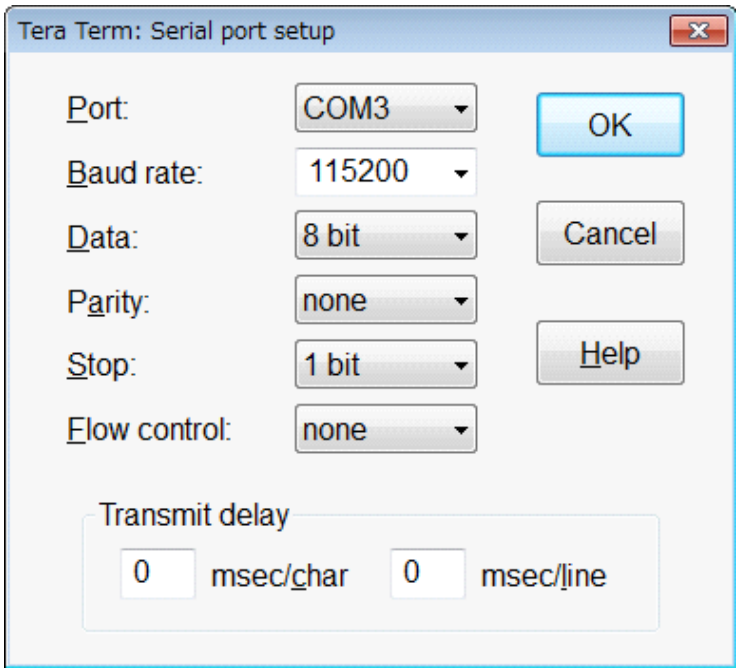


Figure 6.3 Configuration of the Serial Port

(2) When the program is executed and ready for making communications, the menu appears on the terminal software as shown below.

.

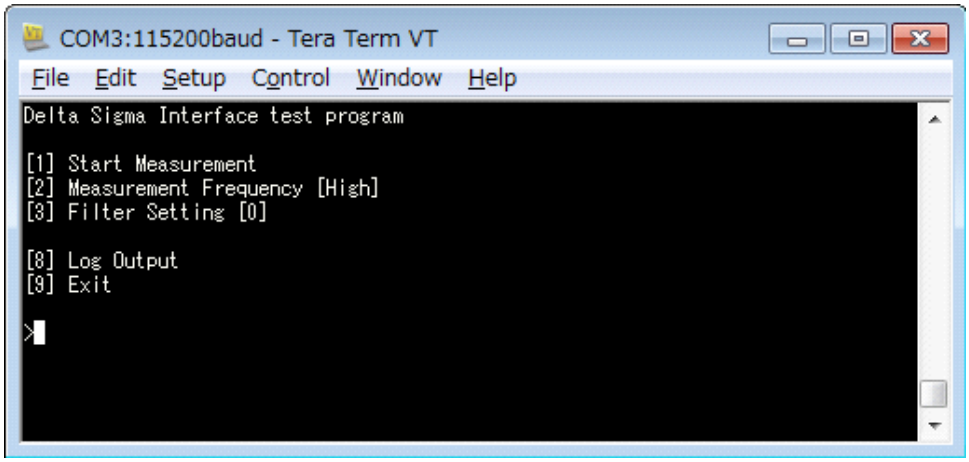


Figure 6.4 Terminal Software Screen after Execution of the Sample Program

6.10.4 Monitoring Values for Current

The value for current is converted to a 16-bit value through filtering. The value is measured as follows.

By selecting [1] from the menu shown in Figure 6.4, monitoring of the value for current starts with the specified scanning frequency and filter settings.

```
Delta Sigma Interface test program

[1] Start Measurement
[2] Measurement Frequency [High]
[3] Filter Settings [0]

[8] Log Output
[9] Exit

>1[Enter]

<start>
33792
```

(1) High-frequency scan mode

In this mode, 10,000 scans procced in less than one second. The log of the results is displayed at once. When the log has ended, the menu appears again.

```
<start>
33792
33280
  .
  .
32128
<end>

Delta Sigma Interface test program

[1] Start Measurement
[2] Measurement Frequency [High]
[3] Filter Settings [0]

[8] Log Output
[9] Exit

>
```

(2) Low-frequency scan mode

In this mode, the values for current are scanned every two seconds. The log of the results is displayed after each scan. Pressing any key stops the scanning and redisplays the menu.

```
<start>
34048
32512
33408
34304
33792
[Key input]
<end>

Delta Sigma Interface test program

[1] Start Measurement
[2] Measurement Frequency [Low]
[3] Filter Settings [0]

[8] Log Output
[9] Exit

>
```

(3) When an error is detected

If an error (X overcurrent abnormality detection error or X short-circuit abnormality detection error) occurred while the value for current were being monitored, the ongoing monitoring is stopped. After the type of error is displayed, the menu is redisplayed.

```
<start>
58496
63232
59392
62336
CHANNEL X OVER CURRENT ERROR
<end>

Delta Sigma Interface test program

[1] Start Measurement
[2] Measurement Frequency [High]
[3] Filter Settings [0]

[8] Log Output
[9] Exit

>
```

6.10.5 Setting Scan Frequency

Select [2] from the menu to change the frequency of scanning.

Select the number 1 or 2 for the required frequency.

If you want to exit without changing the frequency, press [Enter] without specifying a number.

In the example below, [2], Low Frequency is selected.

```
  >2[Enter]

  Input the number to select the measurement mode.

  [1] High Frequency
  [2] Low Frequency

>2[Enter]
```

A message indicating that the setting was changed is displayed. The menu then appears again.

You can confirm that the setting is reflected in the menu.

```
> 2

Set to Low frequency mode.

Delta Sigma Interface test program

[1] Start Measurement
[2] Measurement Frequency [Low]
[3] Filter Settings [0]

[8] Log Output
[9] Exit

>
```

6.10.6 Filter Settings

Select [3] from the menu to change the filter settings.

Select the number from 0 to 14 for the combination of required settings for the filter. See Table 6.1 Allowed Combinations of Filters for the setting values.

If you want to exit without changing the filter settings, press [Enter] without specifying a number.

In the example below, [5] (three-stage filter, decimation clock, MCLK3/256, bit shift [23:8]) is selected.

```
>3[Enter]

Input the number to set the filter (0-14)

                    WORD1GEN[2:0]or    BITSHIFT1[3:0]or
     SINC filter    WORD2GEN[2:0]      BITSHIFT2[3:0]
-----------------------------------------------------------
[0]    3(sinc3)         010b               1000b
[1]    3(sinc3)         011b               0110b
[2]    3(sinc3)         100b               0100b
[3]    3(sinc3)         101b               0010b
[4]    3(sinc3)         110b               0001b
[5]    3(sinc3)         111b               0000b
[6]    2(sinc2)         011b               1001b
[7]    2(sinc2)         100b               0111b
[8]    2(sinc2)         101b               0110b
[9]    2(sinc2)         110b               0101b
[10]   2(sinc2)         111b               0011b
[11]   1(sinc1)         100b               1100b
[12]   1(sinc1)         101b               1011b
[13]   1(sinc1)         110b               1010b
[14]   1(sinc1)         111b               1001b

>5
```

A message indicating that the setting was changed is displayed. The menu then appears again.

You can confirm that the setting is reflected in the menu.

```
> 5

Set to 5.

Delta Sigma Interface test program

[1] Start Measurement
[2] Measurement Frequency [Low]
[3] Filter Settings [5]

[8] Log Output
[9] Exit

>
```

6.10.7 Log Output

Selecting [8] from the menu outputs the log of the results of scanning, i.e., latest values for current. 10 logged values are displayed per line.

```
> 8[Enter]

Log Output
-----------------------------------------------------------------
[1] 35686 35686 32791 32779 32779 32752 32752 32661 32721 32721
[11] 32727 32727 32738 32733 32733 32736 32736 32729 32731 32731
[21] 32726 32726 32716 32723

Delta Sigma Interface test program

[1] Start Measurement
[2] Measurement Frequency [Low]
[3] Filter Settings [5]

[8] Log Output
[9] Exit

>
```

7. Notes Regarding Precision

7.1 Effects of Filter Characteristics on the Precision of Conversion

When the filter settings increase the division ratio of the decimation clock, this extends the time for operations by the filter, resulting in longer times for integration and a higher meaningful resolution.

Though the results of conversion are not updated as frequently, the meaningful resolution is higher, so the absolute precision of the results of conversion will be higher.

The figure below shows the effect of the decimation period on the filter's output.

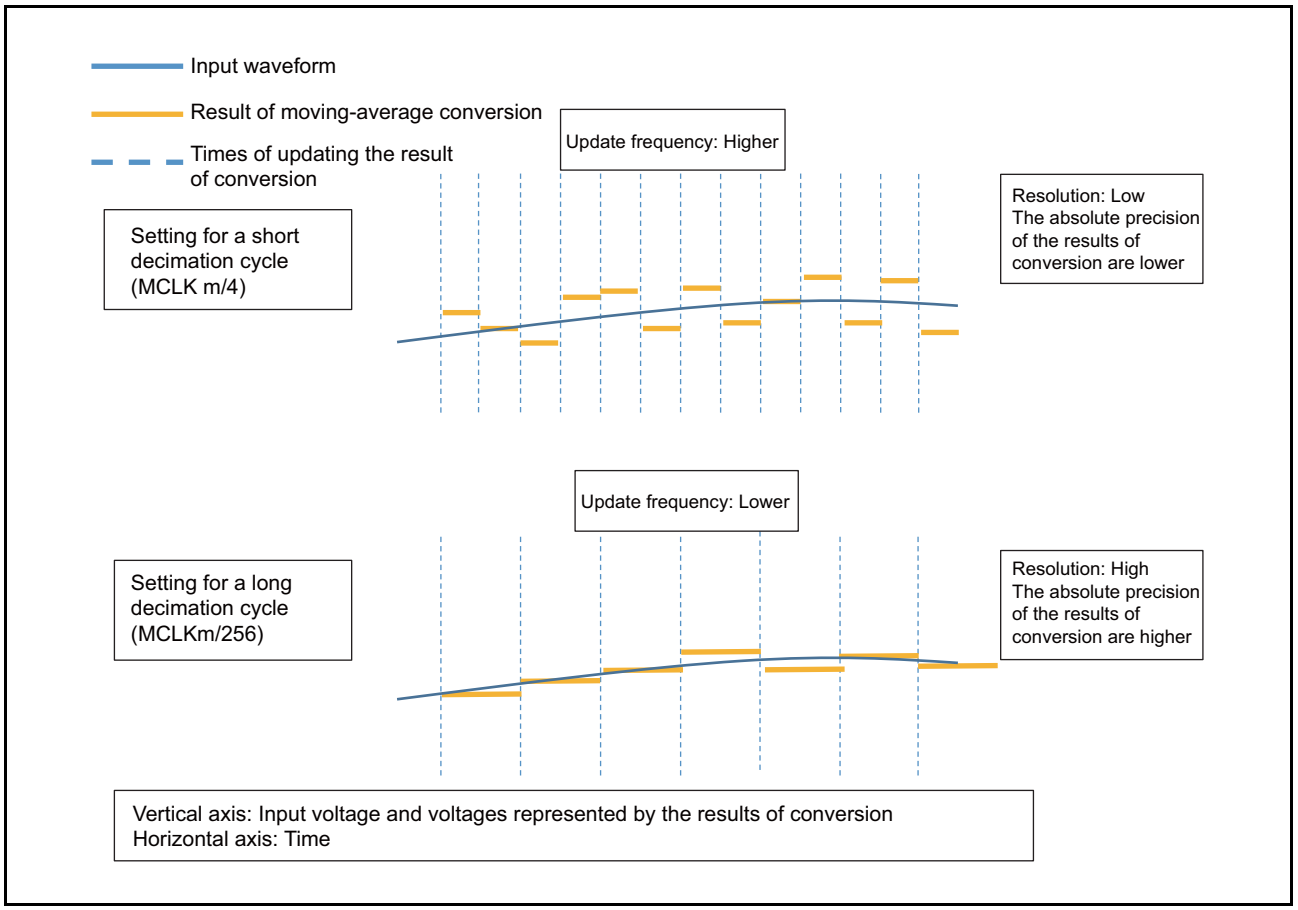


Figure 7.1 Effects of Filter Characteristics on Precision

A higher meaningful resolution generally gives the results of conversion a higher precision, so that they more closely approximate the input waveform.

However, since the results of conversion result are updated less frequently, if the state of the input is subject to sudden changes (the input waveform has high-frequency components), changes in the input cannot be tracked, which lowers the average precision of the results of conversion over the timespan each result covers.

Therefore, when the input waveform has high-frequency components, setting a shorter decimation cycle shorter may improve the precision in general.

The figure below shows the effect of the decimation period on the output of the filter for an input waveform with relatively higher and lower frequencies relative to the decimation period.

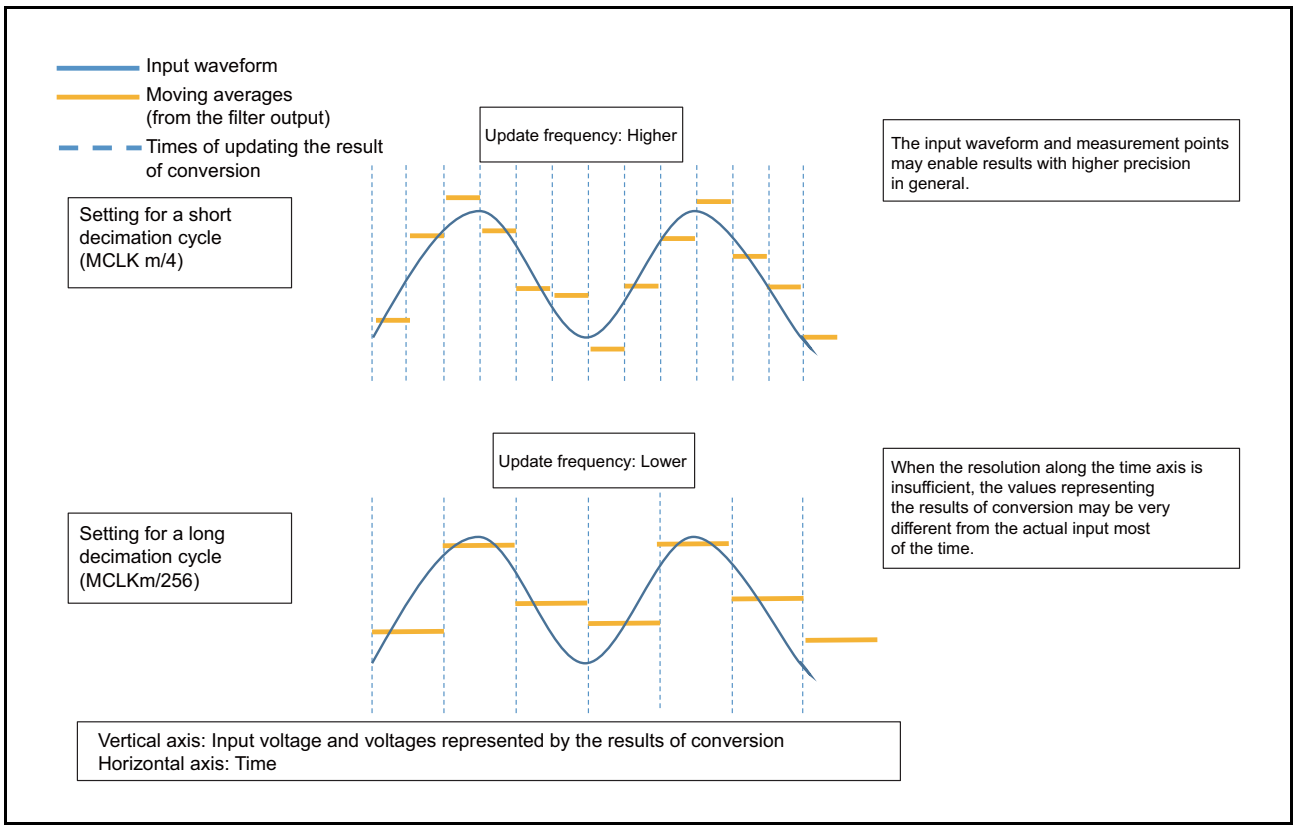


Figure 7.2 Effects of Filter Characteristics on Precision when the Frequency of the Input Waveform is Higher and Lower Relative to that of Decimation

7.2 Effects of Capturing Cycles of the Current Value Register

- The values for current derived from the DSMIF filter output are stored and updated in the current value register in synchronization with the decimation clock, which is a signal derived by frequency division of MCLK.
  For example, if the setting is MCLKm/256, the current value register is updated per 256 counts of MCLK.
- On the other hand, results in the current value register can be acquired without synchronization with the decimation clock; the results are acquired by reading by the CPU or capture in response to a valley/trough trigger from a timer (MTU3a or GPTa) in the PWM mode.
  In this sample program, reading by the CPU proceeds with a specified interval produced by the CMT timer.
- Since the timing of updating is not necessarily synchronized with that of acquisition of the current values, even if the current values are acquired with a specified period, there may be slight deviations as shown below.

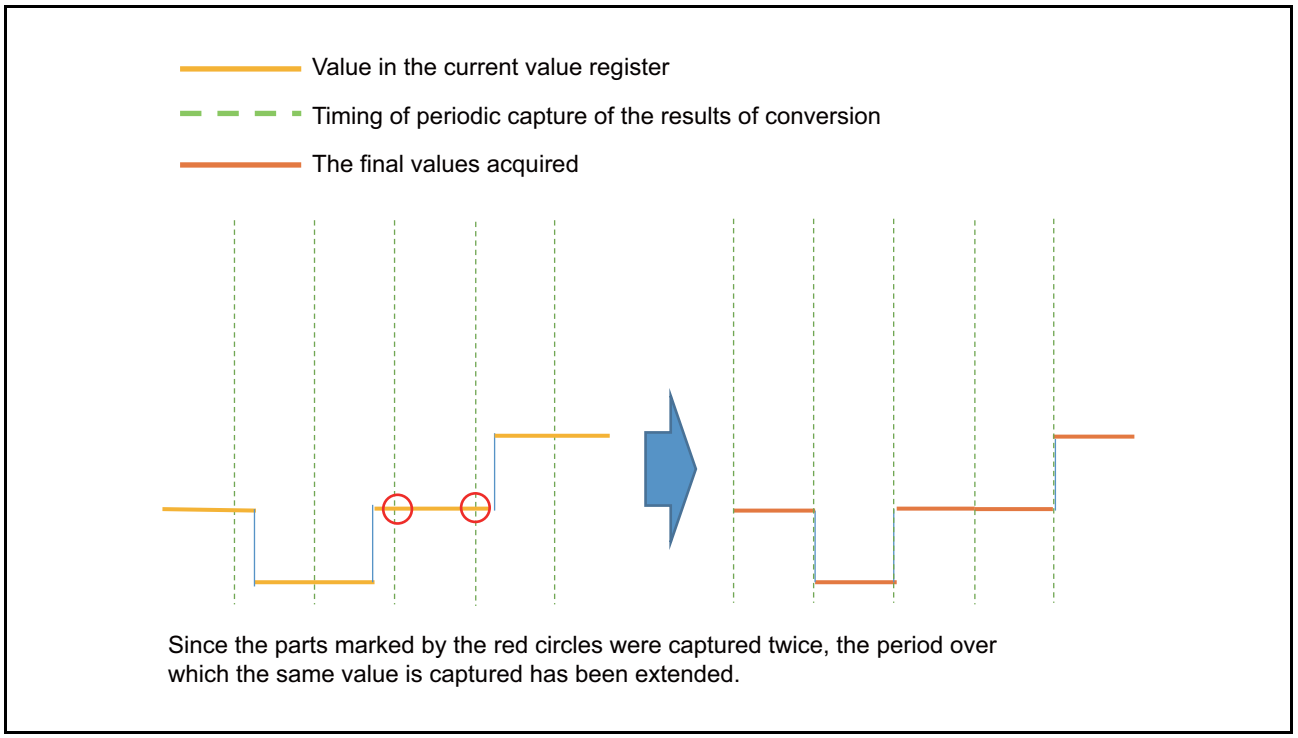


Figure 7.3 Waveform Distortion due to Differences in Timing between Updating of the Filter Output and Capturing Values

8. Sample Code

The sample code is available from the Renesas Electronics website.

9. Reference Documents and Development Environments

- User's Manual: Hardware
  RZ/T1 Group User's Manual: Hardware
  (Download the latest version of the manual from the Renesas Electronics website.)

- RZ/T1 Evaluation Board RTK7910018C00000BE User's Manual
  (Download the latest version of the manual from the Renesas Electronics website.)

- Technical Update / Technical News
  (Download the latest version of the update or news from the Renesas Electronics website.)

- IAR integrated development environment
  For the IAR Embedded Workbench® for Arm, download the latest version from the IAR Systems website.

- Arm integrated development environment
  For the Arm Compiler toolchain, Arm Development Studio 5 (DS-5TM), etc., download the latest version from the Arm ltd. website

- Renesas integrated development environment
  For the e2 studio, download the latest version from the Renesas Electronics website.
  For the compiler and toolchain (GNUARM-NONE), download the latest version from the GNU Tools and Support website (https://gcc-renesas.com/).

- PS9352A sub-board for the RZ/T1 evaluation board
  For the PS9352A sub-board for the RZ/T1 evaluation board, please contact one of the Renesas Electronics distributors in your area. (see Section 10.).

10. Website and Support

Renesas Electronics website

http://www.renesas.com/

Inquiries

http://www.renesas.com/contact/

Revision History	Application Note: ΔΣ Interface (DSMIF) Sample Program

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 13, 2017	—	First Edition issued
1.10	Sep. 14, 2017	2. Operating Environment	
		5	Table 2.1 Operating Environment, modified
		6. Software	
		24	6.10.3 Preparation, description added
1.20	Jun. 07, 2018	2. Operating Environment	
		5	Table 2.1 Operating Environment: The description on the integrated development environment, modified
		9. Reference Documents and Development Environments	
		34	"ARM" changed to "Arm"

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0