RZ/A2M Group

Guidelines for LVDS and MIPI Board Design

Introduction

This application note describes the guidelines for designing boards when LVDS or MIPI is used.

Target LSIs

RZ/A2M group

Notes: The contents in this application note are reference examples, and signal quality in the system is not guaranteed. When incorporated into an actual system, sufficient verification and evaluation of the system overall should be performed, and determination of applicability is the customer's responsibility. "Group" will be omitted in the rest of this application note.

Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- RZ/A Series Hardware Design Guide (R01AN4813EJ)

Contents

1. Introduction

1.1 LVDS

The RZ/A2M LVDS Output Interface is an interface that provides 4-pair (3 data pairs, 1 clock pair) differential output that conforms to the TIA/EIA-644 standard.

Figure 1.1 shows an outline of LVDS connection diagram and Table 1.1 shows the LVDS Output Interface pins.

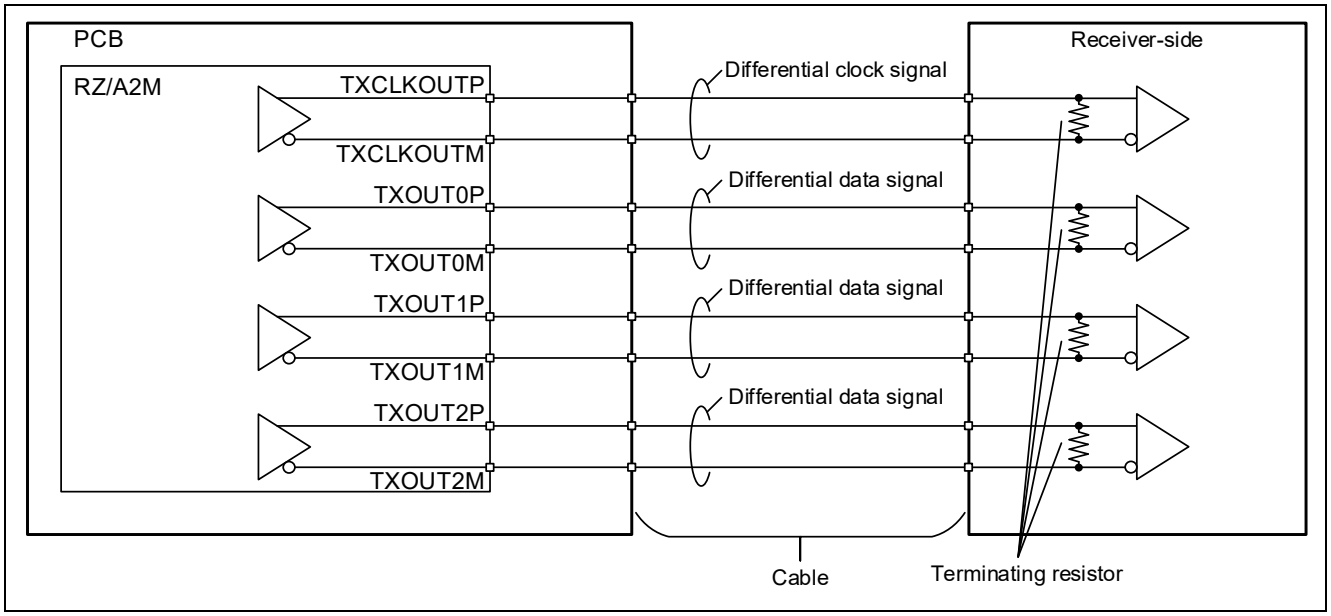


Figure 1.1 Outline of LVDS connection diagram

Table 1.1 LVDS Output Interface pins

Name	Pin Name	Input/Output	Function
LVDS data output pin 0P	TXOUT0P	Output	LVDS differential data output pins
LVDS data output pin 0M	TXOUT0M	Output	
LVDS data output pin 1P	TXOUT1P	Output	
LVDS data output pin 1M	TXOUT1M	Output	
LVDS data output pin 2P	TXOUT2P	Output	
LVDS data output pin 2M	TXOUT2M	Output	
LVDS CLK output pin CP	TXCLKOUTP	Output	LVDS differential clock output pins
LVDS CLK output pin CM	TXCLKOUTM	Output	
LVDS analog power supply pin	LVDSAPVcc	Input	Power supply for LVDS output (Typ.3.3V)
LVDS PLL power supply pin	LVDSPLLVcc	Input	Power supply for LVDS PLL (Typ.1.2V)

1.2 MIPI

The RZ/A2M MIPI CSI2 Interface is a MIPI CSI-2 receiver module that supports MIPI CSI-2 V1.1 and MIPI D-PHY V2.0. The RZ/A2M MIPI CSI2 Interface has a built-in terminating resistor, so an external terminating resistor is not required.

Figure 1.2 shows an outline of MIPI connection diagram and Table 1.2 shows the MIPI CSI2 Interface pins.

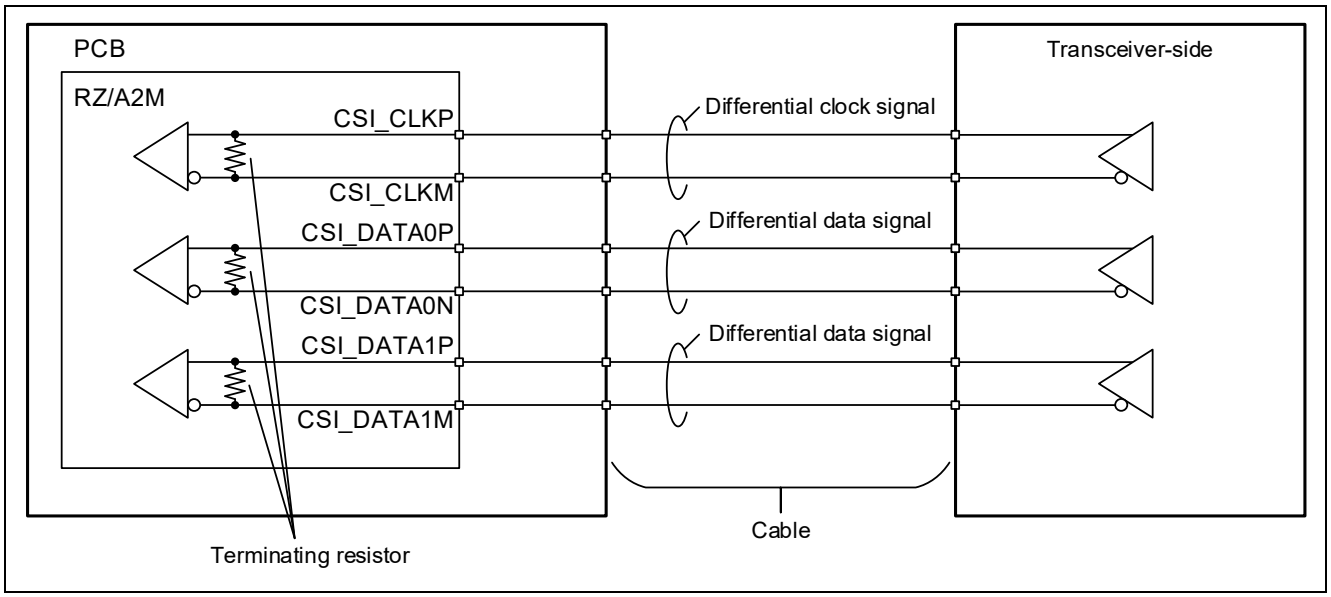


Figure 1.2 Outline of MIPI connection diagram

Table 1.2 MIPI CSI2 Interface pins

Name	Pin Name	Input/Output	Function
Lane 0 positive data pin	CSI_DATA0P	Input	MIPI differential data input pins
Lane 0 negative data pin	CSI_DATA0N	Input	
Lane 1 positive data pin	CSI_DATA1P	Input	
Lane 1 negative data pin	CSI_DATA1N	Input	
Clock lane positive data pin	CSI_CLKP	Input	MIPI differential clock input pins
Clock lane negative data pin	CSI_CLKN	Input	
MIPI analog power supply pin	MIPIAVcc18	Input	Power supply for the MIPI analog circuits (Typ.1.8V)

Note: There are no MIPI CSI2 Interface pins on the 176 pin BGA package.

2. Transmission Lines

The transmission lines are expressed as the wiring pattern that connects RZ/A2M to the LVDS connector and the wiring pattern that connects RZ/A2M to the MIPI connector.

The maximum transmission speed is 609 Mbps/1 channel for LVDS, and 1 Gbps/1 lane for MIPI, so it is necessary to design the transmission lines as a high frequency circuit. Impedance control is necessary for the transmission lines.

Notes on designing the transmission line are described below.

- The characteristic impedance required in transmission lines is a differential impedance of 100 Ω ± 20%.
- The impedance control requires different pattern width and pattern interval according to board thickness, material, and layer configuration. For details, consult the board manufacturer.
- The routing of transmission lines should be short and isometric as much as possible. At this point, not only the wiring length of differential pairs of positive signal line and negative signal line but also all the wiring lengths of all data differential pairs and a clock differential pair should be isometric.
- If a transmission line must turn, do not use sharp angles (right angles), instead use a gentle turn of 135° or a circular arc.
- As far as possible, transmission lines should be allocated on the same layer without vias and laid out on the surface.
- If vias are used, limit the number of vias as much as possible, and make the numbers of vias on the positive and negative signal lines in each of data differential pairs and a clock differential pair the same.
- Also, ensure that stubs are not formed due to vias. Figure 2.1 shows an example of stub formation due to vias.
- At both sides of transmission line vias, allocate symmetrical ground vias. Figure 2.2 shows examples of ground vias placement.
- The lower layer of transmission line must be a ground plane. Do not divide the plane with slits, etc. Figure 2.3 shows examples of ground planes under the transmission lines.
- The components for the EMI/ESD protection must be compatible with all interfaces. Also, by mounting EMI/ESD protection components, an inconsistent impedance may occur on the transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.
- Appropriate spacing between a transmission line and adjacent ground patterns or signal lines is necessary. Table 2.1 shows the recommended spacing value between the transmission lines and adjacent patterns. Figure 2.4 shows examples of spacing between the transmission line and adjacent patterns, and Figure 2.5 shows examples of transmission line pattern design.

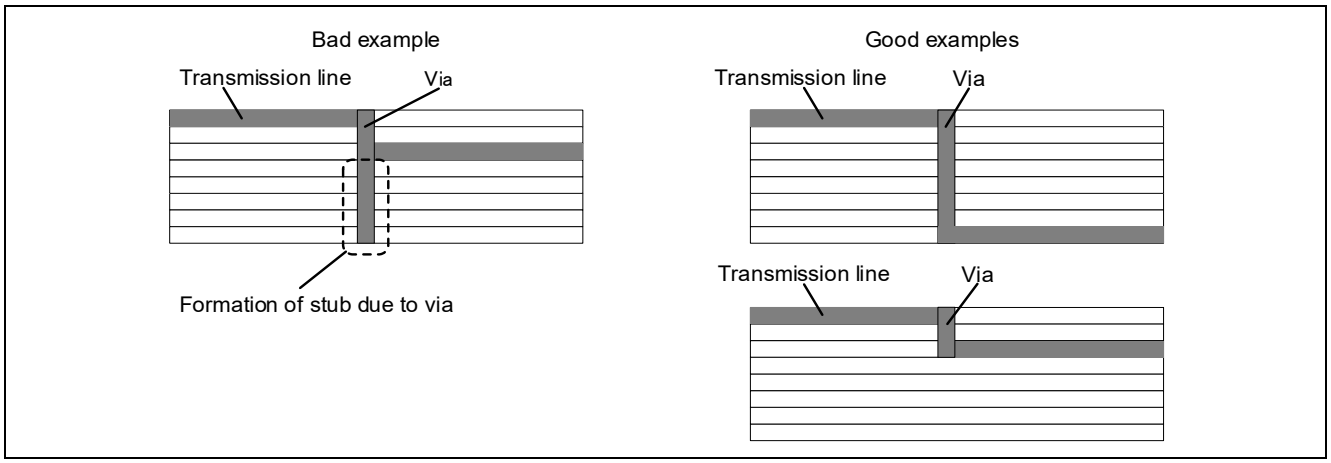


Figure 2.1 Formation of stubs by vias

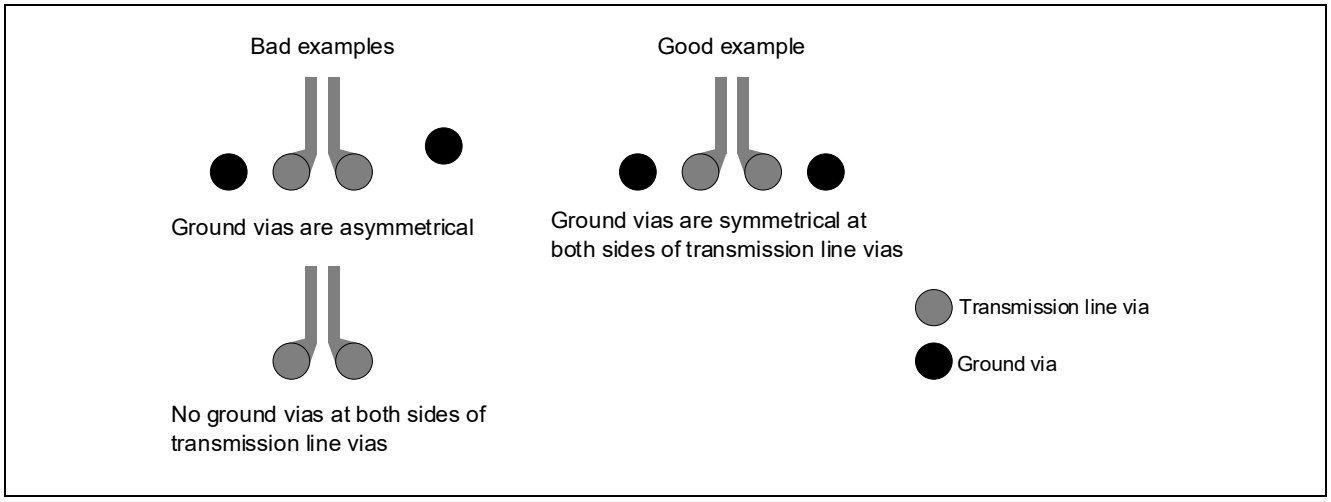


Figure 2.2 Examples of ground vias placement

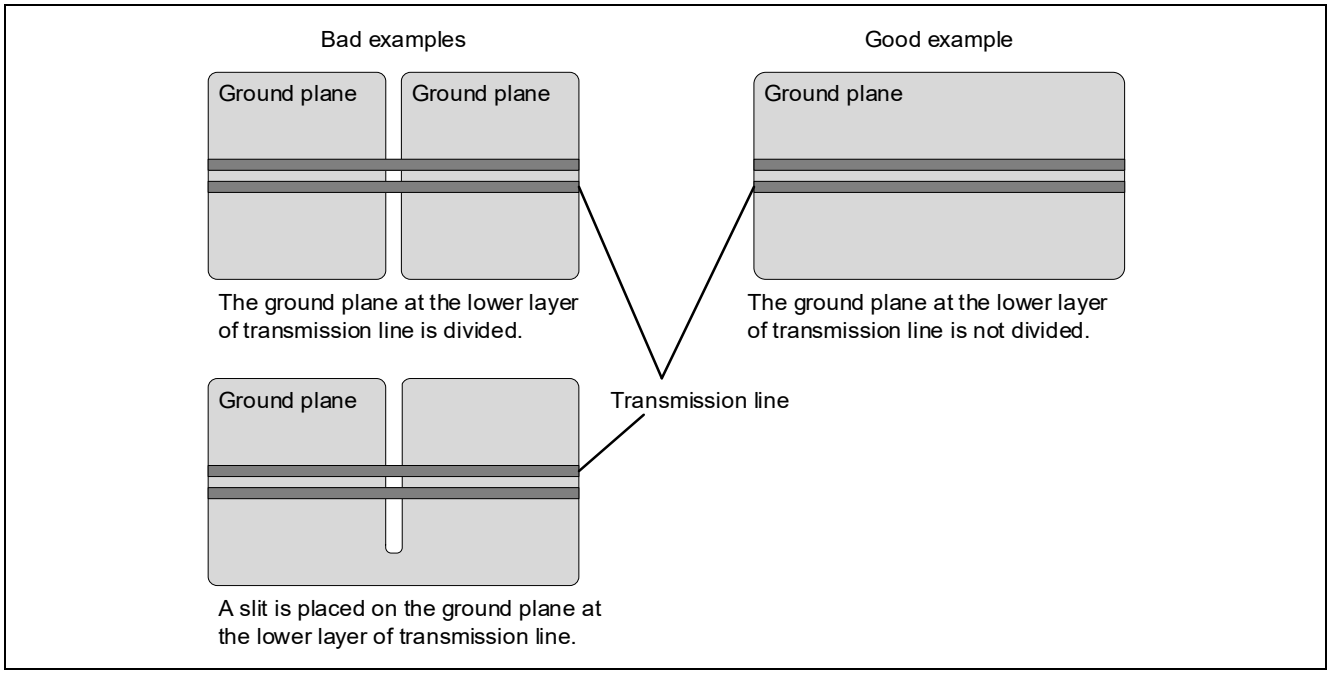


Figure 2.3 Examples of ground plane under transmission lines

Table 2.1 Recommended spacing values between the transmission lines and adjacent patterns

Item	Value
Spacing between differential pair and ground guard	S or more
Spacing to adjacent differential pair	3S or more*1
Spacing between differential pair and adjacent another signal line	3S or more*2

Notes: Spacing between positive signal line and negative signal line is S.
*1. Value when no ground pattern between differential pairs.
*2. Value when no ground pattern between differential pair and another signal line.

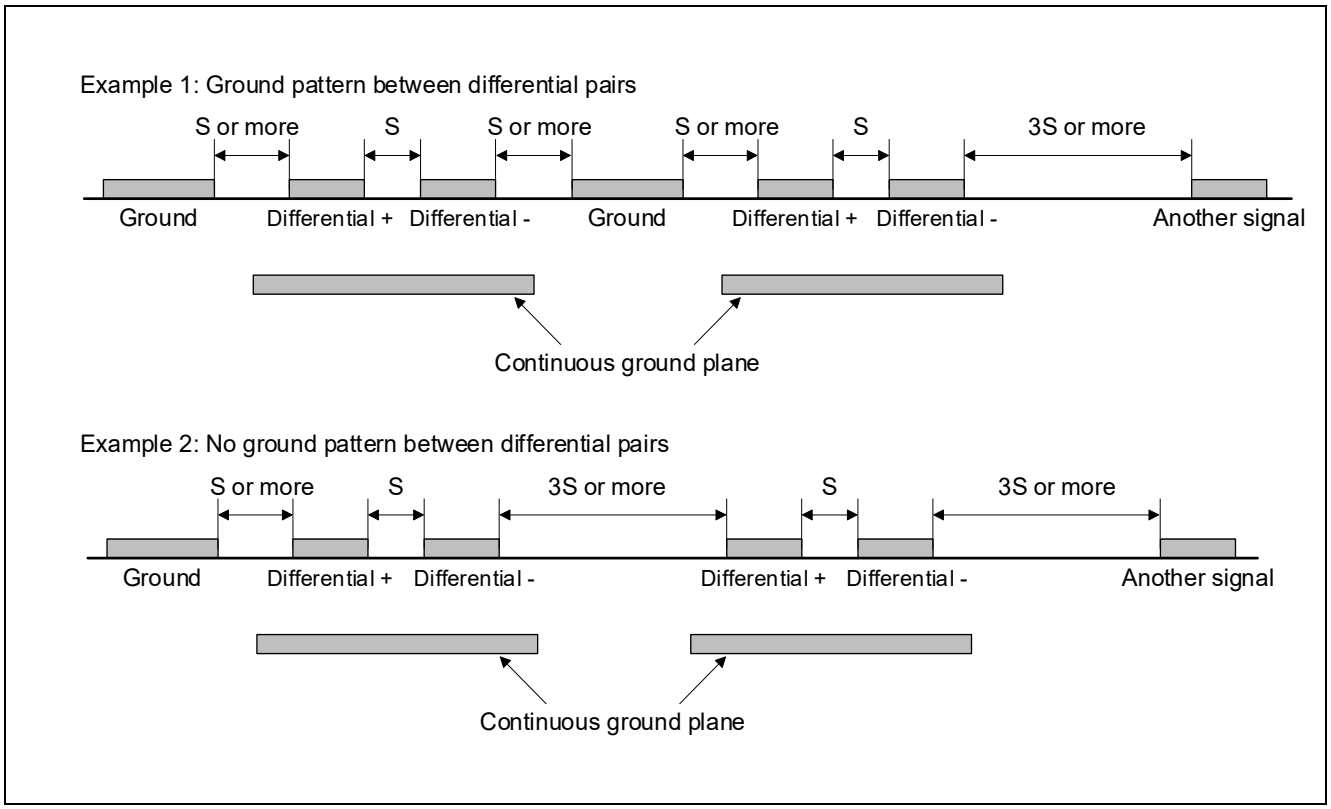
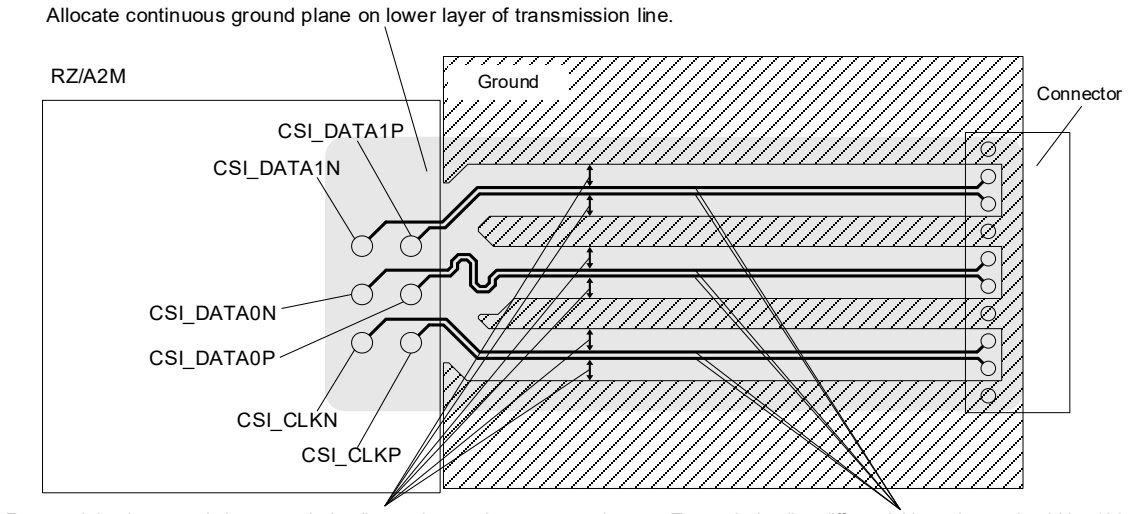


Figure 2.4 Examples of spacing between transmission line and adjacent patterns

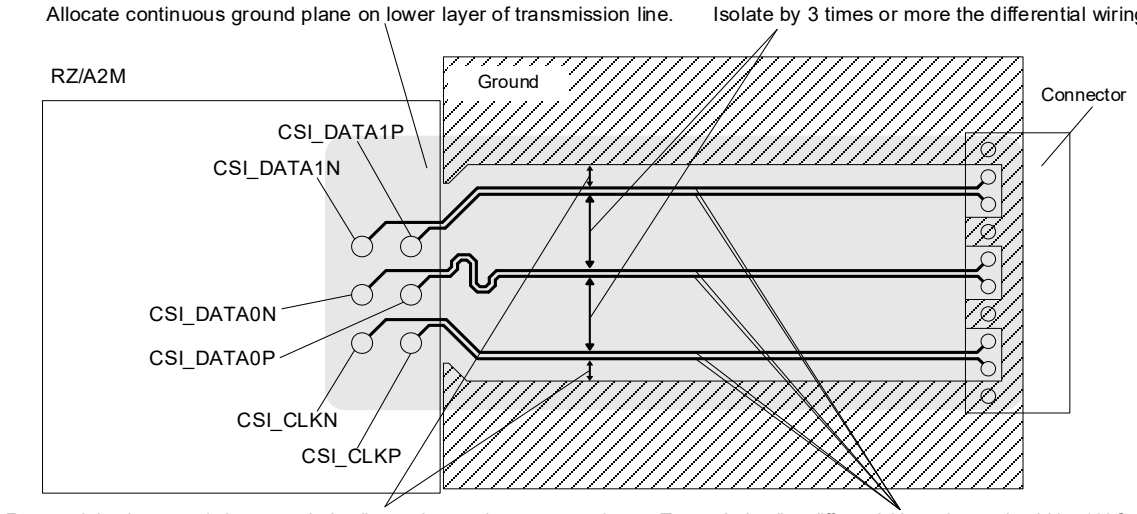
Example 1: Ground pattern between differential pairs



For guard ring by ground, the transmission line and ground pattern must be isolated by the same or greater spacing between the differential wiring.

Transmission line differential impedance should be 100 Ω ± 20%.
Transmission lines should be short and isometric as much as possible.

Example 2: No ground pattern between differential pairs



For guard ring by ground, the transmission line and ground pattern must be isolated by the same or greater spacing between the differential wiring.

Transmission line differential impedance should be 100Ω ± 20%.
Transmission lines should be short and isometric as much as possible.

Figure 2.5 Examples of transmission line pattern design

3. Power Supply Line

The LVDS and MIPI power supply must be isolated from the other RZ/A2M power supplies.

Allocate the bypass capacitor located near the power supply pin. Pay attention to the power supply line's wiring resistance and wiring inductance. Figure 3.1 shows a power supply pin connection diagram and pattern example, Table 3.1 shows the power supply line resistance values, inductance values and bypass capacitor values.

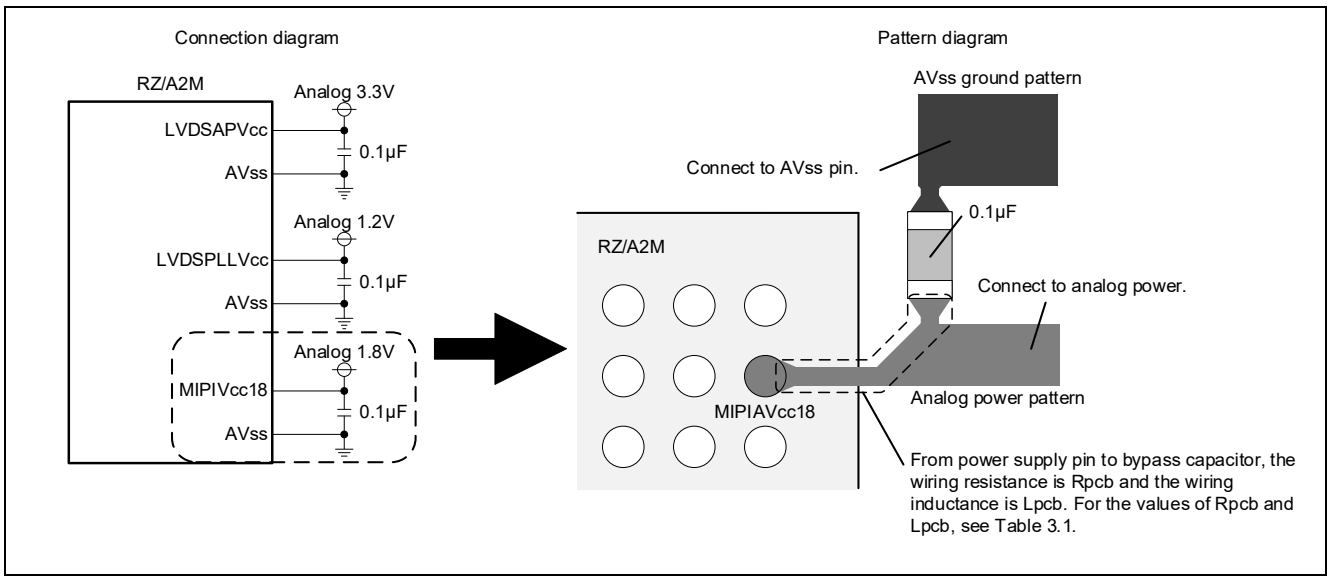


Figure 3.1 Example of power supply pin connection diagram and pattern

Table 3.1 Resistance values, inductance values, and bypass capacitor values of power supply line

Item	LVDS	MIPI
Rpcb	30 mΩ or less	30 mΩ or less
Lpcb*1	3.5 nH or less	4.6 nH or less
Bypass capacitor	0.1 µF	0.1 µF

Note: *1. Use the smallest possible value.
Does not include the inductance component of the bypass capacitor.
The wiring inductance component varies in accordance with the board material and pattern width. For details, consult the board manufacturer.

4. Checklist

Table 4.1 Checklist 1 (circuit diagram)

Item Number	Check Items (circuit diagram)	✔	Reference
1	When using MIPI, are external terminating resistors not attached?		1.2
2	Is the connection to the connector correct?		-
2-1	Is the polarity of the differential pairs connection correct?		-
2-2	Are the channels/lanes correct?		-
3	Is the treatment of pins correct?		-
3-1	Are the voltages for each power supply pin correct? (Are there no unconnected power supply pins?) LVDSAPVcc: 3.3 V LVDSPLLVcc: 1.2 V MIPIAVcc18: 1.8 V		Table 1.1 Table 1.2
3-2	Is there a 0.1 µF bypass capacitor for each power supply pin?		Table 3.1
4	Is power supply isolated?		-
4-1	When using LVDS, are the LVDSAPVcc and other power supplies isolated?		3
4-2	When using LVDS, are the LVDSPLLVcc and other power supplies isolated?		
4-3	When using MIPI, are the MIPIAVcc18 and other power supplies isolated?		

Table 4.2 Checklist 2 (pattern diagram)

Item Number	Check Items (pattern diagram)	✔	Reference
1	Are the transmission lines correct?		-
1-1	Is the differential impedance 100 Ω ± 20%?		2
1-2	Is wiring paired?		-
1-3	Are the positive signal line and negative signal line of differential pair isometric?		2
1-4	Are each of the data differential pairs and a clock differential pair isometric?		
1-5	Is the wiring as short as possible?		
1-6	Are the wiring bends 135° or a circular arc?		
1-7	Does the wiring not use a via?		
1-8	Are the numbers of vias on positive and negative signal lines in each of differential pairs the same?		
1-9	Does not the via create a stub?		Figure 2.1
1-10	Are symmetrical ground vias allocated at both sides of transmission line vias?		Figure 2.2
1-11	Is the ground plane at lower layer of transmission line divided/split?		Figure 2.3
1-12	Is spacing between adjacent patterns sufficient?		Table 2.1 Figure 2.4 Figure 2.5
2	Are the power supply lines correct?		-
2-1	Is the bypass capacitor located near the power supply pin?		3
2-2	Is the wiring resistance from the power supply pin to the bypass capacitor 30 mΩ or less?		Table 3.1
2-3	If using LVDS, is the wiring inductance from the power supply pins (LVDSAPVcc, LVDSPLLVcc) to the bypass capacitor 3.5 nH or less?		
2-4	If using MIPI, is the wiring inductance from the power supply pin (MIPIAVcc18) to the bypass capacitor 4.6 nH or less?		

5. Reference Documents

- Hardware manual
  RZ/A2M Group User's Manual: Hardware (R01UH0746EJ)
  (The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2019.12.23	–	First edition issued.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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