RZ/A1

Guidelines for High-Speed USB2.0 Board Design

Introduction

This application note details guidelines for the design of High-Speed USB2.0 circuit boards.

Target LSIs

The following groups in the RZ/A Series

RZ/A1H*1, *2 group, RZ/A1M*1, *2 group
RZ/A1L*1, *3 group, RZ/A1LU*1, *3 group, RZ/A1LC*1, *3 group

Notes: The contents in this application note are reference examples based on the USB standard, and signal quality in the system is not guaranteed. When incorporated into an actual system, sufficient verification and evaluation of the system overall should be performed, and determination of applicability is the customer's responsibility.
"Group" will be omitted in the rest of this application note.
*1. In this application note, when indicating these groups collectively, it will be noted as "RZ/A1".
*2. In this application note, when indicating these groups collectively, it will be noted as "RZ/A1HM".
*3. In this application note, when indicating these groups collectively, it will be noted as "RZ/A1L".

Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- RZ/A Series Hardware Design Guide (R01AN4813EJ)

Contents

1. Introduction

This application note provides an explanation using the USB2.0 Host/Function Module's pin names. Table 1.1 shows the USB2.0 Host/Function module pin overview.

Table 1.1 USB2.0 Host/Function Module pin overview

Used Pin Name	Input/Output	Function
DP1, DP0	Input and output	USB2.0 Host/Function Module bus D+ data.
DM1, DM0	Input and output	USB2.0 Host/Function Module bus D- data.
VBUS1, VBUS0	Input	USB cable connection monitor pin. Connect to the USB bus VBUS. VBUS connection/disconnection can be detected. If not connected to the USB bus VBUS, fix to 5 V. Supply 5 V during host controller function selection as well. Note: VBUS cannot be supplied to connected peripheral devices.
REFRIN	Input	This pin is for connection to the reference resistor. Connect to USBAPVss via 5.6 kΩ ± 1% resistor. (QFP) Connect to Vss via 5.6 kΩ ± 1% resistor. (BGA package)
USB_X1	Input	Connects the USB crystal oscillator. USB_X1 pin can also input the external clock.
USB_X2	Output	
USBAPVcc	Input	3.3 V analog power supply for pins.
USBAPVss*1	Input	3.3 V analog ground for pins.
USBDPVcc*1	Input	3.3 V digital power supply for pins.
USBDPVss*1	Input	3.3 V digital ground for pins.
USBAVcc	Input	1.2 V analog power supply for cores.
USBAVss*1	Input	1.2 V analog ground for cores.
USBDVcc*1	Input	1.2 V digital power supply for cores.
USBDVss*1	Input	1.2 V digital ground for cores.
USBUVcc*1	Input	480 MHz operation components power supply.
USBUVss*1	Input	480 MHz operation components ground.
PVcc*2	Input	3.3 V power supply for I/O pins.
Vcc*2	Input	1.2 V power supply for internal cores.
Vss*2	Input	3.3 V ground for I/O pins and 1.2 V ground for internal cores.

Notes: *1. Does not exist in BGA package.
*2. PVcc, Vcc, and Vss power supply pins are LSI I/O power supply and core power supply for other than USB.

2. USB Transmission Line

The USB transmission line indicates the wiring pattern that connects the USB connector and the USB transceiver.

USB2.0 has High-Speed, Full-Speed, and Low-Speed communication modes. High-Speed has a communication speed of 480 Mbps, so it is necessary to design the USB transmission line as a high frequency circuit. Impedance control is necessary for a USB transmission line.

Notes on designing the USB transmission line pattern wiring are described below.

- The characteristic impedance required in USB High-Speed transmission lines is a differential impedance of 90 Ω ± 15 %.
- The impedance control requires different pattern width and pattern interval according to board thickness, material, and layer configuration. For details, consult the board manufacturer.
- USB module of RZ/A1 incorporates the terminating resistor for the D+ and D- signals during high-speed operation and the output resistor for the signals during full-speed operation. Therefore, do not place an external resistor on the transmission line.
- The USB transmission line wiring pattern length from RZ/A1 to the USB connector must be designed so that it does not exceed the maximum delay time specified in the USB standard. In addition, taking into account the quality of waveforms during High-Speed, shorter wiring is recommended. Table 2.1 shows the USB transmission line pattern design values taking the maximum delay times into account for print wiring boards using general materials.

Table 2.1 USB transmission line pattern design values in consideration of the maximum delay times

	Maximum Delay Time (USB standard)	Wiring Length*1	Difference in D+, D- Wiring Length
Host controller	3 ns	300 mm or less	2.5 mm or less
Function controller	1 ns	100 mm or less	2.5 mm or less

Note: *1. This example is for 100 ps/cm wiring delay.

- The lower layer of the USB transmission lines must be a ground plane. The ground plane must be at least 1 mm wider than the USB transmission lines. The power supply for the ground plane is USBDPVss*1.
- Do not allocate other signal lines near the USB transmission lines. In particular, separate lines for signals with heavily fluctuating, such as clock or a data bus away from the USB transmission lines. Ensure that the USB transmission lines do not intersect lines for other signals.
- It is recommended to create a guard ring using the USBDPVss*1 for the USB transmission line separated by 3 times (or more) the D+/D- wiring spacing on the same layer (surface layer) as the USB transmission line.
- USB transmission lines should be allocated on the same layer without vias. Also, USB transmission line wiring should not be branched.
- The USB transmission lines should be wired with uniform spaces.
- Separate the USB transmission lines away from oscillators, power supply circuits and any other I/O connectors.
- USB transmission lines should be wired as straight as possible. If a USB transmission line must turn within the layout, use a gentle turn of 135° or a circular arc. Do not use sharp angles (right angles) for the USB transmission lines.

Figure 2.1 shows an example of USB transmission line pattern design when used as a host controller, Figure 2.2 shows an example of USB transmission line pattern design when used as a function controller, Figure 2.3 shows an example of spacing between USB transmission line and ground guard ring.

Note: *1. This is Vss in the BGA package.

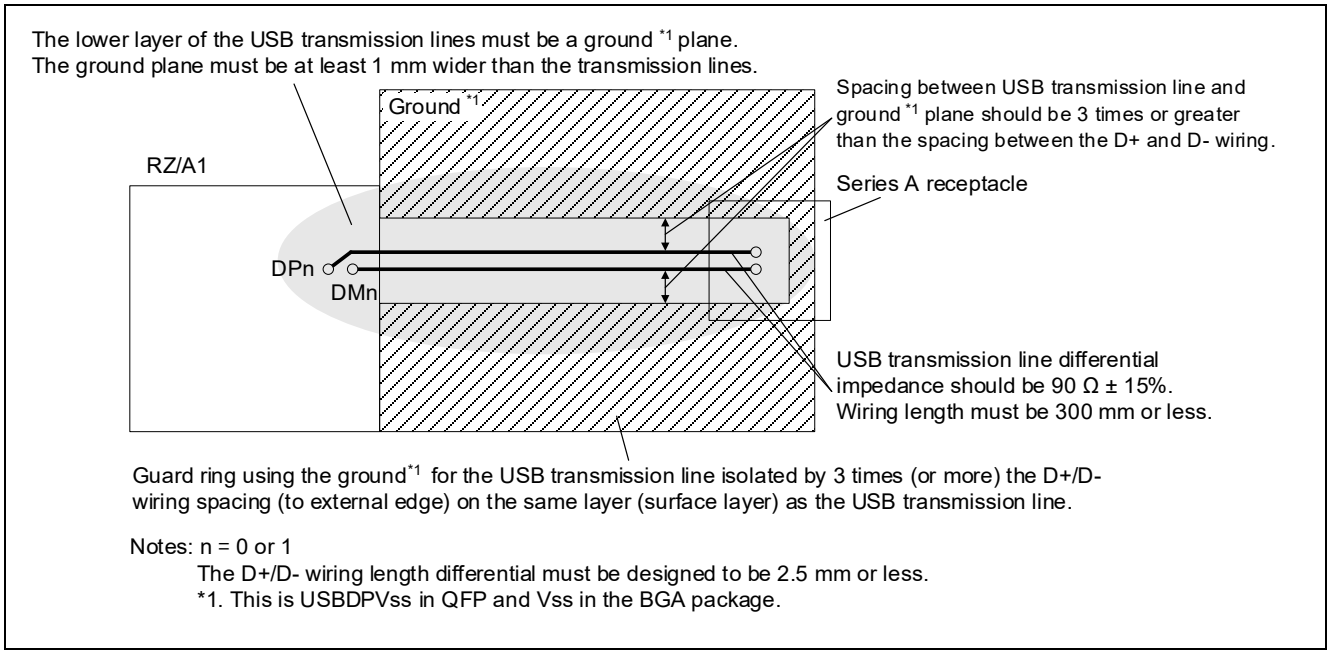


Figure 2.1 Example of USB transmission line pattern design when used as a host controller

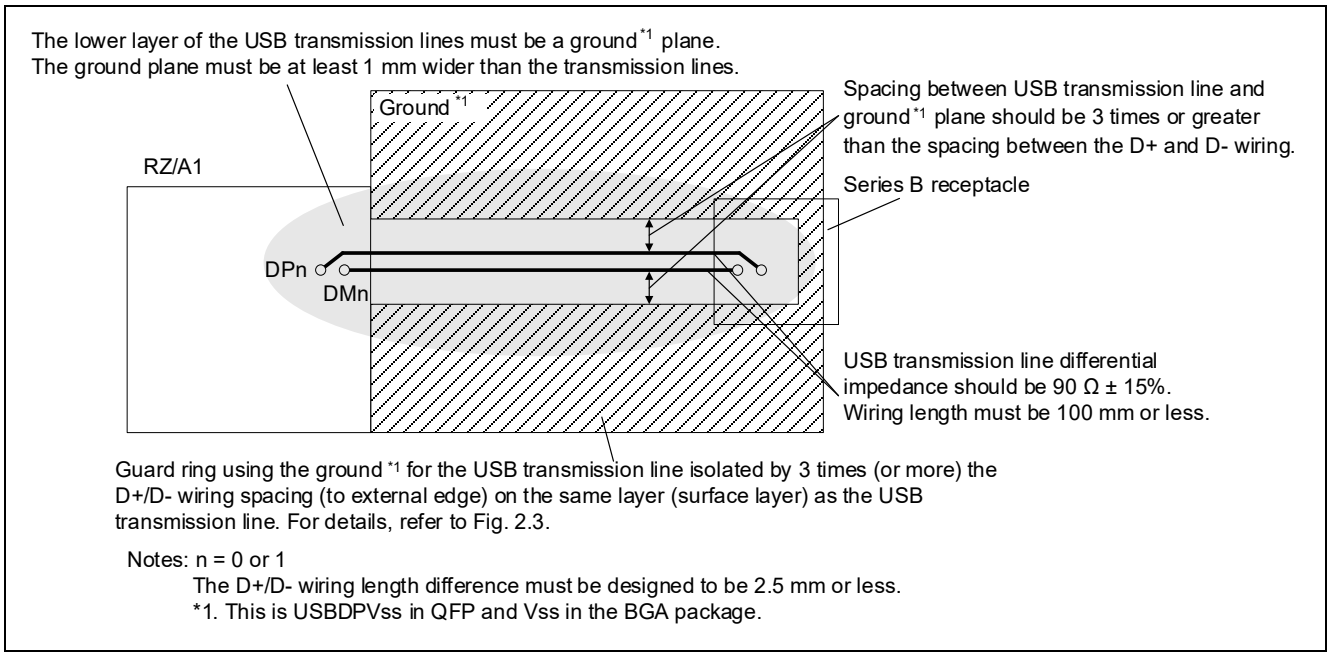


Figure 2.2 Example of USB transmission line pattern design when used as a function controller

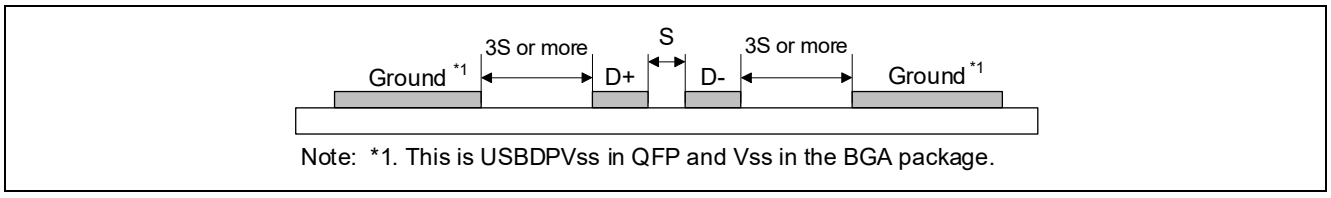


Figure 2.3 Example of spacing between USB transmission line and ground guard ring

3. Power Supply and Ground Patterns

Notes on designing power supply and ground patterns are described below.

- Power supplies and ground patterns should be separated into digital and analog. Table 3.1 and Table 3.2 show the power supply and ground classifications.

Table 3.1 Classification of USB power supply

Pin Name	Classification of Power Supply			
	Analog Power Supply (1.2 V)	Digital Power Supply (1.2 V)	Analog Power Supply (3.3 V)	Digital Power Supply (3.3 V)
USBAVcc	✔			
USBDVcc*1		✔*2		
USBUVcc*1		✔*2		
USBAPVcc			✔	
USBDPVcc*1				✔*3
Vcc		✔*2		
PVcc				✔*3

Notes: ✔: Indicates the power supply used.
*1. Does not exist in BGA package.
*2. USBDVcc, USBUVcc, and Vcc are connected internally in the LSI.
*3. USBDPVcc and PVcc are connected internally in the LSI.

Table 3.2 Classification of USB ground

Pin Name/USB Connector	Classification of Ground	
	Analog Ground (AGND) Symbol: ⏚	Digital Ground (DGND) Symbol: ⏚
USBAVss*1	✔	
USBDVss*1		✔*2
USBUVss*1		✔*2
USBAPVss*1	✔	
USBDPVss*1		✔*2
Vss		✔*2
USB connector ground (Includes frame ground)		✔

Notes: ✔: Indicates the ground used.
*1. Does not exist in BGA package.
*2. USBDPVss, USBDVss, USBUVss, and Vss are connected internally in the LSI.

- The pins connected internally in the LSI shall also be connected to the ground on the board with low impedance.
- The layer plane patterns of power supplies and grounds shall be designed widely as much as possible.
- For the bypass capacitor capacity value, it is recommended that a capacitor of 0.1 µF be placed near the USB power supply pins. Figure 3.1 shows an example of bypass capacitor connection for QFP and Figure 3.2 shows an example of bypass capacitor connection for BGA package.
- Ceramic capacitors having excellent high-frequency characteristics are recommended as power supply capacitors.
- Electrolytic capacitors may affect EYE pattern jitter, so the use of such capacitors requires thoroughly design and tests before use.

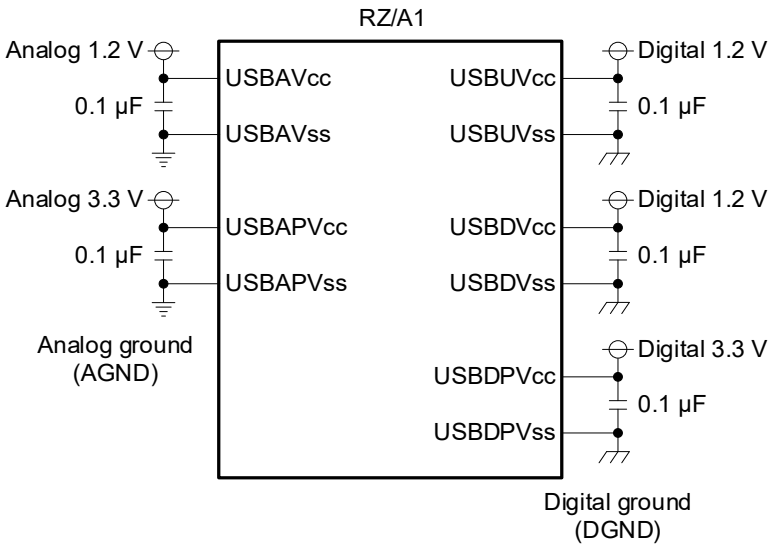
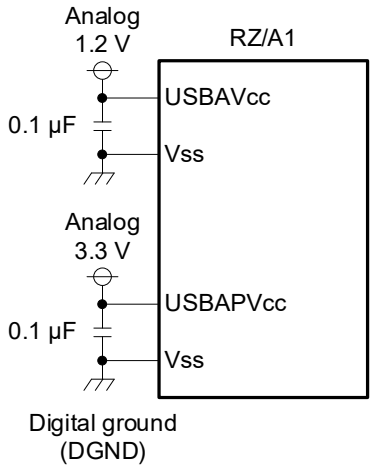


Figure 3.1 Bypass capacitor connection example 1 (QFP)



Note: For BGA package, Vcc and PVcc are used as the USB digital power supply. For the capacity value of the capacitors connected to Vcc and PVcc, refer to the respective LSI hardware manual "Recommended Combination of Bypass Capacitor" section.

Figure 3.2 Bypass capacitor connection example 2 (BGA package)

4. Oscillation Circuit

Notes on designing the oscillation circuit are described below.

- Allocate the oscillator circuit near the USB_X1 USB clock input pin. It is recommended that the USB_X1 be grounded with a guard ring to the digital ground.
- Use oscillators that meet the frequency specifications shown in Table 4.1.

Table 4.1 USB_X1 clock input frequency

Function used	Frequency specification (fEX)
For high-speed transmission	48 MHz ± 100ppm
Using host controller functions, not using high-speed transmission	48 MHz ± 500ppm
Not using host controller functions, not using high-speed transmission	48 MHz ± 2500ppm

- If using a crystal resonator, consult with the manufacturer*1, and determine the circuit constants.

Figure 4.1 shows a crystal resonator connection example, and Figure 4.2 shows a crystal oscillator connection example.

Note: *1. Examples of oscillator and circuit matching suitable for the products for the RZ/A1 are shown on the oscillator manufacturer website below. If the optimized oscillator circuit constant for your system is necessary, ask the oscillator manufacturer.
http://prdct-search.kyocera.co.jp/crystal-ic/?p=en_search/

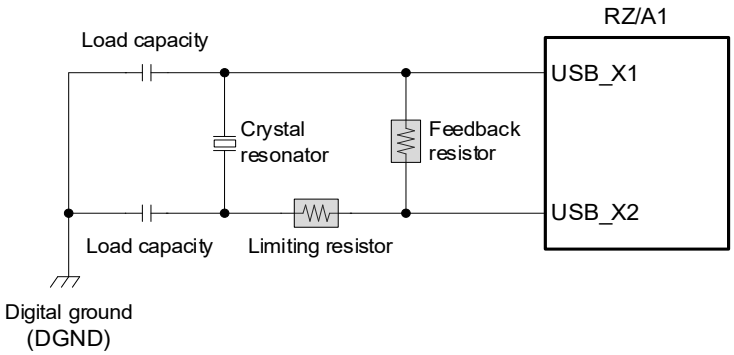


Figure 4.1 Example of crystal resonator connection

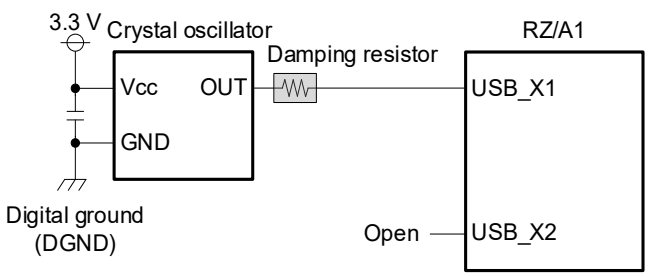


Figure 4.2 Example of crystal oscillator connection

5. VBUS Power Supply Circuit

Notes on designing the VBUS power supply circuit are described below.

- When RZ/A1 is used as a host controller, the additional capacity of the VBUS line should be designed to be 120 µF or more.
- When RZ/A1 is used as a function controller, the additional capacity of the VBUS line should be designed to be between 1.0 µF and 10 µF.
- The VBUS line should include a filter circuit as overshoot may be caused by inconsistent impedance when the USB cable is connected. As a filter circuit, add a 1.0 µF to 10 µF capacitor and 100 Ω to 1 kΩ resistor. The final constants should be defined after confirming that an overshoot has not occurred on the board. Also, a resistor of more than 1 kΩ should not be added.
- When used as a host controller, the VBUS power supply must be supplied to the function devices. A power supply switch IC with over-current protection for the USB power supply bus (hereinafter called “USB power supply switch IC”), such as the Renesas Electronics ISL6186 is recommended for the VBUS power supply control. Make sure to consider the limitation value of the current for the VBUS power supply line based on the current value used by the applicable system power supply and the USB function devices being communicated with. In addition, when designing the VBUS power supply control circuit, refer to the example circuits described in the USB power supply switch IC datasheet.

Figure 5.1 shows an example of the VBUS power supply circuit when it is used as a host controller and Figure 5.2 shows an example of the VBUS power supply circuit when it is used as a function controller.

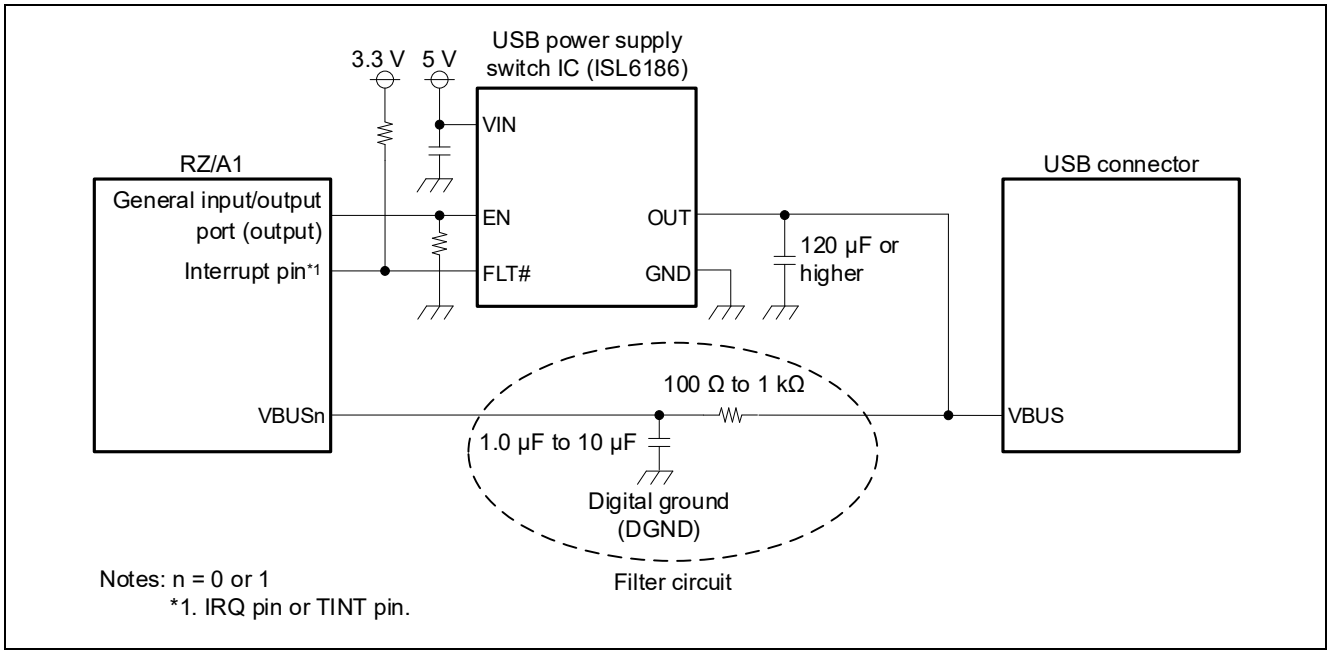


Figure 5.1 Example of VBUS circuit for using RZ/A1 as a host controller

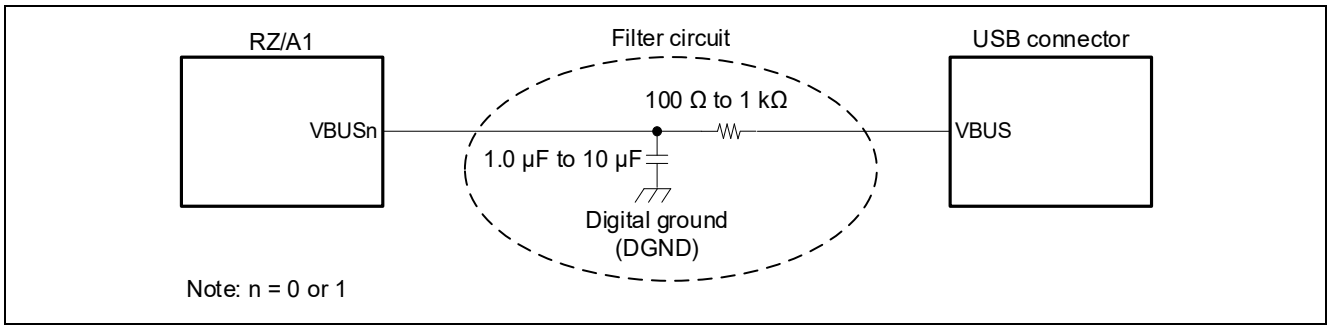


Figure 5.2 Example of VBUS circuit for using RZ/A1 as a function controller

6. REFRIN Pin

Notes on designing the REFRIN pin peripheral circuit are described below.

- Connect a 5.6 kΩ ± 1% resistor (hereinafter called "reference resistor") between the REFRIN pin and USBAPVss*1. The resistor should be connected to REFRIN pin without using a via if at all possible.
- The reference resistor should be allocated as close as possible to RZ/A1.
- The REFRIN pin, reference resistor, and USBAPVss*1 should be connected using the shortest and wide pattern.
- For QFP, connect the reference resistor and USBAPVss pin with independent patterns, and then connected to the analog ground. It is necessary to design patterns to prevent having shared impedance with other signals.
- To prevent crosstalk, do not allow wiring for signals with heavily fluctuating (D+, D-, clock, address/data/control signals, etc.) to intersect or run parallel near the reference resistor or near its patterns. It is recommended to create a guard ring using ground for the reference resistor and its patterns.

Figure 6.1 shows the REFRIN pin peripheral connection diagram and example of pattern design (QFP) and Figure 6.2 shows the REFRIN pin peripheral connection diagram and example of pattern design (BGA package).

Note: *1. This is Vss in the BGA package.

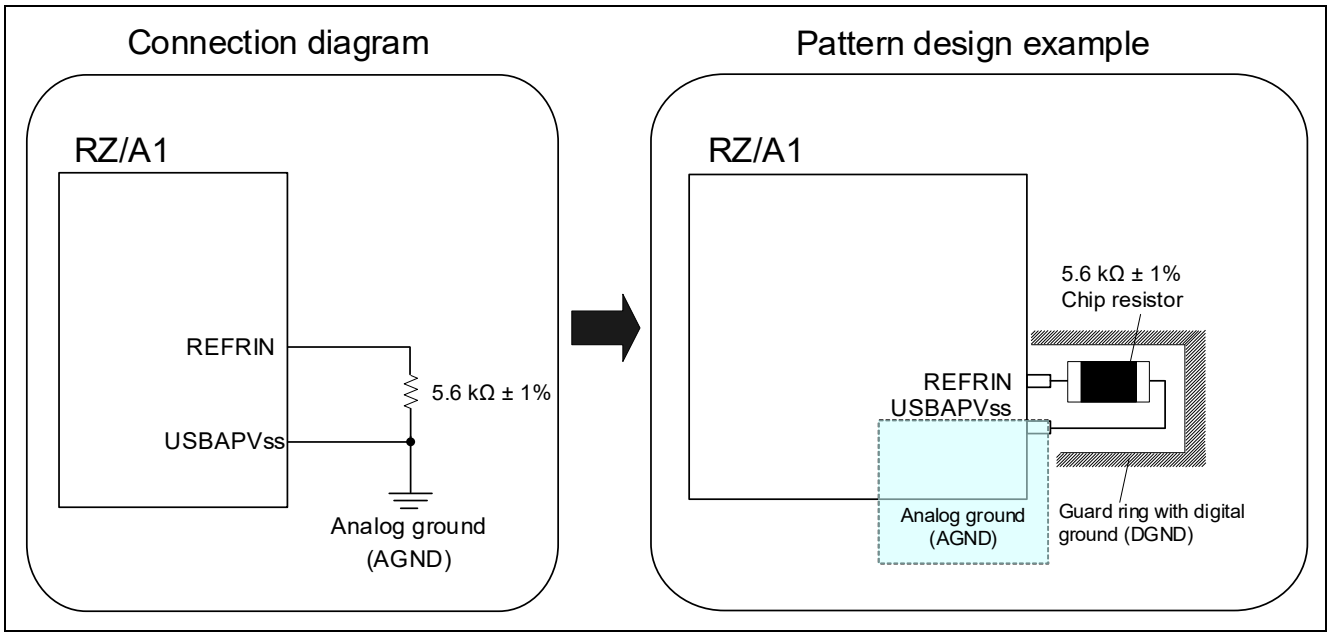


Figure 6.1 REFRIN pin peripheral connection diagram and example of pattern design 1 (QFP)

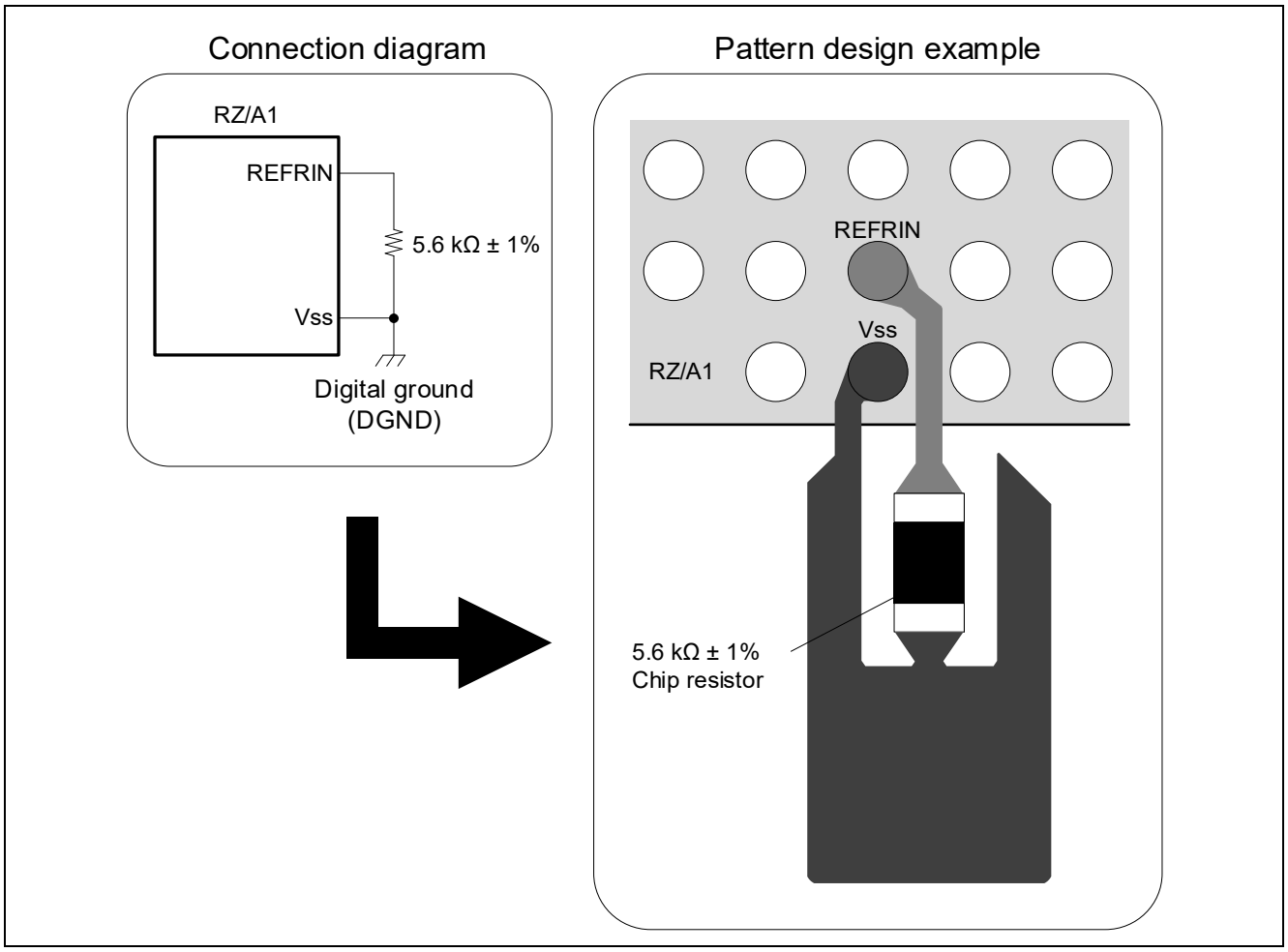


Figure 6.2 REFRIN pin peripheral connection diagram and example of pattern design 2 (BGA package)

7. EMI/ESD Protection

Notes on EMI/ESD protection are described below.

- When components for EMI/ESD protection such as coils and diodes are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.
- The components for the EMI/ESD protection must be USB 2.0 High-Speed compliant. Also, by mounting EMI/ESD protection components, an inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.

Figure 7.1 shows an example of connection when the components for EMI/ESD protection are used.

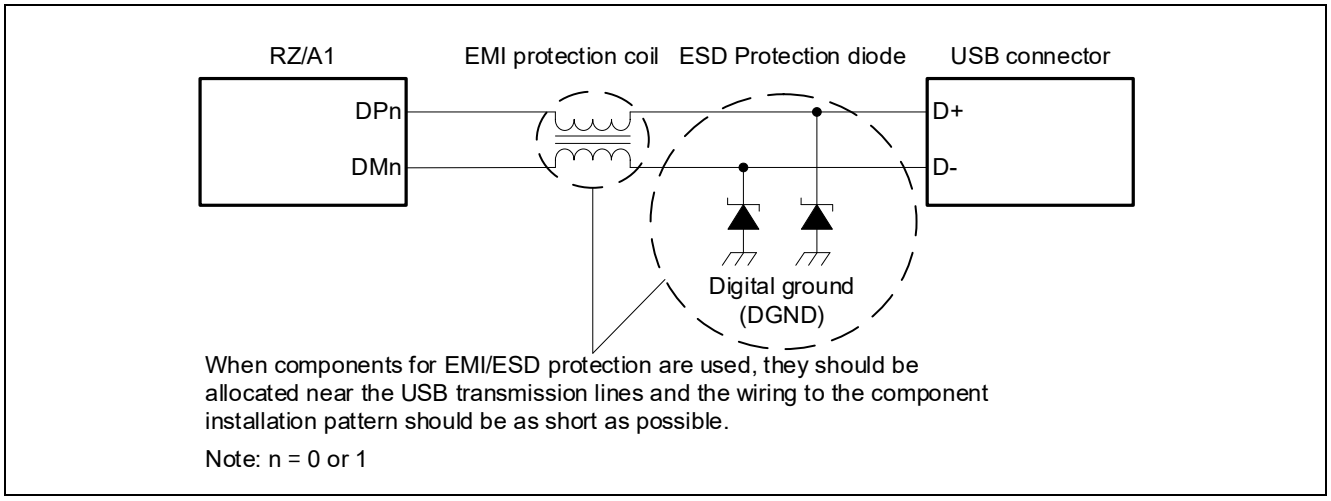


Figure 7.1 Connection example when components for EMI/ESD protection are used

8. Checklist

Table 8.1 Checklist 1 (circuit diagram)

Item Number	Check Items (circuit diagram)	✔	Reference
1	Isn't an external resistor place on the transmission line?		2
2	Is the treatment of pins correct?		-
2-1	Is REFRIN pin connected to USBAPVss*1 via a 5.6 kΩ ± 1% resistor?		Table 1.1 Figure 6.1 Figure 6.2
2-2	Is there a 0.1 µF bypass capacitor for each USB power supply pin?		Figure 3.1 Figure 3.2
2-3	Are the voltages for each power supply pin correct? (Are there no unconnected power supply pins?)		-
2-3-1	USBAPVcc : 3.3 V analog power supply		Table 3.1
2-3-2	USBAVcc : 1.2 V analog power supply		
2-3-3	USBDPVcc : 3.3 V digital power supply (QFP only)		
2-3-4	USBDVcc : 1.2 V digital power supply (QFP only)		
3	Is power supply isolated?		-
3-1	USBAVcc and other power supply		Table 3.1 Figure 3.1 Figure 3.2
3-2	USBAPVcc and other power supply		
3-3	USBAVss and USBAPVss and other ground (QFP only)		Table 3.2 Figure 3.1
4	Is the oscillator circuit correct?		-
4-1	Does the oscillator satisfy the 48 MHz ± 100ppm requirement?		Table 4.1
4-2	Are a limiting resistor, feedback resistor, and load capacitor attached to the crystal resonator?		Figure 4.1
4-3	If using a crystal oscillator, is it connected to the USB_X1 pin? (USB_X2 pin is open)		Figure 4.2
4-4	If using a crystal oscillator, is a damping resistor connected?		
5	Is the VBUS circuit correct?		-
5-1	When using RZ/A1 as a host controller, is a 120 µF or higher capacitor connected to the VBUS line?		Figure 5.1
5-2	When using RZ/A1 as a function controller, is a 1.0 µF to 10µF capacitor connected to the VBUS line?		Figure 5.2
5-3	Is a filter circuit in place for the VBUS line?		-
5-3-1	Capacity: 1.0 µF to 10 µF		Figure 5.1 Figure 5.2
5-3-2	Resistance: 100 Ω to 1 kΩ		

Note: *1. This is Vss in the BGA package.

Table 8.2 Checklist 2 (pattern diagram)

Item Number	Check Items (pattern diagram)	✔	Reference
1	Are the transmission lines correct?		-
1-1	Is the differential impedance 90 Ω ± 15%?		2
1-2	When using RZ/A1 as a host controller, is the wiring length 300 mm or less?		Table 2.1
1-3	When using RZ/A1 as a function controller, is the wiring length 100 mm or less?		
1-4	Is the D+/D- wiring length differential 2.5 mm or less?		
1-5	Is the wiring on the same layer?		2
1-6	Is the wiring not branched?		
1-7	Does the wiring have consistent spacing?		
1-8	Are there no unnecessary wiring bends?		
1-9	Are the wiring bends 135° or a circular arc?		
2	Is the clearance correct?		-
2-1	Is the transmission line lower layer USBDPVss[*1] ground plane at least 1 mm wider than the USB transmission lines?		2 Figure 2.1 Figure 2.2
2-2	Is the spacing between USBDPVss[*1] and the transmission lines at least 3 times the D+/D- wiring spacing?		2 Figure 2.1 Figure 2.2 Figure 2.3
3	Is the bypass capacitor located near the power supply pin?		3
4	Is the oscillator circuit correct?		-
4-1	Is the oscillator circuit located in the vicinity of the USB_X1 pin?		4
4-2	Is a damping resistor placed at the output pin side?		Figure 4.2
5	Is the circuit around the REFRIN pin correct?		-
5-1	Is it connected without using a via?		6
5-2	Is the reference resistor allocated close to RZ/A1?		
5-3	Is it connected using a wide pattern? (REFRIN pin - reference resistor - USBAPVss[*1])		
5-4	Is the wiring as short as possible? (REFRIN pin - reference resistor - USBAPVss[*1])		
5-5	For QFP, are the reference resistor and USBAPVss pin connected with independent patterns?		Figure 6.1
6	Are the EMI/ESD protections correct?		-
6-1	Are protection components located close to the transmission lines?		Figure 7.1
6-2	Is the wiring to the protection components as short as possible?		

Note: *1. This is Vss in the BGA package.

9. Reference Documents

- Hardware manual
  RZ/A1H Group, RZ/A1M Group User's Manual: Hardware (R01UH0403EJ)
  (The latest version can be downloaded from the Renesas Electronics website.)

  RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group User's Manual: Hardware (R01UH0437EJ)
  (The latest version can be downloaded from the Renesas Electronics website.)

10. Design Support Information

- Kyocera Corporation “Crystal Units vs. IC Matching Search”
  http://prdct-search.kyocera.co.jp/crystal-ic/?p=en_search/

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2019.11.26	-	First edition issued (Japanese edition only).
1.10	2019.12.26	-	Unification of notation: • For pin names other than RZ/A1, DP is changed to D+, and DM is changed to D-. • Decoupling capacitor is changed to bypass capacitor.
		14, 15	Table 8.1, Table 8.2: Added checklists.
1.20	2020.05.26	4	Added note on differential wiring.
		14	Check item (Item Number 1) was added.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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