RZ/A Series

Hardware Design Guide

Introduction

This application note is a summary of the items serving as design points as reference materials for use when designing hardware which incorporates RZ/A Series LSIs.

Target LSIs

The following RZ/A Series groups

RZ/A1H group*1*2, RZ/A1M group*1*2

RZ/A1L group*1*3, RZ/A1LU group*1*3, RZ/A1LC group*1*3

RZ/A2M group

Notes: In the rest of this document, unless clearly specifying a particular group, this will be contracted to simply "group",
*1. In this document, when indicating these groups collectively, it will be noted as "RZ/A1".
*2. In this document, when indicating these groups collectively, it will be noted as "RZ/A1HM".
*3. In this document, when indicating these groups collectively, it will be noted as "RZ/A1L".

Reference Application Note

For additional information associated with this document, refer to the following application note.

- RZ/A2M Group Guidelines for High-Speed USB2.0 Board Design (R01AN4964EJ)
- RZ/A1 Guidelines for High-Speed USB2.0 Board Design (R01AN5119EJ)
- RZ/A2M Group Guidelines for LVDS and MIPI Board Design (R01AN5280EJ)

Trademarks

List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communications Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Abbreviation	Full Form
CPHAR	Clock Phase Reception (Input latch timing)
CPHAT	Clock Phase Transmission (Output shift timing)
CPOL	Clock Polarity
EMI	Electromagnetic Interference
EMS	Electromagnetic Susceptibility
ESD	Electrostatic Discharge
RSPI	Renesas Serial Peripheral Interface
SPIBSC	Serial Peripheral Interface Multi I/O Bus Controller

Contents

1. Power Supply

1.1 Power Supply

LSI of this series have the power supplies shown in Table 1.1 and Table 1.2. When designing a board, separate the digital power supply and the analog power supply as much as possible to prevent switching noise from the digital power supply.

In addition, the PLL power supply is sensitive to noise and the like, with the result that interference from other power supplies may cause erroneous operation or malfunctions in the overall system. To prevent such malfunction, the PLL power supply and other power supplies should not supply the same resources on the board if at all possible. Wiring length from the board power supply pins must be as short as possible and pattern width must be as wide as possible to reduce inductive interferences.

Table 1.1 Power supply (RZ/A1)

Symbol	Type*1	Name	Voltage Range
PVcc	D	Power supply for I/O circuits	3.0 V to 3.6 V
Vcc	D	Power supply	1.10 V to 1.26 V
Vss	D	Ground	0 V
USBDPVcc	D	Power supply for transceiver digital pins	3.0 V to 3.6 V
USBDPVss	D	Ground for transceiver digital pins	0 V
USBDVcc	D	Power supply for transceiver digital core	1.10 V to 1.26 V
USBDVss	D	Ground for transceiver digital core	0 V
USBUVcc	D	480-MHz power supply for USB 2.0 host/function module	1.10 V to 1.26 V
USBUVss	D	480-MHz ground for USB 2.0 host/function module	0 V
PLLVcc	D	Power supply for PLL	1.10 V to 1.26 V
LVDSPLLVcc	D	LVDS PLL power supply	1.10 V to 1.26 V
USBAPVcc	A	Power supply for transceiver analog pins	3.0 V to 3.6 V
USBAPVss	A	Ground for transceiver analog pins	0 V
USBAVcc	A	Power supply for transceiver analog core	1.10 V to 1.26 V
USBAVss	A	Ground for transceiver analog core	0 V
VDAVcc	A	Analog power supply	3.0 V to 3.6 V
VDAVss	A	Analog ground	0 V
LVDSAPVcc	A	LVDS analog power supply	3.0 V to 3.6 V
LVDSAPVss	A	LVDS analog ground	0 V
AVcc	A	Analog power supply	3.0 V to 3.6 V*2
AVss	A	Analog ground	0 V
AVref	A	Analog reference voltage	3.0 V to 3.6 V*3

Notes: Connect all power supply and ground pins. LSI operation is not guaranteed if there are open pins.
Some pins may not exist depending on the packages.
*1. Digital systems power supply is shown as "D" and analog systems power supply is shown as "A"
*2. Set within the range of PVcc - 0.3 V ≤ AVcc ≤ PVcc
*3. Set within the range of 3.0 V ≤ AVref ≤ AVcc

Table 1.2 Power supply (RZ/A2M)

Symbol	Type[*1]	Name	Voltage Range
PVcc	D	Power supply for I/O circuits	3.0 V to 3.6 V
Vcc	D	Power supply	1.14 V to 1.26 V
Vss	D	Ground	0V
USBDPVcc1, USBDPVcc0	D	Power supply for transceiver digital pins	3.0 V to 3.6 V
PVcc_SPI, PVcc_SD1, PVcc_SD0	D	1.8-V/3.3-V switchable power supply for I/O circuits	1.7 V to 1.9 V
			3.0 V to 3.6 V
PVcc_HO	D	Power supply for I/O circuits	1.7 V to 1.9 V
AVcc	A	Analog power supply and reference voltage	3.0 V to 3.6 V
AVss	A	Analog ground	0 V
USBAPVcc1, USBAPVcc0	A	Power supply for transceiver analog pins	3.0 V to 3.6 V
LVDSAPVcc	A	LVDS analog power supply	3.0 V to 3.6 V
MIPIAVcc18	A	MIPI analog power supply	1.7 V to 1.9 V
PLLVcc	A	Power supply for PLL	1.14 V to 1.26 V
LVDSPLLVcc	A	LVDS PLL power supply	1.14 V to 1.26 V
USBVss	-[*2]	Ground for transceiver pins	0 V

Notes: Connect all power supply and ground pins. LSI operation is not guaranteed if there are open pins. Some pins may not exist depending on the packages.
*1. Digital systems power supply is shown as "D" and analog systems power supply is shown as "A"
*2. Ground for USB.

1.2 Absolute Maximum Ratings

Design the board so that the absolute maximum ratings for LSI of this series, as shown in Table 1.3 and Table 1.4 are satisfied. Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Table 1.3 Absolute maximum ratings (RZ/A1)

Symbol	Name	Rating Value
PVcc	Power supply for I/O circuits	-0.3 V to 4.2 V
Vcc	Power supply	-0.3 V to 1.6 V
PLLVcc	Power supply for PLL	-0.3 V to 1.6 V
AVcc	Analog power supply voltage	-0.3 V to 4.2 V
AVref	Analog reference voltage	-0.3 V to AVcc*1 + 0.3 V
USBAPVcc	Power supply for transceiver analog pins	-0.3 V to 4.2 V
USBDPVcc*2	Power supply for transceiver digital pins	-0.3 V to 4.2 V
USBAVcc	Power supply for transceiver analog core	-0.3 V to 1.6 V
USBDVcc	Power supply for transceiver digital core	-0.3 V to 1.6 V
USBUVcc	480-MHz power supply for USB 2.0 host/function module	-0.3 V to 1.6 V
VDAVcc	Analog power supply	-0.3 V to 4.2 V
LVDSAPVcc	LVDS analog power supply	-0.3 V to 4.2 V
LVDSPLLVcc	LVDS analog ground	-0.3 V to 1.6 V
VBUS1, VBUS0	VBUS input	-0.3 V to 5.5 V
REFRIN	Reference input	-0.3 V to USBAPVcc*1 + 0.3 V
DP1, DM1, DP0, DM0	USB 2.0 host/function module D+/D- data	-0.3 V to USBDPVcc*1*2 + 0.3 V
VIN2A, VIN1A, VIN2B, VIN1B, VRP, VRM, REXT	Composite video signal (CVBS) input	-0.3 V to VDAVcc*1 + 0.3 V
LVDSREFRIN	Reference input	-0.3 V to LVDSAPVcc*1 + 0.3 V
AN7 to AN0	Analog input pins	-0.3 V to AVcc*1 + 0.3 V*3
Other input pins	-	-0.3 V to PVcc*1 + 0.3 V

Notes: Some pins may not exist depending on the packages.

*1. Rated value changes in accordance with the power supply voltage applied.
For example, when 0 V is applied to AVcc, the AVref rated value will be -0.3 V to 0.3 V.

*2. In case of BGA package, this is PVcc.

*3. This is the rated value when the GPIO ports are set to analog input pins.

Table 1.4 Absolute maximum ratings (RZ/A2M)

Symbol	Name	Rating Value
PVcc	Power supply for I/O circuits	-0.3 V to 4.2 V
PVcc_SPI, PVcc_SD1, PVcc_SD0	1.8-V/3.3-V switchable power supply for I/O circuits	-0.3 V to 4.2 V
PVcc_HO	Power supply for I/O circuits	-0.3 V to 4.2 V
Vcc	Power supply	-0.3 V to 1.6 V
PLLVcc	Power supply for PLL	-0.3 V to 1.6 V
AVcc	Analog power supply and reference voltage	-0.3 V to 4.2 V
USBAPVcc1, USBAPVcc0	Power supply for transceiver analog pins	-0.3 V to 4.2 V
USBDPVcc1, USBDPVcc0	Power supply for transceiver digital pins	-0.3 V to 4.2 V
LVDSAPVcc	LVDS analog power supply	-0.3 V to 4.2 V
LVDSPLLVcc	LVDS PLL power supply	-0.3 V to 1.6 V
MIPIAVcc18	MIPI analog power supply	-0.3 V to 2.6 V
HM_RWDS/OM_DQS, HM_DQ7/OM_SIO7 to HM_DQ0/OM_SIO0	HyperBus Controller and Octa Memory Controller input pins	-0.3 V to PVcc_HO[*1] + 0.3 V
CSI_DATA1P, CSI_DATA1N, CSI_DATA0P, CSI_DATA0N, CSI_CLKP, CSI_CLKN	MIPI CSI-2 Interface input pins	-0.3 V to MIPIAVcc18[*1] + 0.3 V
QSPI1_SSL, QSPI1_IO3 to QSPI1_IO0, QSPI0_IO3 to QSPI0_IO0, RPC_INT#	SPI Multi I/O Bus Controller input pins	-0.3 V to PVcc_SPI[*1] + 0.3 V
SD0_DAT7 to SD0_DAT0, SD0_CMD	SD/MMC Host Interface Channel 0 input pins	-0.3 V to PVcc_SD0[*1] + 0.3 V
SD1_DAT3 to SD1_DAT0, SD1_CMD	SD/MMC Host Interface Channel 1 input pins	-0.3 V to PVcc_SD1[*1] + 0.3 V
RREF0	Reference input	-0.3 V to USBAPVcc0[*1] + 0.3 V
RREF1	Reference input	-0.3 V to USBAPVcc1[*1] + 0.3 V
DP0, DM0	D+/D- data for USB 2.0 host/function module channel 0	-0.3 V to USBDPVcc0[*1] + 0.3 V
DP1, DM1	D+/D- data for USB 2.0 host/function module channel 1	-0.3 V to USBDPVcc1[*1] + 0.3 V
AN007 to AN000	Analog input pins	-0.3 V to AVcc[*1] + 0.3 V[*2]
Other input pins	-	-0.3 V to PVcc[*1] + 0.3 V

Notes: Some pins may not exist depending on the packages.
In RZ/A2M, there is no input pin which uses LVDSAPVcc.
In the RZ/A2M Hardware Manual Table 56.1 Absolute Maximum Rating "Other input pin" item, power supply pins that apply 3.3 V are listed without differentiation, so LVDSAPVcc is included in the RZ/A2M Hardware Manual Table 56.1.
*1. Rated value changes in accordance with the power supply voltage applied.
For example, when 0 V is applied to AVcc, the AN000 rated value will be -0.3 V to 0.3 V.
*2. This is the rated value when the GPIO ports are set to analog input pins.

1.2.1 Points of caution when voltage is applied while system power supply is OFF

Design the board so that the absolute maximum ratings for LSI of this series, as shown in Table 1.3 and Table 1.4 are observed, even when the power supply is OFF.

For example, in the case that the RZ/A2M is used as a USB function module, when the RZ/A2M power supply is OFF and the USB host module is connected, if voltage that exceeds the absolute maximum rating (-0.3 V to 0.3 V) *1 is applied to the RZ/A2M VBUSIN input pin*1, it may permanently damage the LSI. In order to avoid this, refer to the protection circuit shown in Figure 1.1 and ensure that LSI of this series is protected.

Note: *1. The RZ/A2M VBUSIN input pin is multiplexed to the GPIO port, therefore the pin's absolute maximum rating is -0.3 V to PVcc + 0.3 V. For details, refer to "Other input pins" as shown in Table 1.4.

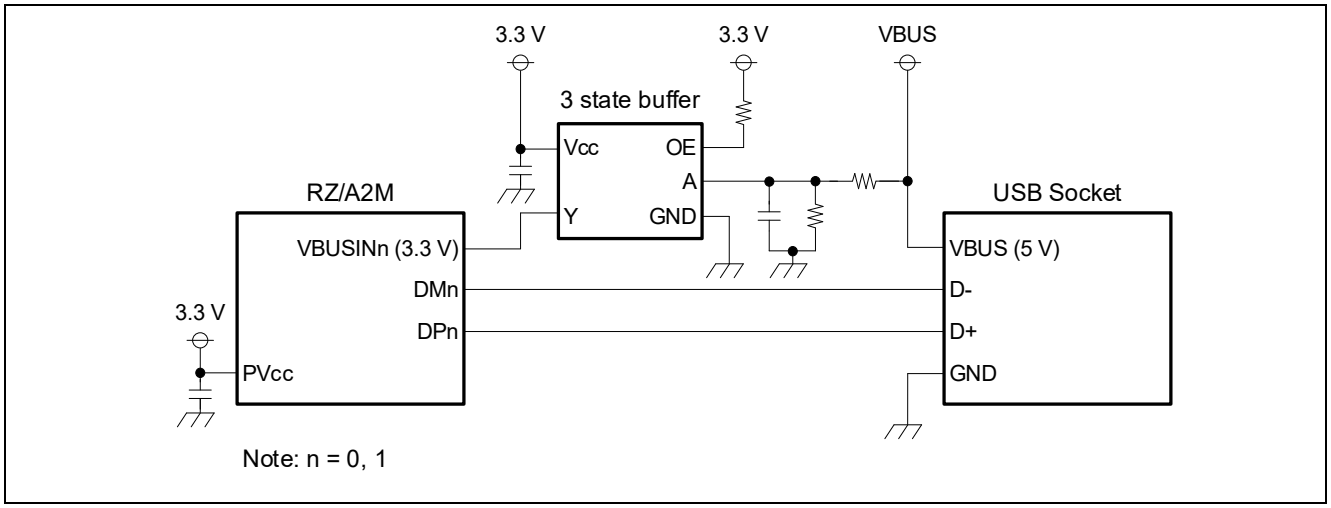


Figure 1.1 Example of LSI protection circuit

1.3 Bypass Capacitor

On the QFP, connect a laminated ceramic capacitor to each power supply pin pair as a bypass capacitor. Examples of QFP bypass capacitor configurations are shown in Figure 1.2 for 256-pin QFP, Figure 1.3 for 208-pin QFP, and Figure 1.4 for 176-pin QFP.

For the BGA package, if it is difficult to connect a bypass capacitor to all power supply pins, it is possible to collectively connect to multiple power supply pins. Figure 1.5 to Figure 1.12 shows the pins which can be grouped.

Locate the capacitor as close as possible to the LSI power supply pin, and use a capacity value from 0.1 µF to 0.33 µF (recommended value) per pin.

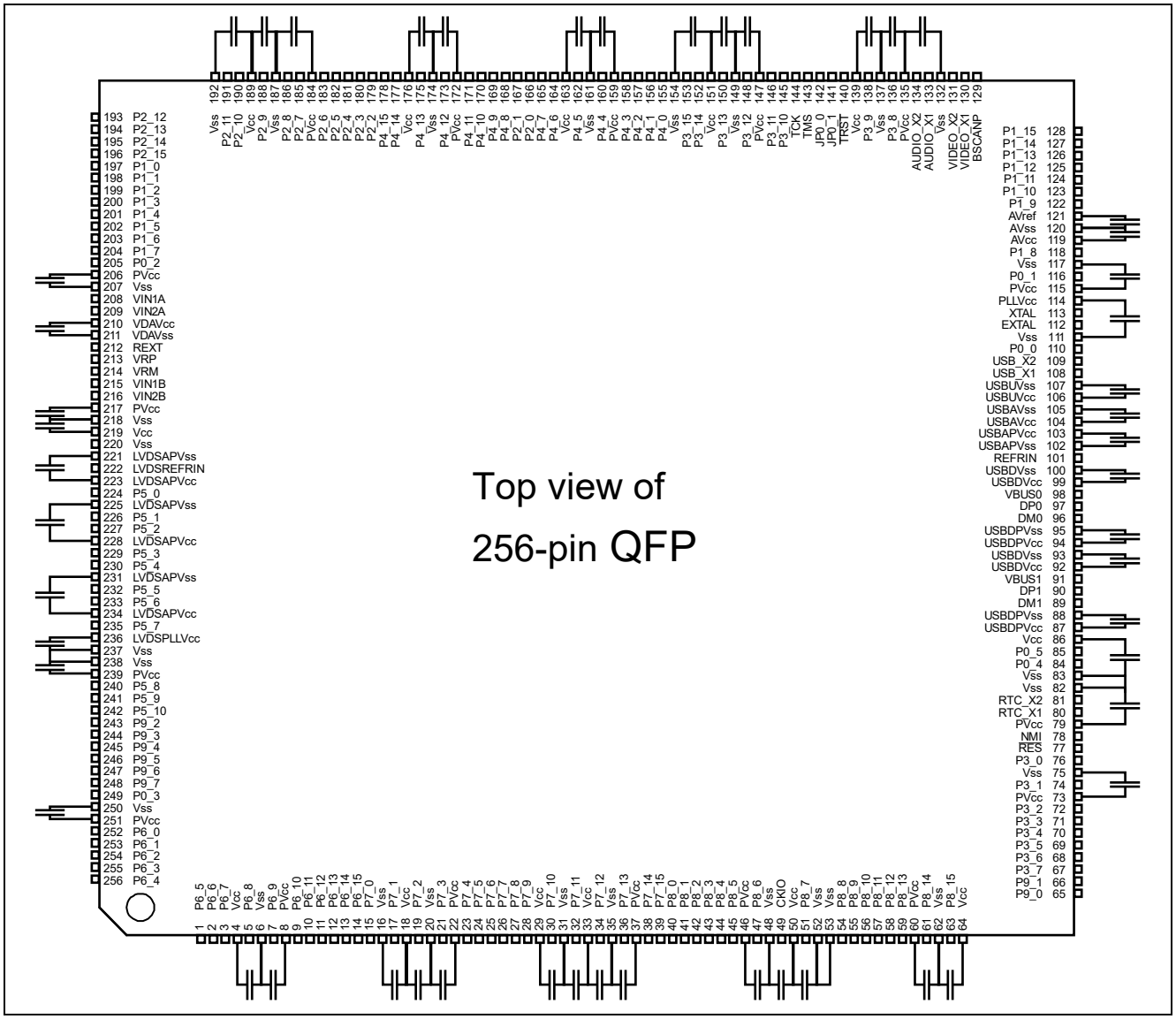


Figure 1.2 Example of 256-pin QFP capacitor configuration (RZ/A1HM)

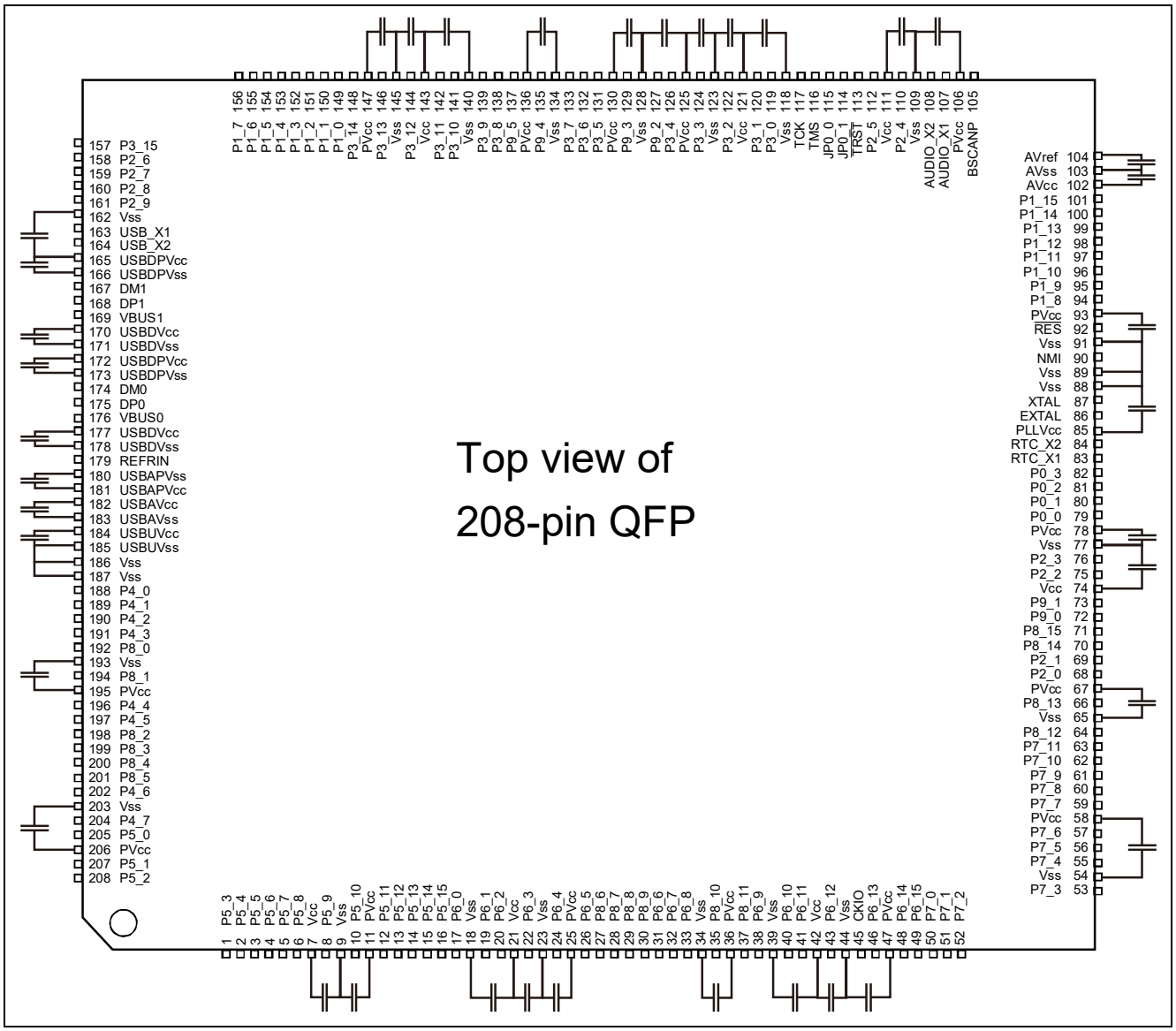


Figure 1.3 Example of 208-pin QFP capacitor configuration (RZ/A1L)

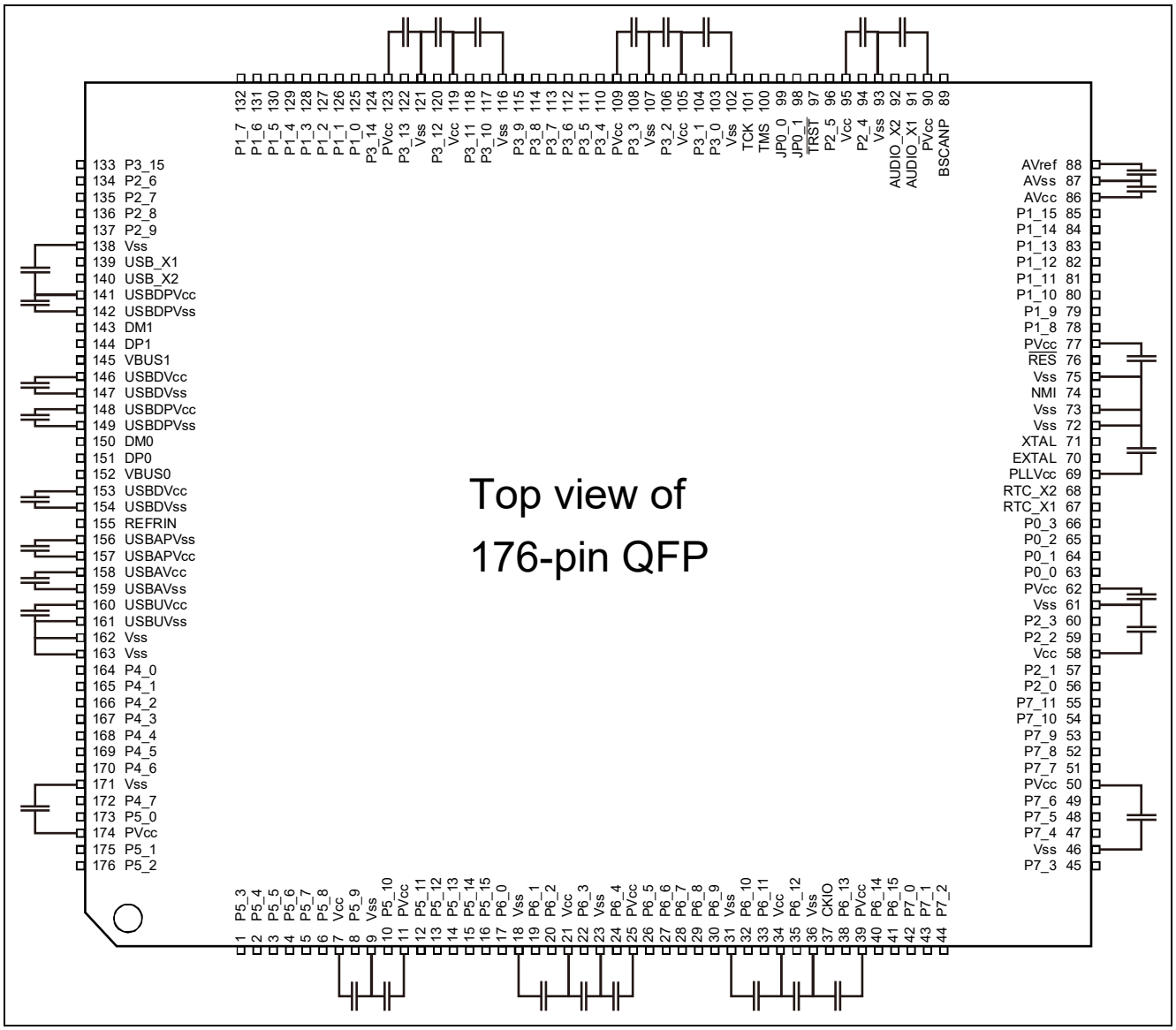


Figure 1.4 Example of 176-pin QFP capacitor configuration (RZ/A1L)

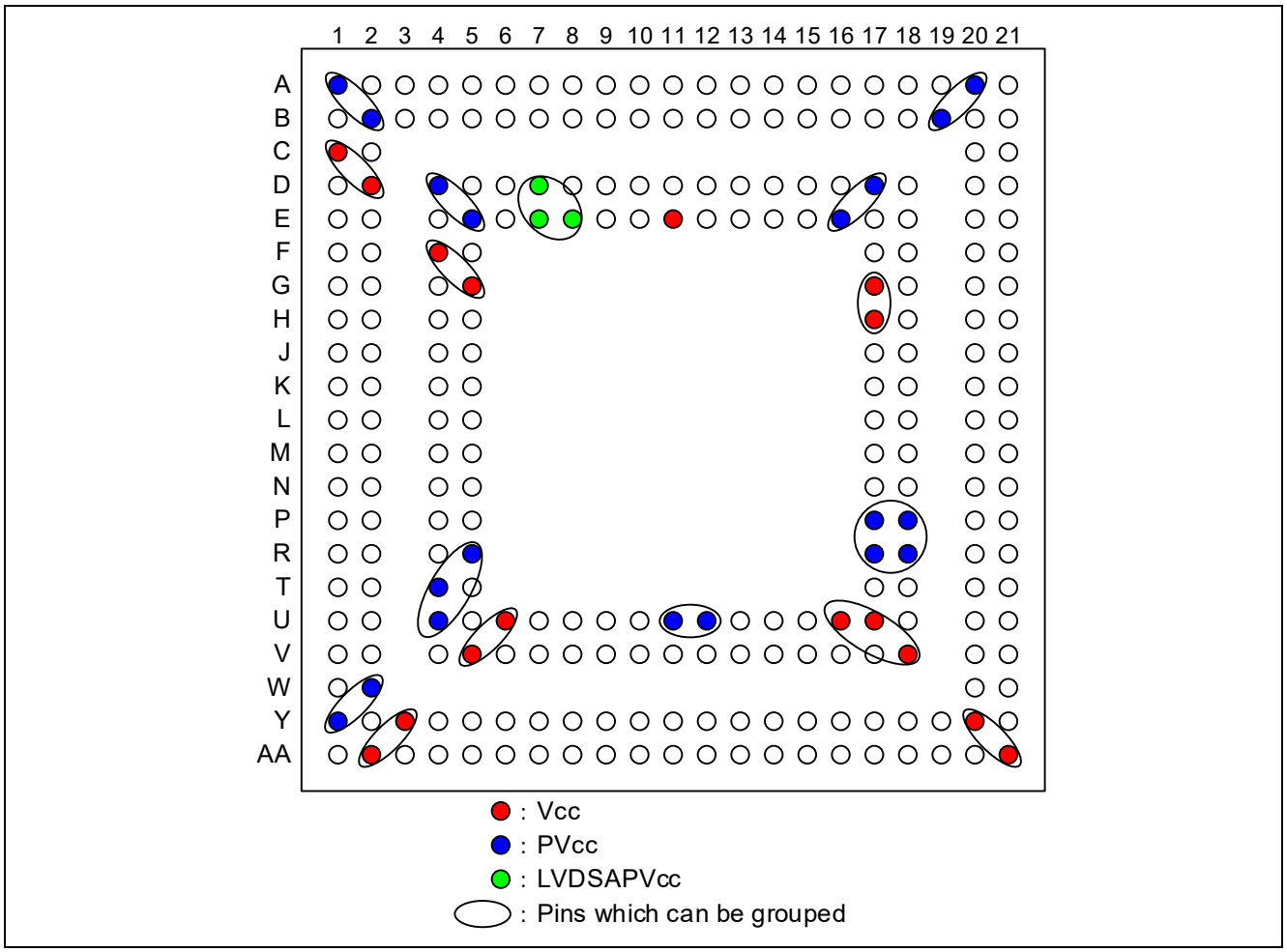


Figure 1.5 Example of 256-pin BGA power supply pin grouping (RZ/A1HM) (Top perspective view)

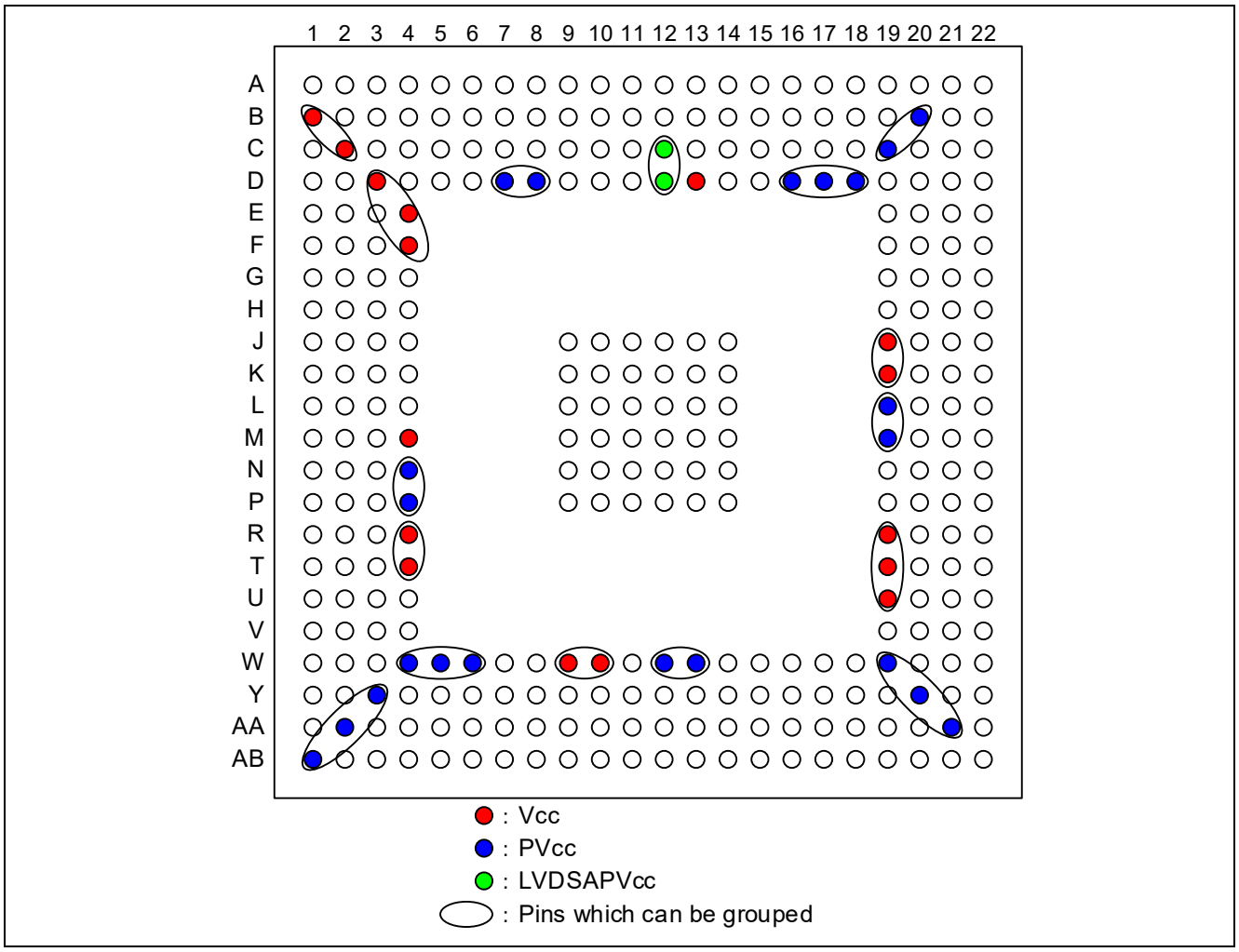


Figure 1.6 Example of 324-pin BGA power supply pin grouping (RZ/A1HM) (Top perspective view)

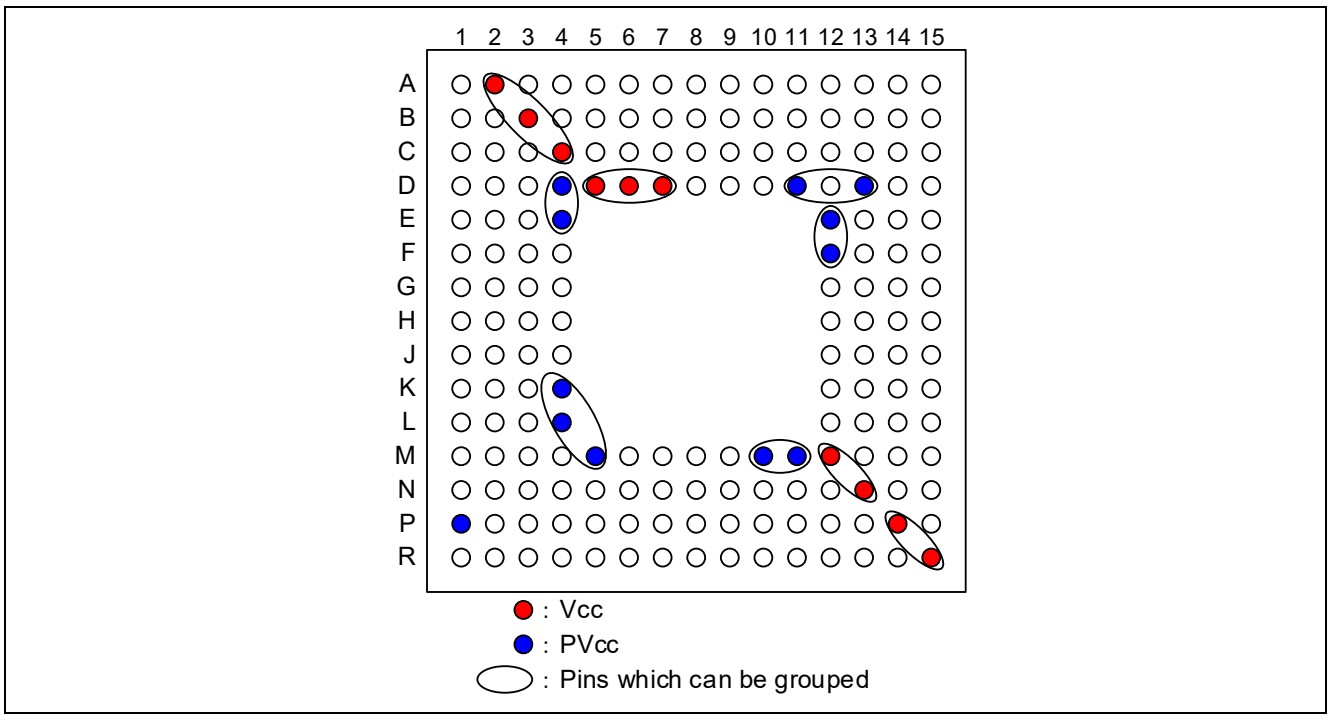


Figure 1.7 Example of 176-pin BGA power supply pin grouping (RZ/A1L) (Top perspective view)

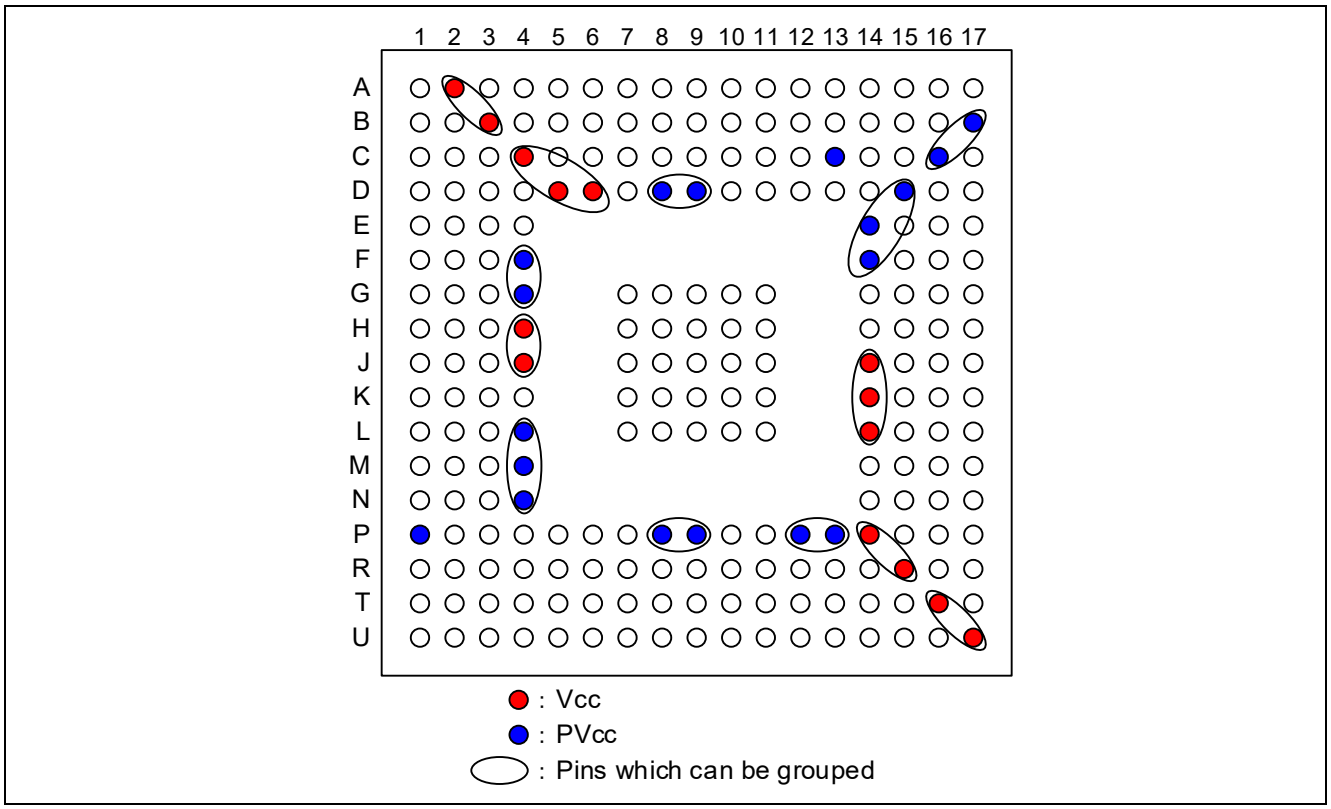


Figure 1.8 Example of 233-pin BGA power supply pin grouping (RZ/A1L) (Top perspective view)

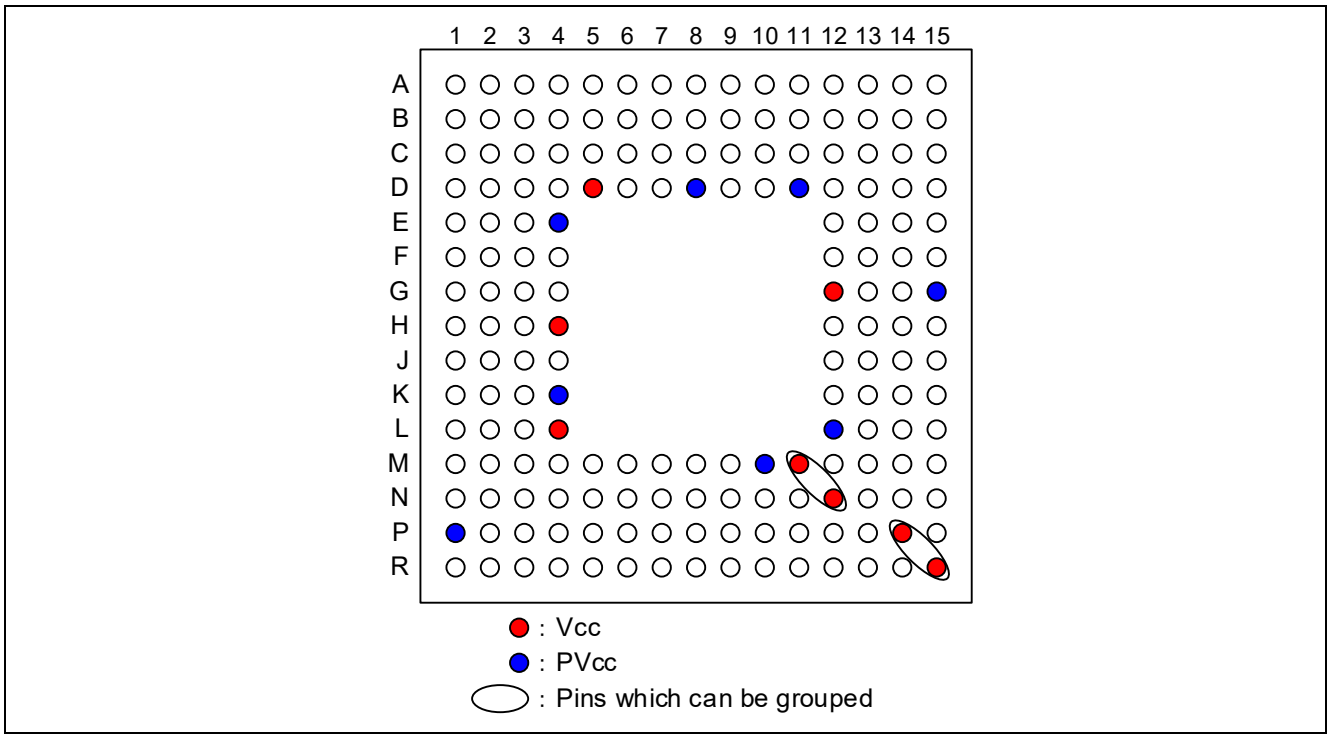


Figure 1.9 Example of 176-pin BGA power supply pin grouping (RZ/A2M) (Top perspective view)

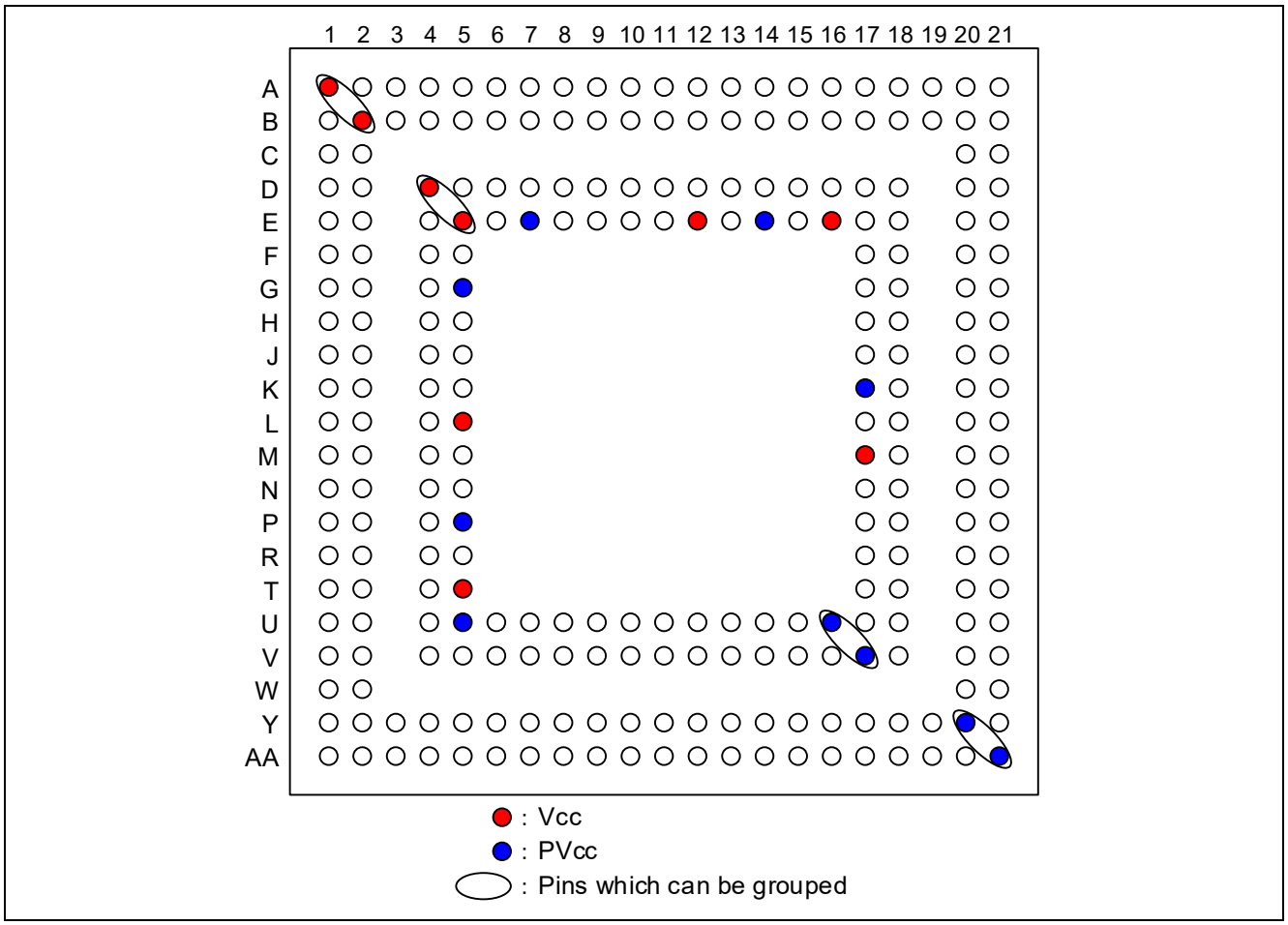


Figure 1.10 Example of 256-pin BGA power supply pin grouping (RZ/A2M) (Top perspective view)

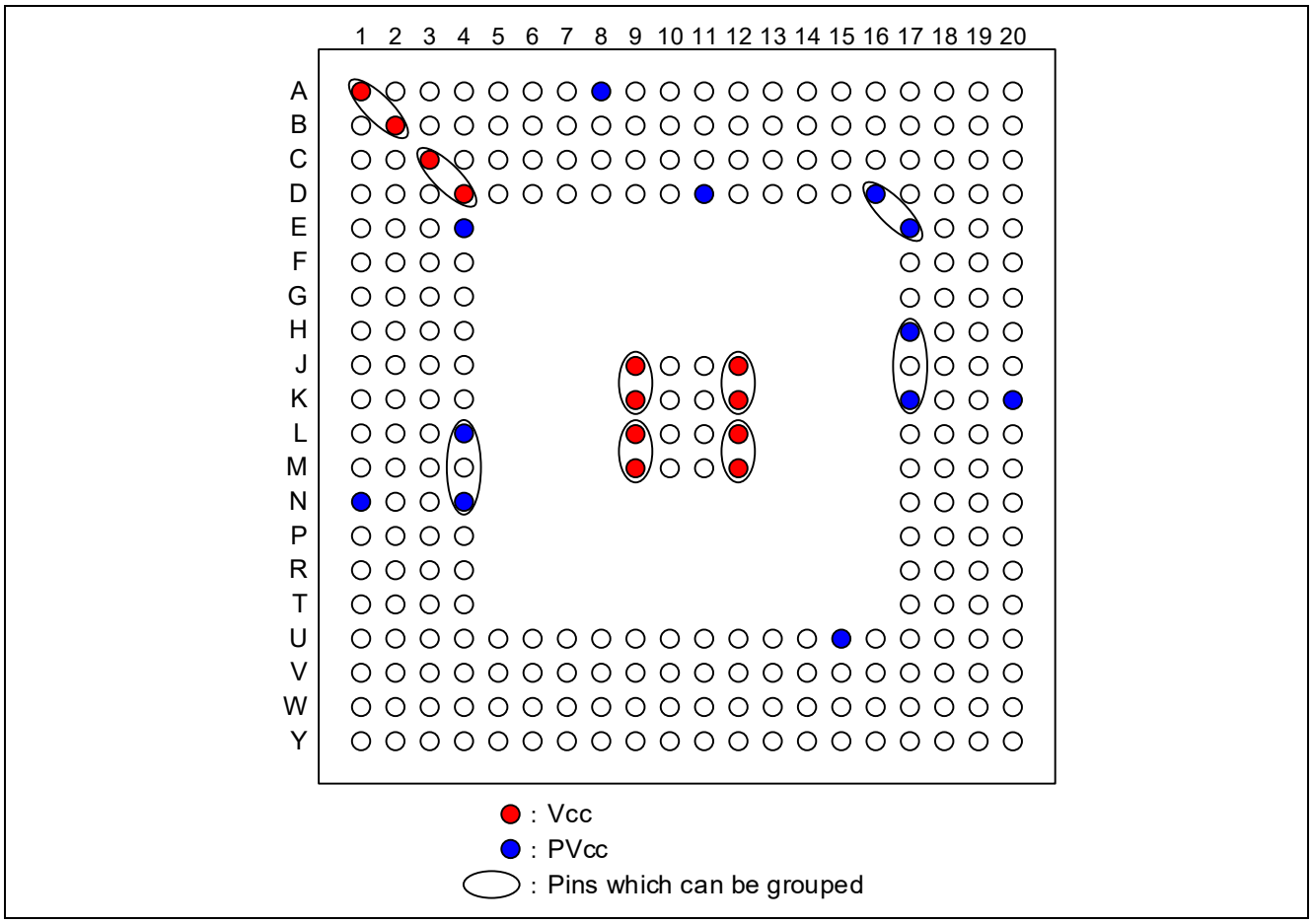


Figure 1.11 Example of 272-pin BGA power supply pin grouping (RZ/A2M) (Top perspective view)

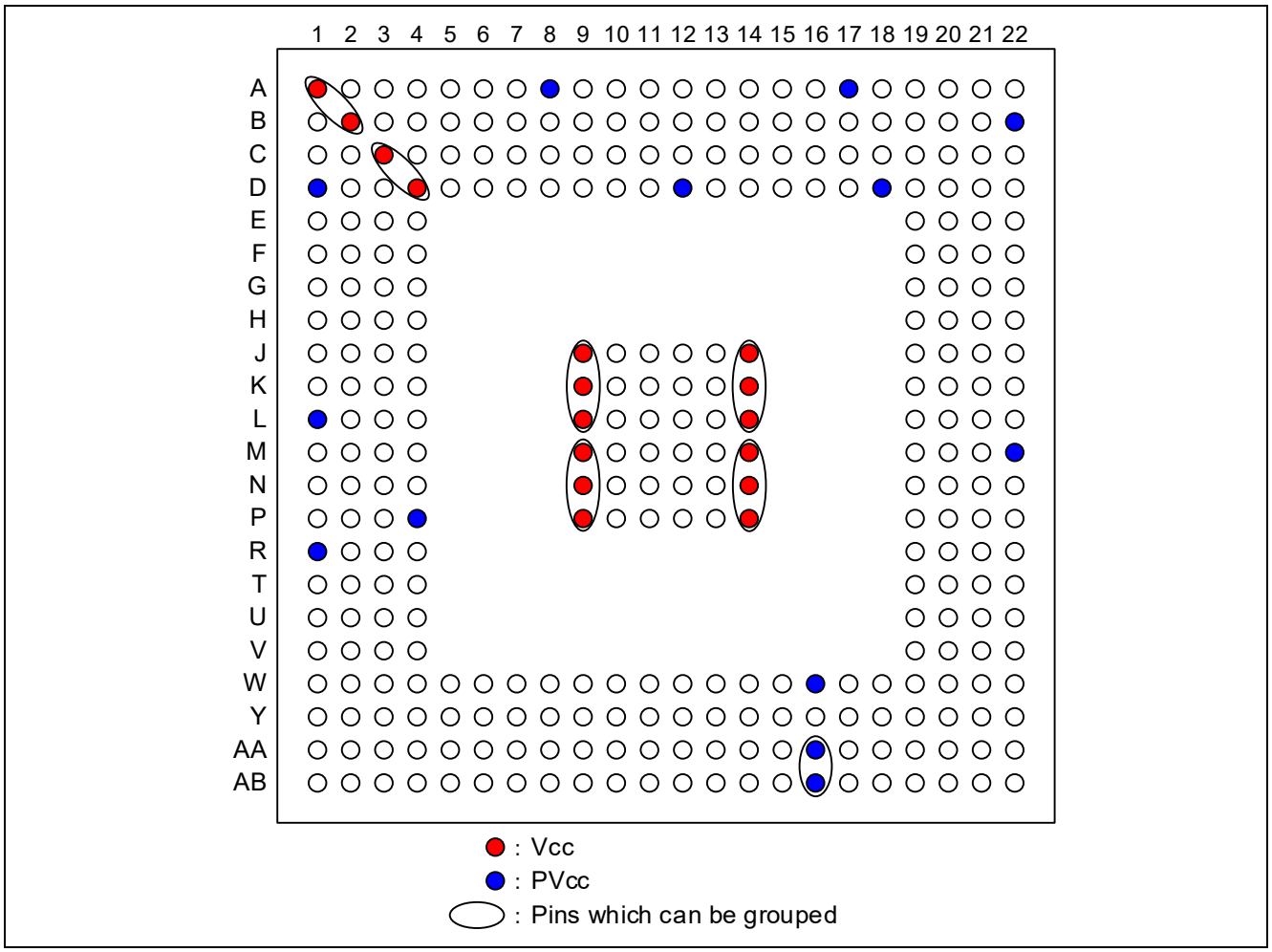


Figure 1.12 Example of 324-pin BGA power supply pin grouping (RZ/A2M) (Top perspective view)

2. Reset

2.1 Power ON and Power OFF Sequences

There is no particular order required for turning the 1.2-V power supply*1, 1.8-V power supply*1*2, 1.8-V/3.3-V switchable power supply*1*2 and 3.3-V power supply*1 on or off.

When turning power on, ensure that TRST# pin and RES# pin are set to low level *3. If this is not observed, the output from the output pin or the I/O pin will become undefined, which may cause erroneous operation or malfunctions in the overall system.

When turning power off, if there is the possibility of the problem described above, ensure that TRST# pin and RES# pin are set to low level.

In addition, ensure that the power on timing requirement shown in Table 2.1 are satisfied.

Notes: *1. For breakdowns of each power supply, refer to Table 1.1 and Table 1.2.
*2. This power supply is not present in RZ/A1.
*3. For details, refer to Table 2.2 and Figure 2.5.

Table 2.1 Timing requirements

Item	Symbol	Min.	Max.	Unit	Reference Figure
SSCG stabilizing time *1*2	tSSCG	1	-	µs	Figure 2.1
RES# input rise time*3	tRSr	-	500	µs	Figure 2.2
RES# negating hold time*1*4	tRSNH	0	-	ns	Figure 2.3
Mode hold time	tMDH	200	-	ns	Figure 2.4

Notes: *1. This stipulation is not present in RZ/A2M.
*2. Ensure that this requirement is satisfied if the SSCG function is used.
*3. For RZ/A1, ensure that this item is satisfied if the TRST# pin and RES# pin are controlled using the same signal.
*4. Ensure that this item is satisfied if the TRST# pin and RES# pin are controlled using different signals separately.

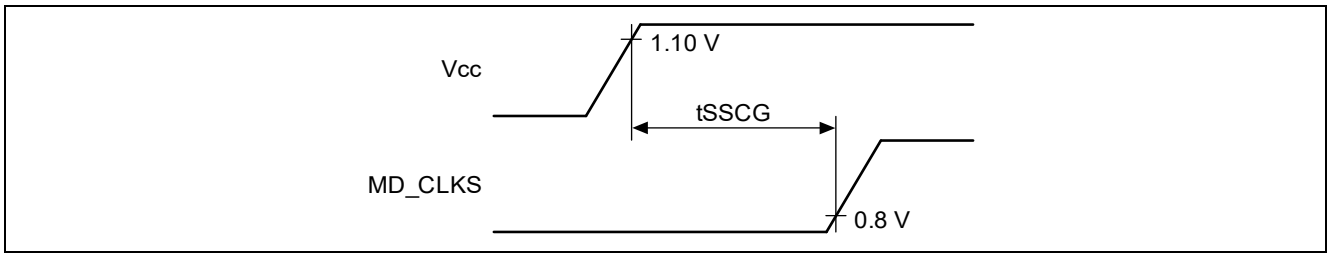


Figure 2.1 SSCG stabilizing time

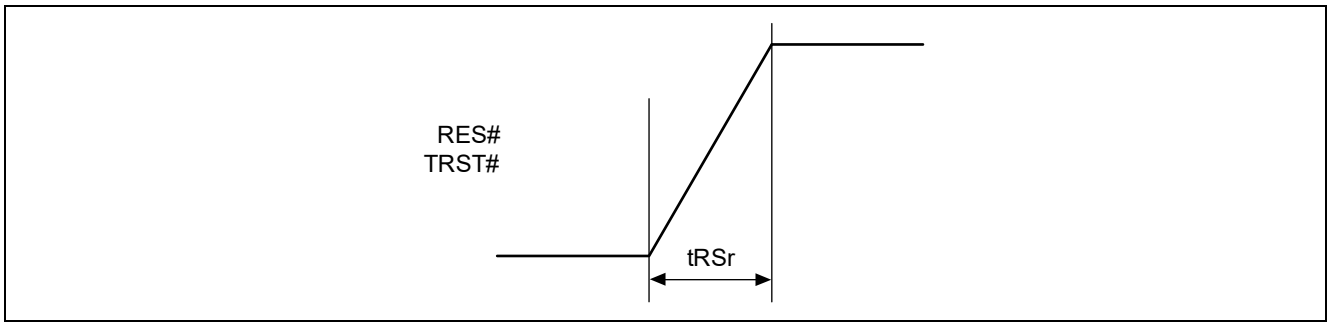
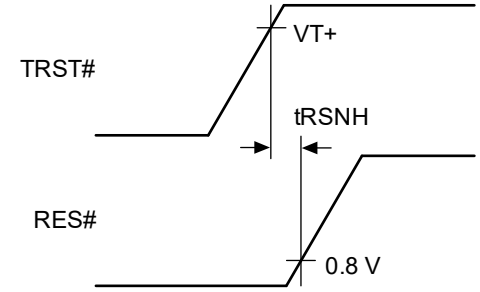
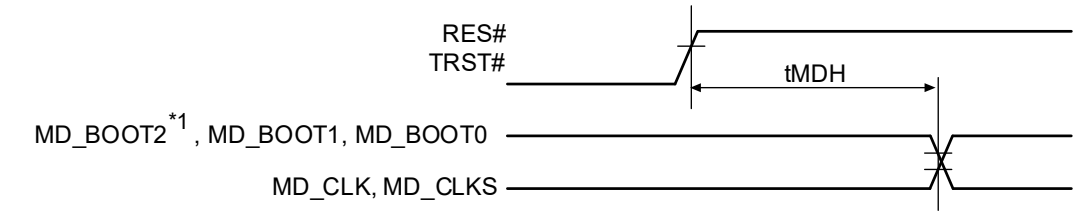


Figure 2.2 RES# input rise time



Note: VT+ values are shown below.
RZ/A1L : PVcc × 0.665 V
RZ/A1HM : PVcc × 0.66 V

Figure 2.3 RES# negating hold time



Note: *1. This pin is not present in RZ/A1L.

Figure 2.4 Mode hold time

2.2 Oscillation Settling Time

If the RES# pin is set to low level, LSI of this series will change to the power on reset state. In order to definitively reset LSI of this series, ensure that the RES# pin and TRST# pin are maintained at low level for the power on oscillation settling time (tROSC + tPOSC) while power supply is switched on.

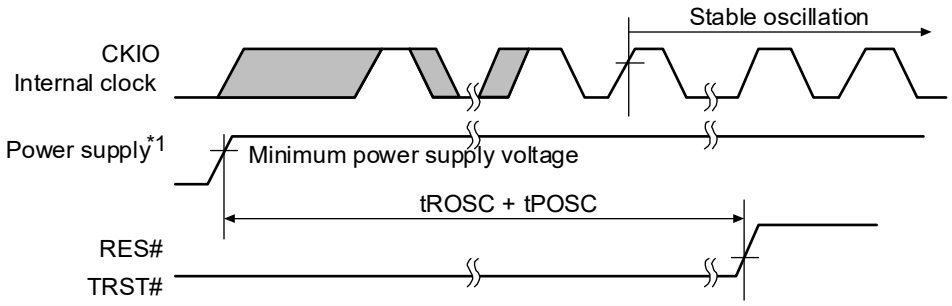
The power on oscillation settling time is stipulated as the time from when the power supply voltage rises above the minimum value until the RES# pin has exceeded the VIL Max. Table 2.2 shows the timing requirements of power on oscillation settling time and Figure 2.5 shows the power on oscillation settling time.

Power on reset control is possible by using the reset IC such as Renesas Electronics ISL88014. Figure 2.6 shows a connection example for the reset IC.

Table 2.2 Timing requirements of power on oscillation settling time

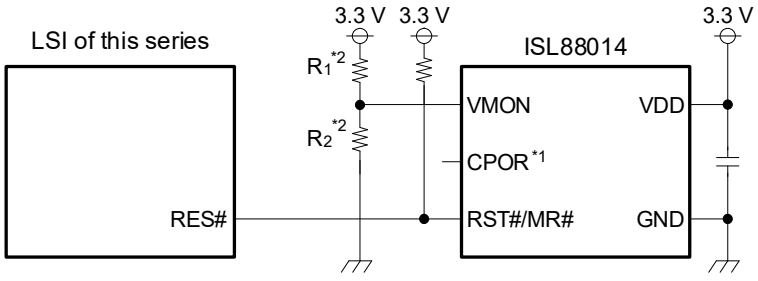
Item	Symbol	Min.	Max.	Unit
On-chip PLL circuit oscillation settling time	tPOSC	1	-	ms
On-chip oscillation circuit oscillation settling time*1	tROSC	-	4*2	ms

Note: *1. When use external clock, this time is unnecessary.
*2. Settings for values smaller than the above specifications may be possible, as long as the values are confirmed through evaluation by the manufacturer of the oscillator.



Note: *1. For details of each power supply, refer to Table 1.1 and Table 1.2.

Figure 2.5 Power on oscillation settling time



Notes: *1. By connecting a capacitor between the CPOR pin and ground, the reset signal can be delayed. For details, refer to the ISL88014 data sheet.
*2. The formula to determine monitor voltage and an example of resistor values when monitor voltage is set to 3 V are shown below.

$$\text{Monitor voltage} = 0.6 \times \frac{(R_1 + R_2)}{R_2} = 0.6 \times \frac{(56\ \text{k}\Omega + 14\ \text{k}\Omega)}{14\ \text{k}\Omega} = 3\ \text{V}$$

When setting the monitor voltage, determine the values of resistors after taking into account the errors (tolerances) of resistors and reset IC monitor voltage.

Figure 2.6 Example of reset IC connection

3. Oscillator Circuit

3.1 Clock Pins

Table 3.1 shows pins to which a crystal resonator can connect or a clock can be input, and their frequencies.

If the clock pin is not used, fix the Xin pin (pull-up, pull-down, or ground connection), and set the Xout pin to open-circuit.

Table 3.1 Clock pins

Xin Pin*1	Xout Pin*1	Comments		Applicable LSIs
EXTAL	XTAL	EXTAL clock input frequency (When providing clock to USB2.0 host/function module)	12 MHz ± 100ppm	RZ/A1
			12 MHz ± 100ppm 24 MHz ± 100ppm *2	RZ/A2M
		EXTAL clock input frequency (When not providing clock to USB2.0 host/function module)	10 MHz to 13.33 MHz	RZ/A1
			10 MHz to 12 MHz 20 MHz to 24 MHz *2	RZ/A2M
USB_X1	USB_X2	During high speed operation	48 MHz ± 100ppm	RZ/A1
		During non-high speed operation and during host operation	48 MHz ± 500ppm	
		During non-high speed operation and during function operation	48 MHz ± 2500ppm	
		USB_X1 clock input frequency (When providing 48MHz clock to USB2.0 host/function module)	48 MHz ± 100ppm	RZ/A2M
AUDIO_X1	AUDIO_X2	When a crystal resonator is connected	10 MHz to 50 MHz	RZ/A Series
		When external clock is input	1 MHz to 50 MHz	
RTC_X1	RTC_X2	32.768 kHz		RZ/A Series
RTC_X3	RTC_X4	4 MHz		RZ/A1HM
VIDEO_X1	VIDEO_X2	27 MHz ± 50ppm*3		RZ/A1HM

Notes: *1. When using an external clock, input to Xin pin, when using a crystal resonator, connect between Xin pin and Xout pin.

*2. Input frequency range changes according to MD_CLK pin. For details, refer to "Table 4.14 Clock mode setting pin and clock I/O relationship".

*3. Reference value. The accuracy of the clock signal affects the quality of images output by the digital video decoder. Input clock signals that are as accurate as is possible.

3.2 Example of External Clock Connection

Figure 3.1 shows an example of an external clock connection. If the Xout pin is set to an open state, the parasitic capacitance must be 10 pF or less.

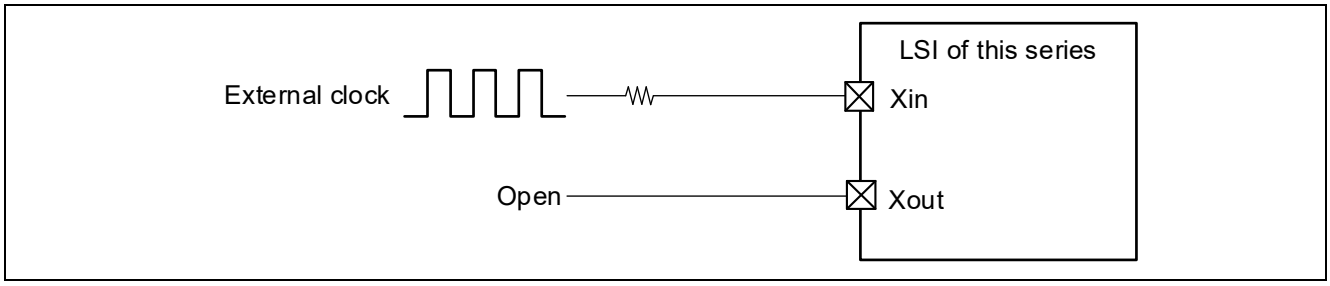


Figure 3.1 Example of external clock connection

3.3 Example of Crystal Resonator Connection

Figure 3.2 shows an example of a crystal resonator connection.

The crystal resonator and capacitors CL1 and CL2 should be placed as close as possible to the Xin pin and the Xout pin. In addition, to avoid inductance and to ensure proper oscillation, make the grounding point common for the resonator and the added capacitors, and ensure that the wiring patterns are not placed close to these parts.

Because the resonator's circuit constants will vary depending on the crystal resonator itself, the floating capacity of the implemented circuit, etc., determine the parameters (resistance and capacity value) after consulting with the resonator manufacturer*1 and performing sufficient evaluations. Although LSI of this series has an on-chip feedback resistor, an external feedback resistor may be required depending on the resonator's properties.

Note: *1. Examples of resonator and circuit matching suitable for the products for LSI of this series are shown on the resonator manufacturer website below. If the optimized resonator circuit constant for your system is necessary, ask the manufacturer of the resonator.
http://prdct-search.kyocera.co.jp/crystal-ic/?p=en_search/

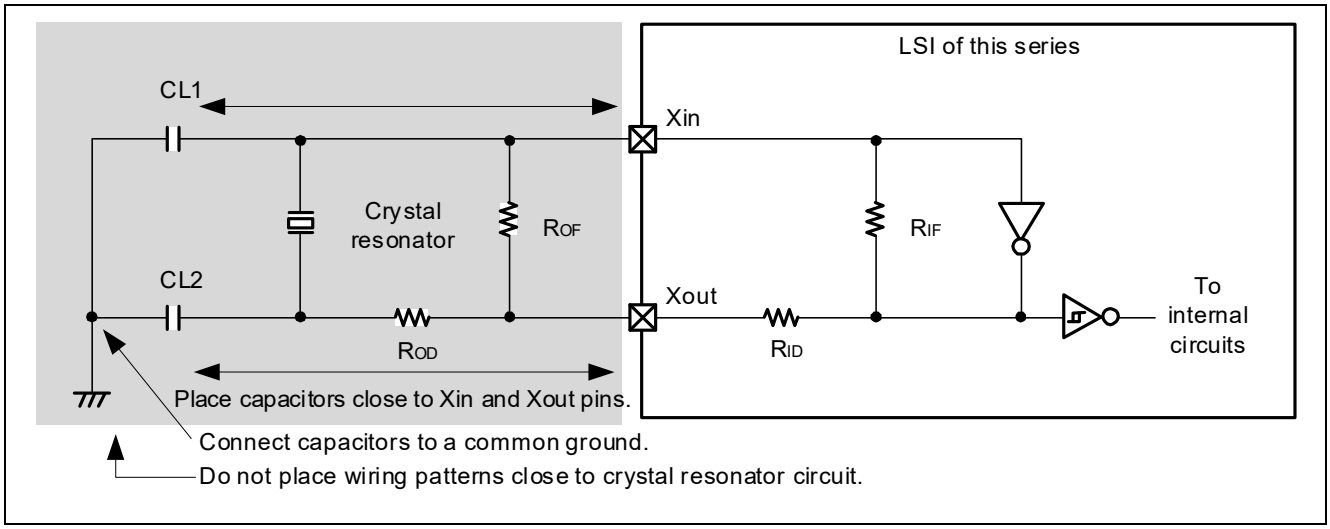


Figure 3.2 Example of crystal resonator connection

4. Operating Mode

4.1 Boot Mode

LSI of this series have the boot modes shown in Table 4.1, and the boot mode is determined using the boot mode setting pins (MD_BOOT2*1 to MD_BOOT0).

Note: *1. MD_BOOT2 pin is not present on RZ/A1L.

4.1.1 Boot Mode Setting Pin (MD_BOOT2 to MD_BOOT0)

For LSI of this series, the boot mode is determined using the boot mode setting pins when the RES# pin is set to low level. The relationship between the boot mode setting pins and the boot modes is shown in Table 4.1. In addition, Figure 5.1 to Figure 5.26 show connection examples for various boot modes.

Ensure that the mode hold time (tMDH) is satisfied on reset cancellation. For details, refer to "2.1 Power ON and Power OFF Sequences".

Table 4.1 Relationship between boot modes and boot mode setting pins (MD_BOOT2 to MD_BOOT0)

Boot Mode	RZ/A1HM			RZ/A1L		RZ/A2M			Connection Diagram
	MD_BOOT			MD_BOOT		MD_BOOT			
	2	1	0	1	0	2	1	0	
CS0 Space 16-bit Boot	N/A*1	0	0	0	0	0	0	0	Figure 5.1
CS0 Space 32-bit Boot	N/A*1	1	0	-	-	-	-	-	Figure 5.2 Figure 5.3
eSD Boot	0	1	1	0	1	0	0	1	-
eMMC Boot	1	1	1	1	1	0	1	0	Figure 5.26
Serial Flash Boot (3.3-V products)	1	0	1	1	0	0	1	1	Figure 5.10 to Figure 5.13
Octal-SPI Flash Boot (1.8-V products)	-	-	-	-	-	1	0	0	Figure 5.14 Figure 5.19
HyperFlash Boot 1 (1.8-V products)	-	-	-	-	-	1	0	1	Figure 5.15
OctaFlash Boot (1.8-V products)	-	-	-	-	-	1	1	0	Figure 5.20
HyperFlash Boot 2 (1.8-V products)	-	-	-	-	-	1	1	1	Figure 5.16

Note: *1. N/A (Not Applicable) indicates that the pin state can be either 0 or 1.

4.1.2 CS0 Space 16-bit Boot

Boot from memory (16-bit bus width) connected to CS0 space.

Table 4.2 shows the pins for which the boot program sets functions in this boot mode.

The initial state for pins from A25 to A21 is as general purpose ports*1, and therefore if the output is indefinite, access to the intended addresses may not be possible. Therefore, if using pins from A25 to A21, use an external pull-down.

An example of connection supported by this boot mode is shown in Figure 5.1.

Note: *1. For RZ/A1, these become the general purpose input port, and for RZ/A2M, these become the general purpose I/O ports in Hi-Z state.

Table 4.2 Pins used in CS0 space 16-bit boot mode

Pin Name	Port		
	RZ/A1HM	RZ/A1L	RZ/A2M*1
A20 to A1	P8_12 to P8_0, P7_15 to P7_9	P4_3 to P4_0, P3_15 to P3_0	PA_4 to PA_0, P9_7 to P9_0, P8_7 to P8_1
D15 to D0	P6_15 to P6_0	P5_15 to P5_0	P2_3 to P2_0, P1_4 to P1_0, P0_6 to P0_0
CS0#	P7_0	P2_7	PB_3
RD#	P7_8	P2_8	P7_7
CKIO	CKIO	CKIO	CKIO

Note: *1. Only for 324-pin BGA package.

4.1.3 CS0 Space 32-bit Boot

Boot from memory (32-bit bus width) connected to CS0 space.

Table 4.3 shows the pins for which the boot program sets functions in this boot mode.

The initial state for pins from A25 to A21 is as general purpose ports, and therefore if the output is indefinite, access to the intended addresses may not be possible. Therefore, if using pins from A25 to A21, use an external pull-down.

Examples of connection supported by this boot mode are shown in Figure 5.2 and Figure 5.3.

Table 4.3 Pins used in CS0 space 32-bit boot mode

Pin Name	Port		
	RZ/A1HM	RZ/A1L	RZ/A2M
A20 to A2	P8_12 to P8_0, P7_15 to P7_10	-	-
D31 to D0	P2_15 to P2_0, P6_15 to P6_0	-	-
CS0#	P7_0	-	-
RD#	P7_8	-	-
CKIO	CKIO	-	-

4.1.4 eSD Boot

Boots from the on-chip NAND flash memory*1 for the SD controller connected to Channel 0 on the SD Host Interface*2.

Table 4.4 shows the pins for which the boot program sets functions in this boot mode.

For RZ/A2M, fix the unused pins from SD0_DAT7 to SD0_DAT4 (pull-up/pull-down). For details, refer to "7.2 Treatment of Unused Pins".

In this boot mode, the write protect pin*3 and card detection pin*4 are not used. Treat pins in accordance with software specifications.

Notes: For development of SD host related products, conclusion of an SD Host/Ancillary Product License Agreement (SD HALA) is necessary.
*1. It is possible to boot the LSI from the embedded SD (eSD) defined by the SD specification part 1 eSD addendum version 2.10 standard.
*2. For RZ/A2M, this is an SD/MMC Host Interface.
*2. Pin names are SD_WP_0 in RZ/A1 and SD0_WP in RZ/A2M.
*3. Pin names are SD_CD_0 in RZ/A1 and SD0_CD in RZ/A2M.

Table 4.4 Pins used in eSD boot

Pin Name	Port		
	RZ/A1HM	RZ/A1L	RZ/A2M
SD_CLK_0	P4_12	P3_3	-
SD_CMD_0	P4_13	P3_2	-
SD_D3_0 to SD_D0_0	P4_14, P4_15, P4_10, P4_11	P3_1, P3_0, P3_5, P3_4	-
SD0_CLK	-	-	SD0_CLK
SD0_CMD	-	-	SD0_CMD
SD0_DAT3 to SD0_DAT0	-	-	SD0_DAT3 to SD0_DAT0

4.1.5 eMMC Boot

Boots from the on-chip NAND flash memory*1 for the MMC controller connected to Channel 0 on the MMC Host Interface*2 (4-bit width for RZ/A1 and 8-bit width for RZ/A2M).

Table 4.5 shows the pins for which the boot program sets functions in this boot mode.

Examples of the connection supported by this boot mode are shown in Figure 5.26 and Figure 5.27.

Note: *1. Boot is possible only from eMMC devices which comply with the JEDEC STANDARD JESD84 A44 (MMCA 4.4). (Cannot boot from MMC card.)
*2. For RZ/A2M, this is an SD/MMC Host Interface.

Table 4.5 Pins used in eMMC boot

Pin Name	Port		
	RZ/A1HM	RZ/A1L	RZ/A2M
MMC_CLK	P3_12	P7_4	-
MMC_CMD	P3_13	P7_5	-
MMC_D3 to MMC_D0	P3_14, P3_15, P3_10, P3_11	P7_6, P7_7, P7_2, P7_3	-
SD0_CLK	-	-	SD0_CLK
SD0_CMD	-	-	SD0_CMD
SD0_DAT7 to SD0_DAT0	-	-	SD0_DAT7 to SD0_DAT0
SD0_RST#	-	-	SD0_RST#

4.1.6 Serial Flash Boot (3.3-V products)

Boot from serial flash memory (3.3-V products) connected to SPI multi-I/O bus space.

Table 4.6 shows the pins for which the boot program sets functions in this boot mode.

In this boot mode, after released from the reset state, because read is performed from the serial flash memory setting as shown in Table 4.7, ensure that products which satisfy these are used.

Examples of connection supported by this boot mode are shown in Figure 5.10 to Figure 5.13.

Table 4.6 Pins used in serial flash boot

Pin Name	Port		
	RZ/A1HM	RZ/A1L	RZ/A2M
SPBCLK_0	P9_2	P4_4	-
SPBSSL_0	P9_3	P4_5	-
SPBMO0_0	P9_4	P4_6	-
SPBMI0_0	P9_5	P4_7	-
QSPI0_SPCLK	-	-	QSPI0_SPCLK
QSPI0_SSL	-	-	QSPI0_SSL
QSPI0_IO0	-	-	QSPI0_IO0
QSPI0_IO1	-	-	QSPI0_IO1

Table 4.7 Serial flash boot settings

Item	Description
Bit rate*1	12.5 MHz to 16.67 MHz (RZ/A1) 13.75 MHz to 16.5 MHz (RZ/A2M)
Opcode	READ (03h)
Address cycle	3 bytes
Dummy cycle	None
Bus width	1-bit
CPOL	Positive polarity
CPHAR	Receive data on odd number edge (RZ/A1) Receive data on even number edge (RZ/A2M)
CPHAT	Transmit data on even number edge

Note: *1. RZ/A1 : SPBCLK_0
RZ/A2M : QSPI0_SPCLK
Bit rate is dependent on input frequency.

4.1.7 Octal-SPI Flash Boot (1.8-V products)

Boot from Octal-SPI flash memory connected to SPI multi-I/O bus space (1.8-V products).

Table 4.8 shows the pins for which the boot program sets functions in this boot mode.

In this boot mode, RZ/A2M operates the same as serial flash boot.

Examples of connection supported by this boot mode are shown in Figure 5.14 and Figure 5.19.

Table 4.8 Pins used in Octal-SPI flash boot

Pin Name	Port		
	RZ/A1HM	RZ/A1L	RZ/A2M
QSPI0_SPCLK	-	-	QSPI0_SPCLK
QSPI0_SSL	-	-	QSPI0_SSL
QSPI0_IO0	-	-	QSPI0_IO0
QSPI0_IO1	-	-	QSPI0_IO1

4.1.8 HyperFlash Boot 1 (1.8-V products)

Boot from HyperFlash connected to SPI multi-I/O bus space (1.8-V products).

Table 4.9 shows the pins for which the boot program sets functions in this boot mode.

An example of connection supported by this boot mode is shown in Figure 5.15.

Table 4.9 Pins used in HyperFlash boot 1

Pin Name	Port		
	RZ/A1HM	RZ/A1L	RZ/A2M
QSPI0_SSL	-	-	QSPI0_SSL
QSPI0_SPCLK	-	-	QSPI0_SPCLK
QSPI1_SPCLK	-	-	QSPI1_SPCLK
QSPI0_IO3 to QSPI0_IO0	-	-	QSPI0_IO3 to QSPI0_IO0
QSPI1_IO3 to QSPI1_IO0	-	-	QSPI1_IO3 to QSPI1_IO0
QSPI1_SSL	-	-	QSPI1_SSL
RPC_RESET#	-	-	RPC_RESET#

4.1.9 OctaFlash Boot (1.8-V products)

Boot from OctaFlash connected to OctaFlash space (1.8-V products).

Table 4.10 shows the pins for which the boot program sets functions in this boot mode.

In this boot mode, after released from the reset state, because read is performed from the OctaFlash setting as shown in Table 4.11, ensure that products which satisfy these are used.

An example of connection supported by this boot mode is shown in Figure 5.20.

Table 4.10 Pins used in OctaFlash boot

Pin Name	Port		
	RZ/A1HM	RZ/A1L	RZ/A2M
OM_SCLK	-	-	OM_SCLK
OM_CS0#	-	-	OM_CS0#
OM_SIO1, OM_SIO0	-	-	OM_SIO1, OM_SIO0

Table 4.11 Settings for OctaFlash boot

Item	Description
Bit rate (OM_SCLK)*1	13.75 MHz to 16.5 MHz
Opcode	READ (03h)
Address cycle	3 bytes
Dummy cycle	None
Bus width	1-bit
CPOL	Positive polarity
CPHAR	Receive data on even number edge
CPHAT	Transmit data on even number edge

Note: *1. Bit rate is dependent on input frequency.

4.1.10 HyperFlash Boot 2 (1.8-V products)

Boot from HyperFlash connected to HyperFlash space (1.8-V products).

Table 4.12 shows the pins for which the boot program sets functions in this boot mode.

An example of connection supported by this boot mode is shown in Figure 5.16.

Table 4.12 Pins used in HyperFlash boot 2

Pin Name	Port		
	RZ/A1HM	RZ/A1L	RZ/A2M
HM_CS0#	-	-	HM_CS0#
HM_CK	-	-	HM_CK
HM_CK#	-	-	HM_CK#
HM_DQ7 to HM_DQ0	-	-	HM_DQ7 to HM_DQ0
HM_RWDS	-	-	HM_RWDS
HM_RESET#	-	-	HM_RESET#

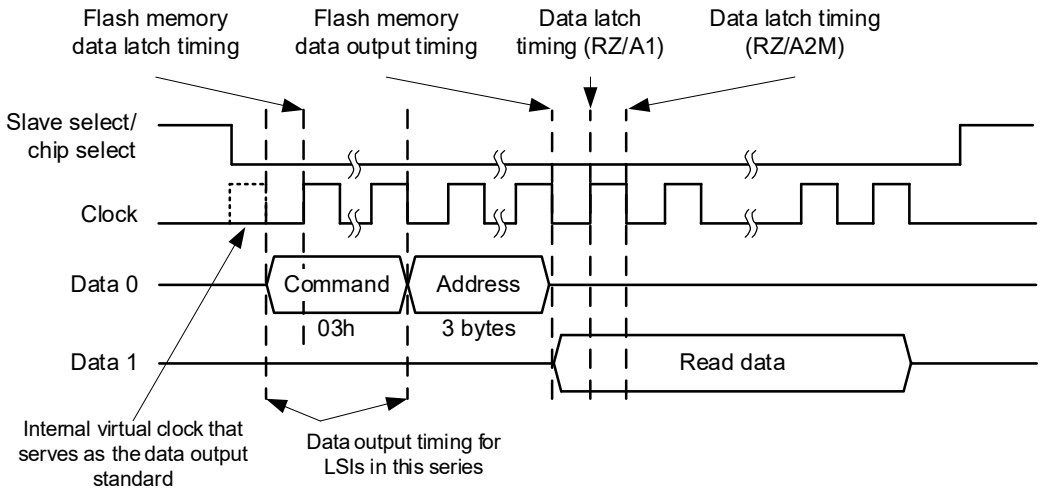
4.1.11 Points of caution when selecting flash memory for use as boot memory

When selecting flash memory used for serial flash boot, Octal-SPI flash boot OctaFlash boot, select a product which can receive the read command issued by LSI of this series when released from the reset state (refer to Figure 4.1). The selection criteria are shown below.

1. Flash memory with independent reset pin
   When cancelling busy state and initializing operation mode by reset signal input, if the reset pin is multiplexed and set as pin for another function, the reset may not be received and initialization may not be possible.
   E.g.: If the RESET#/SIO3 pin is set to SIO3, reset input may not be received.

2. Flash memory that is initialized to a 3-byte address cycle and 1-bit command bit width by reset signal
   Flash memory that fulfills these requires are shown below.
   - Flash memory that can set the address cycle and command bit width in a volatile register
     or
   - Flash memory that can set the address cycle and command bit width using a command

   Both types should initialize to a 3-byte address cycle and 1-bit command bit width by reset signal. Do not set 4-byte address cycle or 4-bit command bit width to a non-volatile register.



Note: Pin names are shown below.

Name	I/O	Pin Name			
		Serial Flash Boot		Octal-SPI Flash Boot	OctaFlash Boot
		RZ/A1	RZ/A2M		
Slave select/ chip select	Output	SPBSSL_0	QSPI0_SSL	QSPI0_SSL	OM_CS0#
Clock	Output	SPBCLK_0	QSPI0_SPCLK	QSPI0_SPCLK	OM_SCLK
Data 0	Output	SPBMO0_0	QSPI0_IO0	QSPI0_IO0	OM_SIO0
Data 1	Input	SPBMI0_0	QSPI0_IO1	QSPI0_IO1	OM_SIO1

Figure 4.1 Read command sequence

4.2 Clock Mode

4.2.1 Clock Mode Setting Pin

LSI of this series can switches clock modes by the setting of the MD_CLKS pin while the RES# pin is set to low level. Depending on the clock mode, for RZ/A1, the clock provision source is determined, and for RZ/A2M, the clock input frequency range is determined.

The relationship between the RZ/A1 clock mode setting pin and clock I/O is shown in Table 4.13, and the relationship between the RZ/A2M clock mode setting pin and clock I/O is shown in Table 4.14.

Table 4.13 Clock mode setting pin and clock I/O relationship (RZ/A1)

Clock Mode	MD_CLK	Clock I/O		
		Supply source	Input frequency	CKIO output frequency
0	0	EXTAL/crystal resonator	10 MHz to 13.33 MHz	50 MHz to 66.67 MHz
1	1	USB_X1/crystal resonator	48 MHz*1	64 MHz

Note: *1. For acceptable error range, refer to Table 3.1 Clock pin.

Table 4.14 Clock mode setting pin and clock I/O relationship (RZ/A2M)

Clock Mode	MD_CLK	Clock I/O		
		Supply source	Input frequency	CKIO output frequency*1
0	0	EXTAL/crystal resonator	10 MHz to 12 MHz	27.5 MHz to 132 MHz (Bφ) 27.5 MHz to 66 MHz (P1φ)
1	1	EXTAL/crystal resonator	20 MHz to 24 MHz	

Note: *1. The CKIO frequency range changes according to the CKIO selection register (CKIOSEL [1:0]) setting value. For details, refer to RZ/A2M Group User's Manual: Hardware.

5. External Memory

5.1 Connectable Memory

Table 5.1 shows the memory which can be connected to LSI of this series, the supported controllers, and the maximum operating frequency.

Figure 5.1 to Figure 5.27 show examples of connection for various memories.

Table 5.1 List of connectable memory

Connectable Memory	Supported Controller	Maximum Operating Frequency			Connection Diagram
		RZ/A1HM	RZ/A1L	RZ/A2M	
Parallel NOR flash memory	Bus State Controller	66.67 MHz	66.67 MHz	132 MHz*1	Figure 5.1 to Figure 5.3
SDRAM		66.67 MHz	66.67 MHz	132 MHz*1	Figure 5.4 to Figure 5.6
EEPROM	RSPI	33.33 MHz	33.33 MHz	33 MHz	Figure 5.7
	I2C Bus Interface	400 kHz (High speed mode)	400 kHz (High speed mode)	1 MHz (High speed mode plus)	Figure 5.8
Serial flash memory	RSPI	33.33 MHz	33.33 MHz	33 MHz	Figure 5.9
	SPIBSC	66.67 MHz/SDR	66.67 MHz/DDR*2 66.67 MHz/SDR*3	66 MHz/DDR	Figure 5.10 to Figure 5.13
Xccela flash memory	SPIBSC	-	-	132 MHz/DDR	Figure 5.14
HyperFlash	SPIBSC	-	-	132 MHz/DDR	Figure 5.15
	HyperBus Controller	-	-	132 MHz/DDR	Figure 5.16
HyperRAM		-	-	132 MHz/DDR	Figure 5.17
OctaFlash	SPIBSC	-	-	132 MHz/DDR	Figure 5.19
	Octa Memory Controller	-	-	132 MHz/DDR	Figure 5.20
OctaRAM		-	-	132 MHz/DDR	Figure 5.21
NAND flash memory	NAND Flash Memory Controller*4	16.67 MHz	-	33 MHz	Figure 5.23
eSD, SD card	SD Host Interface*5	33.33 MHz (High Speed)	33.33 MHz (High Speed)	132 MHz (UHS-I/SDR104)	Figure 5.24 Figure 5.25
eMMC, MMC	MMC Host Interface*5	33.33 MHz (High Speed)	33.33 MHz (High Speed)	132 MHz (HS200)	Figure 5.26 Figure 5.27

Notes: *1. Can connect only to 324-pin BGA package.
*2. For RZ/A1LU group.
*3. For RZ/A1L group, RZ/A1LC group.
*4. NAND Flash Controller for RZ/A2M.
*5. SD/MMC Host Interface for RZ/A2M.

5.2 Parallel NOR Flash Memory

RZ/A1 can connect to 8-, 16- and 32-bit width data buses while RZ/A2M can connect to 8- and 16-bit width data buses.

When a parallel NOR flash memory is used as a boot memory, and the pins from A25 to A21 are used, place pull-down resistors for these pins. In addition, LSI of this series and the flash memory must be reset at the same time.

Figure 5.1 to Figure 5.3 show examples of parallel NOR flash memory connection.

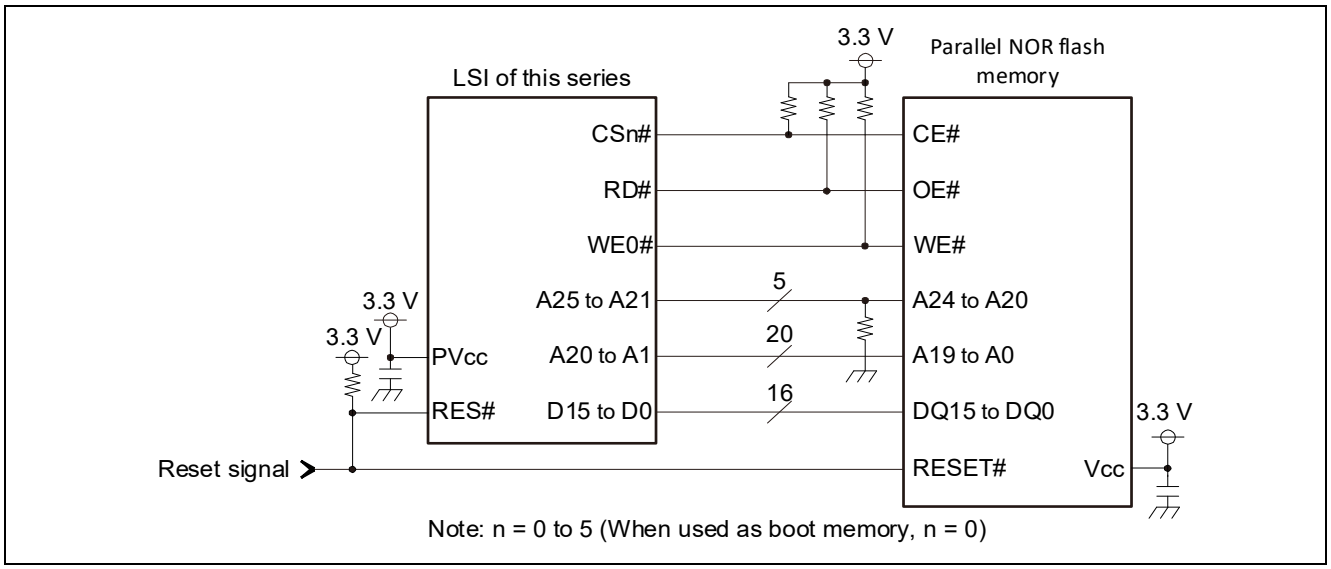


Figure 5.1 Example of parallel NOR flash memory connection 1 (16-bit width, connection to 1 x 16-bit product)

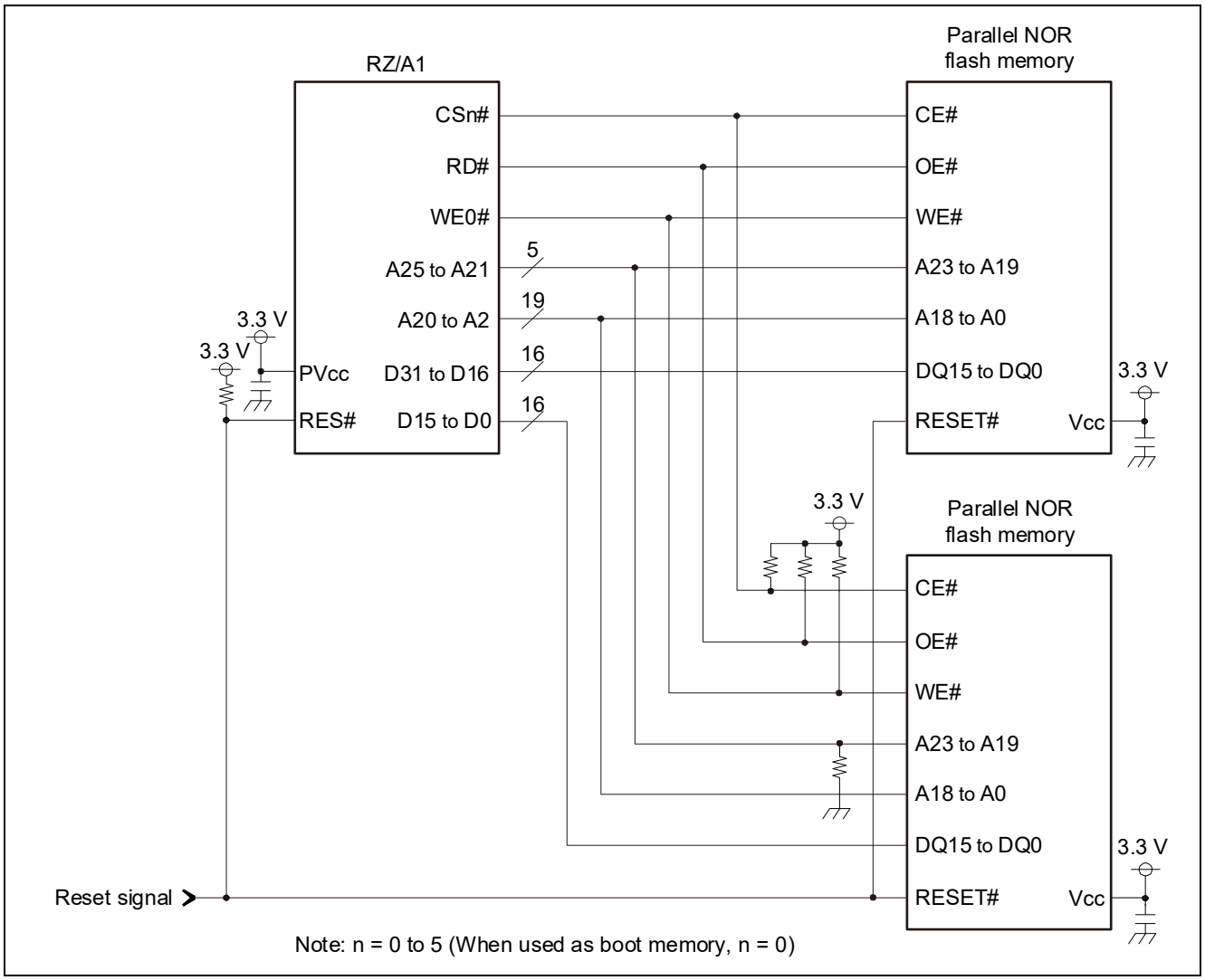


Figure 5.2 Example of parallel NOR flash memory connection 2 (32-bit width, connection to 2 x 16-bit products (RZ/A1))

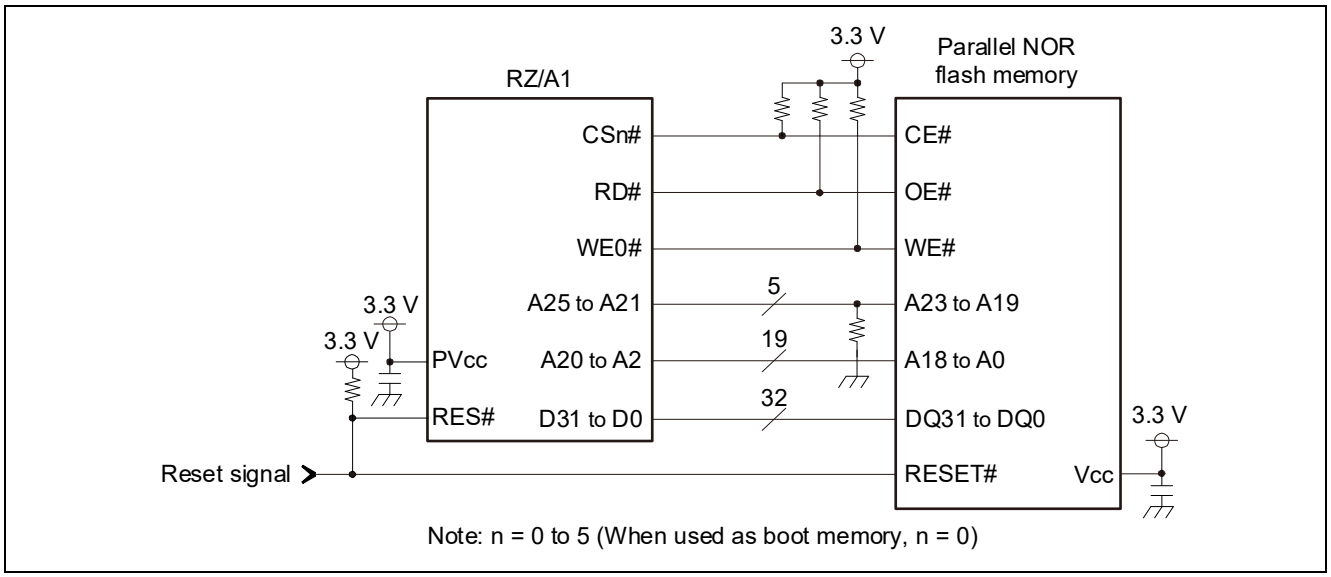


Figure 5.3 Example of parallel NOR flash memory connection 3 (32-bit width, connection to 1 x 32-bit product (RZ/A1))

5.3 SDRAM

RZ/A1 can connect to 16- and 32-bit width data buses while RZ/A2M can connect to 16-bit width data bus.

Change the treatment of CKE and DQM pins to match the SDRAM initialization sequence.

Figure 5.4 to Figure 5.6 show examples of SDRAM connection.

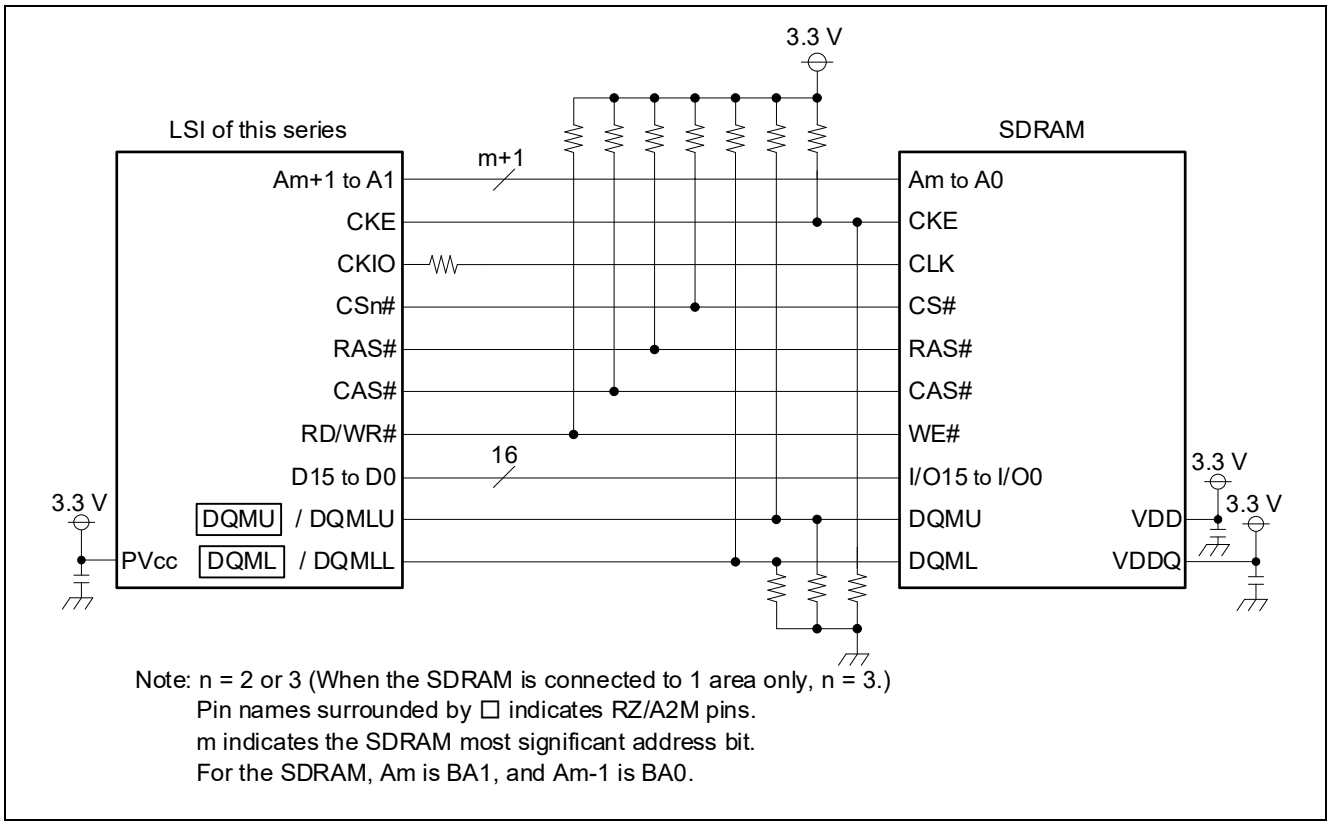


Figure 5.4 Example of SDRAM connection 1 (16-bit width, connection to 1 x 16-bit product)

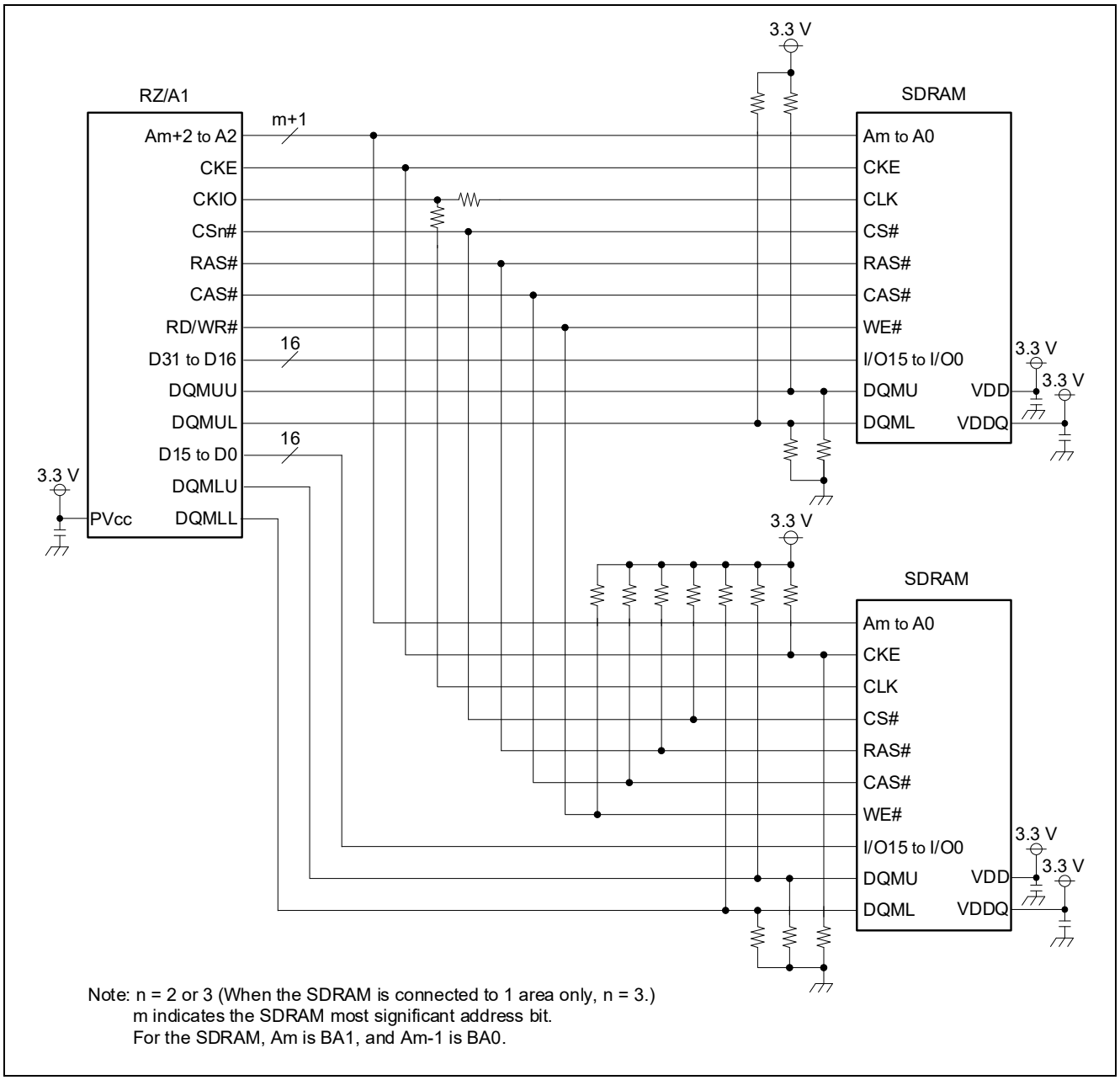


Figure 5.5 Example of SDRAM connection 2 (32-bit width, connection to 2 x 16-bit products (RZ/A1))

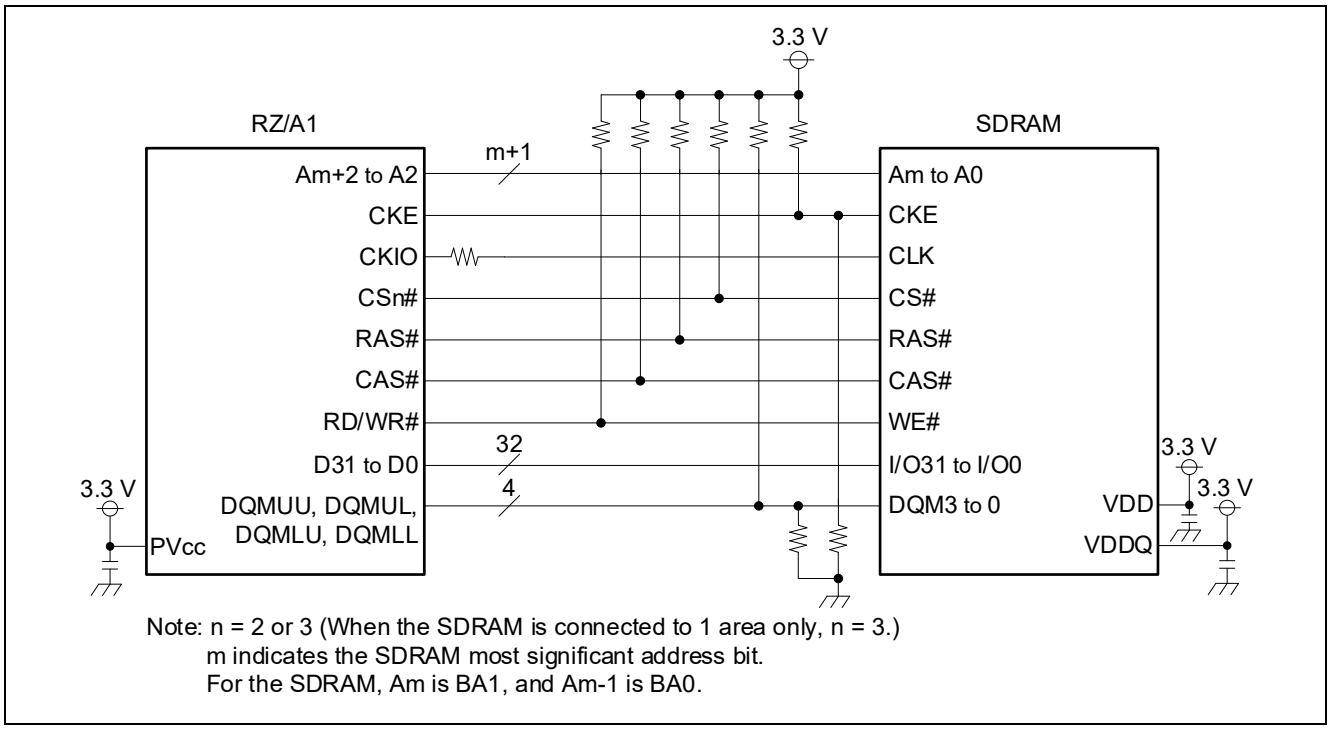


Figure 5.6 Example of SDRAM connection 3 (32-bit width, connection to 1 x 32-bit product (RZ/A1))

5.4 EEPROM

Change the treatment of W#, HOLD# and WP pins to match EEPROM polarity.

Figure 5.7 and Figure 5.8 show examples of connection between EEPROM and various controllers.

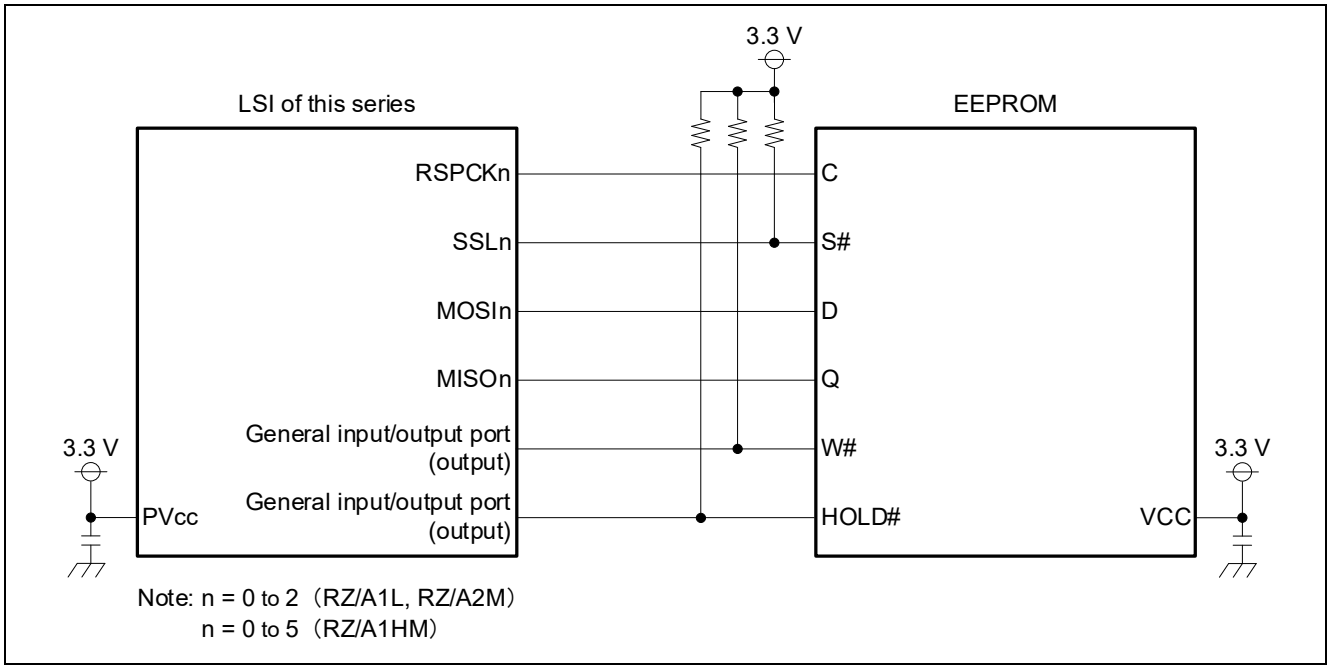


Figure 5.7 Example of EEPROM connection 1 (RSPI)

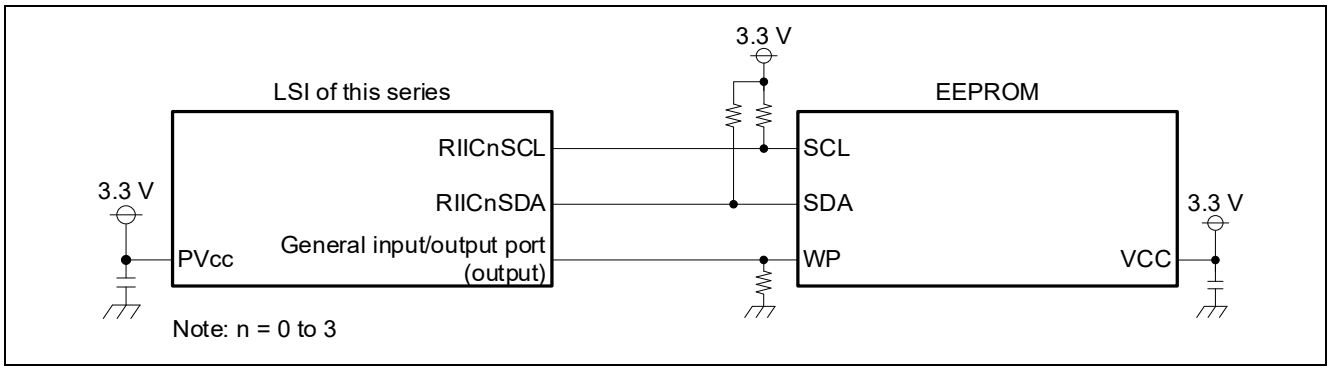


Figure 5.8 Example of EEPROM connection 2 (I2C Bus Interface)

5.5 Serial Flash Memory

RZ/A1 can connect to 1-, 2- and 4-bit width data buses while RZ/A2M can connect to 1- and 4-bit width data buses. In the case of RZ/A2M, when 2 units of serial flash are connected, 2 serial flash memory devices are connected in parallel to implement an 8-bit bus interface.

When using serial flash memory as boot memory, use the flash memory having an independent reset pin, and ensure that it must be reset at the same time as LSI of this series.

For RZ/A2M, connect the RPC_RESET# pin that outputs the reset which is synchronized to the RES# input to the flash memory RESET# pin.

For points of caution when selecting serial flash memory, refer to "4.1.11 Points of caution when selecting flash memory for use as boot memory".

Change the treatment of pins so that the data I/O pin and the multiplexed function pins match the serial flash polarity.

Figure 5.9 to Figure 5.13 show examples of connection between serial flash memory and various controllers.

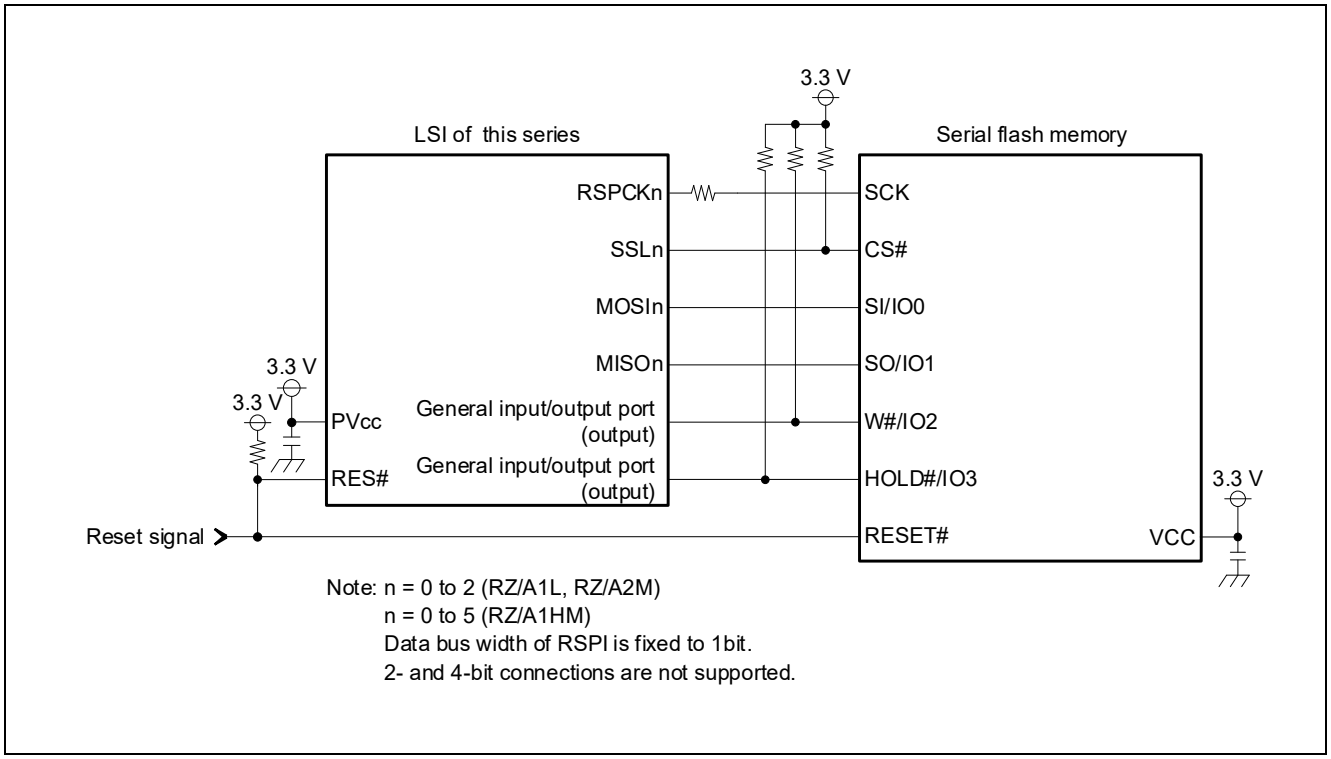


Figure 5.9 Example of serial flash memory connection 1 (RSPI)

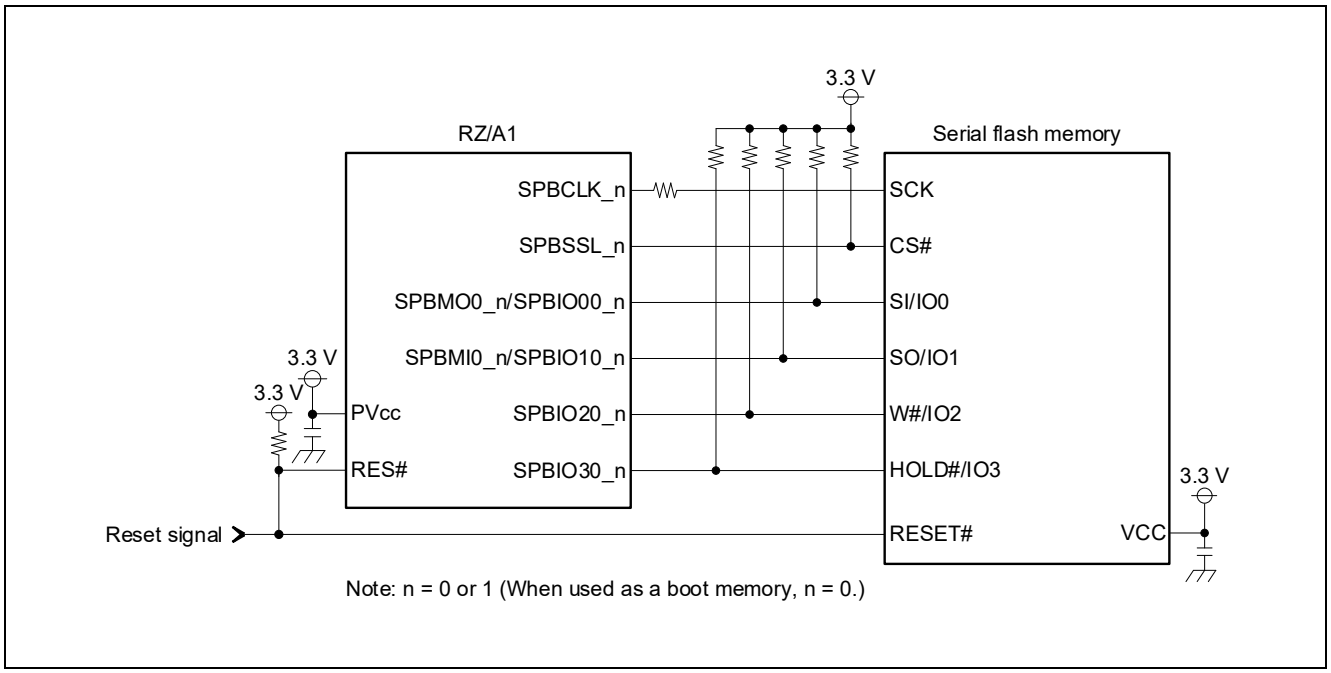


Figure 5.10 Example of serial flash memory connection 2
(SPIBSC, 4-bit bus width, connection to 1 x 4-bit product) (RZ/A1)

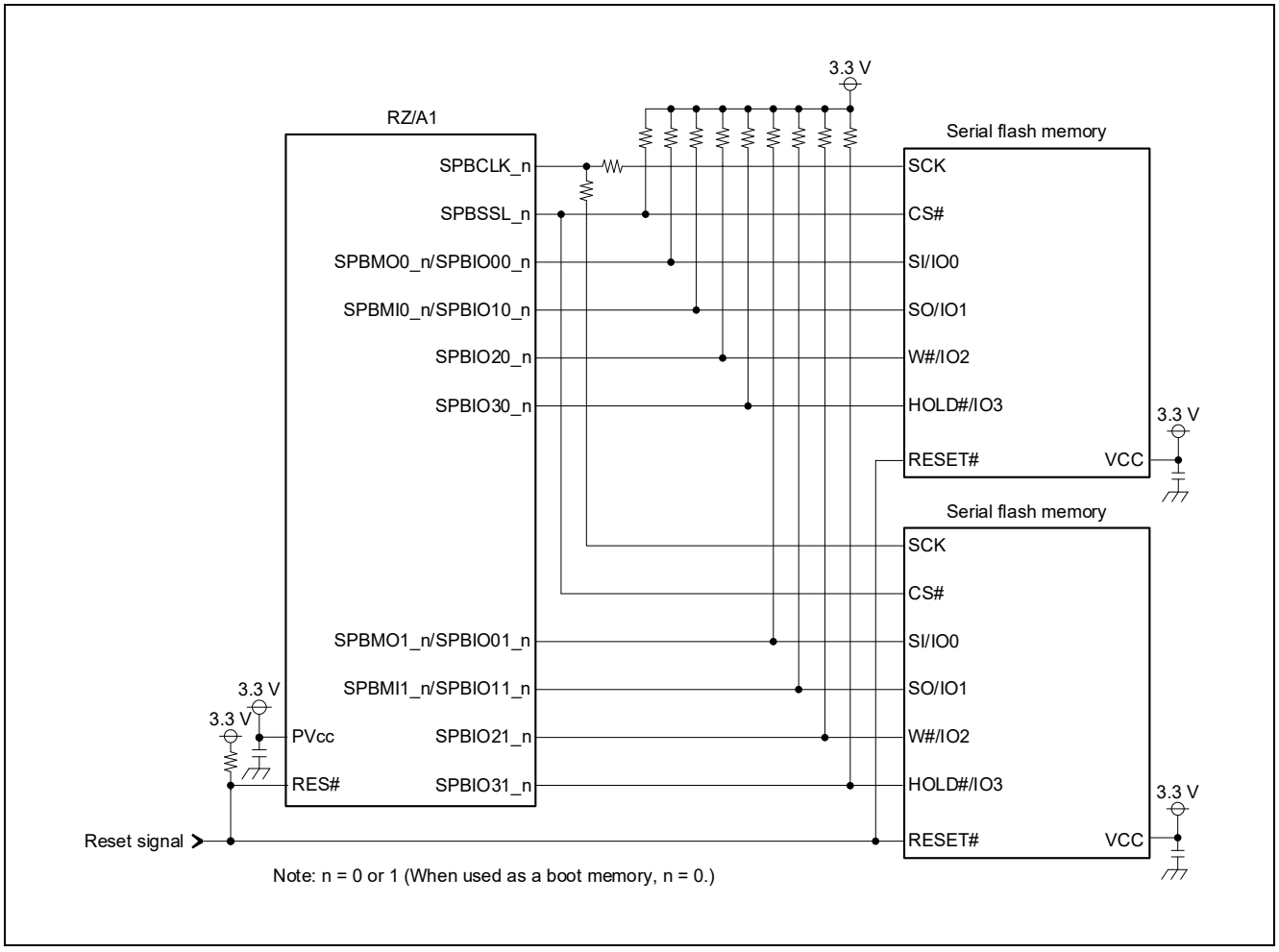


Figure 5.11 Example of serial flash memory connection 3
(SPIBSC, 8-bit bus width, connection to 2 x 4-bit products) (RZ/A1)

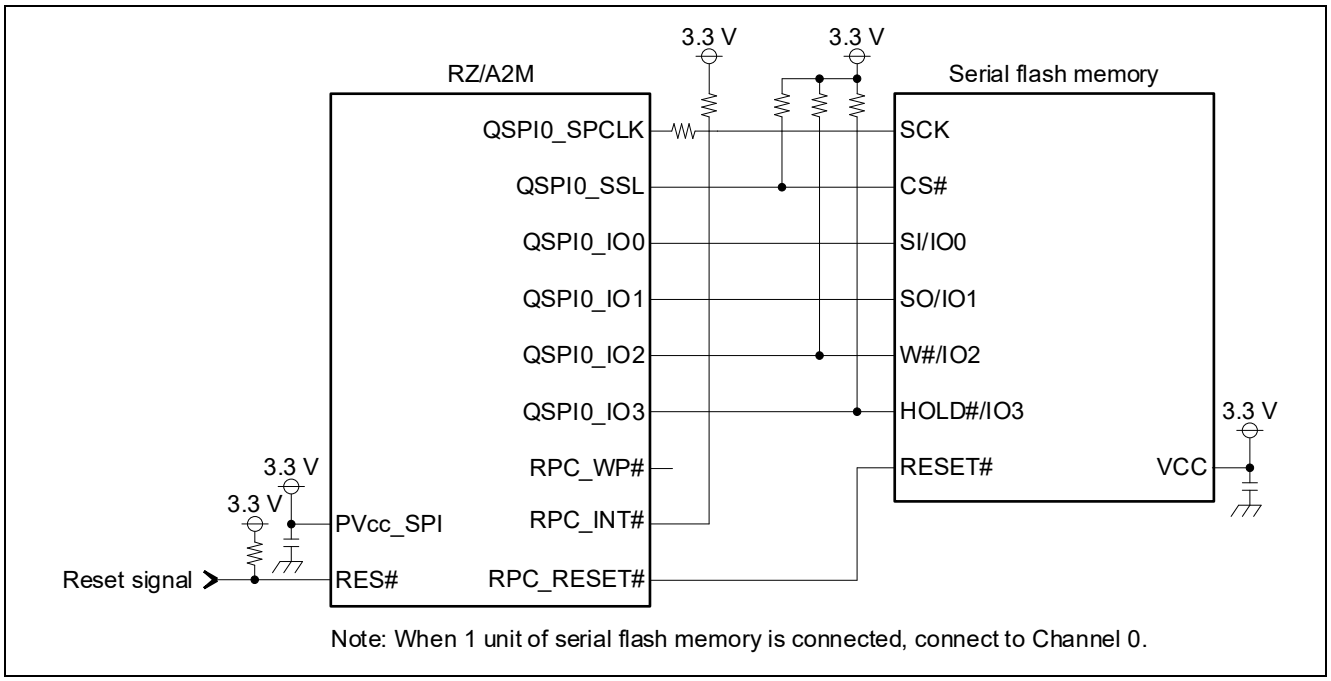


Figure 5.12 Example of serial flash memory connection 4
(SPIBSC, 4-bit bus width, connection to 1 x 4-bit product) (RZ/A2M)

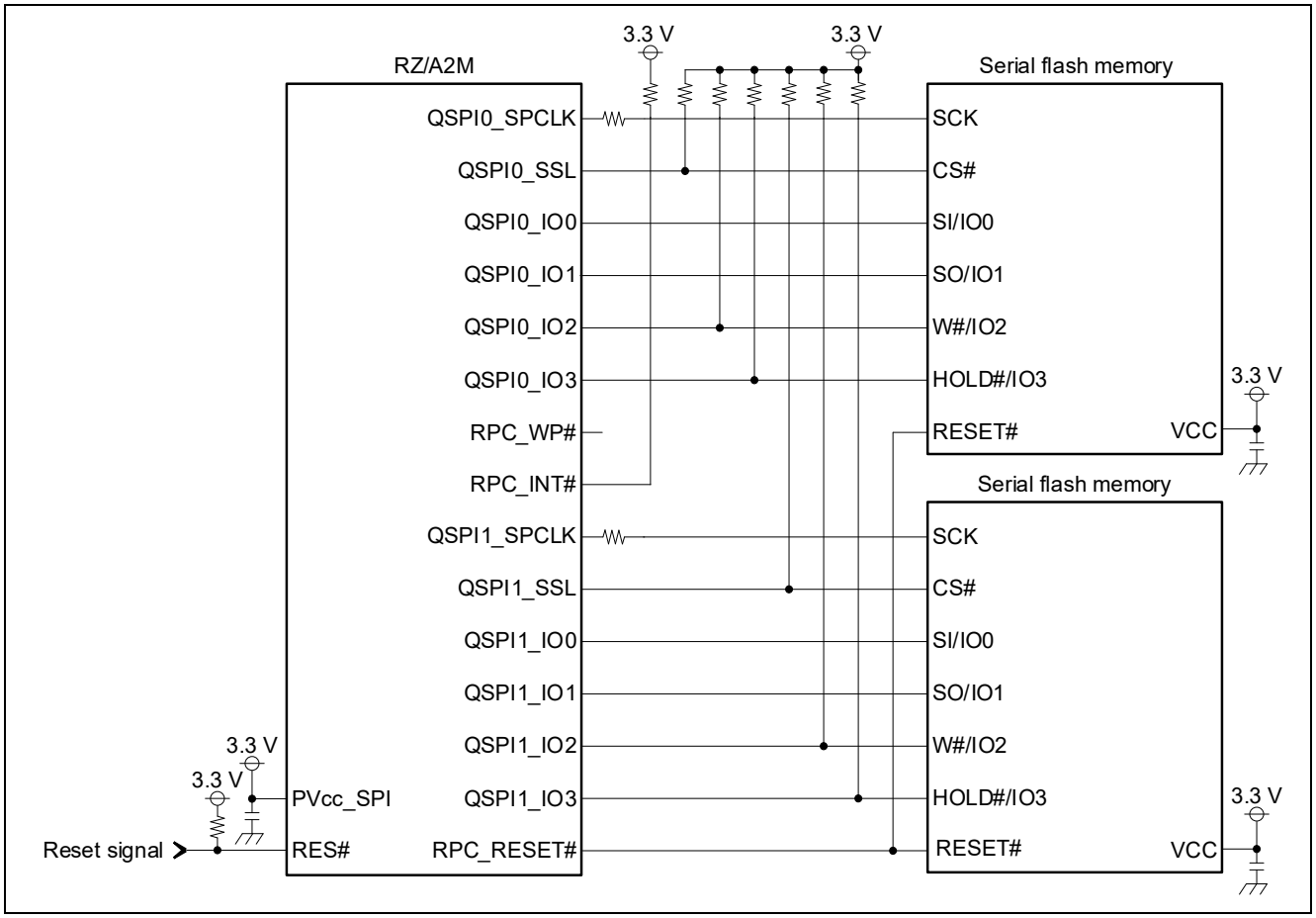


Figure 5.13 Example of serial flash memory connection 5
(SPIBSC, 8-bit bus width, connection to 2 x 4-bit products) (RZ/A2M)

5.6 Xccela Flash Memory

When using Xccela flash memory as boot memory, connect the RPC_RESET# pin that outputs the reset which is synchronized to the RES# input to the Xccela flash memory RESET# pin.

For points of caution when selecting Xccela flash memory, refer to "4.1.11 Points of caution when selecting flash memory for use as boot memory".

Figure 5.14 shows an example of Xccela flash memory connection.

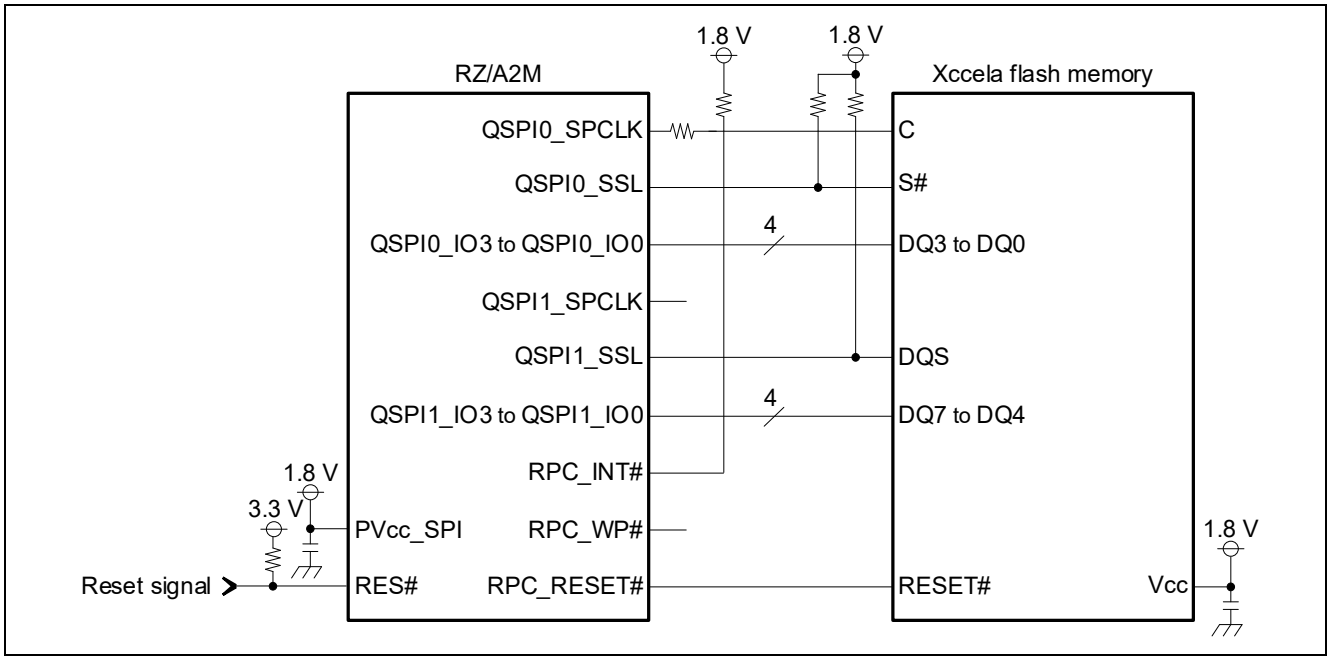


Figure 5.14 Example of Xccela flash memory connection

5.7 HyperBus Memory

When HyperBus memory is connected to a HyperBus Controller (Figure 5.16 to Figure 5.18), ensure to place a pull-down resistor of 200 kΩ or more for the HyperBus memory RWDS pin.

5.7.1 HyperFlash

When using HyperFlash as boot memory, connect the RPC_RESET# pin that outputs the reset which is synchronized to the RES# input or the HM_RESET#/OM_RESET# pin to the HyperFlash RESET# pin.

Figure 5.15 and Figure 5.16 show examples of HyperFlash and controller connection.

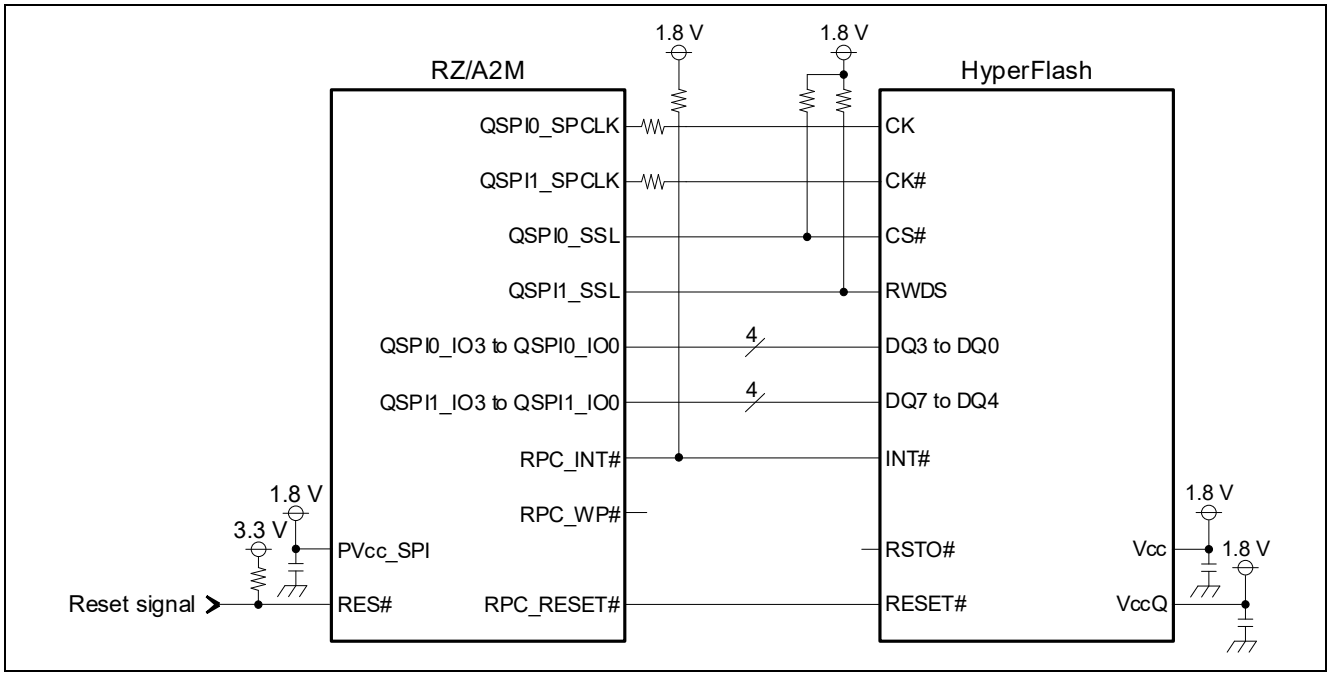


Figure 5.15 Example of HyperFlash connection 1 (SPIBSC)

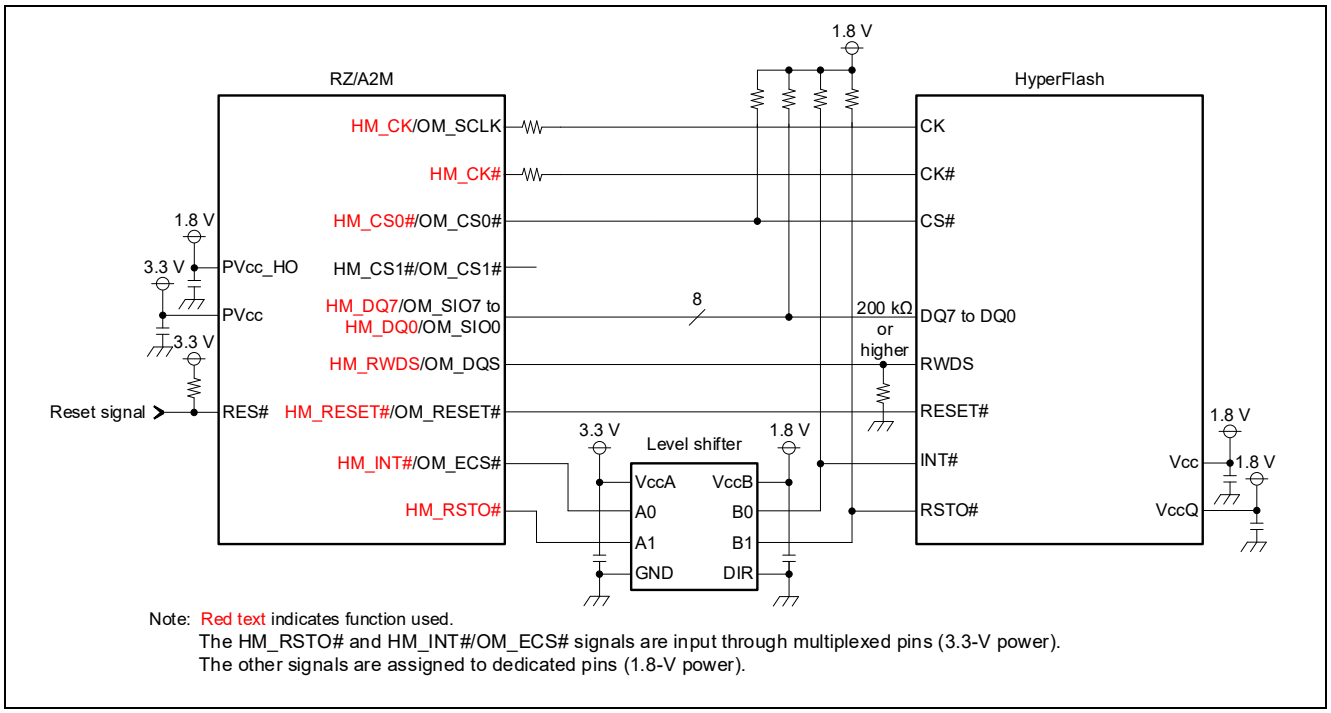


Figure 5.16 Example of HyperFlash connection 2 (HyperBus Controller)

5.7.2 HyperRAM

Figure 5.17 shows an example of HyperRAM connection.

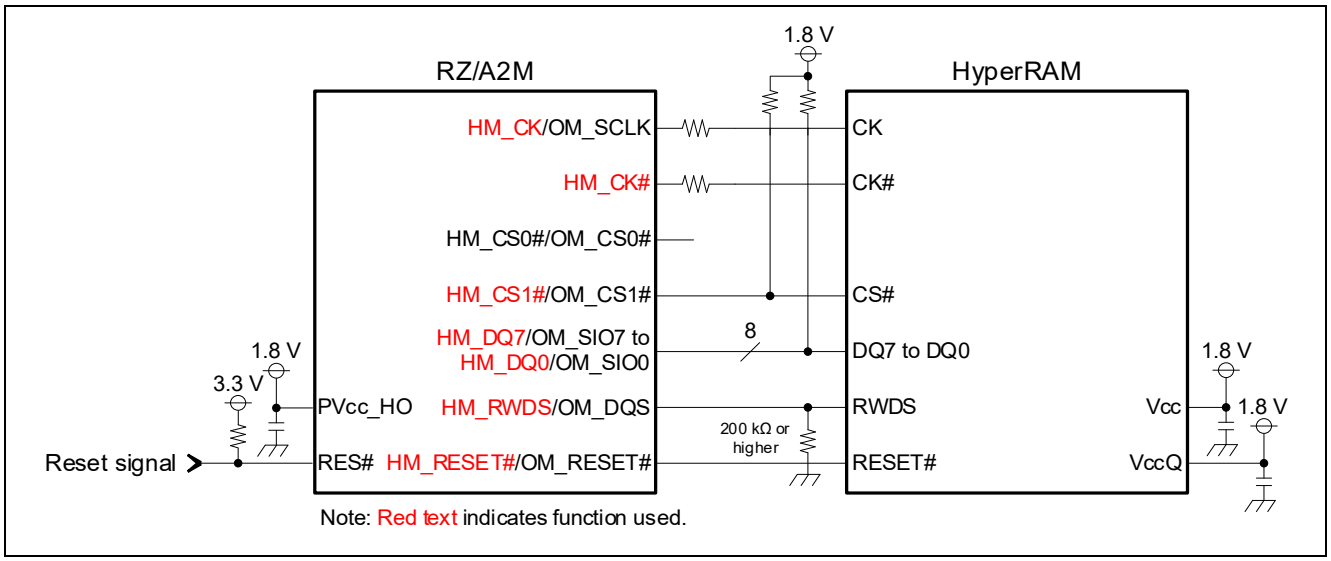


Figure 5.17 Example of HyperRAM connection

5.7.3 HyperMCP

HyperMCP is a multi-chip module that contains HyperFlash and HyperRAM.

Connect the HyperMCP CS1# pin to HM_CS0# pin and the CS2# pin to HM_CS1# pin.

Figure 5.18 shows an example of HyperMCP connection.

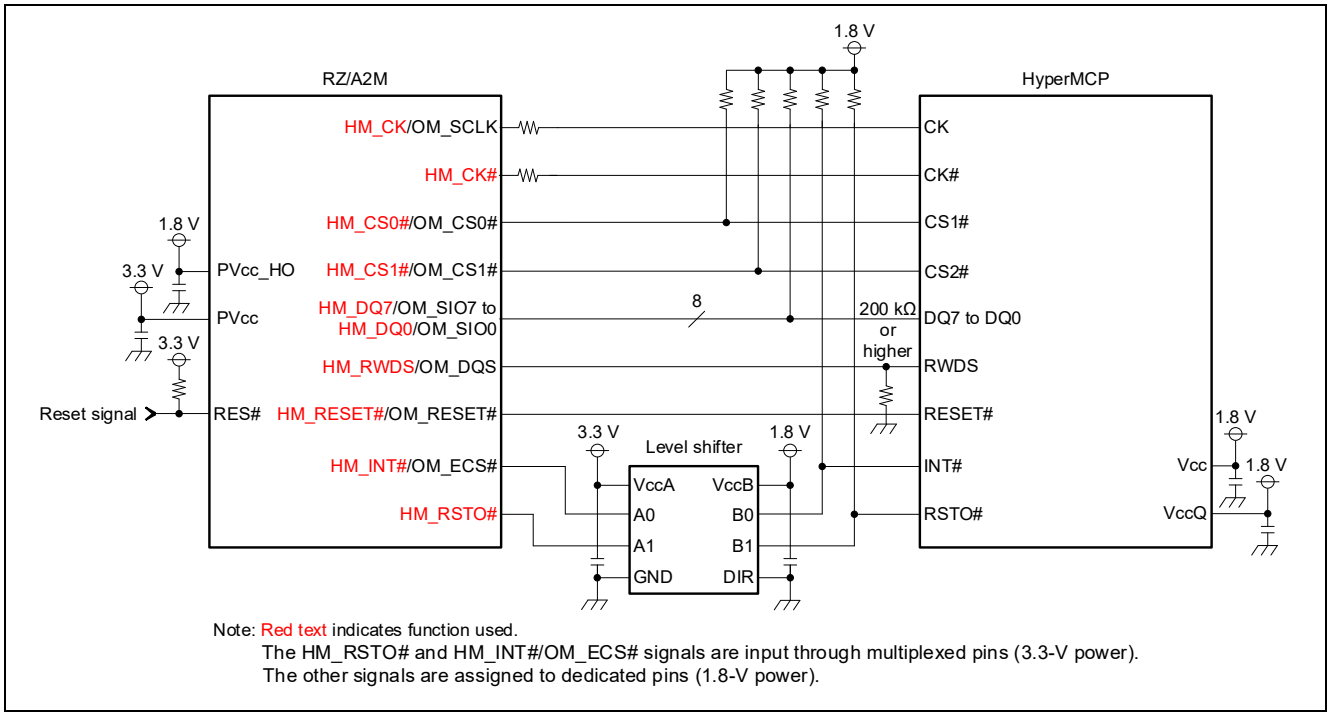


Figure 5.18 Example of HyperMCP connection

5.8 Octa Memory

5.8.1 OctaFlash

When using OctaFlash as boot memory, connect the RPC_RESET# pin that outputs the reset which is synchronized to the RES# input or the HM_RESET#/OM_RESET# pin to the OctaFlash RESET# pin.

For points of caution when selecting OctaFlash memory, refer to "4.1.11 Points of caution when selecting flash memory for use as boot memory".

Figure 5.19 and Figure 5.20 show examples of OctaFlash and controller connection.

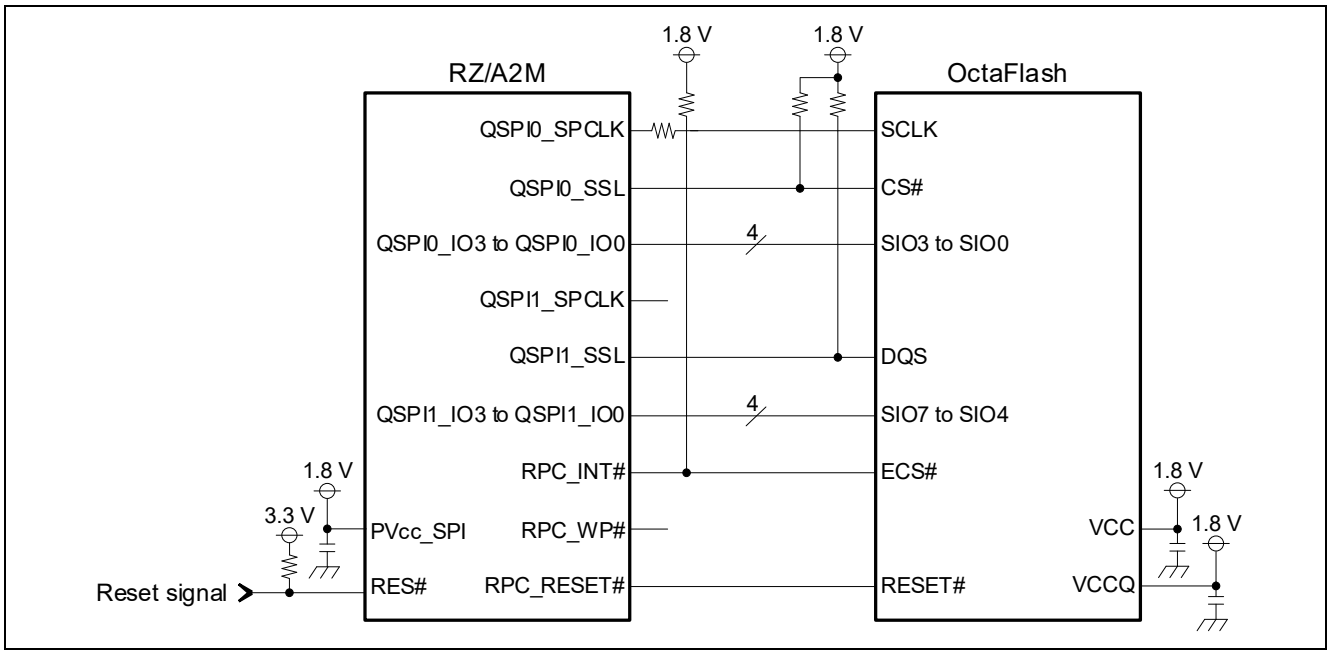
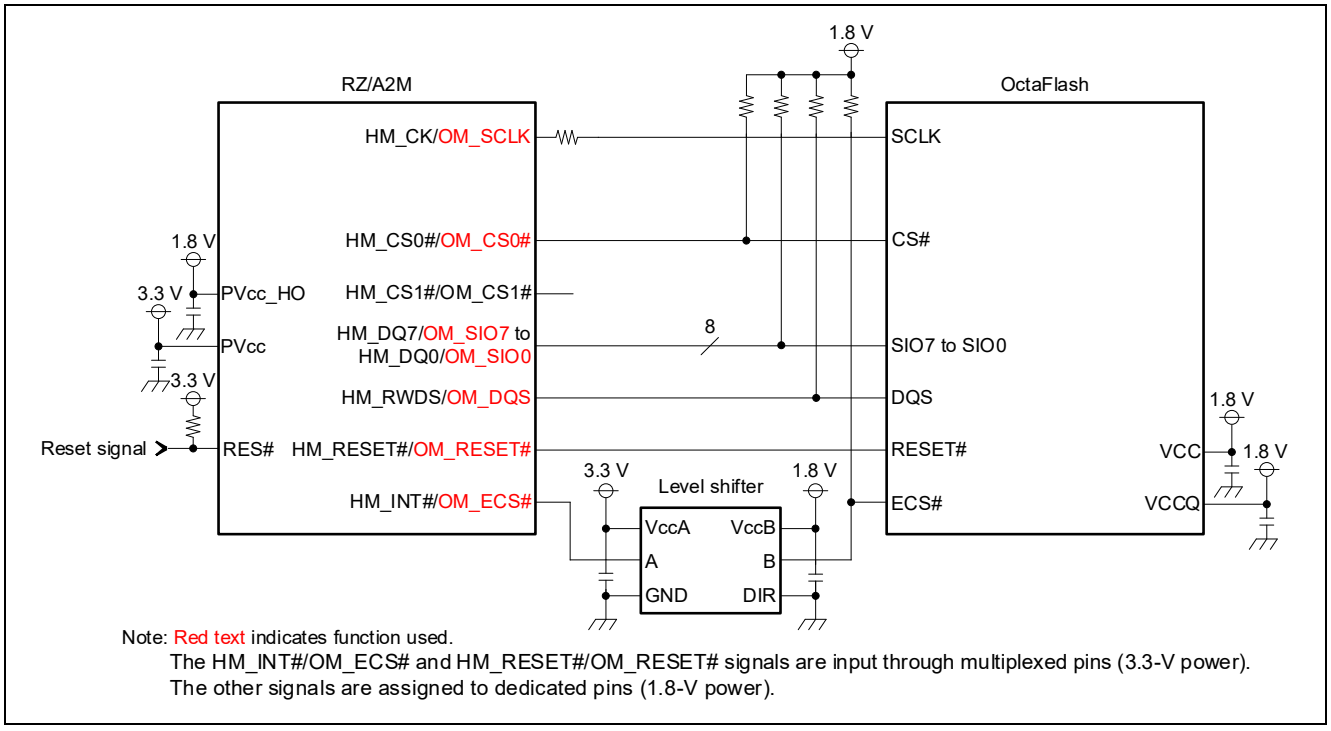


Figure 5.19 Example of OctaFlash connection 1 (SPIBSC)



Note: Red text indicates function used.
The HM_INT#/OM_ECS# and HM_RESET#/OM_RESET# signals are input through multiplexed pins (3.3-V power).
The other signals are assigned to dedicated pins (1.8-V power).

Figure 5.20 Example of OctaFlash connection 2(Octa Memory Controller)

5.8.2 OctaRAM

Figure 5.21 shows an example of OctaRAM connection.

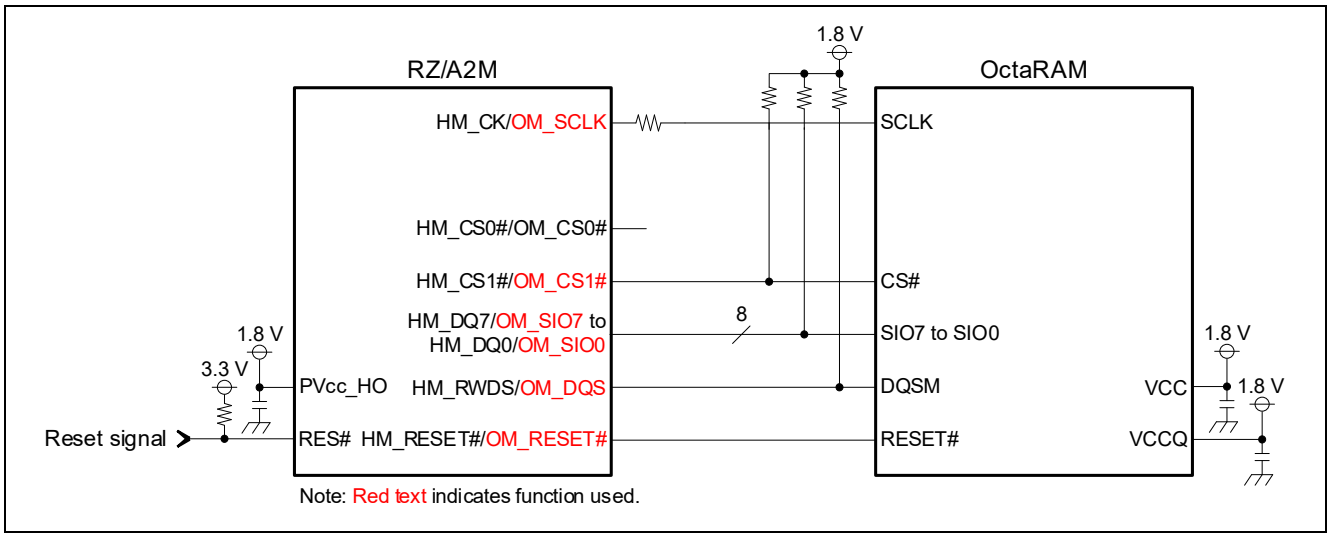


Figure 5.21 Example of OctaRAM connection

5.8.3 OctaMCP

OctaMCP is a multi-chip module that contains OctaFlash and OctaRAM.

Connect the OctaMCP CS#_F pin to OM_CS0# pin and the CS#_R pin to OM_CS1# pin.

Figure 5.22 shows an example of OctaMCP connection.

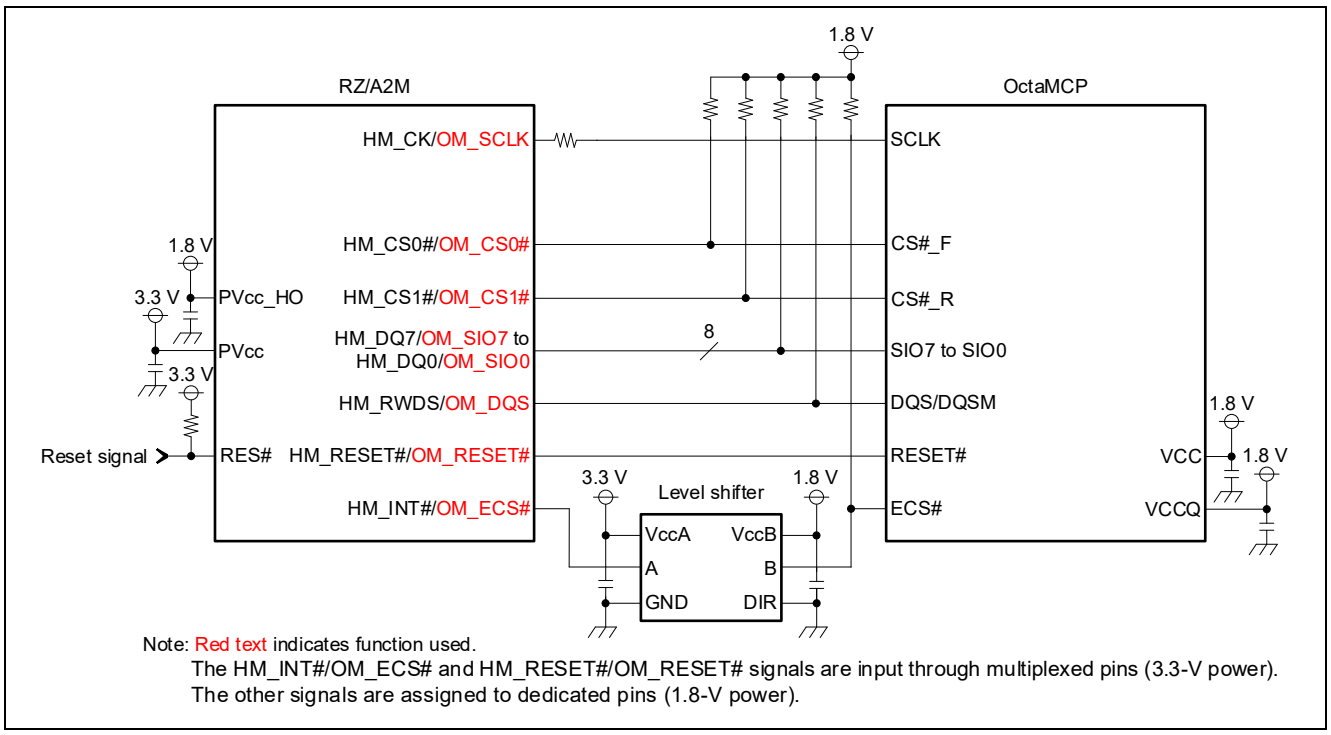


Figure 5.22 Example of OctaMCP connection

5.9 NAND Flash Memory

The RZ/A2M NAND Flash Controller has an on-chip ECC unit, and bit error correction is possible. However, the RZ/A1 NAND Flash Memory Controller does not have the ECC function. Therefore, when use NAND flash memory on RZ/A1, ensure that NAND flash memory with ECC function is used.

Figure 5.23 shows an example of NAND flash memory connection.

Note: Use ONFi 1.x specification (excluding timing mode 3, 4, and 5) NAND flash devices with RZ/A2M.

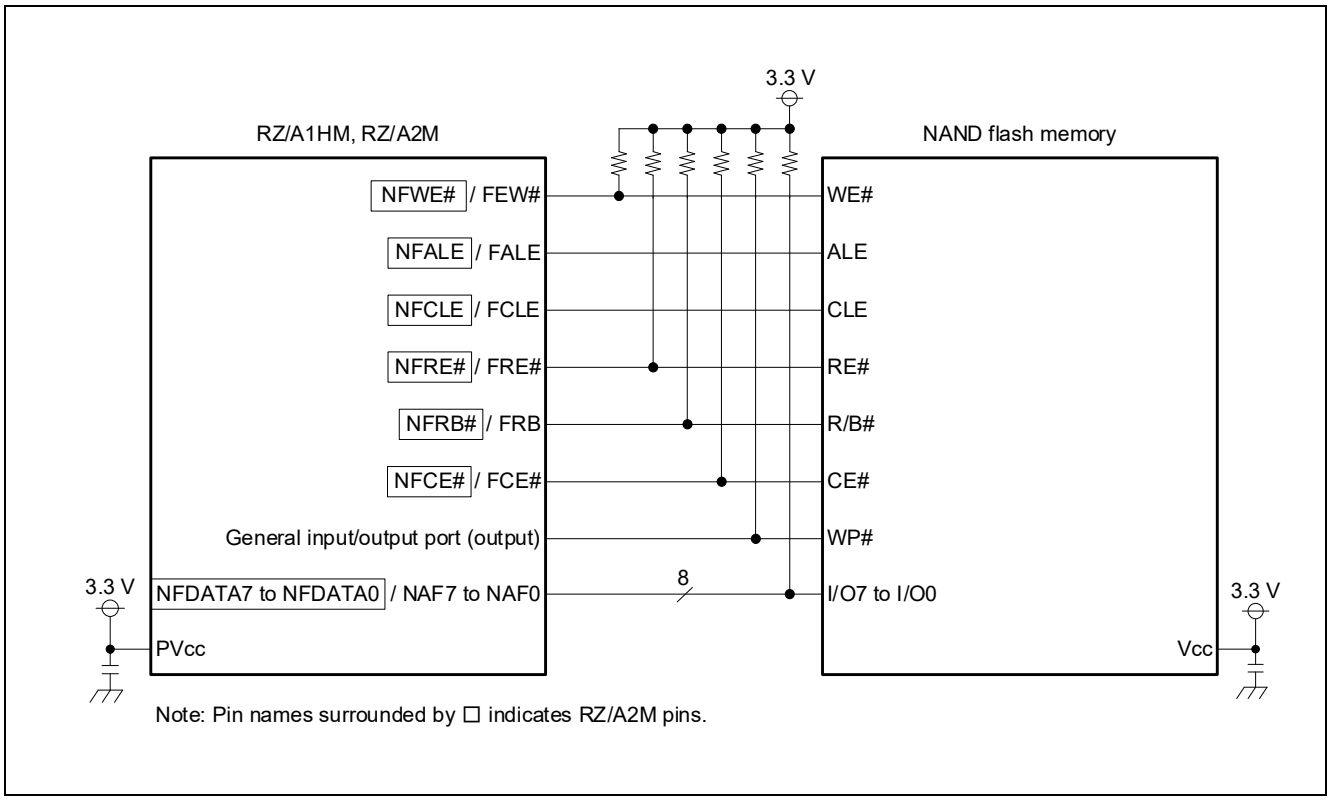


Figure 5.23 Example of NAND flash memory connection

5.10 SD Card

Change the treatment of CD pin*1 and WP pin*2 to match the system specification. Figures 5.24 and 5.25 are examples where the CD and WP pins are low active. To reverse the logic, pull down the CD and WP pins and supply 3.3V to the COMMON pin.

For CMD and DAT3 to DAT0 pins, pull-up of 10 kΩ to 100 kΩ.

If use the eSD boot, pleas supply power to SD card when power is turned on.

For RZ/A2M, when operation starts, supply 3.3 V to SDVcc, and switch between 1.8 V and 3.3 V in accordance with the operation mode.

Figure 5.24 and Figure 5.25 show examples of SD card slot connection.

Notes: *1. It's a card detection pin. Pin names are SD_CD_n in RZ/A1 and SDn_CD in RZ/A2M. (n = 0, 1)
*2. It's a write protect pin. Pin names are SD_WP_n in RZ/A1 and SDn_WP in RZ/A2M. (n = 0, 1)

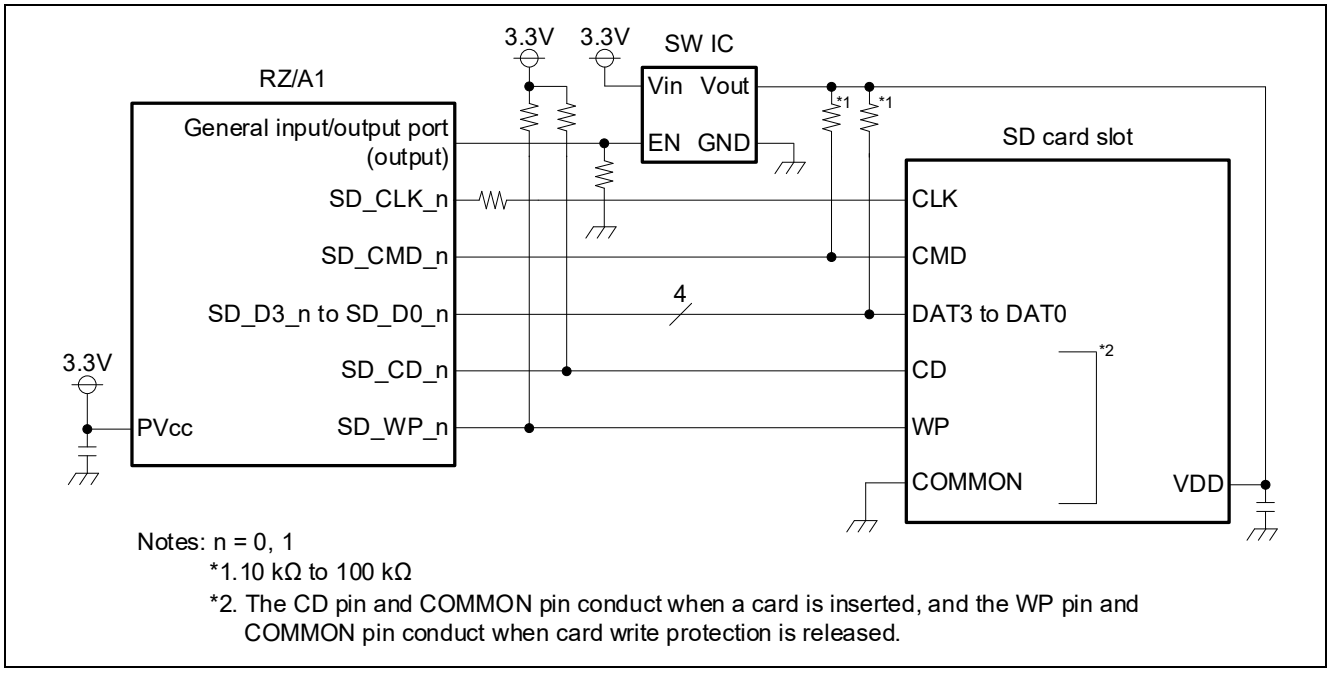


Figure 5.24 Example of SD card slot connection 1 (RZ/A1)

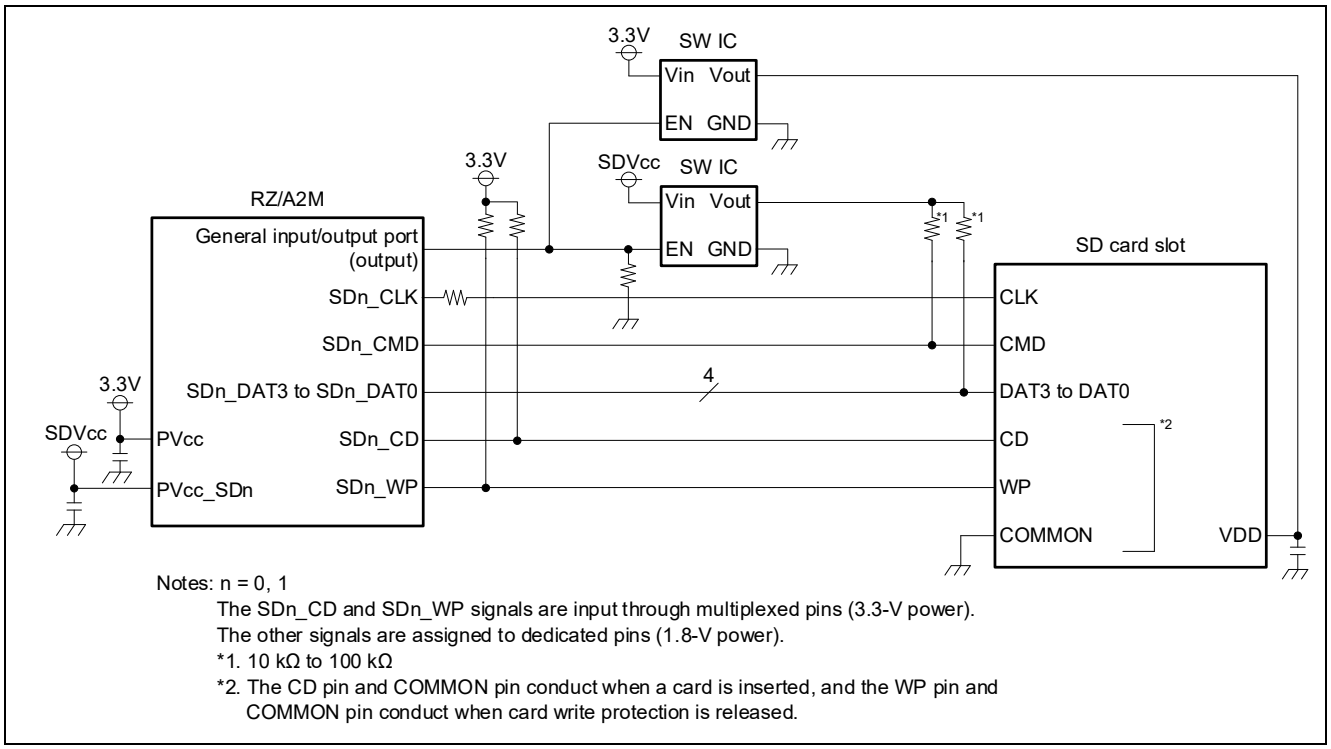


Figure 5.25 Example of SD card slot connection 2 (RZ/A2M)

5.11 eMMC

RZ/A2M can connect to 1-, 4- and 8-bit width data buses on Channel 0, and 1- and 4-bit width data buses on Channel 1.

For RZ/A1, use pull-up resistors of 4.7 kΩ to 100 kΩ for the CMD pin and pull-up resistors of 10 kΩ to 100 kΩ on the DAT7 to DAT0 pins.

For RZ/A2M, use pull-up resistors of 4.7 kΩ to 50 kΩ for the CMD pin and pull-up resistors of 10kΩ to 50 kΩ for the DAT7 to DAT0 pins. Also, when operation starts, supply 3.3 V to MMCVcc, and switch between 1.8-V and 3.3-V in accordance with the operation mode.

When an eMMC is used as a boot memory, ensure that it must be reset at the same time as LSI of this series.
For RZ/A2M, connect the SDn_RST# pin to the eMMC RST_n pin.

Figure 5.26 and Figure 5.27 show examples of eMMC connection.

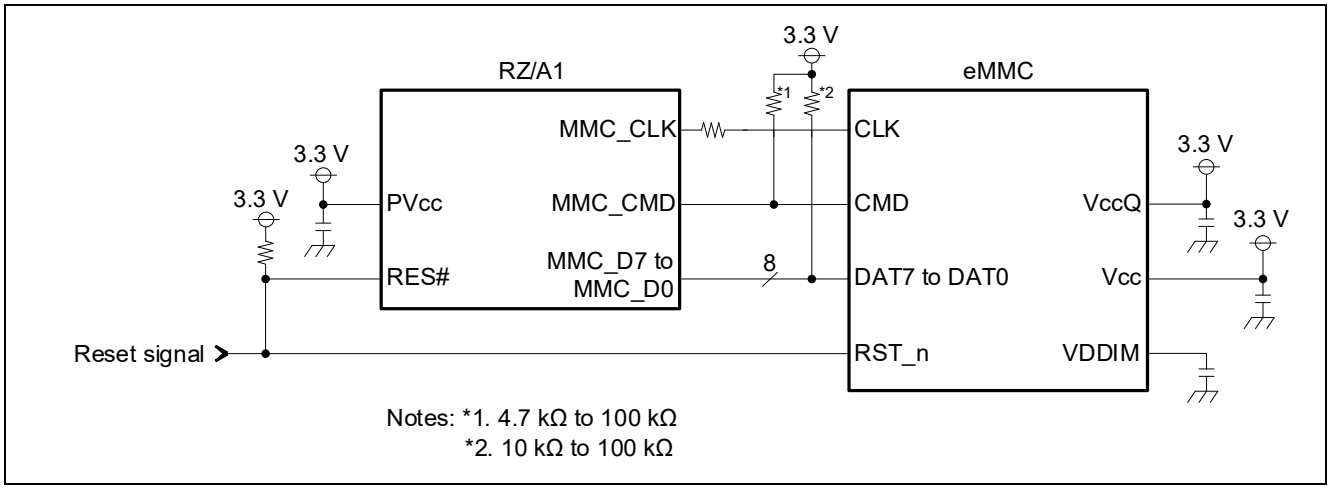


Figure 5.26 Example of eMMC connection 1 (RZ/A1)

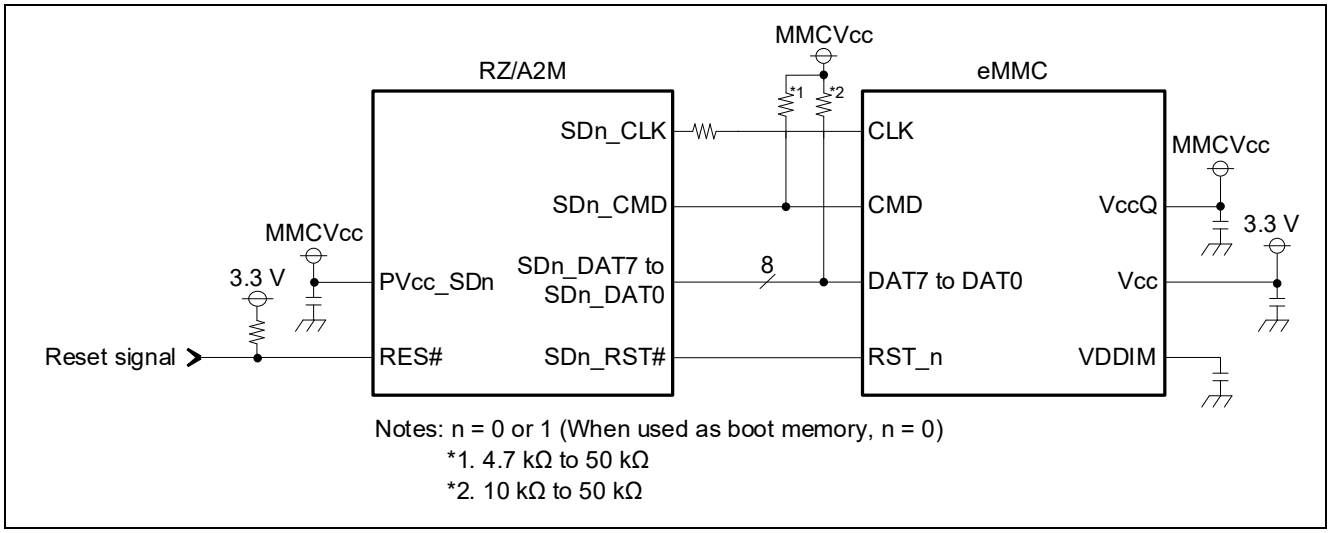


Figure 5.27 Example of eMMC connection 2 (RZ/A2M)

6. Debugger Interface

6.1 Characteristics

The debugger interface for LSI of this series is a serial I/O interface with the JTAG interface and the CoreSight debug interface*1, with a TAP controllers for the boundary scan and CoreSight debug function.

The boundary scan controller is selected by setting the BSCANP pin to high level, and when it is set to low level, the CoreSight debug TAP controller is selected. Table 6.1 shows the JTAG pin mode table.

Note: *1. For details on CoreSight, refer to Arm Ltd. Technical Reference Manual.

Table 6.1 JTAG pin mode table

BSCANP	JTAG Pin Mode
0	Normal operation (CoreSight debug mode)
1	Boundary scan mode

6.2 Treatment of TRST# Pin

TRST# pin is for use as the debugger interface module initialization signal input pin. Set TRST# to low level for a specified time period when power is turned on, regardless whether or not the debugger interface module function is used.

When designing a board that can use an emulator, ensure that TRST# is set to low level at power on, and that the TRST# pin can be controlled independently. When the emulator is not used, either fix to low level, or connect to same signal as RES# pin.

6.3 Example of Emulator Connection

Figure 6.1 shows an example of reset circuit and Figure 6.2 to Figure 6.4 show the examples of emulator connection. When the interface pins that are not in the examples of VTREF and DBGACK connection are used, treat the pins in accordance with the emulator specifications. For LSI of this series, treat unconnected pins in accordance with "7.2 Treatment of Unused Pins".

The dotted line in Figure 6 shows the "reset circuit" part of the following figure.

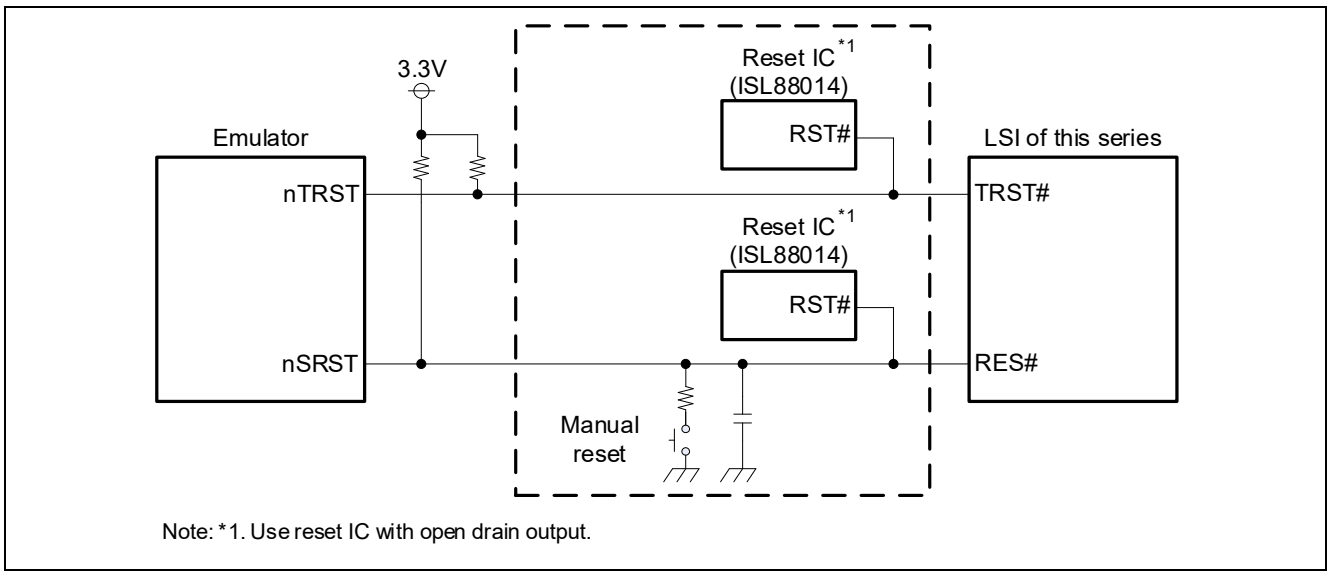


Figure 6.1 Example of reset circuit

6.3.1 JTAG Interface

Figure 6.2 shows an example of JTAG interface connection.

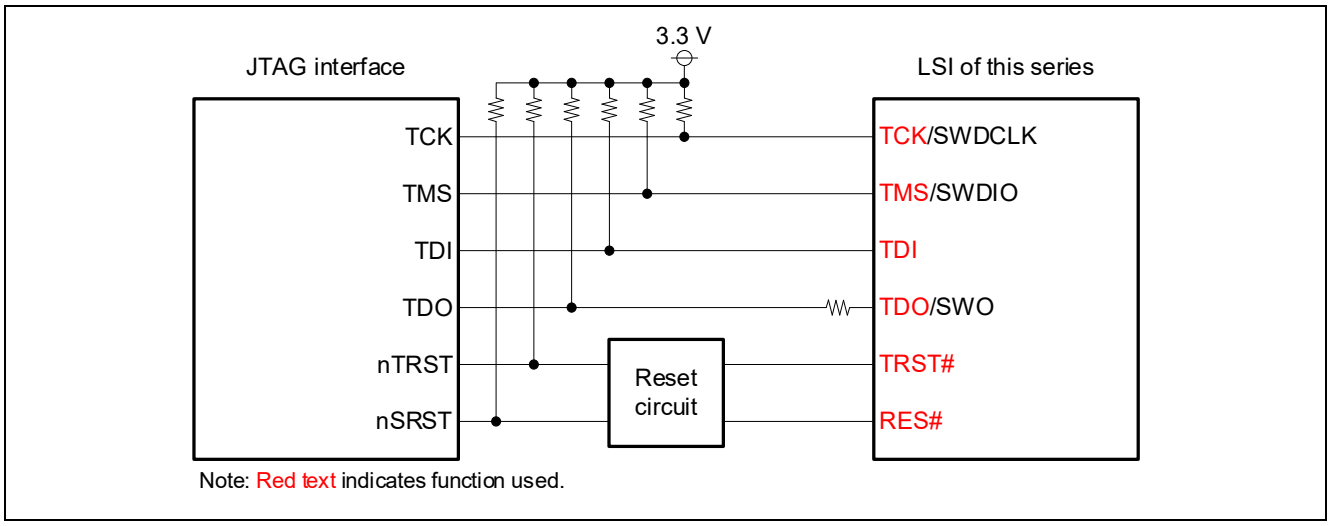


Figure 6.2 Example of JTAG interface connection

6.3.2 SWD Interface

Figure 6.3 shows an example of SWD interface connection.

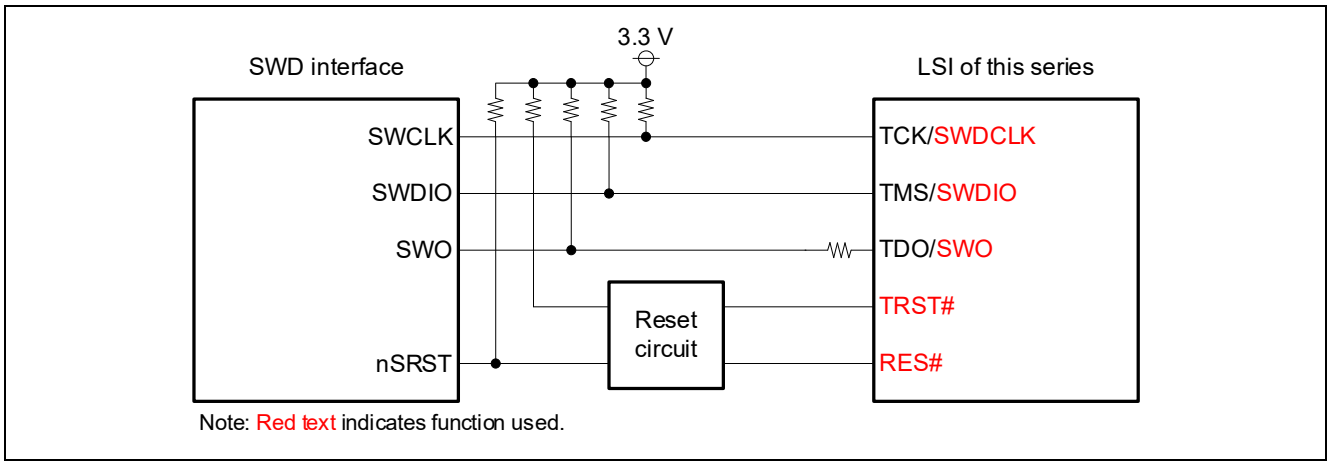


Figure 6.3 Example of SWD interface connection

6.3.3 TRACE Interface

Figure 6.4 shows an example of TRACE interface connection.

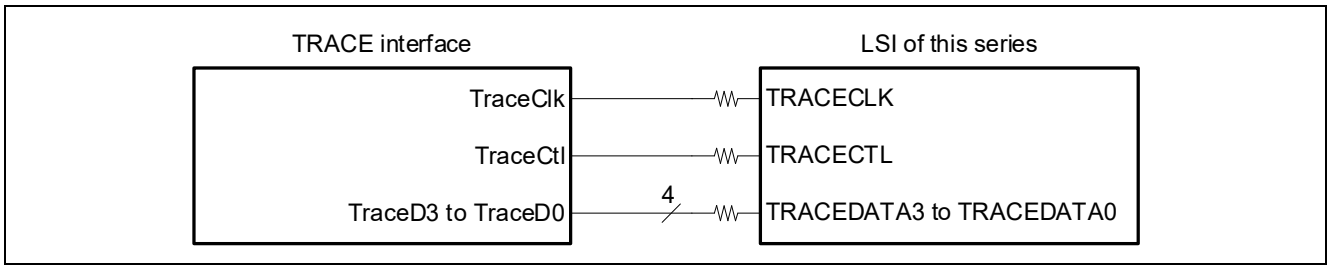
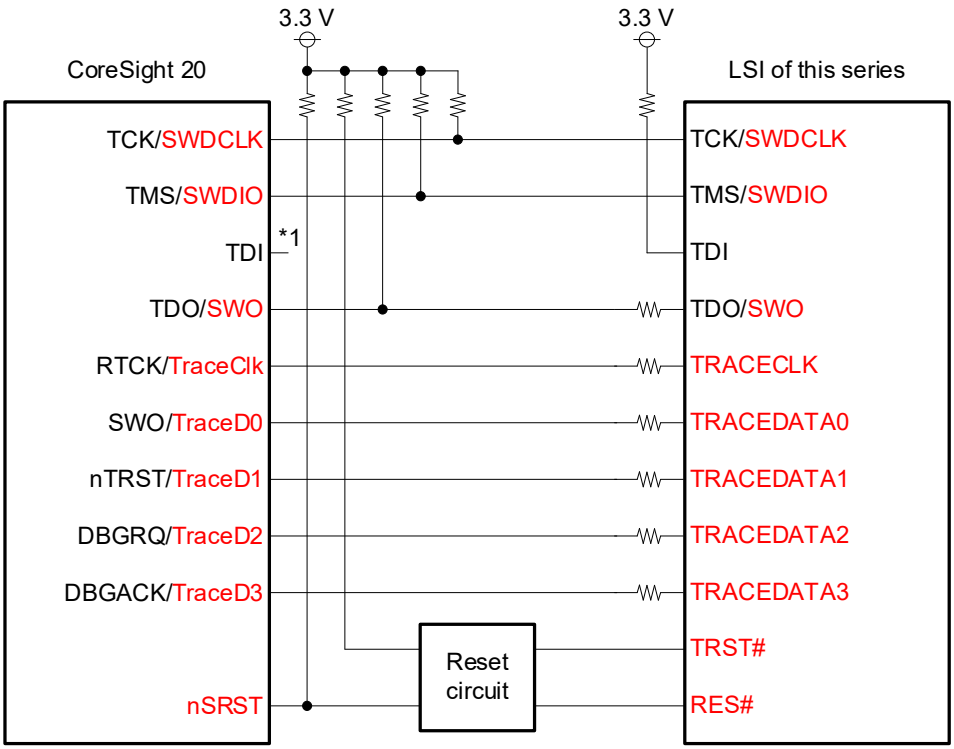


Figure 6.4 Example of TRACE interface connection

6.3.4 Connection to CoreSight 20 Connector

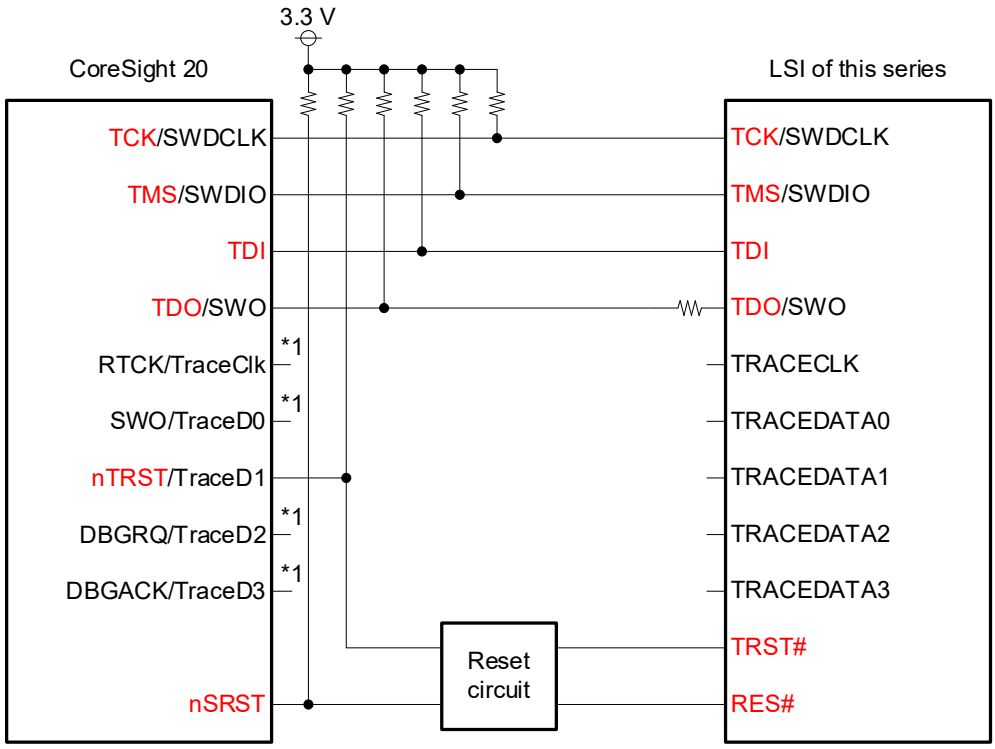
Because the CoreSight 20 connector is multiplexed to nTRST and TraceD1, when using the TRACE function, it is necessary to connect using the SWD interface. When connected to the JTAG interface, the TRACE function cannot be used.

Figure 6.5 shows an example of SWD and TRACE interface connection and Figure 6.6 shows an example of JTAG interface connection.



Notes: Red text indicates function used.
*1. Treat the pin in accordance with the specification for the emulator used.

Figure 6.5 Example of CoreSight 20 connection 1 (SWD and TRACE interface connection)



Notes: Red text indicates function used.
*1. Treat the pin in accordance with the specification for the emulator used.

Figure 6.6 Example of CoreSight 20 connection 2 (JTAG interface connection)

6.3.5 Connection to CoreSight 10 Connector

Even when the nTRST pin does not exist, as in the CoreSight 10 connector, when powering on, the TRST# pins on LSI of this series must be fixed to low level, and a signal separate from the RES# pin should be input.

Figure 6.7 shows an example of connection to CoreSight 10.

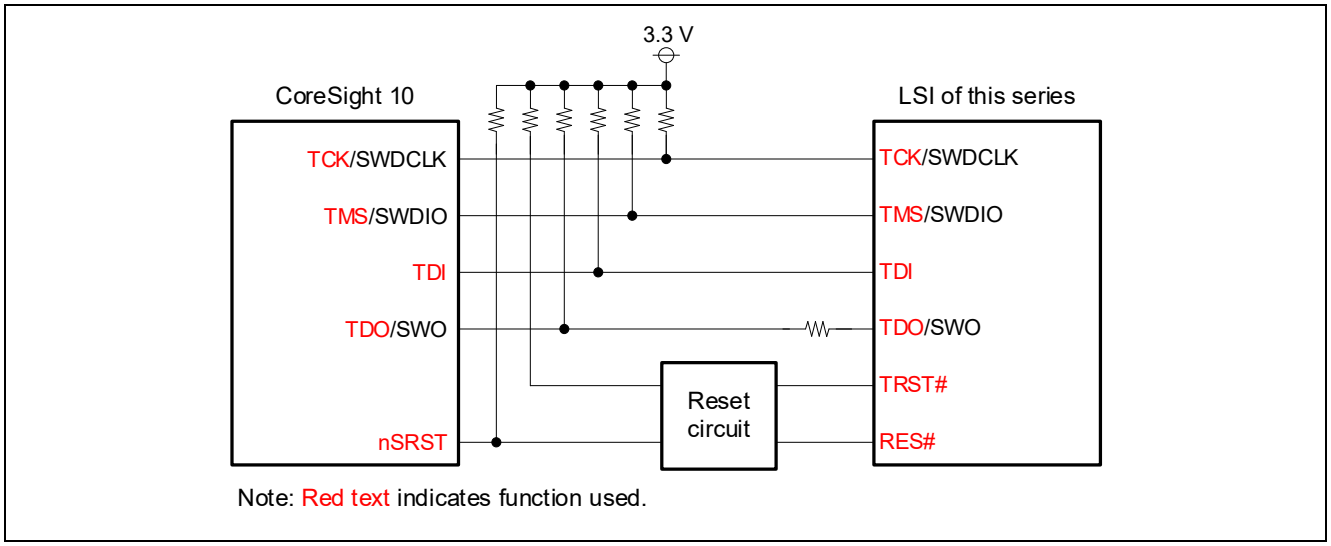


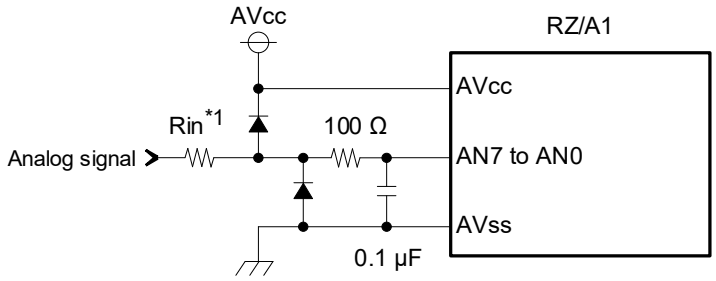
Figure 6.7 Example of CoreSight 10 connection (JTAG interface connection)

7. Treatment of Pins

7.1 Analog Pin Protection Circuit

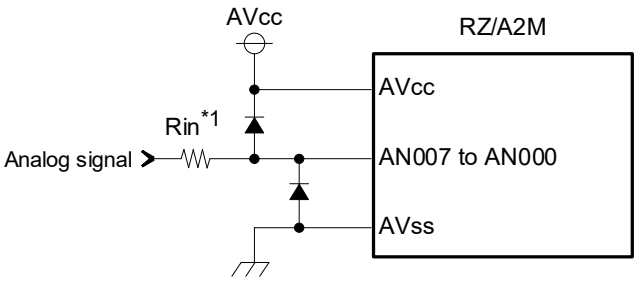
Design a protection circuit as shown in Figure 7.1 and Figure 7.2 to protect the analog input pin*1 from abnormal voltage (such as excessive surges). Furthermore, determine the circuit constants based on the actual use conditions.

Note: *1. RZ/A1 : AN7 to AN0
RZ/A2M : AN007 to AN000



Note: *1. Rin is the signal source impedance.
Set to 3 kΩ or less.

Figure 7.1 Example of analog input pin protection circuit (RZ/A1)



Note: *1. Rin is the signal source impedance.
Set to 1 kΩ or less.

Figure 7.2 Example of analog input pin protection circuit (RZ/A2M)

7.2 Treatment of Unused Pins

Table 7.1 shows the treatment of unused pins for RZ/A1, and Table 7.2 shows the treatment of unused pins for RZ/A2M. Treat the unused pins as shown in each of the tables.

Table 7.1 Treatment of unused pins (RZ/A1)

Module	Pin Name	Handling
Interrupt Controller	NMI	Fixed to high level (pull-up*1 or connect to the power supply)
USB2.0 Host/Function Module	DP1, DP0, DM1, DM0, VBUS1, VBUS0	Connect to USBDPVss (QFP) Connect to Vss (BGA package)
	REFRIN	Connect to USBAPVcc via a 5.6 kΩ ± 20% resistor
	USBAVcc, USBDVcc, USBUVcc	Supply power at 1.18 V.
	USBAPVcc, USBDPVcc	Supply power at 3.3 V.
	USBAPVss, USBDPVss, USBAVss, USBDVss, USBUVss	Connect to ground.
	USB_X1	Fix the level on the pin (pull-up*1 or down*1, or connect to the power supply or ground level).
	USB_X2	Open-circuit
A/D Converter	AVref	Connect to AVcc.
	AVcc	Supply power at 3.3 V.
	AVss	Connect to ground.
Digital Video Decoder	VIN1A, VIN2A, VIN1B, VIN2B, VRP, VRM, REXT	Open-circuit
	VDAVcc	Supply power at 3.3 V.
	VDAVss	Connect to ground.
	VIDEO_X1	Fix the level on the pin (pull-up*1 or down*1, or connect to the power supply or ground level).
	VIDEO_X2	Open-circuit
LVDS Output Interface	LVDSREFRIN	Open-circuit
	LVDSAPVcc	Supply power at 3.3 V.
	LVDSPLLVcc	Supply power at 1.18 V.
	LVDSAPVss	Connect to ground.
Debugger Interface	BSCANP	Fix this pin at a low level (pull-down*1 or connect to the ground level).
	TRST#	Fix this pin at a low level (pull-down*1 or connect to the ground level) *3. Or connect to another pin which operates in the same manner as the RES# pin
	TCK, TMS, TDI	Fix the level on the pins (pull them up*1 or down*1, or connect them to the power supply or ground level).
	TDO	Open-circuit *5
Clock Pulse Generator	EXTAL	Fix the level on the pin (pull-up*1 or down*1, or connect to the power supply or ground level).
	XTAL	Open-circuit
Realtime Clock	RTC_X1, RTC_X3	Fix the level on the pins (pull them up*1 or down*1, or connect them to the power supply or ground level).
	RTC_X2, RTC_X4	Open-circuit
Serial Sound Interface	AUDIO_X1	Fix the level on the pin (pull-up*1 or down*1, or connect to the power supply or ground level).
	AUDIO_X2	Open-circuit
General I/O ports	P0_5*4 to P0_0, P1_15 to P1_8	Fix the level on the pins (pull them up*1 or down*1, or connect them to the power supply or ground level)*2.
	Other General I/O pins	Set as input pin and fix (pull them up*1 or pull them down*1) *2 or set as output and open-circuit.

Notes: Some pins may not exist depending on the packages.

Pull-up voltage is 3.3V.

*1. We recommend that the values of pull-up or pull-down resistors are in the range from 4.7 kΩ to 100 kΩ.

*2. For pins which can disable input buffer by the "Port input buffer control register (PIBCn/JPIBC0)" setting, pin fixing is not required. For details, refer to the hardware manual for each LSI.

*3. When not fixed to low level, ensure that the RES# input rise time and the RES# negating hold time are satisfied. For details, refer to "2.1 Power ON and Power OFF Sequences".

*4. This is P0_3 for RZ/A1L.

*5. When an emulator is not connected, this pin can be fixed to pull-up*1.

Table 7.2 Treatment of unused pins (RZ/A2M)

Module	Pin Name	Handling
Interrupt Controller	NMI	Fix this pin at a high level (pull-up[*1*4] or connect to a power supply).
USB2.0 Host/Function Module	DP1, DP0, DM1, DM0	Connect these pins, via a 10 kΩ resistor, to GND.
	RREF0, RREF1	Open-circuit
	USBAPVcc0, USBAPVcc1, USBDPVcc0, USBDPVcc1	Supply power at 3.3 V.
	USBVss	Connect to ground.
	USB_X1	Fix the level on the pin (pull-up[*1*4] or down[*1], or connect to the power supply or ground level).
	USB_X2	Open-circuit
12-Bit A/D Converter	AVcc	Supply power at 3.3 V.
	AVss	Connect to ground.
LVDS Output Interface	LVDSAPVcc	Supply power at 3.3 V.
	LVDSPLLVcc	Supply power at 1.2 V.
MIPI CSI2 Interface	MIPIAVcc18	Supply power at 1.8 V.
	CSI_CLKP, CSI_CLKN, CSI_DATA0P, CSI_DATA0N, CSI_DATA1P, CSI_DATA1N	Connect to ground.
SD/MMC Host Interface	PVcc_SD1, PVcc_SD0	Supply power at 3.3 V.
	SD1_CMD, SD0_CMD, SD1_DAT3 to SD1_DAT0, SD0_DAT7 to SD0_DAT0	Fix the level on the pins (pull them up[*1*4] or down[*1]).
	SD1_CLK, SD0_CLK, SD0_RST#	Open-circuit
SPI Multi I/O Bus Controller	PVcc_SPI	Supply power at 3.3 V.
	QSPI1_SPCLK, QSPI0_SPCLK, QSPI1_SSL, QSPI0_SSL, QSPI1_IO3 to QSPI1_IO0, QSPI0_IO3 to QSPI0_IO0, RPC_RESET#, RPC_WP#	Open-circuit
	RPC_INT#	Fix this pin at a high level (pull−up[*1*4]/ connect to a power supply).
HyperBus Controller, Octa Memory Controller	PVcc_HO	Supply power at 1.8 V.
	HM_RWDS/OM_DQS, HM_DQ7/OM_SIO7 to HM_DQ0/OM_SIO0	Fix the level on the pins (pull them up[*1*5] or down[*1]).
	HM_CK/OM_SCLK, HM_CK#, HM_CS0#/OM_CS0#, HM_CS1#/OM_CS1#, HM_RESET#/OM_RESET#	Open-circuit
Debugger Interface	BSCANP	Fix this pin at a low level (pull down[*1] or connect to the ground level).
	TRST#	Fix this pin at a low level (pull down[*1] or connect to the ground level). Or connect to another pin which operates in the same manner as the RES# pin
	TCK, TMS, TDI	Fix the level on the pins (pull them up[*1*4] or down[*1], or connect them to the power supply or ground level).
	TDO	Open-circuit[*3]
Clock Pulse Generator	EXTAL	Fix the level on the pin (pull-up[*1*4] or down[*1], or connect to the power supply or ground level).
	XTAL	Open-circuit
Realtime Clock	RTC_X1	Fix the level on the pin (pull-up[*1*4] or down[*1], or connect to the power supply or ground level).
	RTC_X2	Open-circuit
Serial Sound Interface	AUDIO_X1	Fix the level on the pin (pull-up[*1*4] or down[*1], or connect to the power supply or ground level).
	AUDIO_X2	Open-circuit
General I/O Ports	P5_7 to P5_0, PL_4 to PL_0	Fix the level on the pins (pull them up[*1*4] or down[*1], or connect them to the power supply or ground level)[*2].
	I/O pins other than those listed above	Set as input pin and fix (pull them up[*1*4] or pull them down[*1]) [*2] or set as output and open-circuit.

Notes: Some pins may not exist depending on the packages.

*1. We recommend that the values of pull-up or pull-down resistors are in the range from 4.7 kΩ to 100 kΩ.

*2. For pins which can be set to input Hi-Z state by the "Port direction register (PDR)" setting, pin fixing is not required. For details, refer to RZ/A2M Group User's Manual: Hardware

*3. When an emulator is not connected, this pin can be fixed to pull-up[*1].

*4. Pull-up voltage is 3.3V.

*5. Pull-up voltage is 1.8V.

8. Layout Guide

8.1 Layout and Wiring

When designing a board, start layout from the components that input and output high speed signals, and layout wiring from the clock and high speed signals which require thick and/or short wiring. At this point, ensure that the bypass capacitor has the shortest wiring.

Because inductance may cause malfunctions in analog circuits or have a negative effect on A/D conversion values, lay out the wiring to separate analog signals and digital signals. In addition, the analog ground (AVss) should be connected with the stabilized digital ground (Vss) on the board at one point.

Caution is required for wiring of high speed memory interfaces. When using HyperBus memory, refer to the layout guide provided by Cypress Semiconductor Corporation[*1]. When using Octa memory, refer to the layout guide provided by Macronix International Co., Ltd.[*2].

Notes: *1. HyperFlash and HyperRAM Layout Guide (AN211622)
*2. OctaBus Memory PCB Layout Guide (AN0444)

8.2 Differential Signal

8.2.1 Impedance Control

Impedance control*1 on the differential interface transmission line is necessary. Table 8.1 shows the characteristics impedance for the differential interface supported in LSI of this series.

Note: *1. Pattern width and pattern interval will differ according to board thickness, material, and layer configuration. For details, consult the board manufacturer.

Table 8.1 Characteristic impedance

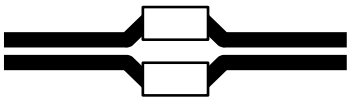
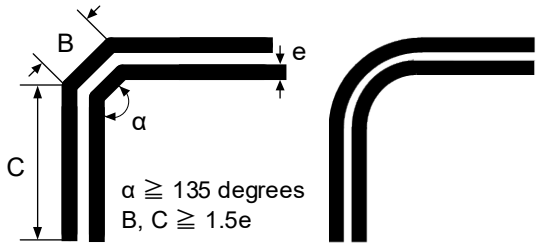
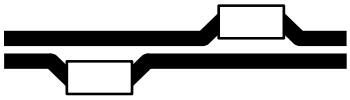
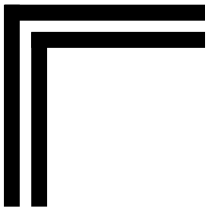
Standard	Differential Impedance
USB	90 Ω
LVDS	100 Ω
MIPI	100 Ω

Note: *1. For details, refer to each Reference Application Note described in Introduction.

8.2.2 Cautions for Wiring

For paired differential signals, lay out wiring as isometrically parallel and when placing components over those lines, ensure symmetry in placement is maintained. For clock synchronized type, lay out wiring isometrically for clock and data, not just pairs. If the pattern includes curves, avoid 90 degree turns, instead use circular arcs or repeated gentle curves (for example 135 degrees). Table 8.2 shows examples of wiring patterns.

Table 8.2 Examples of wiring patterns

	Placement of Differential Pair Components	Curve
Good example		
Bad example		

9. Noise Countermeasures

9.1 EMI Countermeasures

The PLL circuit for LSI of this series have an on-chip SSCG. The SSCG is a function that can suppress EMI noise peaks by slightly modulating the output frequency (frequency modulations). Table 9.1 shows the SSCG specifications.

The SSCG circuit's SSCG function ON/OFF is controlled by the MD_CLKS pin. When the SSCG function is turned ON, with the exception of clocks *1 supplying some peripheral modules, the clock will use a fluctuating frequency. Table 9.2 shows the SSCG operation settings.

Ensure that the SSCG stabilizing time (tSSCG)*2 requirement is satisfied if the SSCG function is used.

Notes: *1. For details, refer to the hardware manual for each LSI.
*2. For details, refer to "2.1 Power ON and Power OFF Sequences".

Table 9.1 SSCG specification

Item	Parameters	Applicable LSIs
Modulation type (modulation profile)	Triangle wave	RZ/A Series
Spread type	Down spread	RZ/A Series
Modulation rate	Clock mode 0: -3.3% Clock mode 1: -3.1%	RZ/A1
	-2.2%	RZ/A2M
Modulation frequency	20 kHz to 26.67 kHz (EXTAL frequency ÷ 500) 24 kHz (USB_X1 frequency × (1/4) ÷ 500)	RZ/A1
	20 kHz to 24 kHz (Clock mode 0: EXTAL frequency ÷ 500 Clock mode 1: EXTAL frequency ÷ 1000)	RZ/A2M

Table 9.2 SSCG operation setting

MD_CLKS	SSCG Operation
0	OFF
1	ON

In addition, EMI can be reduced by implementing the following measures.

Measures in circuit design

- To reduce overshoot, undershoot, and ringing, use damping resistors, ferrite cores, and/or capacitors.
- To absorb power fluctuation and smooth the power, use a bypass capacitor.
- Use an EMI filter.

Measures in pattern design

- To avoid characteristic impedance fluctuations;

  Do not change wiring width partway through the wiring.

  Do not turn at right angles (turn 2 times 135 degrees).
- To suppress cross-talk;

  Do not place wiring beneath crystal resonators and crystal resonator devices.

  Implement a guard ring by ground for the clock line.

  Do not layout wiring in parallel (When bus wiring or other measures are difficult, implement ground guard ring for small groupings).
- In order to maintain the return path, do not divide or split the ground pattern (solid plane ground).
- Surround the circuit board periphery with a ground wiring, and avoid wiring at board edges.
- Place a bypass capacitor in the vicinity of the power supply pin.
- Place a damping resistor at the output pin side.
- Place a electrical termination such as pull-up/pull-down resistor and capacitor at the input pin side.

9.2 EMS Countermeasures

Implement EMI measures as EMS countermeasures. By implementing EMI measures to prevent electromagnetic noise from escaping externally, it is expected that EMS will be improved by reducing noise that enters the system from outside.

In addition, in terms of static electricity discharge countermeasures, it is recommended that ESD protection devices be used and that ESD protection circuit design be optimized using the variety of simulations.

10. Checklist

Table 10.1 Checklist 1 (Circuit diagram (1))

Item Number	Check Items (circuit diagram)	✔	Reference
1	Is the treatment of pins correct?		-
1-1	Are the voltages for each power supply pin correct? (Are there no unconnected power supply pins?)		Table 1.1 Table 1.2
1-2	Are unused pins treated appropriately?		7.2
1-3	Is there a bypass capacitor for each power supply pin pair? (QFP)		1.3
1-4	Is there a bypass capacitor from 0.1 µF to 0.33 µF for each power supply pin? (BGA)*1		
1-5	Is there a bypass capacitor 0.01 µF for each USB power supply? (RZ/A2M)		*2
1-6	Is a protection circuit implemented if the pin is used as an analog input pin?		7.1
1-7	Can the TRST# pin be controlled independently when using an emulator?		6.2
1-8	Can the PVcc_SDn power supply switch between 1.8 V and 3.3 V when using SDR104 or HS200 mode? (RZ/A2M)		Figure 5.25 Figure 5.27
1-9	Is voltage not applied to non-tolerant pins when the power is OFF? (RZ/A2M)		1.2.1
2	Are the digital power supply and analog power supply separated?		1.1
3	Are the PLL power supply and other power supply separated resources?		
4	Is the input frequency correct?		-
4-1-1	EXTAL/XTAL (RZ/A1) / UCKSEL*3 12 MHz ± 100ppm / 1 10 MHz to 13.33 MHz / 0		Table 3.1
4-1-2	EXTAL/XTAL (RZ/A2M) / UCLKSEL*3 / MD_CLK 12 MHz ± 100ppm / 0 / 0 24 MHz ± 100ppm / 0 / 1 10 MHz to 12 MHz / 1 / 0 20 MHz to 24 MHz / 1 / 1		
4-2-1	USB_X1/USB_X2 (RZ/A1) / Usage condition 48 MHz ± 100ppm / Hi-Speed 48 MHz ± 500ppm / Non-Hi-Speed and Host 48 MHz ± 2500ppm / Non-Hi-Speed and Function		
4-2-2	USB_X1/USB_X2 (RZ/A2M) / UCLKSEL*3 48 MHz ± 100ppm / 1 Not required (Fix USB_X1) / 0		
4-3	AUDIO_X1/AUDIO_X2: 10 MHz to 50 MHz (crystal resonator), 1 MHz to 50 MHz (external clock) (RZ/A1)		
4-4	RTC_X1/RTC_X2: 32.768 kHz		
4-5	RTC_X3/RTC_X4 (RZ/A1HM): 4 MHz		
4-6	VIDEO_X1/VIDEO_X2 (RZ/A1HM): 27 MHz ± 50ppm		
5	Is the external clock connected to the Xin pin? (Is Xout pin open-circuit?)		Figure 3.1
6	Are there a limiting resistor, feedback resistor, and load capacitor attached to the crystal resonator?		Figure 3.2
7	Is the mode pin setting correct?		-
7-1	MD_BOOT2 to MD_BOOT0 (boot mode): Are the values consistent?		Table 4.1
7-2	MD_CLK (supply source): 0 = EXTAL/XTAL, 1 = USB_X1/USB_X2 (RZ/A1)		Table 4.13
7-3	MD_CLK (frequency): 0 = 10 MHz to 12 MHz, 1 = 20 MHz to 24 MHz (RZ/A2M)		Table 4.14
7-4	BSCANP (JTAG pin mode): 0 = Normal operation, 1 = Boundary scan mode		
7-5	MD_CLKS (SSCG operation): 0 = OFF, 1 = ON		Table 9.2

Notes: : Items applicable only to RZ/A1, : Items applicable only to RZ/A2M.

*1. Refer to Item Number 1-5 for USB power supply of RZ/A2M.

*2. For details, refer to “RZ/A2M Group Guidelines for High-Speed USB2.0 Board Design (R01AN4964EJ)”.

*3. This bit selects the clock supplying to USBPHY. For details, refer to the hardware manual for each LSI.

Table 10.2 Checklist 2 (Circuit diagram (2))

Item Number	Check Items (circuit diagram)	✔	Reference
8	Are the timing requirements at power on satisfied?		-
8-1	SSCG stabilizing time: tSSCG ≥ 1 µs (RZ/A1)		Figure 2.1
8-2	RES# input rise time: tRSr ≤ 500 µs		Figure 2.2
8-3	RES# negating hold time: tRSNH ≥ 0 ns(RZ/A1)		Figure 2.3
8-4	Mode hold time: tMDH ≥ 200 ns		Figure 2.4
8-5	On-chip circuit oscillation settling time: tROSC ≤ 4 ms		Figure 2.5
8-6	On-chip PLL circuit oscillation settling time: tPOSC ≥ 1 ms		
9	Is the treatment of pins for external devices correct?		-
9-1	Are there pull-down resistors on pins A25 to A21? (When the boot device uses pins from A25 to A21.)		4.1.2 4.1.3
9-2	Is a pull-up resistor applied to the CSn# pin? (recommended)		5.2
9-3	Are pull-up resistors applied to the RD#, RD/WR#, and WEn# pins? (recommended)		5.3
9-4	Does the treatment of CKE and DQM pins match the SDRAM initialization sequence?		5.3
9-5	Does the treatment of write protect and hold pins match the device polarity?		5.4 5.5
9-6	Is a pull-down resistor of 200 kΩ or more applied to the RWDS pin of HyperBus memory when connected to HyperBus Controller?		Figure 5.16 Figure 5.17 Figure 5.18
9-7	Are there pull-up resistors from 10 kΩ to 100 kΩ on the SD card CMD and DAT pins?		Figure 5.24 Figure 5.25
9-8	Is the treatment of SD card WP and CD pins in accordance with the software specification?		4.1.4 Figure 5.24
9-9	Is a pull-up resistor from 4.7 kΩ to 50 kΩ applied to the eMMC CMD pin?		Figure 5.26
9-10	Is a pull-up resistor from 10 kΩ to 50 kΩ applied to the eMMC DAT pin?		Figure 5.27
10	Is the connection for external devices correct?		-
10-1	Is the CS# pin of the memory that executes CS0 space boot connected to the CS0# pin?		5.2
10-2	Is the CS3# pin (not CS2#) connected if an SDRAM is connected to only 1 area?		5.3
10-3	Are the address connections correct? -For 16-bit width, connect A1 of LSI of this series to A0 of the external device -For 32-bit width, connect A2 of LSI of this series to A0 of the external device		5.2 5.3
10-4	When using eSD as boot memory, is Channel 0 connected?		4.1.4
10-5	When performing eSD boot, is power supplied to SD card during power on?		Figure 5.24 Figure 5.25
10-6	When using eMMC as boot memory, is Channel 0 connected? (RZ/A2M)		Figure 5.27
10-7	For eMMC boot, is the connection 4-bit width or more? (RZ/A1)		4.1.5
10-8	For eMMC boot, is the connection 8-bit width? (RZ/A2M)		5.11
10-9	Is Channel 0 connected when using serial flash as boot memory? (RZ/A1)		Figure 5.10 Figure 5.11
10-10	When using HyperFlash, are the HM_CS0# pin of RZ/A2M and CS# pin connected? (RZ/A2M)		Figure 5.16
10-11	When using HyperRAM, are the HM_CS1# pin of RZ/A2M and CS# pin connected? (RZ/A2M)		Figure 5.17
10-12	When using HyperMCP, are the HM_CS0# pin of RZ/A2M and CS1# pin connected, and are the HM_CS1# pin of RZ/A2M and CS2# pin connected? (RZ/A2M)		Figure 5.18
10-13	When using OctaFlash, are the OM_CS0# pin of RZ/A2M and CS# pin connected? (RZ/A2M)		Figure 5.20
10-14	When using OctaRAM, are the OM_CS1# pin of RZ/A2M and CS# pin connected? (RZ/A2M)		Figure 5.21
10-15	When using OctaMCP, are the OM_CS0# pin of RZ/A2M and CS#_F pin connected, and are the OM_CS1# pin of RZ/A2M and CS#_R pin connected? (RZ/A2M)		Figure 5.22
11	Is the selection of external devices correct?		-
11-1	Does the eSD boot device conform to the SD Specification Part1 eSD Addendum (Version 2.10) standard?		4.1.4
11-2	Does the eMMC boot device conform to the JESD84 A44 (MMCA 4.4) standard?		4.1.5
11-3	Does the boot memory have an independent reset pin, and is the system reset inputted? (Serial flash boot, Octal-SPI flash boot, OctaFlash boot)		4.1.11

Note: : Items applicable only to RZ/A1, : Items applicable only to RZ/A2M.

Table 10.3 Checklist 3 (Circuit diagram (3))

Item Number	Check Items (circuit diagram)	✔	Reference
12	Others		-
12-1	Isn't using an input-only port as the output port? RZ/A2M: P5_7 to P5_0、PL_4 to PL_0、JP0_0 RZ/A1HM: P0_5 to P0_0、P1_15 to P1_8、JP0_1、JP0_0 RZ/A1L: P0_3 to P0_0、P1_15 to P1_8、JP0_1、JP0_0		-

Table 10.4 Checklist 3 (pattern diagram)

Item Number	Check Items (pattern diagram)	✔	Reference
1	Are the crystal resonator and the load capacitor NOT located in the vicinity of the clock pin?		3.3
2	Is there NO wiring pattern close to the crystal resonator circuit?		
3	Are the wirings of the analog signal and the digital signal placed apart?		8.1
4	Are there NO changes in the wiring width from one end to the other?		9.1
5	Are there NO right angle curves on the wirings?		
6	Is there a guard ring connected to the ground for the clock line?		
7	Is there NO parallel wiring? If there is, is a guard ring connected to the ground placed for each small grouping?		
8	Is the periphery of the circuit board surrounded by a ground wiring?		
9	Is there NO wiring on the edges of the circuit board?		
10	Is the bypass capacitor located in the vicinity of the power supply pins?		
11	Is a damping resistor placed at the output pins side?		
12	Are the electrical terminations such as pull-up/pull-down resistors and capacitors placed at the input pins side?		

11. Reference Documents

- Hardware manual
  RZ/A1H Group, RZ/A1M Group User's Manual: Hardware (R01UH0403EJ)
  (The latest version can be downloaded from the Renesas Electronics website.)

  RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group User's Manual: Hardware (R01UH0437EJ)
  (The latest version can be downloaded from the Renesas Electronics website.)

  RZ/A2M Group User's Manual: Hardware (R01UH0746EJ)
  (The latest version can be downloaded from the Renesas Electronics website.)

- HyperBus Memory Layout Guide
  HyperFlash and HyperRAM Layout Guide (AN211622)
  (The latest version can be obtained from the following page on the Cypress Semiconductor Corporation website.
  https://www.cypress.com/documentation/application-notes/an211622-hyperflash-and-hyperram-layout-guide)

- OctaBus Memory PCB Layout Guide
  OctaBus Memory PCB Layout Guide (AN0444)
  (For the latest version, search the AN number (AN0444) on the follow page on the Macronix International Co., Ltd. website.
  http://www.macronix.com)

12. Design Support

- Kyocera Corporation “Crystal Units vs. IC Matching Search”
  http://prdct-search.kyocera.co.jp/crystal-ic/?p=en_search/

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2019.06.20	-	First edition issued. (Japanese version only.)
1.10	2019.09.05	21	Deleted specifications related to RTC_X1 and RTC_X3 in Table 2.2.
		31	Correct 4.1.11 section titles and text, added diagrams.
		34 to 51	Move some notations in diagrams to main text. Added power supply pins to diagram. Added RES# pin for LSI of this series for diagram when inputting reset signal to external memory.
		34, 40, 43, 44, 46, 51	Added points of caution when using as boot device.
		40	Added connectable data bus width to main text.
		42 to 47, 51	Deleted pull-up from wiring to output reset signal from RZ/A2M when external memory is connected.
		44 to 47	Added the pin treatment (pull-up) for I/O pin to the connection examples when using HyperBus Controller or Octa Memory Controller.
		44, 45, 46, 47, 50	Added notation to diagram, added explanation about shared pin and exclusive pin.
		49, 51	Revised diagram with separate explanations for RZ/A1 and RZ/A2M.
1.20	2019.12.23	1	Reference application notes were added.
		49	SD card slot connection example was corrected as shown below • COMMON pin was added. • The power supplies to CMD, DAT3 to DAT0, and VDD pins were changed to supplying via switch IC.
		56	CoreSight 10 connection example was added.
		58, 59	The descriptions of pin treatment were changed to being summarized by each module. RPC_INT# pin treatment was changed to being fixed to high level (pull-up). PVccSD1, PVcc_SD0, PVcc_SPI, and PVcc_HO were added to the table of unused pin treatment. A pullup power supply was added to the note.
		61	A note regarding the reference application notes that have detailed information was added to Table 8.1.
		64, 65	Check items (1-5, 7-4, 10-4 to 10-6, and 10-10 to 10-15) were added.
1.30	2020.05.26	19	Added a caption for the timing requirements reference.
		21	Added TRST# pin to the text as a pin that needs to be kept at low level during power on oscillation settling time.
		21	Added note when using external clock.
		40	Added explanation the bus width supported by LSI of this series in Figure 5.9.
		41, 48	Added pin treatment (pull-up) to data bus of Figure 5.10, Figure 5.11 and Figure 5.23.
		59	Added "connect to a power supply" to RPC_INT# pin treatment.
		66	Check item (Table 10.3) was added.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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