RYZ014A

Module Integration Guide

Introduction

This Application note helps customers creating their own board(s) based on the RYZ014A module successfully integrate and test their product.

It presents Integration Guidelines for:

- All RYZ014A Interface Requirements
- Tips and “how-to”s for troubleshooting

The rules and tips laid out in this document improve the quality of the final product. The process is split into three sections:

1. System Overview
2. Hardware and software design guidelines
3. Bring-up verification and test

Target Device

RYZ014A

Related Documents

- RYZ014A LTE Category M1 Module Datasheet (R19DS0111)

Contents

1. Overview

1.1 System Architecture

Figure 1-1 provides an overview of the Host - RYZ014A interfaces. They are detailed later in this document.

This picture includes:

- The digital interfaces between the RYZ014A and the host platform
- The power supply requirement (Vbat).

Note: V_{BAT1} range is 3.1V to 4.5V for 3GPP compliant operation. It can be pushed up to 5.5 V with loss of performance.

It does not show the RYZ014A local terminations.

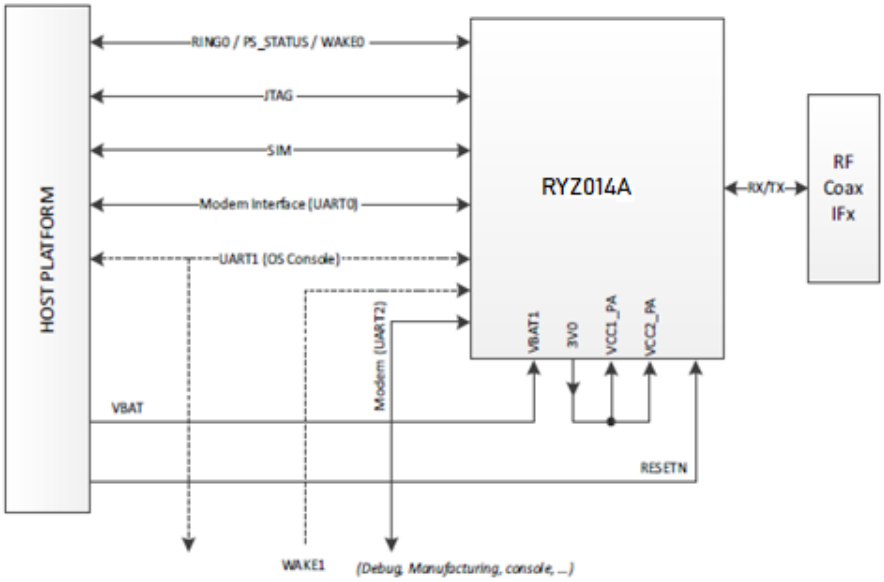

Figure 1-1. RYZ014A-Based System Architecture

1.2 Recommended Design Flow

Please follow the following instructions carefully during the design process.

1.2.1 Design Modifications

With respect to the RYZ014A reference design, only the following BOM modifications are allowed:

- SIM connector
- Level shifter on UARTs
- Circuitry on RESET_N

Please discuss any BOM modification with Renesas.

1.2.2 Schematics Review

Ensure by careful examination that the schematics complies with Renesas's module requirements. It is recommended to follow Renesas' Schematics Checklist available.

1.2.3 PCB Placement and Layout Review

To ascertain that the PCB layout meets the requirements, and avoid costly and time- consuming reworking, please follow Renesas' schematics checklist rules on component placement, RF and digital routing, final layout levels, etc.

1.2.4 Optimization

Once the board has been manufactured, engineers can decide to further optimize the design. It is also recommended to share the improvements with Renesas, which can help validate the implementation.

1.2.5 Functional Validation

A thorough testing of the design performance is required in order to undergo the final conformance checks confidently. Sharing the tests' results with Renesas helps identify any particular problem fixable at an early stage and increases the likelihood of qualification success. This should be done for all the tests that involve Renesas' chipsets.

Hardware Test Preparation explains how to set up the hardware prior to the test phases.

1.2.6 Manufacturing Recommended Process

The manufacturing process is described in the dedicated in the Module Manufacturing Guide.

2. Hardware Integration Recommendations

This chapter provides information about the various RYZ014A interfaces, as well as software-configurable features thereof and, more generally, good practices in board design.

Table 2-1 describes the requirements for trace characteristics.

Important: Requirements vary according to the signals routed. Please observe the following recommendations carefully.

Table 2-1. Requirements Overview: Trace Characteristic

Trace Characteristics	Description
Digital	Generic digital track of reasonable high impedance
Supply	Broader tracks whose DC resistance and inductance w/r to ground must be kept as low as possible. Use of multiple decoupling capacitors located as close as possible to the power pads is strongly encouraged
50 Ohm	Conventionally used for RF tracks. The impedance must be kept constant. Mitigation measures such as mitered corners must be used at the bends
Quiet	Keep the tracks short and away from digital signals, if possible on a buried layer
Ground	Connect the RYZ014A ground pads to the host ground using the shortest, lowest possible impedance paths. Do not hesitate to maximise the via count to lower the overall impedance

2.1 Power Supply

2.1.1 Synthesis of the Power Supplies

Table 2-2 provides an overview of the power supplies and their characteristics. Please refer to the RYZ014A Datasheet for more information..

Note: Each output reference voltage (pads 3, 9, 11) is switched off when the module is in deep sleep mode. They must therefore not be used to power external components that require an uninterrupted supply.

Table 2-2. Power Supply Signals

Pin Name	Pin Number	Trace Style	Direction	Notes
1V8	3	Supply	Out	Reference voltage. See the note above.
3V0	9,11	Supply	Out	Connect to VCC1_PA and VCC2_PA only. These pads must not be used for any other usage. See the note above
VBAT1	107, 108	Supply	In	Voltage used for qualification is 3.8 V, range 3.1 V to 4.5 V
VCC1_PA	97	Supply	In	To be connected to 3V0
VCC2_PA	98, 99	Supply	In	To be connected to 3V0

Table 2-3. Power Supply Digital Enable Signal

Pin Name	Pin Number	Trace Style	Direction	Notes
POWER_EN	106	Digital	In	Reserved. Must be connected to a 470 kΩ pull-down

2.1.2 Peak Current Consumption

Information provided here is measured peak current consumption for the RYZ014A Module in various LTE Tx/Rx configurations, with and without the DC/DC losses. It represents the maximum RMS current. The power consumption depends on LTE band of operation. Table 2-3 is provided by Bands for RRC Connected, 23dBm Tx, with UL and DL traffic.

Table 2-4. Peak Current Consumption by Bands

LTE Band	Measured Battery Peak Current (for VBAT1=3.1 V)
Band 1	680 mA
Band 4	630 mA
Band 13	610 mA
Band 19	620 mA

2.1.3 Power Supply Circuit Example

2.1.3.1 Test Points and Measurement Access

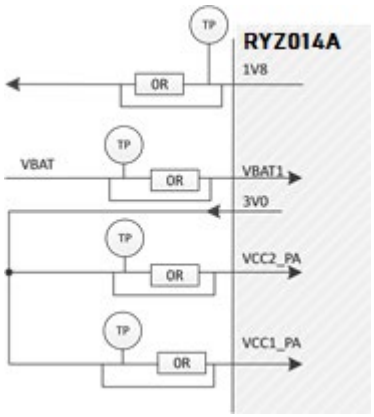

Figure 2-1. Power Supply System Example

A test point access is recommended on all supply nets so that the supply voltages can be measured.

Gaps filled with 0 Ω series bridges (as shown in Figure 2-1) are recommended on all supply nets. The 0 Ω bridges can be soldered/removed at will to ease the measure of the load currents of each supply source. The size of both the tracks and the 0 Ω chips must match the expected load current.

2.1.3.2 Special Layout Considerations

Please refer to Section Track Characteristic Design.

2.2 SIM Interface

2.2.1 Interface Description

Table 2-5 lists the RYZ014A's SIM interface pins.

Table 2-5. SIM Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Electrical Characteristics
SIM_CLK	14	Digital	Output from Module	SIM_VCC
SIM_DETECT Note	16	Digital	Input to Module	1V8
SIM_IO	17	Digital	Input or Output to/from Module	SIM_VCC
SIM_RESETN	12	Digital	Output from Module	SIM_VCC
SIM_VCC	18	Digital	Output from Module	1V8 or 3V0

2.2.2 Other Hardware Considerations

- Use a 100 nF decoupling capacitor on SIM_VCC.
- Use a 4.7 kOhm resistor between SIM_VCC and SIM_IO.
- Place the SIM tray as close as possible to the RYZ014A.
- A good ground connection must exist between the SIM card and the RYZ014A.
- If the application handles SIM card hot swapping, the SIM slot must contain a card detector in order for the software to process the event immediately. The software configuration defaults to SIM_DETECT support.
- If the SIM card tray does not support SIM_DETECT (not recommended), keep the SIM_DETECT signal high and configure the module for SIM card detection in polling mode.

2.3 Host Communications Signals

2.3.1 Introduction to UART Interfaces

Three UART interfaces, named UART 0, UART 1 and UART 2, drive the communication between the RYZ014A and the host platform. All support flow control.

UART interfaces can be configured as:

- Host-Modem interface (also named 'AT Commands mode'): the UART provides a means to configure the modem using AT commands. It also carries application data. This mode requires preferably a high-speed UART port with flow control.
- Debug interface (also referred to as DCP): it connects the Debug Tool during design verification or debugging. This mode also allows SFU upgrades.

Table 2-6. UART Interfaces Usage Synthesis

Pin Name	Available Usage of Port	Default Usage of port
UART0	Host-Modem AT commands OS Console	Host-Modem AT commands
UART1	Host-Modem AT commands OS Console	OS Console
UART2	Host-Modem AT commands DCP	DCP

The default configuration is set as shown in Table 2-6 and is configurable by software.

Important:

Important: A design based on the RYZ014A must provide access to UART 2 with

hardware flow control in order to perform debugging and upgrades during the development of the product. A simple UART connector or, more conveniently, a dedicated UART-to-USB converter chip and a USB connector, as implemented in the RYZ014A reference design, must be included during the hardware design. Renesas does not support module upgrades by other means than a UART 2 connection.

Various UART-to-USB converters work with RYZ014A Module based platforms, such as the Exar XR21V1410™ , the FTDI FT234XD™ or the FTDI FT4232H™ . Implementation examples are available in Renesas's or RYZ014A's reference designs schematics.

2.3.2 General Notes on UART Connections

RYZ014A uses the DCE-DTE convention for UART lines. It is designed for use as DCE (Data Communication Equipment).

The output from the device at one end of the link connects to the input at the other end of the link and vice versa. Figure 2-2 represents the typical implementation for the UART connection (including hardware flow control in case of high-speed UART).

The DCE (Data Communication Equipment) device speaks to the customer application (DTE) using the following signals:

- Port TXD on Application sends data to the RYZ014A's TXD signal line.
- Port RXD on Application receives data from the RYZ014A's RXD signal line.

Caution: If the Host does not support flow control, then connect RTS and

CTS signals to GND to prevent any interface lock up. Since the host does not know if the module is ready to receive data, one of the following additional mechanisms (hardware option or software option) is mandatory to avoid data loss:

- Hardware option: The host MCU samples the PS_STATUS signal to monitor the module's status
- Software option: The host MCU polls the module with a specific AT command until it gets correct answer. It then proceeds with its next AT command.

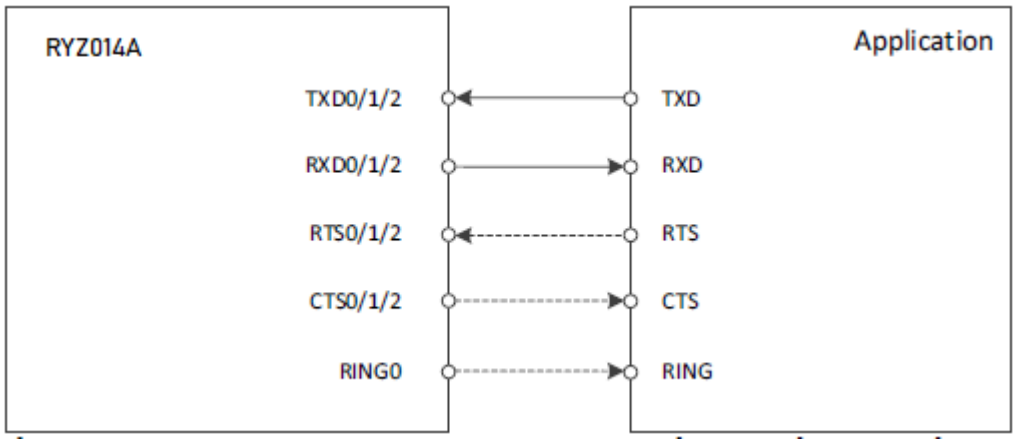

Figure 2-2. UART0, UART1, UART2 Connection Implementation

2.3.3 UART0 Interface

2.3.3.1 Interface Description

Important:

- See the Section Table 2-6 for usage of UART 0.
- If not used, the UART0 signals should be connected to test points.

Table 2-7 lists the RYZ014A pads dedicated to the UART0.

Table 2-7. UART0 Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Electrical Characteristics	Notes
RXD0	79	Digital	Out	1.8 V	UART0 RXD
TXD0	77	Digital	In	1.8 V	UART0 TXD
RTS0	75	Digital	In	1.8 V	UART0 RTS
CTS0	76	Digital	Out	1.8 V	UART0 CTS
GPIO25/RING0	89	Digital	Out	1.8 V	UART0 RING. It is recommended to pull-up this pin with the application host processor supply as it will become high impedance when module is in PS-PM suspend mode.

2.3.3.2 Default Configuration

The default software configuration of UART0 is AT Commands mode.

Important:

UART0 is configured for hardware flow control (RTS0, CTS0). During the boot cycle, it is mandatory that the host's serial port connected to UART 0 handle hardware flow control, because the module sends a +SYSSTART URC. If this isn't the case, the module can fail to boot properly.

The serial link settings are as follows:

- Baud rate: 921600
- Data: 8 bits
- Parity: None
- Stop: 1 bit
- Flow control: Hardware (RTS0/CTS0)

2.3.3.3 Behavior in Low Power Mode

- The module power mode selection is internally managed by the module software.
- RTS0 signal is used by the Host to wake the module up.
- The module will drive RING0 low to wake the Host up.

Note: URCs and data are sent immediately after RING0 goes down. The host might lose URCs and data if it does not read its serial port quickly enough.

Note: If UART 0 is not configured for hardware flow control, the host must observe the state of the PS_STATUS signal, or use AT polling, before sending any AT command after wake up. Commands sent before the UART is ready to accept them are likely either to be discarded or return an ERROR message.

2.3.4 UART1 Interface

2.3.4.1 Interface Description

Important:

- See the Section Host Communications Signals for usage of UART 1.
- If not used, the UART1 signals should be connected to test points.

Table 2-8 lists the RYZ014A pads dedicated to UART 1.

Table 2-8. UART1 Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Electrical Characteristics	Notes
GPIO15/RXD1	80	Digital	Out	1.8 V	UART1 RXD optional signal multiplexed with GPIO15. Default setting is RXD1.
GPIO14/TXD1	78	Digital	In	1.8 V	UART1 TXD optional signal multiplexed with GPIO14. Default setting is TXD1.
GPIO16/RTS1	83	Digital	In	1.8 V	Provisional UART1 RTS signal. Reserved.
GPIO17/CTS1	81	Digital	Out	1.8 V	Provisional UART1 CTS signal. Reserved.

2.3.4.2 Default Configuration

UART 1 defaults to console mode. Boot messages are sent on this interface as explained in section Confirm Module Power-Up Operation.

The serial link settings are as follows:

- Baud rate: 115200
- Data: 8 bits
- Parity: None
- Stop: 1 bit
- Flow control: None (no RTS1/CTS1)

2.3.4.3 Behavior in Low Power Mode

By default, UART1 cannot be used to wake the module from low power mode.

2.3.5 UART2 Interface

2.3.5.1 Interface Description

Important:

- See the Section Host Communications Signals for usage of UART 2.
- If not used, the UART2 signals should be connected to test points.

Table 2-9 lists the RYZ014A pins related to the UART2 interface.

Table 2-9. UART2 Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Electrical Characteristics	Notes
RXD2	56	Digital	Out	1.8 V	UART 2 RXD.
TXD2	58	Digital	In	1.8 V	UART 2 TXD
GPIO28/RTS2	10	Digital	In	1.8 V	UART 2 RTS
GPIO27/CTS2	8	Digital	Out	1.8 V	UART 2 CTS

2.3.5.2 Default Configuration

The default software configuration of UART2 is DCP mode, for debugging or upgrading.

Note: Hardware flow control is mandatory on UART2.

The serial link settings are as follows:

- Baud rate: 921600
- Data: 8 bits
- Parity: None
- Stop: 1 bit
- Flow control: Hardware (RTS2/CTS2)

Note: This interface can be used for software recovery in Firmware-From-Host (FFH) mode. The FFH mode is triggered when the FFF_FFH signal is driven low.

2.3.5.3 Behavior in Low Power Mode

UART2 cannot not be used to wake the module from low power mode.

2.4 RF Interface

2.4.1 RF Signals

2.4.1.1 RF Interface Signals

Table 2-10 RF Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Electrical Characteristics	Notes
LTE_ANT0	54	RF	In/Out	RF	LTE antenna. Special RF routing conditions

2.4.1.2 RF Control Signals

Table 2-11 RF Control Signals.

Pin Name	Pin Number	Trace Style	Direction	Electrical Characteristics	Notes
RFDATA12	39	Digital	In/Out		Reserved
RFDATA16	40	Digital	In/Out		Reserved
RFDATA17	41	Digital	In/Out		Reserved

2.4.2 Circuit Diagram Example

Important:

Figure 2-3 should be strictly followed as a topology reference. It is advised to copy the schematics verbatim. This document also describes the imperative layout constraints.

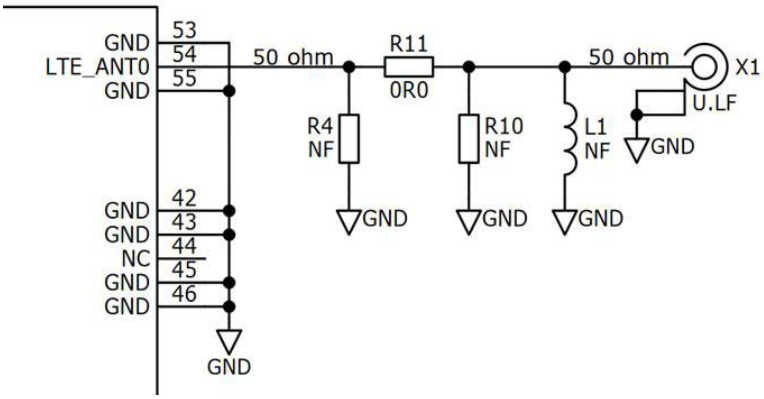

Figure 2-3. RF Typical Circuit

Note: The RF connector called X1 is for example purpose only. The presence of a connector and the type thereof are design dependent.

LTE_ANT0 is the primary (main) antenna pin and serves for both Tx and Rx signals.

Connect 50 Ω transmission lines from this pin to the 50 Ω primary antenna/antenna connector.

Figure 2-3 shows, between the LTE_ANT0 and the antenna connector, an impedance matching π-type network.

See Section Antennas and RF Design Considerations for more detail on connecting to these pins and for information on the π-type matching network and ESD protection.

2.4.3 Test Points and Measurement Access

50 Ohm termination points, for example P1 in Figure 2-3, are needed for Engineering and Production teams to assess the board's RF performance.

It might be needed to measure the RF path (as in RF Path) to tune the T-type matching network.

This requires access to the LTE_ANT0 pin #54, besides the 50 Ω RF connector. As there is, by design, no RF connector wired directly to pin #54, a coaxial cable (usually ø 1.25 mm semi-rigid) can be manually tied to it for precision impedance measurements. A grounded copper area on the top layer adjacent to this pin is required (GND pad are typically sufficient) to properly connect the cable to the RF ground and provide a sturdy physical binding.

Please refer to Section Antennas and RF Design Considerations for more detail on managing the RF Trace Design.

2.4.4 Antennas and RF Design Considerations

Antennas require special interfacing for optimum RX and TX Performance.

2.4.4.1 Antenna Impedance Matching

A 3-component π-type (or T-type) matching network is recommended. The three components of the matching network should be laid out adjacent one to another to minimise the interconnecting tracks' lengths. Use small parts with high Q.

Solder the ground side of the shunt(s) part directly to a ground plane, or use wide and short tracks to minimise the series inductance. The shunt part(s) need not be fitted if matching is unnecessary. The ground plane used for grounding the shunt element(s) of the matching circuit should ideally be the same as the 50 Ω transmission line's reference ground plane.

2.4.4.2 ESD Protection

ESD protection is a discretionary requirement and only required, if necessary, for higher ESD specifications than those provided by the RYZ014A.

It is recommended to select an ESD device with very low capacitance and small size (0201) to avoid impacting the RF impedance.

2.4.4.3 Standard Impedance Transmission Lines

There are four possible methods to design 50 Ohm transmission lines:

1.If the RF track runs on the outer metal layer:

- Microstrip
- Coplanar waveguides

2. If the RF track runs on an inner metal layer:

- Embedded microstrip
- Stripline

Irrespective of which one is selected:

- Pay attention that the maximum insertion loss between the RF pad and the antenna must be kept under 0.5 dB.
- Transmission lines EM fields extend beyond the RF track and couple to adjacent layers:

For microstrip, the lateral gap running along the track must be at least twice (ideally three times) the thickness between the track and its underlying ground plane.

Both in microstrip and co-planar cases, adjacent metal areas must be present and properly connected to the main ground plane, so as to absorb the fringing EM fields.

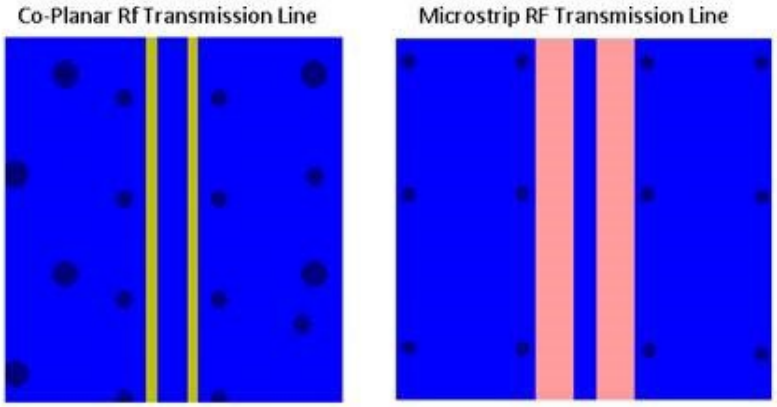

Figure 2-4. Transmission Line Implementation Examples

Figure 2-4 provides examples of both transmission line implementations, specifically showing:

a) The distance between the transmission line and the side-running grounded area on layer 1.

b) The periodic via connections connecting the top metal layer to the reference GND layer of the transmission line.

- Avoid routing of noisy signal tracks adjacent to RF transmission lines to minimize cross-coupling into RYZ014A's RF ports.
- The component pads of the SMD parts used in the 3-component π/T-type matching circuit are effectively very short transmission lines. To minimise the RF insertion loss (s11, VSWR) caused by the width step, use tapered ends.

2.4.4.4 ANT_LTE Specific Footprint Design

The ANT_LTE pad must be considered as a short transmission line whose width is the same as the pad's width. To minimise discontinuity, the ground layer immediately below the pad must be cut out as shown in Figure 2-5. Use a quasi-static (in coplanar wave mode) or fullwave EM simulator to compute the extent of the underlying ground area that needs to be removed in order to reach the 50 Ω goal impedance.

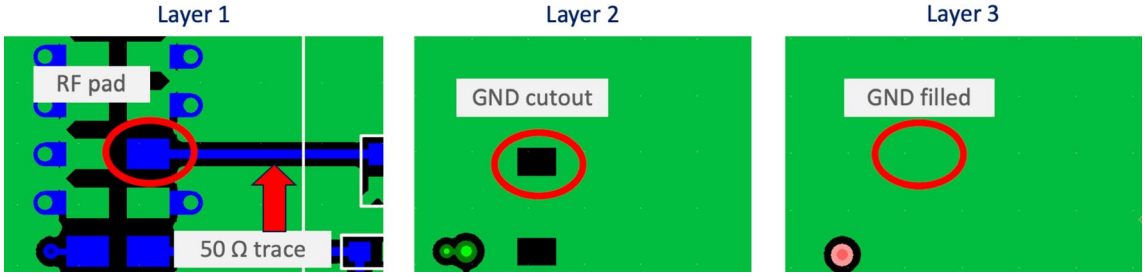

Figure 2-5. ANT_LTE Pad Design

2.5 Reset and Environmental Signals

Table 2-12 lists the Reset and other environmental signals and the following subsections describe their purpose and termination requirements.

Table 2-12 Non-Interfacing Signals

Pin Name	Pin Number	Trace Style	Direction	Electrical Characteristics	Notes
GPIO2/ PS_STATUS	6	Digital	Out	1V8	- Power Saving status - Should be connected to a test point for debug purpose • High level: module is active • Low level: module is in Low Power Mode This signal can be used to inform the host that the module needs waking using RTS0, WAKE0 or WAKE1 before sending data or AT command on the UARTs.
GPIO3/STATUS _LED	2	Digital	In/Out	1V8	Status LED (STATUS_LED, OUT) by default. LED is inactive by default
JTAG_TDO	48	Digital	Out		JTAG interface. Each signal should be connected to a test point. It is helpful to add a 1.8V and GND test points to ease the connection (or even better, an unfitted test pin header).
JTAG_TRSTN	49	Digital	In		
JTAG_TMS	50	Digital	In		
JTAG_TDI	51	Digital	In		
JTAG_TCK	52	Digital	In		
RESERVED/ FFF_FFH	5	Digital	In	1V8	Reserved pad: it must be Pulled Up and connected to a Test Point. Pin #3 (1V8) can be used to pull it up. FFF_FFH: Active high by default (FFF: Firmware From Flash). Firmware From Host (FFH) if driven low.
RESETN	47	Digital	In	1V8	Pull up this signal with a voltage up to 3.6V (active low, 1V8 recommended)
WAKE1	96	Digital	In		Wake input. WAKE inputs are level triggered (configurable by software to 0 or 1). Minimum level duration for reliable detection: 100 µs. Not set as a wake-up source by default. Active high or low level.
WAKE0	104	Digital	In		Wake input. Note: WAKE inputs are level triggered (configurable by software to 0 or 1). Minimum level duration for reliable detection: 100 µs. Not set as a wake-up source by default. Active high or low level.

2.6 PCB Layout Rules

This section provides general good practices in defining a PCB layout.

2.6.1 Placement

Placement should be performed before any routing. This is especially important for:

- The RYZ014A module
- The RF interface

Initial placement of these parts allows assessment of the PCB floor layer usage and prevents significant changes to final routed areas of the design, should a placement issue be found. It also provides an opportunity for Renesas to review the PCB.

When placing these elements:

1. Keep them in a similar quadrant than the other parts they interface with
2. Choose the orientation to keep track crossings to a bare minimum
3. Keep every part as close as possible to the RYZ014A module.

2.6.2 Trace Characteristic Design

This section explains some standard design rules applicable to the different types of signals (digital, power supply, RF).

2.6.2.1 Digital Traces

1. Careful and logical placement of digital signals is required to minimize cross- coupling between tracks.
2. Pay attention to ground currents during routing. Make sure that the grounding surrounding the tracks (from source to load) remains continuous, with no notches or gaps. Long and/or winding ground return currents can create EMI problems.
3. Ensure the tips listed in Section Controlled Impedance Traces are taken into account for digital traces requiring specific impedance.
4. Keep digital tracks with no impedance needs thin to avoid a build-up of capacitance, while keeping them within manufacturing constraints.
5. If tracks are routed one atop the other, keep them orthogonal. Alternate layer tracks' direction to minimize cross-coupling.
6. Important recommendations related to SIM connector placement can be found in the section Table 2-5
7. Shield the clock signal vias.
8. The top and bottom layers should be filled with ground planes and only the minimal number of tracks.
9. Bury as many tracks as possible, especially data (UART, etc) and clock tracks. If it is not possible to bury everything, leave only static signals (such as RESETN, etc) on the external layers.
10. A few signals can be further filtered, although this is not typically necessary. These signals are:
    - 1V8_LTE, with a π filter.
    - All SIM signals, with decoupling capacitors placed as close as possible to the SIM connector.
11. The tracks between the SIM connector and the RYZ014A should be kept as short as possible, and away from the antenna.
12. Data and clock signals should be routed as far as possible from the antenna area.

2.6.2.2 Power Supply Traces

1. Size the power supply tracks appropriately to provide a low resistance, low impedance source. Pay attention to the number of vias used when routing tracks across multiple layers, as they add spurious series resistance. This is especially true for high current signals such as the PA supply voltage.
2. The decoupling capacitors ground pad of each power supply signal must be connected to the ground return of the source.
3. Keep digital tracks well away from the power supply tracks.

2.6.2.3 RF Traces

1. Avoid burying these traces as much as possible, because it increases RF losses w/r to top/bottom routing.
2. Keep as short as possible to help reduce RF losses.
3. Try to mitigate impedance discontinuities. Use tapered ends to improve the matching with SMD pads.
4. Ensure the steps provided in section Controlled Impedance Traces are taken into account when computing the trace width.

2.6.2.4 Controlled Impedance Traces

- Calculation of traces width and spacing:

  Use simple RF design tools to calculate the copper trace thicknesses based upon:

  (a) The thickness of the dielectric substrate lying between the RF copper trace and the ground plane.

  (b) The spacing between the copper trace and the adjacent ground plane (on the same layer).

  (c) The dielectric constant (ε r) of the substrate material.

  If the required trace width is impossible to manufacture, consider one of the following measures:

  – Thicker substrate

  – Moving the reference ground plane down one layer by cutting out the ground plane under the transmission line under design

- General good practice guidelines

  (a) Careful placement is required to keep RF traces short and straight.

  (b) Do not route RF traces on buried layers.

  (c) Ground planes beneath RF traces should be continuous.

  (d) The ground plane running along the RF tracks should be kept distant enough to not alter the track's impedance.

- RF matching component footprints

  Use tapering to minimise impedance mismatch at the end of tracks. If the parts are significantly wider than the transmission lines, the ground reference should be lowered.

2.6.2.5 Grounding

1. RF ground planes should be as large and continuous as possible and not be cut into chunks. Check that strings of signal vias do not inadvertently create slots in ground.
2. Apply ground plane flooding on all layers.
3. Apply extensive via stitching. Make sure to scatter the vias evenly over the ground planes.
4. Use extra vias around sensitive areas such as RF tracks and noisy lines.
5. Stitch tight all along the board edges to create a Faraday's cage.

2.6.3 Thermal Considerations

This section summarizes important design requirements about thermal dissipation. Unless the board is meant to be used in a cold environment, designing for an efficient thermal flow is critical. The temperature of the module, measured by the embedded thermistor, must always remain within acceptable limits (85 °C), especially when the product operates at its maximum permissible ambient temperature in a closed, not vented box.

2.6.3.1 Module Grounding Pads

- All Gxx pads must be tied to a large ground plane which serves as a thermal sink.
- That ground area below the Gxx pads must be stitched with through vias, which conduct heat towards the opposite side of the board.
- Besides, adding blind vias surrounding the Gxx pads area help spread the heat flow evenly amongst layers.
- If a metal casing is used, it should ideally be in tight contact with the bottom ground layer so as to serve as a terminal heat sink.
- If these measures cannot be implemented, or do not suffice, additional elements such as heat sinks, fans or thermal grease (*GapPad*™) can be used.

3. Bring-Up and Testing

3.1 Introduction

The purpose of this chapter is to describe board bring-up, test and qualification.

The expectations at this stage are:

1. Any inconsistent and potentially hazardous manufacturing faults must be eliminated.
2. Clearance to proceed with further detailed calibration and measurements.
3. Evaluate the board's performances.

3.2 Prerequisites

Hardware Qualification consist of:

- Checking for RF losses between the RYZ014A RF ports and the board's RF output
- A sanity check of the connections to the RYZ14A
- Debugging, if necessary

Hardware Qualification procedures make use of:

1. An external Host PC / Laptop for monitoring the UART 1 interface

Note: Detailed information will be provided in a future revision of this document.

2. LTE RF test equipments:

   (a) A shielding box to avoid any RF interference caused by the environment

   (b) RF components such as: cables, splitters, 50 Ω dummy loads

3. A power supply with ammeter

3.3 Functional Verification without Assembled Module

3.3.1 Power Supply

3.3.1.1 Test Procedure

Figure 3-1 presents the equipment necessary to perform the next following test steps and the required configuration for test.

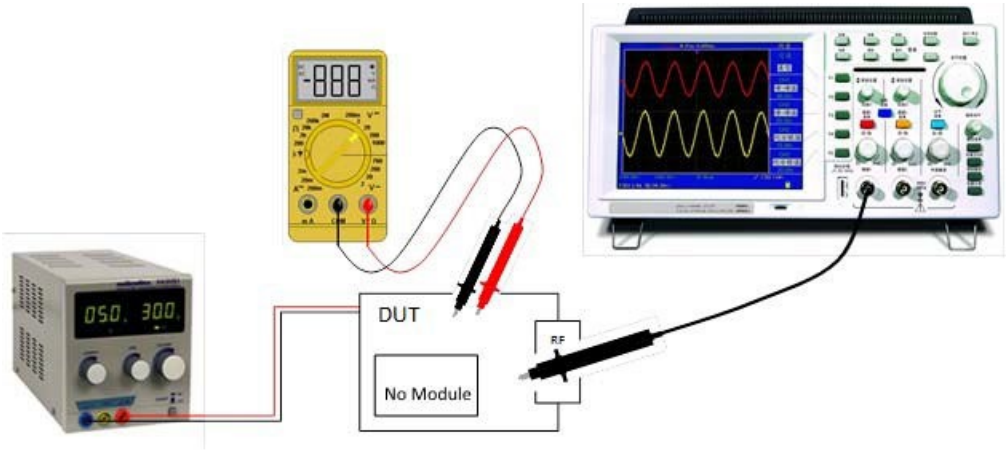

Figure 3-1. Pre-Test Configuration (No Module on Board)

- Test voltage values

  Test the DC nature of the voltage delivered by the power supply with an oscilloscope before connecting the DUT. Confirm that the voltage level is correct and stable. Once the power supply is confirmed, you can power the DUT and measure accurately the test points voltage with a multimeter. At this stage, only VBAT1 can be tested.

  Check at each voltage test point, as illustrated on Figure 3-2, that the voltage value corresponds to what is expected. The value of VBAT1 must be in the range specified in the RYZ014A Datasheet, section Electrical Operating Conditions.

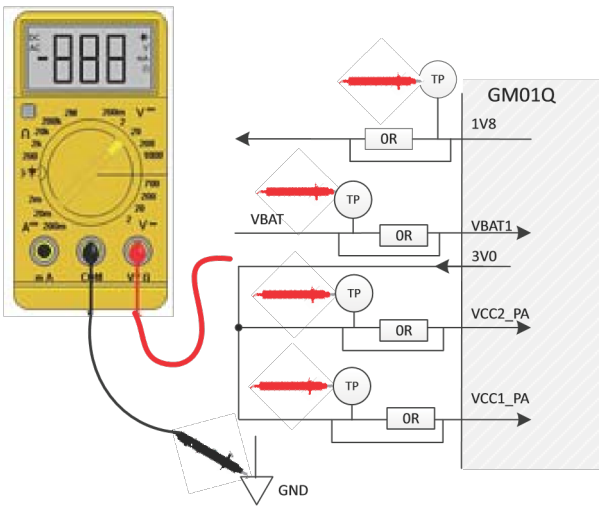

Figure 3-2. Measuring Voltage Value (RYZ014A)

3.3.1.2 Troubleshooting

If the VBAT1 voltage is incorrect, check any resistor link to detect unexpected short or open circuits.

3.3.2 RF Path

3.3.2.1 Test Procedure

Important:
Those tests should be run or supervised by engineers with RF measurement.

- RF path check
  To avoid any issue on RF extra path (from the RYZ014A module antenna output to the board antenna connector), the purpose of this part is to check its integrity. It corresponds to losses between RYZ014A pin 54 and the antenna port of the board.
  Figure 3-3 provides an overview of the equipment configuration for this test. The connection to the block labeled “RF” is a connection to the RYZ014A pin 54, using an RF soldered coaxial probe and RF cable connected to the SMA RF connector.

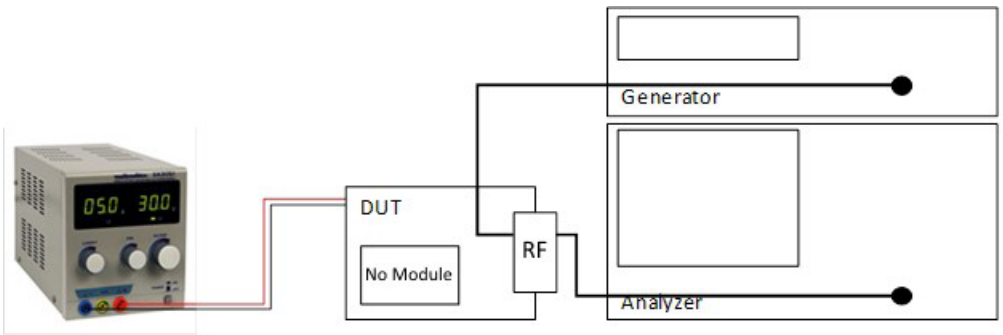

Figure 3-3. RF Path Check Setup

(a) Measure and record the insertion loss on all the supported LTE bands for the antenna from pin 54 of the RYZ014A to LTE port antenna
(b) By design, the extra RF path loss must be lower than 0.5 dB, to assume having good RF performances.

3.3.2.2 Troubleshooting

- In case of unexpected RF losses:
  1. Check the coaxial connectors for dry joints or mismatched placement.
  2. Test with an ohmmeter that the soldered SMA is not shorted or opened.
  3. Verify the RF equipment calibration, including the coaxial cable used to connect to the RYZ014A pin 54 and LTE port antenna.
  4. Verify the RF matching.

3.4 Functional Verification with Assembled Module

The following tests aim at validating the assembly process of the module.
They cover:
1. RYZ014A pins and features:
   (a) Power supply

(b) UART1 console output during power-up operation
(c) SIM Interface
(d) GPIOs
2. Nominal power consumption
3. RYZ014A's boot

3.4.1 Power Supply

3.4.1.1 Test Procedure

1. Turn on the device under test.
2. Confirm voltages of the power supplies remain in line with the specifications from the datasheet. See the test points involved on Figure 3-2.

   Caution:
   If, at this point, the voltages are incorrect, stop immediately to diagnose the cause of the issue.

3. Confirm that the current is nominal from the Host power supply

3.4.1.2 Troubleshooting

- Excessive current draw
  Check all RYZ014A voltage supplies. Confirm that there is no RYZ014A supply short circuits. Voltage should be nominal.
- No, or too little, current:
  1. Check the external power supply wiring
  2. Check for dry joint between adjacent RYZ014A pin(s) and the power supply source.

3.4.2 Confirm Module Power-Up Operation (UART1)

The console (on UART 1) should display these messages (when booting in FFF mode):

```
[0000000000] RBGerbil 11.11@35517 '5.1.1.0 [35517]'
[0000000004] Reset cause 'EXT'(real 'EXT' ) (bootWDG : '0')
 [rawRst '0x00000001']
[0000000012] regConfig 0xC8ECF1E8@1
[0000000015] boot: Current flash, timeout 10000, proto thp
[0000000020] boot: FFF mode
[0000000183] elf: ELF format selected
[0000000186] elf: Header finished
[0000000189] elf: Waiting for 480 bytes
[0000000193] elf: PH 0x00001000, 132 bytes
...
[0000000252] elf: PH 0x00750000, 108336 bytes
[0000000259] elf: PH 0x007A0000, 325792 bytes
[0000000272] elf: Program Header finished
[0000000276] boot: Can't allocate memory for ext boot ABI
 descriptor
[0000000282] sbp: Booting at 0x1C1C0320...
>INFO> DCP : Init over='serial'
[fs] Overlay filesystem mounted on /fs
[PSP] initializing
```

3.4.3 GPIOs

3.4.3.1 Procedure

This section helps to confirm a GPIO's behavior.

Use the command AT+SMGT.
The first 32-bits triplet of parameters is a bit-mask to address the GPIO, the second 32-bits triplet of parameters is the bit-mask of the value the GPIO must take, and the third 32- bits triplet provides the expected polarity setting for the GPIO. Refer to Manual for more detail on this command.

The following command sets RYZ014A_GPIO_38 (GPIO[38]) to 1, active low. Value 38 is represented by the bitmask 0x4000000000, coded as triplet 0,0x40,0.

AT+SMGT=0,0x40,0,0,0x40,0,0,0x40,0
Test the expected behaviour as needed by your implementation.

3.4.3.2 Troubleshooting

- Unexpected AT command error:
  Make sure that the version of the firmware used is correct.
- Unexpected GPIO behavior:
  Ensure that there exists no short or open circuit between the test point and the RYZ014A.

3.4.4 SIM Communication

3.4.4.1 Procedure

Use AT+SMST?to check the SIM, as described in the Manual. Wait for the response:

+SMST=<status>. <status>can be:

– OK: Test OK.

– NO SIM: No SIM card was detected.

– NOK: Test completed and NOK.

3.4.4.2 Troubleshooting

- Unexpected AT command error
  Make sure the firmware version is correct.
- Unexpected SIM behavior
  - Check all the connections between the SIM housing and the RYZ014A module comply to the tips given in the section SIM Interface.
  - Ensure that there exists no short or open circuit between the SIM housing and the RYZ014A.
  - Check ground continuity.

Appendix

A Abbreviations

Table A-1 Abbreviations

(1/2)

AC	Alternate Current
ACLR	Adjacent Channel Leakage Ratio
LTE_ANT0	Antenna 0 for LTE
AT Command	Modem-type commands prefixed with AT characters
ATR	Answer To Reset (SIM)
BOM	Bill Of Material
cDRX	Connected Discontinuous Reception
CLI	Command Line Interface
CMOS	Complementary Metal Oxide Semiconductor
COM	Communication
CPU	Central Processing Unit
CS	Chip Select
dB	decibel
DC	Direct Current
DCP	Data Communication Protocol
DL	Downlink
DRX	Discontinuous Reception
DUT	Device Under Test
DVM	Digital Voltmeter
EM	Electromagnetic
EMI	Electromagnetic interference
FFF	Firmware From Flash module boot mode
FFH	Firmware From Host module boot mode
FS	File System
FW	Firmware
GND	Ground
GPIO	General Purpose Input/Output
HW	Hardware
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
IT	Interrupt
LNA	Low-Noise Amplifier
LTE	Long-Term Evolution. See also www.3gpp.org/.

Table A-1 Abbreviations

(2/2)

MAC	Medium Access Control protocol layer
MII	Medium Independent Interface
MIO	Multiple Input/Output
MXA	Signal Analyzer
MXG	Signal Generator
NIE	Internal format for data representation
OBB	Opaque Binary Blob file format
PA	Power amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PPS	Protocol and Parameters Selection (SIM)
PS	Power Supply
PS-P	Power supply state. See section Operating Modes.
PS-PA	Power supply state. See section Operating Modes.
PSI	Platform Specification Interface
R	Short notation for Ohm
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RX	Reception
S/N	Serial Number
SIM	Subscriber Identity Module
SMA	RF connector type
SMD	Storage Module Device
SPI	Serial Peripheral Interface
SW	Software
TX	Transmission or Emission
UART	Universal Asynchronous Receiver Transmitter
UE	User Equipment
UL	Uplink
USB	Universal Serial Bus
USIM	Universal SIM.
WP	Write Protect

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug.19.21	—	First release document
1.10	Jun.27.22	—	Added 2.1.2 Peak Current Consumption Removed ADC, GNSS Removedd Appendix Checklist Update all pages

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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