RX660 Group

Initial Settings Example

Introduction

This application note describes the settings that must be made after a reset of a RX660 Group microcontroller, including clock settings, disabling of peripheral functions still running after a reset, and nonexistent port settings.

Target Device

- RX660 Group 144-pin versions, ROM capacity: 1 MB/512 KB
- RX660 Group 100-pin versions, ROM capacity: 1 MB/512 KB
- RX660 Group 80-pin versions, ROM capacity: 1 MB/512 KB
- RX660 Group 64-pin versions, ROM capacity: 1 MB/512 KB
- RX660 Group 48-pin versions, ROM capacity: 1 MB/512 KB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

The sample code makes settings to disable peripheral functions still running after a reset, nonexistent port settings, and clock settings. The description in this application note applies to the processing that occurs following power-on (cold start).

1.1 Disabling Peripheral Functions Still Running After a Reset

Some peripheral functions start operating immediately after power-on, and some have the module stop function disabled. The processing covered under this item disables the following functions:

DMAC, DTC, RAM

Note that the above processing is not performed by the sample code. As necessary, overwrite the corresponding constants to execute the processing.

1.2 Nonexistent Port Settings

The direction control bits for nonexistent ports must be set as described in 20.4, “Initialization of the Port Direction Register (PDR),” in the hardware manual. The initial settings contained in the sample code accompanying this application note are appropriate for 144-pin products.

Change constants appropriate to the product used.

1.3 Clock Settings

1.3.1 Overview

The procedure for making clock settings is as follows:

1. Sub-clock settings
2. Main clock settings
3. HOCO clock settings
4. PLL clock settings
5. System clock switching

By making changes to the constants defined in r_init_clock.h, the sample code described in this application note can be used to change the various clock settings.

The sample code sets the PLL clock as the system clock and does not use a sub-clock. Overwrite the constants as necessary to match the clocks you wish to use.

1.3.2 Clock Specifications Assumed in Sample Code

Table 1.1 lists the clock specifications assumed in sample code.

Table 1.1 Clock Specifications Assumed in Sample Code

Clock	Oscillation Frequency	Oscillation Stabilization Time	Remarks
Main clock oscillator	24 MHz*1	4.2 ms*2	Crystal
Sub-clock oscillator	32.768 kHz*1	1.3 s*2	
PLL clock	240 MHz (HOCO clock ×1/1 ×12)	—*3	
HOCO clock	20 MHz	—*3	

Note 1. Oscillation disabled by the sample code.

Note 2. The oscillator's stabilization time will differ due to factors such as the wiring pattern and oscillation constant of the system. To obtain the oscillation stabilization time, request an evaluation by the oscillator manufacturer of the system in which the oscillator will be used.

Note 3. See Electrical Characteristics in User's Manual: Hardware.

1.3.3 Clock Selection

By making changes to the constants defined in r_init_clock.h, the sample code described in this application note can be used to select settings such as the clock source of the system clock and whether each clock is oscillating or stopped. To determine which constants can be changed, see the listing of (user changeable) constants used by the sample code in Table 3.7 and Table 3.8.

Table 1.2 and Table 1.3 lists clock selection examples. The sample code sets the PLL clock (Clock source: HOCO clock) as the system clock and does not use a sub-clock (No. 1).

Table 1.2 Clock Selection Examples (1/2)

No.	1	2	3	4
System clock	PLL clock (Clock source: HOCO clock)	PLL clock (Clock source: HOCO clock)	PLL clock (Clock source: Main clock)	PLL clock (Clock source: Main clock)
PLL clock	Oscillating	Oscillating	Oscillating	Oscillating
Main clock	Stopped	Stopped	Oscillating	Oscillating
HOCO clock	Oscillating	Oscillating	Stopped	Stopped
Sub-clock	Stopped	Oscillating (using RTC)	Stopped	Oscillating (using RTC)
Constants				
SEL_SYSCLK	CLK_PLL	CLK_PLL	CLK_PLL	CLK_PLL
SEL_PLL	B_USE_PLL_HOCO	B_USE_PLL_HOCO	B_USE_PLL_MAIN	B_USE_PLL_MAIN
REG_PLLCR*3	1710h	1710h	1300h	1300h
SEL_MAIN	B_NOT_USE	B_NOT_USE	B_USE	B_USE
SEL_HOCO	B_USE	B_USE	B_NOT_USE	B_NOT_USE
SEL_SUB*1*2	B_NOT_USE	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_RTC*1*2	B_NOT_USE	B_USE	B_NOT_USE	B_USE

Note 1. Set SEL_SUB to B_USE (use) when the sub-clock is used as the system clock, and set SEL_RTC to B_USE when the sub-clock is used as the RTC count source. The sub-clock oscillates when either SEL_SUB or SEL_RTC, or both of them, are set to B_USE.

Note 2. The sub-clock and RTC cannot be used in products with no sub-clock oscillator. In this case, set SEL_SUB and SEL_RTC to B_NOT_USE (not use).

Note 3. This is the value to set in PLL Control Register (PLLCR).

Table 1.3 Clock Selection Examples (2/2)

No.	5	6	7	8
System clock	HOCO clock	HOCO clock	Main clock	Main clock
PLL clock	Stopped	Stopped	Stopped	Stopped
Main clock	Stopped	Stopped	Oscillating	Oscillating
HOCO clock	Oscillating	Oscillating	Stopped	Stopped
Sub-clock	Stopped	Oscillating (using RTC)	Stopped	Oscillating (using RTC)
Constants				
SEL_SYSCLK	CLK_HOCO	CLK_HOCO	CLK_MAIN	CLK_MAIN
SEL_PLL	B_NOT_USE	B_NOT_USE	B_NOT_USE	B_NOT_USE
REG_PLLCR*3	1710h*4	1710h*4	1710h*4	1710h*4
SEL_MAIN	B_NOT_USE	B_NOT_USE	B_USE	B_USE
SEL_HOCO	B_USE	B_USE	B_NOT_USE	B_NOT_USE
SEL_SUB*1*2	B_NOT_USE	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_RTC*1*2	B_NOT_USE	B_USE	B_NOT_USE	B_USE

Note 1. Set SEL_SUB to B_USE (use) when the sub-clock is used as the system clock, and set SEL_RTC to B_USE when the sub-clock is used as the RTC count source. The sub-clock oscillates when either SEL_SUB or SEL_RTC, or both of them, are set to B_USE.
Note 2. The sub-clock and RTC cannot be used in products with no sub-clock oscillator. In this case, set SEL_SUB and SEL_RTC to B_NOT_USE (not use).
Note 3. This is the value to set in PLL Control Register (PLLCR).
Note 4. The value of REG_PLLCR is arbitrary because PLL clock is stopped.

1.4 Notes on Voltage Level Setting Register (VOLSR)

1.4.1 Notes on Setting VOLSR

For RX660, the voltage level setting register (VOLSR) needs to be set properly according to conditions and voltages used.

Conditions and voltages:

- Whether to use the RIIC, and when used, voltage level of power supply (VCC)

In this application note, the voltage level setting register (VOLSR) is set to initial values shown in the following table assuming to use Renesas Starter Kit for RX660 with factory settings.

Table 1.4 Initial Values Set in the Voltage Level Setting Register (VOLSR)

Symbol	Bit Name	Function	Initial Value	Description of Why the Initial Value is Used
RICVLS	RIIC operating voltage setting bit	0: VCC ≥ 4.5 V 1: VCC < 4.5 V	1	Factory setting of power supply on Renesas Starter Kit for RX660 is 3.3 V.

2. Operation Confirmation Conditions

The operation of the sample code referenced in this application note (No. 1 to 6 in Table 1.2) has been confirmed under the following conditions.

Table 2.1 Operation Confirmation Conditions

Item		Contents
MCU used		R5F56609HDFB (RX660 Group)
Operating frequency	PLL clock (Clock source: HOCO clock) selected as system clock (No. 1 and 2 in Table 1.2) (No.1 is default setting of sample code)	HOCO clock: 20MHz PLL clock: 240 MHz (HOCO clock ×1/1 ×12) System clock (ICLK): 120 MHz (PLL clock ×1/2) Peripheral module clock A (PCLKA): 120 MHz (PLL clock ×1/2) Peripheral module clocks B D (PCLKB PCLKD): 60 MHz (PLL clock ×1/4) Flash interface clock (FCLK): 60 MHz (PLL clock ×1/4) External bus clock (BCLK): 60 MHz (PLL clock ×1/4)
	HOCO clock selected as system clock (No. 5 and 6 in Table 1.3)	HOCO clock: 20 MHz System clock (ICLK): 20 MHz (HOCO clock ×1) Peripheral module clock A (PCLKA): 20 MHz (HOCO clock ×1) Peripheral module clock B D (PCLKB PCLKD): 20 MHz (HOCO clock ×1) Flash interface clock (FCLK):20 MHz (HOCO clock ×1) External bus clock (BCLK):20 MHz (HOCO clock ×1)
	Main clock selected as system clock (No. 7 and 8 in Table 1.3)	Main clock: 24MHz System clock (ICLK): 8 MHz (main clock ×1) Peripheral module clock A (PCLKA): 24 MHz (main clock ×1) Peripheral module clock B D (PCLKB PCLKD): 24 MHz (main clock ×1) Flash interface clock (FCLK): 24 MHz (main clock ×1) External bus clock (BCLK): 24 MHz (main clock ×1)
Operating voltage		3.3 V
Integrated development environment		Renesas Electronics e^2 studio Version: 2022-04
C compiler		Renesas Electronics C/C++ Compiler Package for RX Family V 3.04
		Compiler option The integrated development environment default settings are used.
iodefine.h version		V 1.00
Endian		Little endian or big endian
Operating mode		Single-chip mode
Processor mode		Supervisor mode
Sample code version		Version 1.00
Board used		Renesas Starter Kit for RX660 (Product No. RTK556609Hxxxxxxxx)

3. Software

After disabling peripheral functions still running after a reset and making nonexistent port settings, the sample code makes clock settings.

3.1 Disabling Peripheral Functions Still Running After a Reset

The sample code disables peripheral functions still running after a reset.

Only the peripheral modules listed below are not in the module stop state after a reset is canceled. To transition a module to the module stop state, set the corresponding module stop bit to 1 (transition to module stop state). Putting modules into the module stop state and halting functions can reduce the power consumption of the device.

In the sample code the value of the constant MSTP_STATE_<target module name> is 0 (MODULE_STOP_DISABLE), so the target module does not transition to the module stop state. To transition one or more modules to the module stop state on the target system, set the corresponding constant(s) to 1 (MODULE_STOP_ENABLE) in r_init_stop_module.h.

Table 3.1 lists the peripheral modules that are not in the module stop state after a reset.

Table 3.1 Peripheral Modules Not in Module Stop State After a Reset

Peripheral Module	Module Stop Setting Bit	Value After Reset	Setting When Not Using Module
DMAC/DTC	MSTPCRA.MSTPA28 bit	0 (module stop state canceled)	1 (transition to module stop state)
RAM	MSTPCRC.MSTPC0 bit		

3.2 Nonexistent Port Settings

3.2.1 Processing Overview

The sample code sets the bits in the PDR registers corresponding to nonexistent ports to 1 (output). When writing in byte units to PDR or PODR registers containing nonexistent ports after this function has been called, set the direction control bits corresponding to the nonexistent ports to 1 and the port output data storage bits corresponding to the nonexistent ports to 0.

Table 3.2 lists the nonexistent ports.

Table 3.2 Nonexistent Ports

Port Symbol	144-Pin Products	Pins	100-Pin Products	Pins	80-Pin Products	Pins
PORT0	-	-	P00～P02	3	P00～P02	3
PORT1	P10 P11	2	P10 P11	2	P10 P11	2
PORT2	-	-	-	-	P22～P25	4
PORT3	-	-	-	-	P33	1
PORT4	-	-	-	-	-	-
PORT5	P57	1	P56 P57	2	P50～P53 P56 P57	6
PORT6	-	-	P60～P67	8	P60～P67	8
PORT7	-	-	P70～P77	8	P70～P77	8
PORT8	P84 P85	2	P80～P87	8	P80～P87	8
PORT9	P94～P97	4	P90～P97	8	P90～P97	8
PORTA	-	-	-	-	PA7	1
PORTB	-	-	-	-	-	-
PORTC	-	-	-	-	PC0 PC1	2
PORTD	-	-	-	-	PD3～PD7	5
PORTE	-	-	-	-	PE6 PE7	2
PORTF	PF0～PF4	5	PF0～PF7	8	PF0～PF7	8
PORTH	PH4 PH5	2	PH4 PH5	2	PH4 PH5	2
PORTJ	PJ0 PJ2	2	PJ0 PJ2 PJ4 PJ5	4	PJ0 PJ2～PJ5	5
PORTK	PK0 PK1 PK6 PK7	4	PK0～PK7	8	PK0～PK7	8
PORTL	PL2～PL7	6-	PL0～PL7	8-	PL0～PL7	8
PORTN	PN0～PN5	6	PN0～PN5 PN7	7	PN0～PN5 PN7	7

Port Symbol	64-Pin Products	Pins	48-Pin Products	Pins
PORT0	P00～P02 P04～P06	6	P00～P07	8
PORT1	P10～P13	4	P10～P13	4
PORT2	P20～P25	6	P20～P25	6
PORT3	P33 P34	2	P32～P34	3
PORT4	-	-	P43 P44	2
PORT5	P50～P53 P56 P57	6	P50～P57	8
PORT6	P60～P67	8	P60～P67	8
PORT7	P70～P77	8	P70～P77	8
PORT8	P80～P87	8	P80～P87	8
PORT9	P90～P97	8	P90～P97	8
PORTA	PA2 PA5 PA7	3	PA0 PA2 PA5 PA7	4
PORTB	PB2 PB4	2	PB2 PB4 PB6 PB7	4
PORTC	PC0 PC1	2	PC0～PC3	4
PORTD	PD0～PD7	8	PD0～PD7	8
PORTE	PE6 PE7	2	PE0 PE5～PE7	4
PORTF	PF0～PF7	8	PF0～PF7	8
PORTH	PH4 PH5	2	PH4～PH7	4
PORTJ	PJ0～PJ5	6	PJ0～PJ5	6
PORTK	PK0～PK7	8	PK0～PK7	8
PORTL	PL0～PL7	8	PL0～PL7	8
PORTN	PN0～PN5 PN7	7	PN0～PN5 PN7	7

3.2.2 Pin Count Setting

The setting in the sample code (PIN_SIZE=144) is for 144-pin products. The other pin counts supported by this application note are 144, 100, 80,64, and 48. If the pin count of the target device is other than 144, change the value of PIN_SIZE in r_init_port_initialize.h to match the target device.

3.3 Clock Settings

3.3.1 Clock Setting Procedure

Table 3.3 lists the steps in the clock setting procedure, the processing performed in each step, and the default settings of the sample code. Using the default settings, the sample code sets the PLL clock as the HOCO clock and turns off the main clock and sub-clock.

Table 3.3 Clock Setting Procedure

Step	Processing	Details of Processing		Sample Code Default Settings
1	Sub-clock setting*2	Not used	Initializes the sub-clock control circuit.	The sub-clock is not used.
		Used	Initializes the sub-clock control circuit, sets the drive capacity, and sets in SOSCWTCR the waiting time until output of the sub-clock to the internal clock starts; then starts oscillation by the sub-clock. After this, waits for the clock oscillation stabilization waiting time*1.	
2	Main clock setting*2	Not used	This setting is unnecessary.	The main clock is not used.
		Used	Sets the main clock drive capacity and sets in MOSCWTCR the waiting time until output of the main clock to the internal clocks starts, then starts oscillation by the main clock. After this, waits for the clock oscillation stabilization waiting time*1.	
3	HOCO clock setting*2	Not used	Turns off the HOCO clock power supply.	The HOCO clock is used.
		Used	Sets the HOCO clock frequency, then starts oscillation by the HOCO clock. After this, waits for the clock oscillation stabilization waiting time*1.	
4	PLL clock setting*2	Not used	Turns off the PLL clock power supply.	The PLL clock is used.
		Used	Sets the PLL clock input division ratio and frequency multiplication factor, then starts oscillation by the PLL clock. After this, waits for the clock oscillation stabilization waiting time*1.	
5	Clock division ratio settings	Changes the clock division ratios.		• ICLK and PCLKA: ×1/2 • PCLKB PCLKD, BCLK, and FCLK: ×1/4 • BCLK: Output stopped
6	System clock switching	Switches according to the system used.		Switches to PLL clock.

Note 1. Confirms that the appropriate bit in the oscillation stabilization flag register (OSCOVFSR) is set to 1.

Note 2. Change the values of the constants in r_init_clock.h as necessary to match the selection of the clocks you wish to use or not use.

3.4 Section Configuration

Table 3.4 lists the.Information of the Section Changed in the Sample Code (r01an6015_rx660_clock).

To add, change, or delete sections, refer to the latest version of the RX Family CC-RX Compiler User's Manual.

Table 3.4 Information of the Section Changed in the Sample Code (r01an6015_rx660_clock)

Section Name	Change	Address	Description
End_of_RAM	Add	0001 FFFCh	End address of the on-chip RAM

3.5 File Composition

Table 3.5 lists the files used in the sample code. Files generated by the integrated development environment are not included in this table.

Table 3.5 Files Used in the Sample Code

File Name	Outline	Remarks
main.c	Main processing routine	
r_init_stop_module.c	Disable peripheral functions still running after a reset	
r_init_stop_module.h	Header file of r_init_stop_module.c	
r_init_port_initialize.c	Initial nonexistent port settings	
r_init_port_initialize.h	Header file of r_init_port_initialize.c	
r_init_clock.c	Initial clock settings	
r_init_clock.h	Header file of r_init_clock.c	

3.6 Option-Setting Memory

Table 3.6 lists the option-setting memory configured in the sample code. When necessary, set a value suited to the user system.

Table 3.6 Option-Setting Memory Configured in the Sample Code

Symbol	Address	Setting Value	Contents
OFS0	0012 0068h to 0012 006Bh	FFFF FFFFh	IWDT stopped after a reset WDT stopped after a reset
OFS1	0012 006Ch to 0012 006Fh	FFFF FFFFh	Voltage monitor 0 reset disabled after a reset HOCO oscillation disabled after a reset
MDE	0012 0064h to 0012 0067h	FFFF FFFFh	Little endian

3.7 Constants

Table 3.7 and Table 3.8 list the (user changeable) constants used by the sample code, Table 3.9 lists the (non user changeable) constants used by the sample code, and Table 3.10 to Table 3.12 list the constants specific to each package.

Table 3.7 Constants (User Changeable) Used by Sample Code (1/2)

Constant Name	Setting Value	Contents
SEL_MAIN*1	B_NOT_USE	Main clock enable/disable selection B_USE: Used (main clock enabled) B_NOT_USE: Not used (main clock disabled)
MAIN_CLOCK_HZ*1	24,000,000 L	Main clock oscillator frequency (Hz)
REG_MOFCR*1	00h	Main clock oscillator drive capacity setting (setting value of MOFCR register)
REG_MOSCWTCR*1	53h	Setting value of main clock wait control register
SEL_SUB*1*2*4	B_NOT_USE	Sub-clock usage selection (used as system clock) B_USE: Used B_NOT_USE: Not used
SEL_RTC*1*4	B_NOT_USE	Sub-clock usage selection (used as RTC count source) B_USE: Used B_NOT_USE: Not used
SUB_CLOCK_HZ*1	32,768 L	Sub-clock oscillator frequency (Hz)
REG_SOSCWTCR*1	21h	Setting value of sub-clock wait control register
SEL_PLL*1	B_USE_PLL_HOCO	PLL clock enable/disable selection B_USE_PLL_MAIN: Used (main clock) B_USE_PLL_HOCO: Used (HOCO) B_NOT_USE: Not used (PLL clock disabled)
REG_PLLCR*1	1710h	PLL clock input division ratio, frequency multiplication factor settings and clock source selection settings (setting value of PLLCR register)
REG_VOLSR *1*3	80h	Settings for VCC voltage level when using RIIC (setting value of the VOLSR register)

Note 1. Change the settings values in r_init_clock.h to match the target system.
Note 2. The sub-clock oscillates when either SEL_SUB or SEL_RTC, or both of them, are set to B_USE (use).
Note 3. When changing setting values in this register, follow the User's Manual: Hardware.
Note 4. The sub-clock and RTC cannot be used in products with no sub-clock oscillator. In this case, set SEL_SUB and SEL_RTC to B_NOT_USE (not use).

Table 3.8 Constants (User Changeable) Used by Sample Code (2/2)

Constant Name	Setting Value	Contents
SEL_HOCO*1	B_USE	HOCO clock enable/disable selection B_USE: Used (HOCO clock enabled) B_NOT_USE: Not used (HOCO clock disabled)
REG_HOCOCR2*1	FREQ_20MHZ	HOCO clock frequency selection FREQ_16 MHZ: 16 MHz FREQ_18 MHZ: 18 MHz FREQ_20 MHZ: 20 MHz
SEL_HOCO_FLL*4	B_NOT_USE	FLL enable/disable selection B_USE: Used (FLL enabled) B_NOT_USE: Not used (FLL disabled)
SEL_SYSCLK*1	CLK_PLL	Clock source selection for the system clock CLK_PLL: PLL clock CLK_ HOCO: HOCO clock CLK_ MAIN: main clock CLK_SUB: sub-clock
REG_SCKCR	2182 1212h	Internal clock division ratio(setting value of SCKCR register)
REG_SCKCR2	0x2011	Peripheral clock (CANFD clock) division ratio (SCKCR2 register setting value)
MSTP_STATE_DMACDTC*2	MODULE_STOP_ DISABLE	DMAC and DTC module stop state selection MODULE_STOP_DISABLE: Disable module stop MODULE_STOP_ENABLE: Transition to module stop
MSTP_STATE_RAM*2	MODULE_STOP_ DISABLE	RAM module stop state selection MODULE_STOP_DISABLE: Disable module stop MODULE_STOP_ENABLE: Transition to module stop
PIN_SIZE*3	144	Pin count of target device

Note 1. Change the settings values in r_init_clock.h to match the target system.
Note 2. Change the settings values in r_init_stop_module.h to match the target system.
Note 3. Change the settings values in r_init_port_initialize.h to match the target system.
Note 4. The sub clock must be enabled.

Table 3.9 Constants (Non User Changeable) Used by Sample Code

Constant Name	Setting Value	Contents
B_NOT_USE	0	Not used
B_USE	1	Used
B_USE_PLL_MAIN	2	The PLL clock is used. (Clock source: Main clock)
B_USE_PLL_HOCO	3	The PLL clock is used. (Clock source: HOCO clock)
FREQ_16MHZ	00h	HOCO clock frequency: 16 MHz
FREQ_18MHZ	01h	HOCO clock frequency: 18 MHz
FREQ_20MHZ	02h	HOCO clock frequency: 20 MHz
CLK_PLL	0400h	Clock source: PLL clock
CLK_HOCO	0100h	Clock source: HOCO clock
CLK_SUB	0300h	Clock source: Sub-clock
CLK_MAIN	0200h	Clock source: Main clock
SUB_CLOCK_CYCLE	(1,000,000,000L / SUB_CLOCK_HZ)	Sub-clock cycle (ns)
FOR_CMT0_TIME	121212L	Count cycle (ns) of timer for RTC software wait cycles (CMT0) = 1/LOCO (264 kHz) ×32 (LOCO = 264 kHz (max.), PCLKB ×1/32)
MODULE_STOP_ENABLE	1	Transition to module stop state
MODULE_STOP_DISABLE	0	Cancel module stop state

Note 1. The setting value differs depending on the selected system clock clock source.

Table 3.10 Constants for 144Pin Products (PIN_SIZE=144)

Constant Name	Setting Value	Contents
DEF_P0PDR	0x00	Port P0 direction register setting value
DEF_P1PDR	0x03	Port P1 direction register setting value
DEF_P2PDR	0x00	Port P2 direction register setting value
DEF_P3PDR	0x00	Port P3 direction register setting value
DEF_P4PDR	0x00	Port P4 direction register setting value
DEF_P5PDR	0x80	Port P5 direction register setting value
DEF_P6PDR	0x00	Port P6 direction register setting value
DEF_P7PDR	0x00	Port P7 direction register setting value
DEF_P8PDR	0x30	Port P8 direction register setting value
DEF_P9PDR	0xF0	Port P9 direction register setting value
DEF_PAPDR	0x00	Port PA direction register setting value
DEF_PBPDR	0x00	Port PB direction register setting value
DEF_PCPDR	0x00	Port PC direction register setting value
DEF_PDPDR	0x00	Port PD direction register setting value
DEF_PEPDR	0x00	Port PE direction register setting value
DEF_PFPDR	0x1F	Port PF direction register setting value
DEF_PHPDR	0x30*1	Port PH direction register setting value
DEF_PJPDR	0x05	Port PJ direction register setting value
DEF_PKPDR	0xC3	Port PK direction register setting value
DEF_PLPDR	0xFC	Port PL direction register setting value
DEF_PNPDR	0x3F*2	Port PN direction register setting value

Note 1.Products with a sub-clock oscillator do not have PH6 and PH7. Set 1 for b6 and b7 please.
Note 2.Products with JTAG do not have PN7. Set 1 for b7 please.

Table 3.11 Constants for 100-Pin Products (PIN_SIZE=100)

Constant Name	Setting Value	Contents
DEF_P0PDR	0x07*1	Port P0 direction register setting value
DEF_P1PDR	0x03	Port P1 direction register setting value
DEF_P2PDR	0x00	Port P2 direction register setting value
DEF_P3PDR	0x00	Port P3 direction register setting value
DEF_P4PDR	0x00	Port P4 direction register setting value
DEF_P5PDR	0xC0	Port P5 direction register setting value
DEF_P6PDR	0xFF	Port P6 direction register setting value
DEF_P7PDR	0xFF	Port P7 direction register setting value
DEF_P8PDR	0xFF	Port P8 direction register setting value
DEF_P9PDR	0xFF	Port P9 direction register setting value
DEF_PAPDR	0x00	Port PA direction register setting value
DEF_PBPDR	0x00	Port PB direction register setting value
DEF_PCPDR	0x00	Port PC direction register setting value
DEF_PDPDR	0x00	Port PD direction register setting value
DEF_PEPDR	0x00	Port PE direction register setting value
DEF_PFPDR	0xFF	Port PF direction register setting value
DEF_PHPDR	0x30*2	Port PH direction register setting value
DEF_PJPDR	0x35	Port PJ direction register setting value
DEF_PKPDR	0xFF	Port PK direction register setting value
DEF_PLPDR	0xFF	Port PL direction register setting value
DEF_PNPDR	0xBF	Port PN direction register setting value

Note 1. Products with JTAG do not have P03. Set 1 for b7 please.
Note 2. Products with a sub-clock oscillator do not have PH6 and PH7. Set 1 for b6 and b7 please.

Table 3.12 Constants for 80-Pin Products (PIN_SIZE=80)

Constant Name	Setting Value	Contents
DEF_P0PDR	0x07	Port P0 direction register setting value
DEF_P1PDR	0x03	Port P1 direction register setting value
DEF_P2PDR	0x3C	Port P2 direction register setting value
DEF_P3PDR	0x08	Port P3 direction register setting value
DEF_P4PDR	0x00	Port P4 direction register setting value
DEF_P5PDR	0xCF	Port P5 direction register setting value
DEF_P6PDR	0xFF	Port P6 direction register setting value
DEF_P7PDR	0xFF	Port P7 direction register setting value
DEF_P8PDR	0xFF	Port P8 direction register setting value
DEF_P9PDR	0xFF	Port P9 direction register setting value
DEF_PAPDR	0x80	Port PA direction register setting value
DEF_PBPDR	0x00	Port PB direction register setting value
DEF_PCPDR	0x03	Port PC direction register setting value
DEF_PDPDR	0xF8	Port PD direction register setting value
DEF_PEPDR	0xC0	Port PE direction register setting value
DEF_PFPDR	0xFF	Port PF direction register setting value
DEF_PHPDR	0x30*1	Port PH direction register setting value
DEF_PJPDR	0x3D	Port PJ direction register setting value
DEF_PKPDR	0xFF	Port PK direction register setting value
DEF_PLPDR	0xFF	Port PL direction register setting value
DEF_PNPDR	0xBF	Port PN direction register setting value

Note 1.Products with a sub-clock oscillator do not have PH6 and PH7. Set 1 for b6 and b7 please.

Table 3.133 Constants for 64-Pin Products (PIN_SIZE=64)

Constant Name	Setting Value	Contents
DEF_P0PDR	0x77	Port P0 direction register setting value
DEF_P1PDR	0x0F	Port P1 direction register setting value
DEF_P2PDR	0x3F	Port P2 direction register setting value
DEF_P3PDR	0x18	Port P3 direction register setting value
DEF_P4PDR	0x00	Port P4 direction register setting value
DEF_P5PDR	0xCF	Port P5 direction register setting value
DEF_P6PDR	0xFF	Port P6 direction register setting value
DEF_P7PDR	0xFF	Port P7 direction register setting value
DEF_P8PDR	0xFF	Port P8 direction register setting value
DEF_P9PDR	0xFF	Port P9 direction register setting value
DEF_PAPDR	0xA4	Port PA direction register setting value
DEF_PBPDR	0x14	Port PB direction register setting value
DEF_PCPDR	0x03	Port PC direction register setting value
DEF_PDPDR	0xFF	Port PD direction register setting value
DEF_PEPDR	0xC0	Port PE direction register setting value
DEF_PFPDR	0xFF	Port PF direction register setting value
DEF_PHPDR	0x30*[1]	Port PH direction register setting value
DEF_PJPDR	0x3F	Port PJ direction register setting value
DEF_PKPDR	0xFF	Port PK direction register setting value
DEF_PLPDR	0xFF	Port PL direction register setting value
DEF_PNPDR	0xBF	Port PN direction register setting value

Note 1.Products with a sub-clock oscillator do not have PH6 and PH7. Set 1 for b6 and b7 please.

Table 3.144 Constants for 48-Pin Products (PIN_SIZE=48)

Constant Name	Setting Value	Contents
DEF_P0PDR	0xFF	Port P0 direction register setting value
DEF_P1PDR	0x0F	Port P1 direction register setting value
DEF_P2PDR	0x3F	Port P2 direction register setting value
DEF_P3PDR	0x1C	Port P3 direction register setting value
DEF_P4PDR	0x18	Port P4 direction register setting value
DEF_P5PDR	0xFF	Port P5 direction register setting value
DEF_P6PDR	0xFF	Port P6 direction register setting value
DEF_P7PDR	0xFF	Port P7 direction register setting value
DEF_P8PDR	0xFF	Port P8 direction register setting value
DEF_P9PDR	0xFF	Port P9 direction register setting value
DEF_PAPDR	0xA5	Port PA direction register setting value
DEF_PBPDR	0xD4	Port PB direction register setting value
DEF_PCPDR	0x0F	Port PC direction register setting value
DEF_PDPDR	0xFF	Port PD direction register setting value
DEF_PEPDR	0xE1	Port PE direction register setting value
DEF_PFPDR	0xFF	Port PF direction register setting value
DEF_PHPDR	0xF0*[1]	Port PH direction register setting value
DEF_PJPDR	0x3F	Port PJ direction register setting value
DEF_PKPDR	0xFF	Port PK direction register setting value
DEF_PLPDR	0xFF	Port PL direction register setting value
DEF_PNPDR	0xBF	Port PN direction register setting value

Note 1.Products with a sub-clock oscillator do not have PH6 and PH7. Set 1 for b6 and b7 please.

3.8 Functions

Table 3.15 lists the functions.

Table 3.15 Functions

Function Name	Outline
main	Main processing routine
R_INIT_StopModule	Disable peripheral functions still running after a reset
R_INIT_Port_Initialize	Initial nonexistent port settings
R_INIT_Clock	Initial clock settings
CGC_oscillation_main	Main clock oscillation enable
CGC_oscillation_HOCO	HOCO clock oscillation enable
CGC_oscillation_PLL	PLL clock oscillation enable
CGC_oscillation_sub	Sub-clock oscillation enable
CGC_disable_subclk	Sub-clock disable
oscillation_subclk	Sub-clock oscillation enable
resetting_wtcr_subclk	Sub-clock wait control register resetting
init_rtc	Initialization when using RTC
cmt0_wait	Software wait cycles using CMT0

3.9 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing routine
Header	None
Declaration	void main(void)
Description	Calls the settings function for disabling peripheral functions still running after a reset, the initial nonexistent port settings function, and the initial clock settings function.
Arguments	None
Return Value	None

R_INIT_StopModule	
Outline	Disable peripheral functions still running after a reset
Header	r_init_stop_module.h
Declaration	void R_INIT_StopModule(void)
Description	Makes settings to transition to the module stop state.
Arguments	None
Return Value	None
Remarks	In the sample code, no transition to the module stop state occurs.

R_INIT_Port_Initialize	
Outline	Initial nonexistent port settings
Header	r_init_port_initialize.h
Declaration	void R_INIT_Port_Initialize(void)
Description	Makes initial settings to the port direction registers corresponding to the pins of nonexistent port.
Arguments	None
Return Value	None
Remarks	The setting in the sample code (PIN_SIZE=144) is for 144-pin products. When writing in byte units to PDR or PODR registers containing nonexistent ports after this function has been called, set the direction control bits corresponding to the nonexistent ports to 1 and the port output data storage bits corresponding to the nonexistent ports to 0.

R_INIT_Clock	
Outline	Initial clock settings
Header	r_init_clock.h
Declaration	void R_INIT_Clock(void)
Description	Makes initial clock settings.
Arguments	None
Return Value	None
Remarks	In the sample code processing is selected that sets the PLL clock as the system clock and does not use a sub-clock.

CGC_oscillation_main	
Outline	Main clock oscillation enable
Header	r_init_clock.h
Declaration	void CGC_oscillation_main (void)
Description	Sets the drive capacity of the main clock and sets the MOSCWTCR register, then starts oscillation of the main clock. After this, waits for the main clock oscillation stabilization waiting time.
Arguments	None
Return Value	None

CGC_oscillation_HOCO	
Outline	HOCO clock oscillation enable
Header	r_init_clock.h
Declaration	void CGC_oscillation_HOCO (void)
Description	Sets the HOCO clock frequency, then starts oscillation of the HOCO clcok. After this, waits for the HOCO clock oscillation stabilization waiting time.
Arguments	None
Return Value	None

CGC_oscillation_PLL	
Outline	PLL clock oscillation enable
Header	r_init_clock.h
Declaration	void CGC_oscillation_PLL (void)
Description	Sets the PLL clock input division ratio and frequency multiplication factor, then starts oscillation of the PLL clock. After this, waits for the PLL clock oscillation stabilization waiting time.
Arguments	None
Return Value	None

CGC_oscillation_sub	
Outline	Sub-clock oscillation enable
Header	r_init_clock.h
Declaration	void CGC_oscillation_sub (void)
Description	Makes settings for using the sub-clock as the system clock or as the RTC count source, or for both.
Arguments	None
Return Value	None

CGC_disable_subclk	
Outline	Sub-clock disable
Header	r_init_clock.h
Declaration	void CGC_disable_subclk (void)
Description	Makes settings for when the sub-clock is not used as the system clock and the RTC count source.
Arguments	None
Return Value	None

oscillation_subclk	
Outline	Sub-clock oscillation enable
Header	None
Declaration	static void oscillation_subclk (void)
Description	Makes settings to start sub-clock oscillation.
Arguments	None
Return Value	None

resetting_wtcr_subclk	
Outline	Sub-clock wait control register resetting
Header	None
Declaration	static void resetting_wtcr_subclk (void)
Description	Resets the wait control register when returning from software standby mode. In this case the wait control register is set to the minimum value.
Arguments	None
Remarks	

init_rtc	
Outline	Initialize RTC
Header	None
Declaration	static void init_rtc(void)
Description	Makes initial settings for using the RTC (clock supply setting and RTC software reset).
Arguments	None
Return Value	None

cmt0_wait		
Outline	Software wait cycles using CMT	
Header	None	
Declaration	static void cmt0_wait(uint32_t cnt)	
Description	Used when waiting before writing to the RTC register.	
Arguments	uint32_t cnt	Wait time cnt = Wait time (ns) ÷ FOR_CMT0_TIME*1
Return Value	None	
Remarks	Note 1. The duration of FOR_CMT0_TIME is calculated based on LOCO = 264 kHz (max.). The actual wait time will differ depending on the LOCO frequency.	

3.10 Flowcharts

3.10.1 Main Processing

Figure 3.1 shows the main processing.

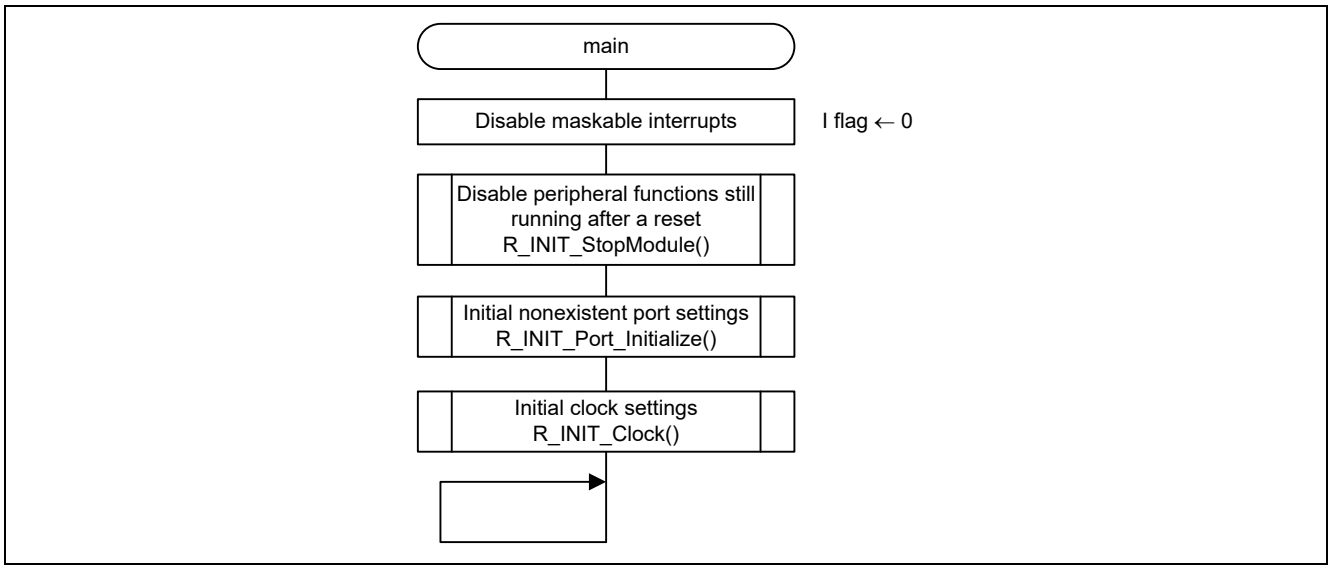
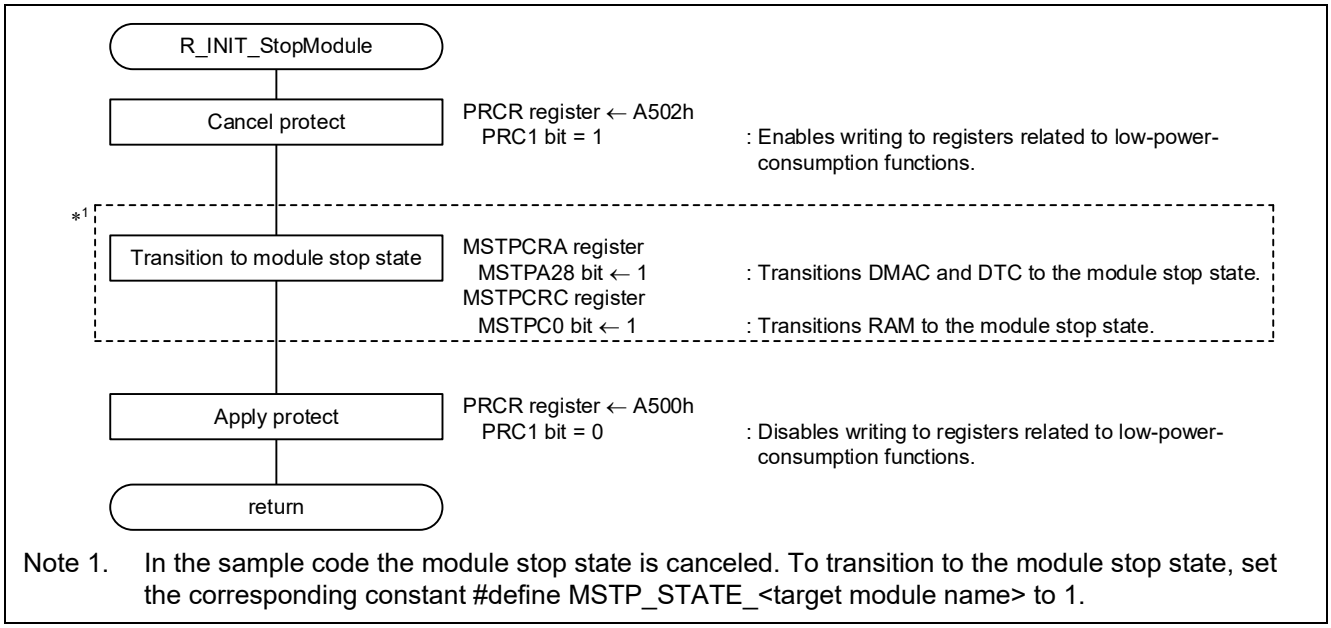


Figure 3.1 Main Processing

3.10.2 Disable Peripheral Functions Still Running After a Reset

Figure 3.2 is a flowchart of the processing for disabling of peripheral functions still running after a reset.

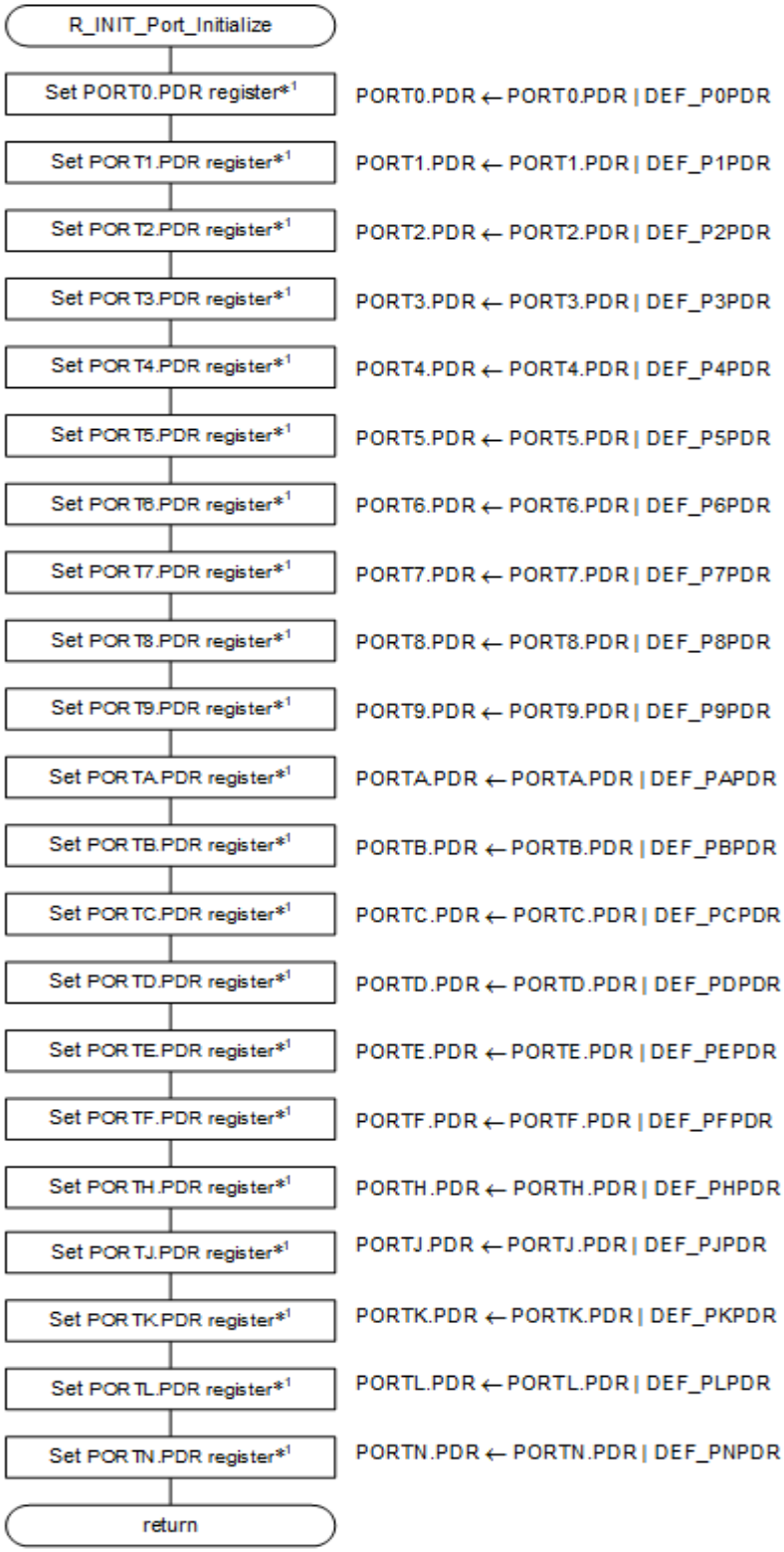


Note 1. In the sample code the module stop state is canceled. To transition to the module stop state, set the corresponding constant #define MSTP_STATE_<target module name> to 1.

Figure 3.2 Disable Peripheral Functions Still Running After a Reset

3.10.3 Initial Nonexistent Port Settings

Figure 3.3 is a flowchart of the processing for making initial nonexistent port settings.

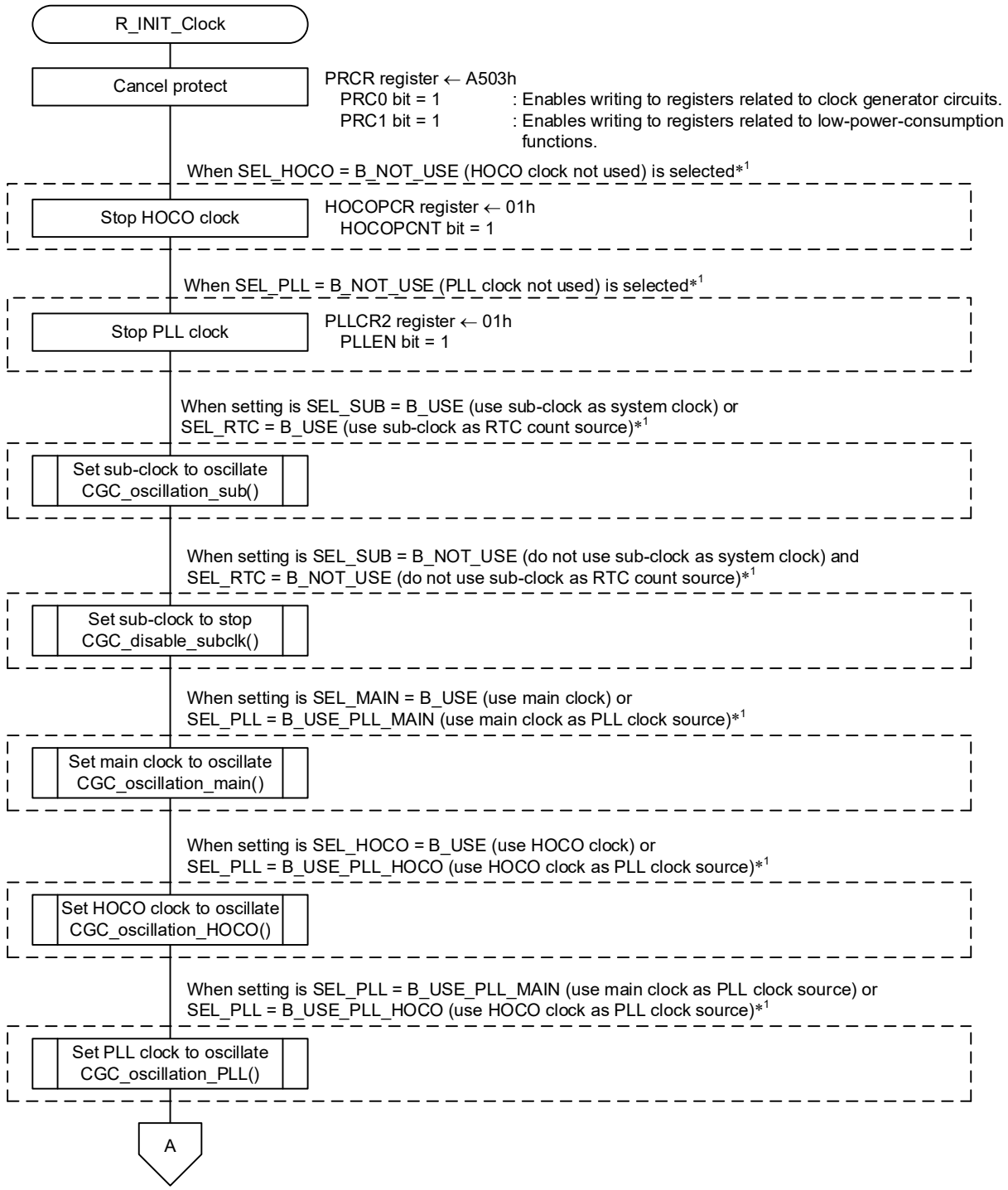


Note 1. No processing of settings is performed for registers in which all bits correspond to existing pins (omitted during compile).

Figure 3.3 Initial Nonexistent Port Settings

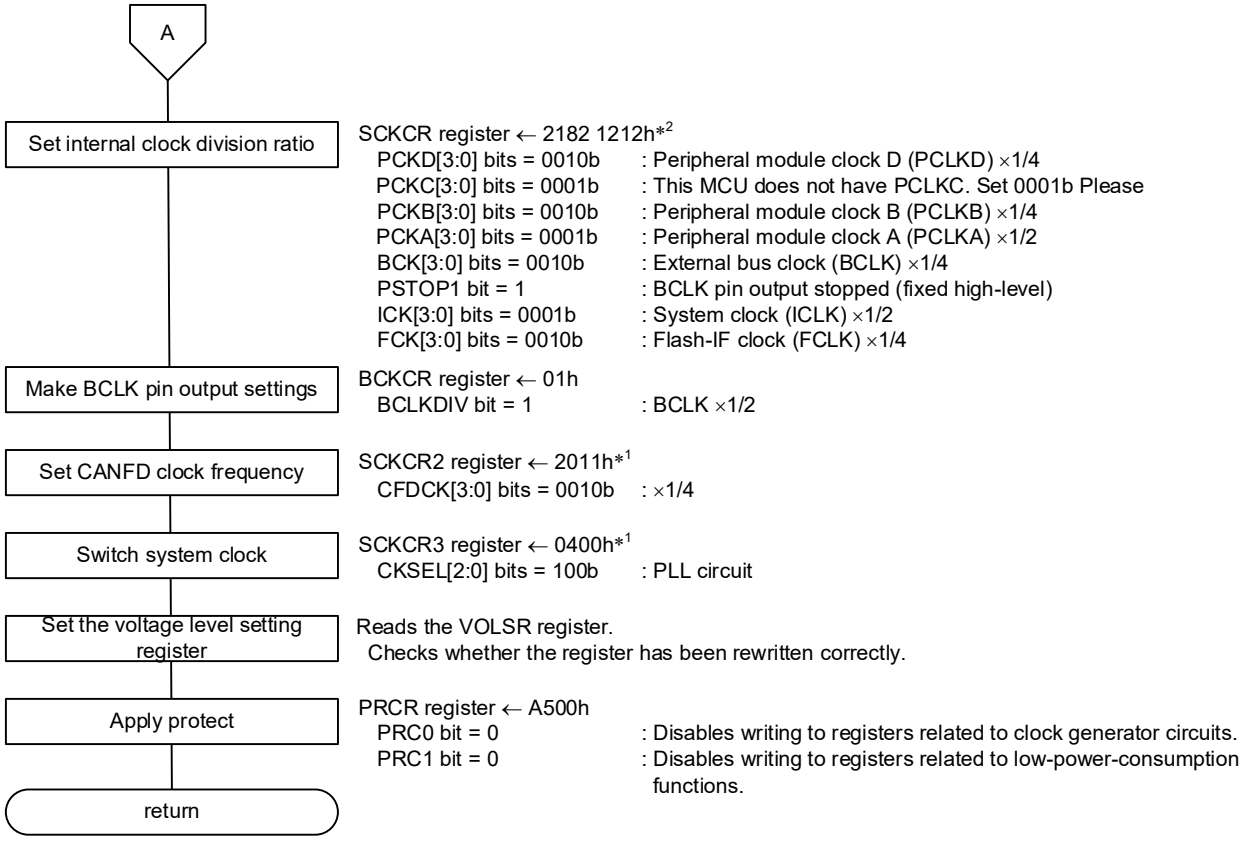
3.10.4 Initial Clock Settings

Figure 3.4 and Figure 3.5 are flowcharts of the processing for making initial clock settings (1/2) and (2/2).



Note 1. Change the values of the relevant constants to match the characteristics of the target system.

Figure 3.4 Initial Clock Settings (1/2)

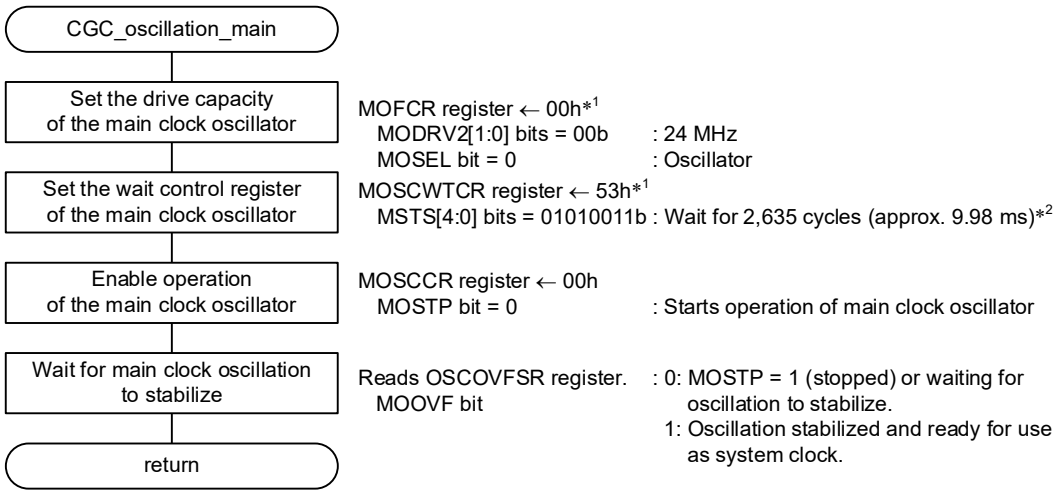


Notes 1. Change the values of the relevant constants to match the characteristics of the target system.
Notes 2. The setting values differ depending on the system clock selected by the constant.

Figure 3.5 Initial Clock Settings (2/2)

3.10.5 Main Clock Oscillation Enable

Figure 3.6 is a flowchart of the processing for starting oscillation of the main clock.

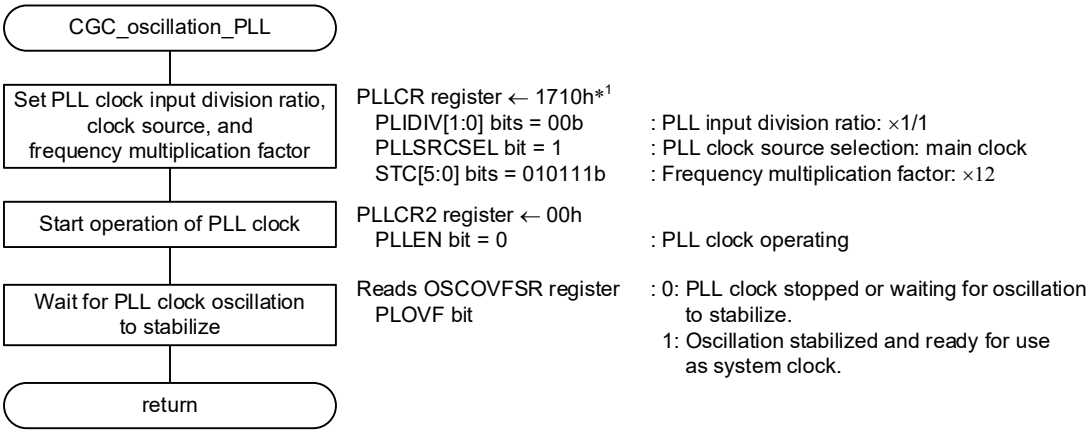


Note 1. Change the values of the relevant constants to match the characteristics of the target system.
Note 2. The sample code accompanying this application note uses the initial value of the register.

Figure 3.6 Main Clock Oscillation Enable

3.10.6 PLL Clock Oscillation Enable

Figure 3.7 is a flowchart of the processing for starting oscillation of the PLL clock.

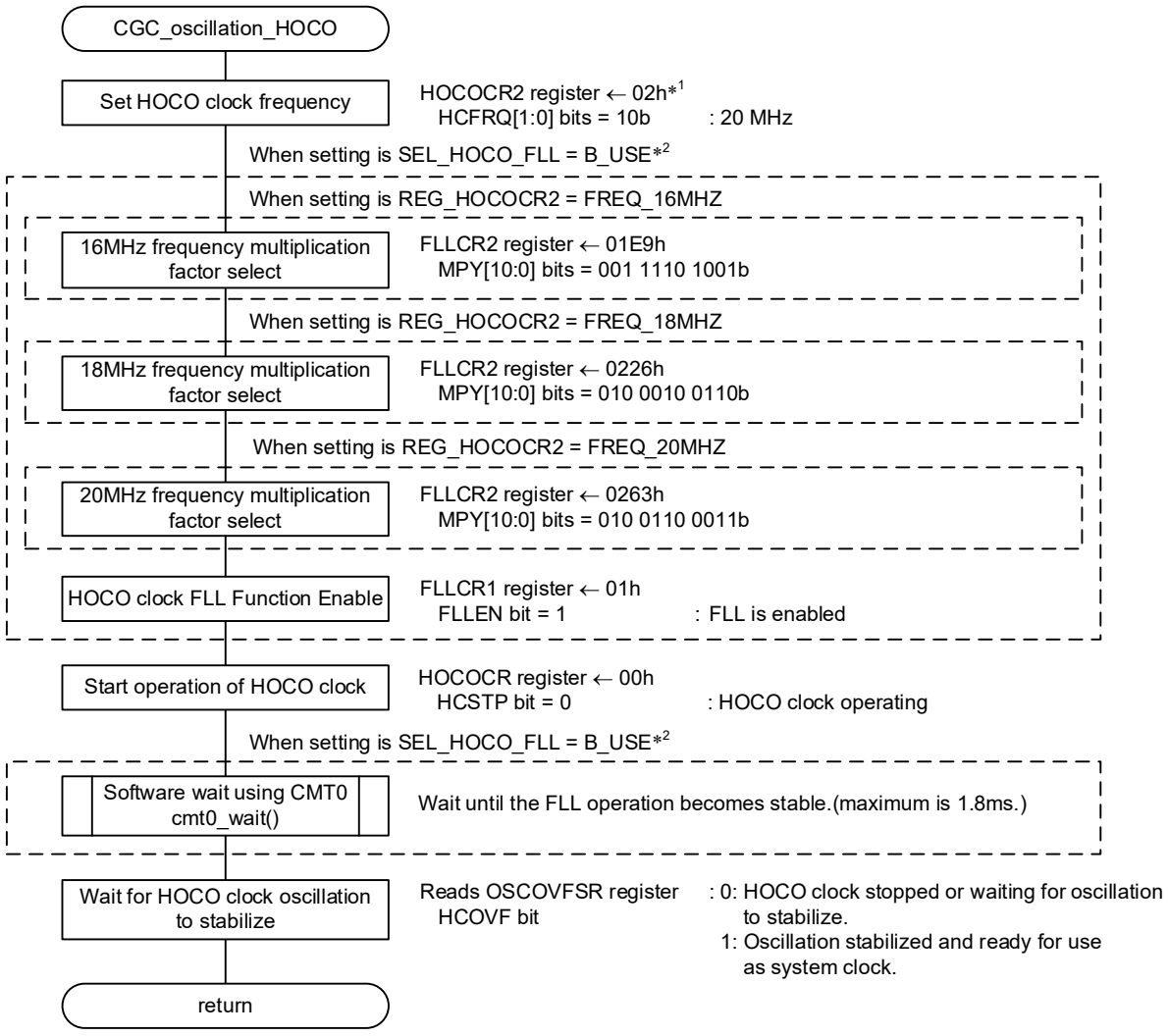


Note 1. Change the values of the relevant constants to match the characteristics of the target system.

Figure 3.7 PLL Clock Oscillation Enable

3.10.7 HOCO Clock Oscillation Enable

Figure 3.8 is a flowchart of the processing for starting oscillation of the HOCO clock.

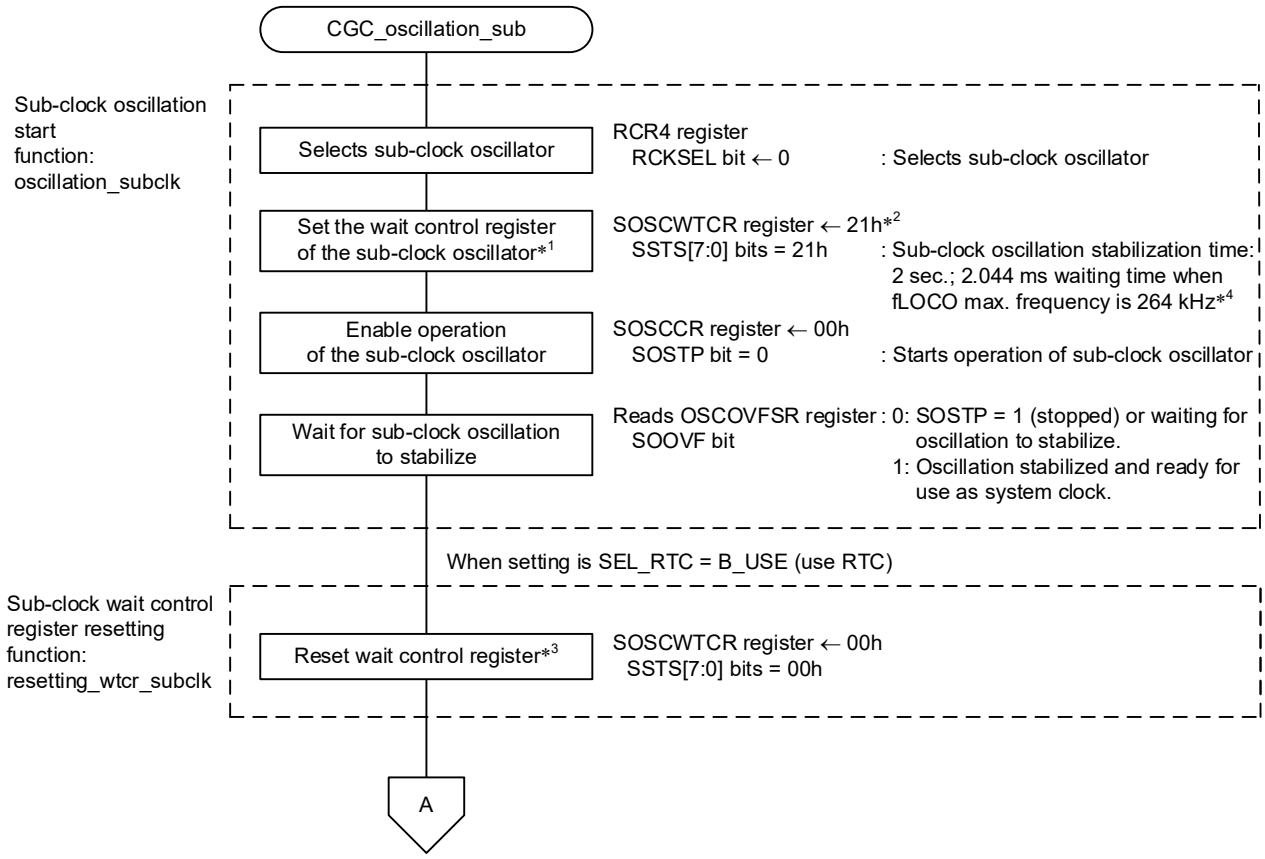


Note 1. Change the values of the relevant constants to match the characteristics of the target system.
Note 2. If you want to use the FLL feature, you must to enable the sub-clock.

Figure 3.6 HOCO Clock Oscillation Enable

3.10.8 Sub-clock Oscillation Enable

Figure 3.9 and Figure 3.10 are flowcharts of the processing for starting oscillation of the sub-clock.



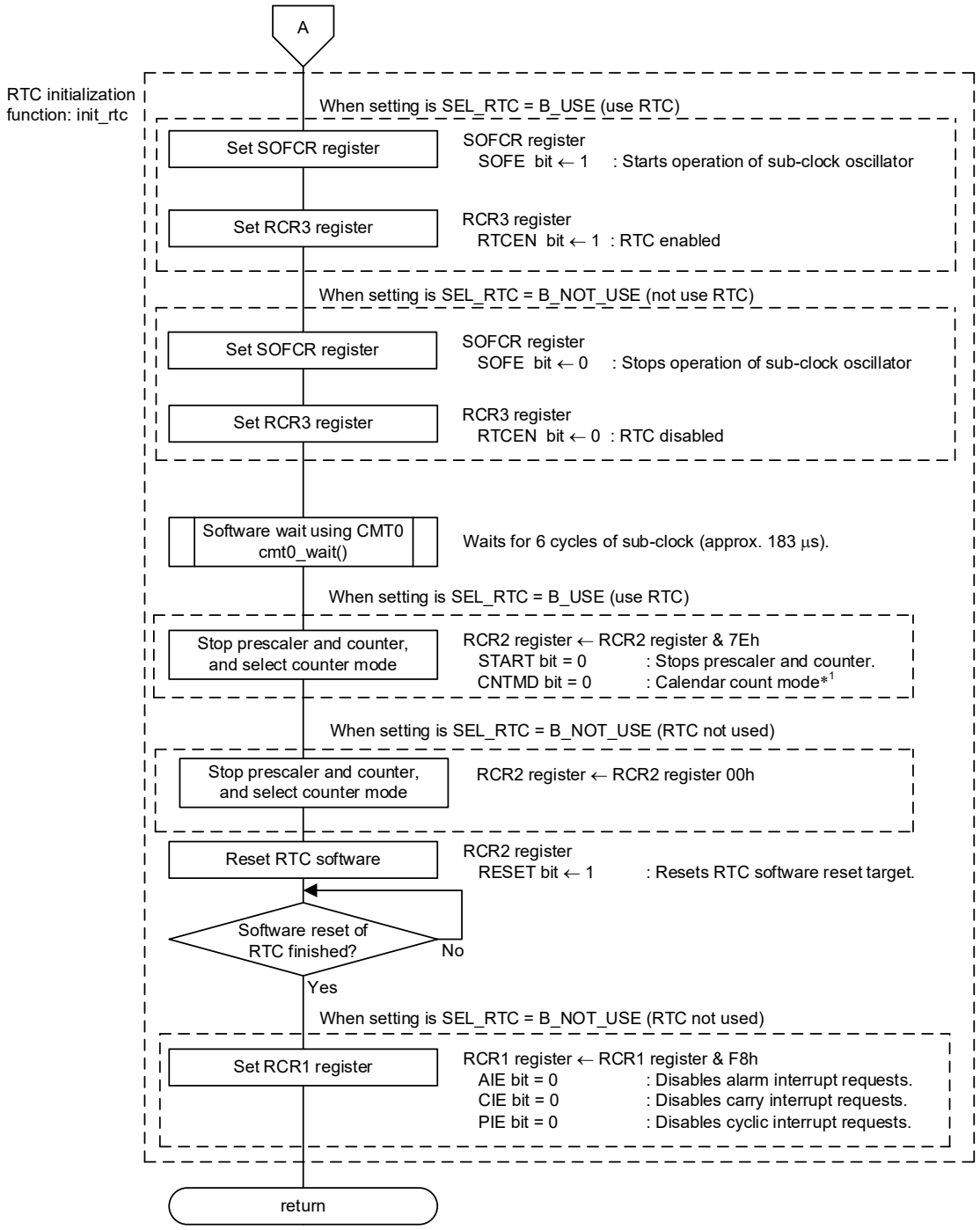
Note 1. Use the formulas in 9.2.19, Sub-Clock Oscillator Wait Control Register (SOSCWTCR), in RX660 Group User's Manual: Hardware to calculate the waiting time. Note that the sample code accompanying this application note uses the initial value of the register.

Note 2. Change the value of the constant to match the characteristics of the target system.

Note 3. When the sub-clock is to be used as the source to drive counting by the realtime clock or the operating clock of the remote control signal receiver (REMC), set the SOFCR.SOFE bit to 1 (forcibly making the sub-clock oscillator run) and the SOSCCR.SOSTP bit to 0 (making the sub-clock oscillator run). When the sub-clock is not to be used as the source to drive counting by the realtime clock or the operating clock of the REMC but is to be used as the system clock, set the SOSCCR.SOSTP bit to 0 (making the sub-clock oscillator run).

Note 4. The sample code accompanying this application note uses the initial value of the register.

Figure 3.9 Sub-clock Oscillation Enable (1/2)



Note 1. The sample code accompanying this application note selects the calendar count mode. Change the values of the constants to match the characteristics of the target system.

Figure 3.10 Sub-clock Oscillation Enable (2/2)

3.10.9 Sub-clock Disable

Figure 3.11 is a flowchart of the processing for stopping the sub-clock.

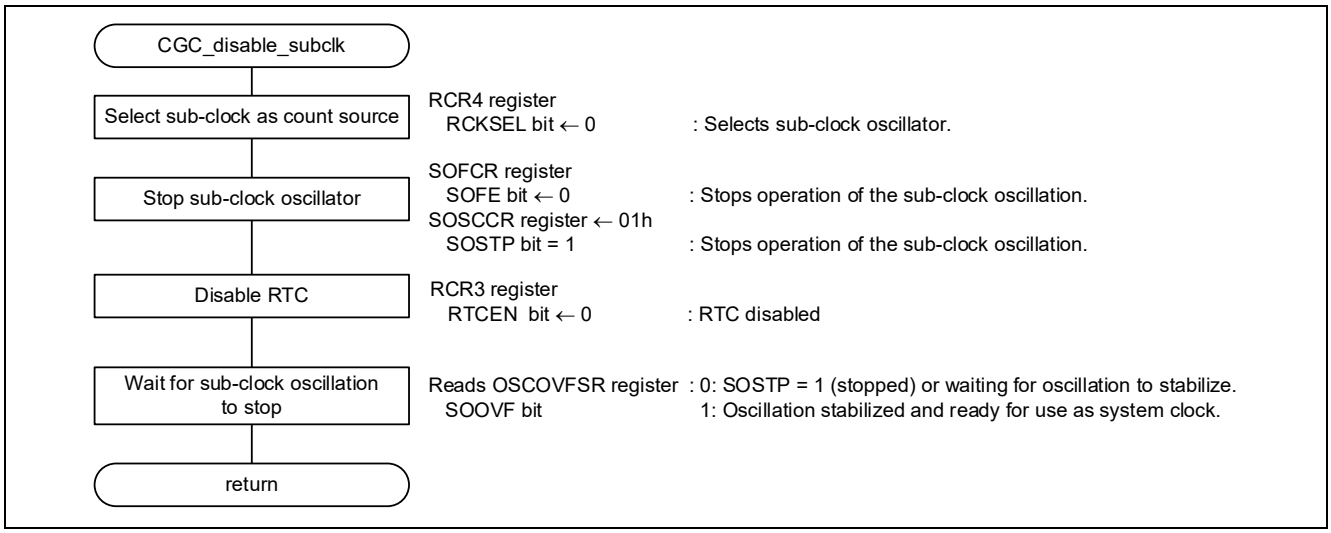
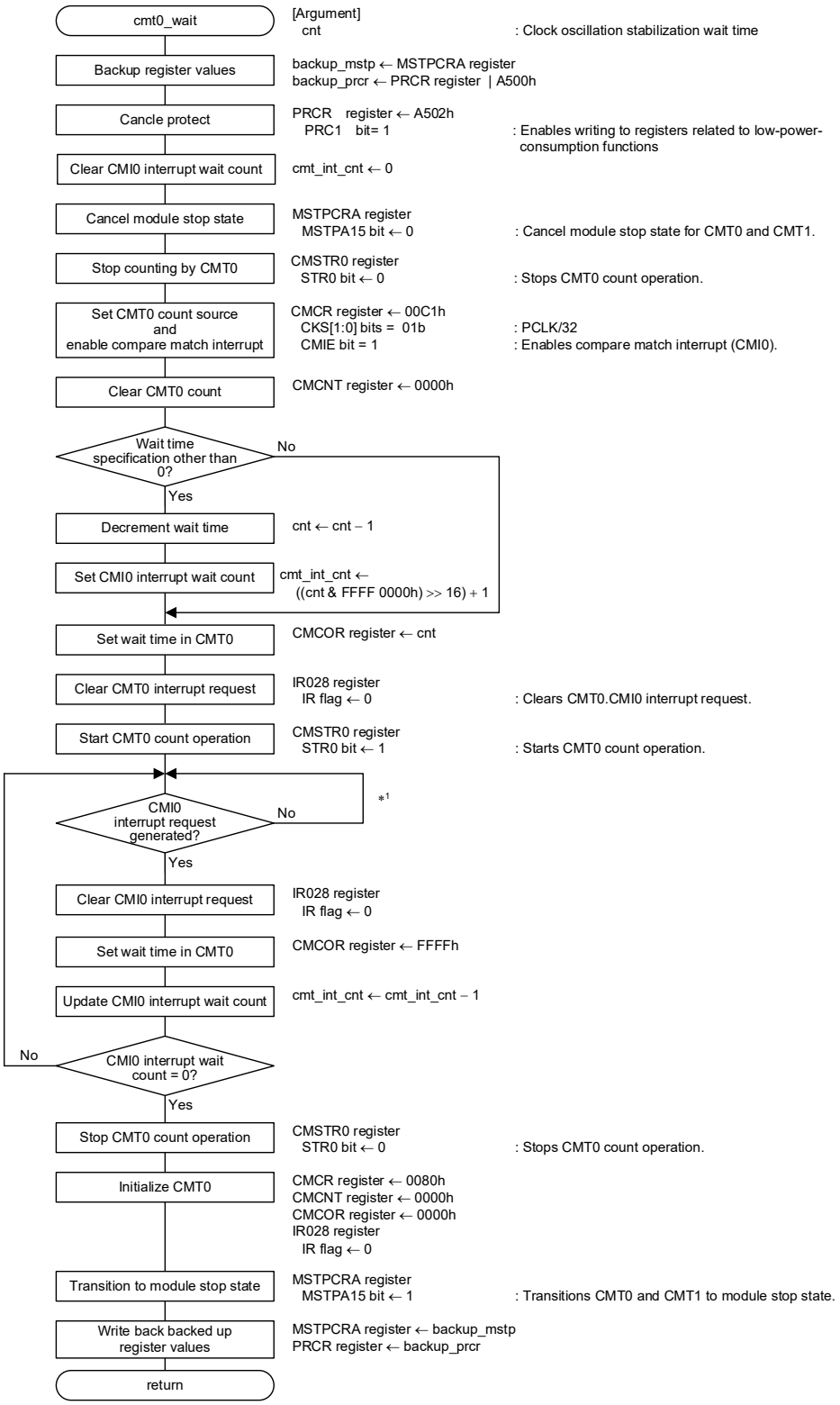


Figure 3.7 Sub-clock Disable

3.10.10 Software Wait Cycles Using CMT0

Figure 3.12 is a flowchart of the processing for implementing a software wait using CMT0.



Note 1. When the watchdog timer (WDT) and independent watchdog timer (IWDT) are counting, use processing loop to refresh the WDT and IWDT.

Figure 3.8 Software Wait Cycles Using CMT0

4. Importing a Project

The sample code is provided as the e² studio project. This section describes importing a project into the e² studio and CS+. After importing a project, confirm that the build settings and the debug settings are correct.

4.1 Importing a Project into the e² studio

Follow the steps below to import your project into the e² studio.
(Windows/dialogs may differ depending on the e² studio version used.)

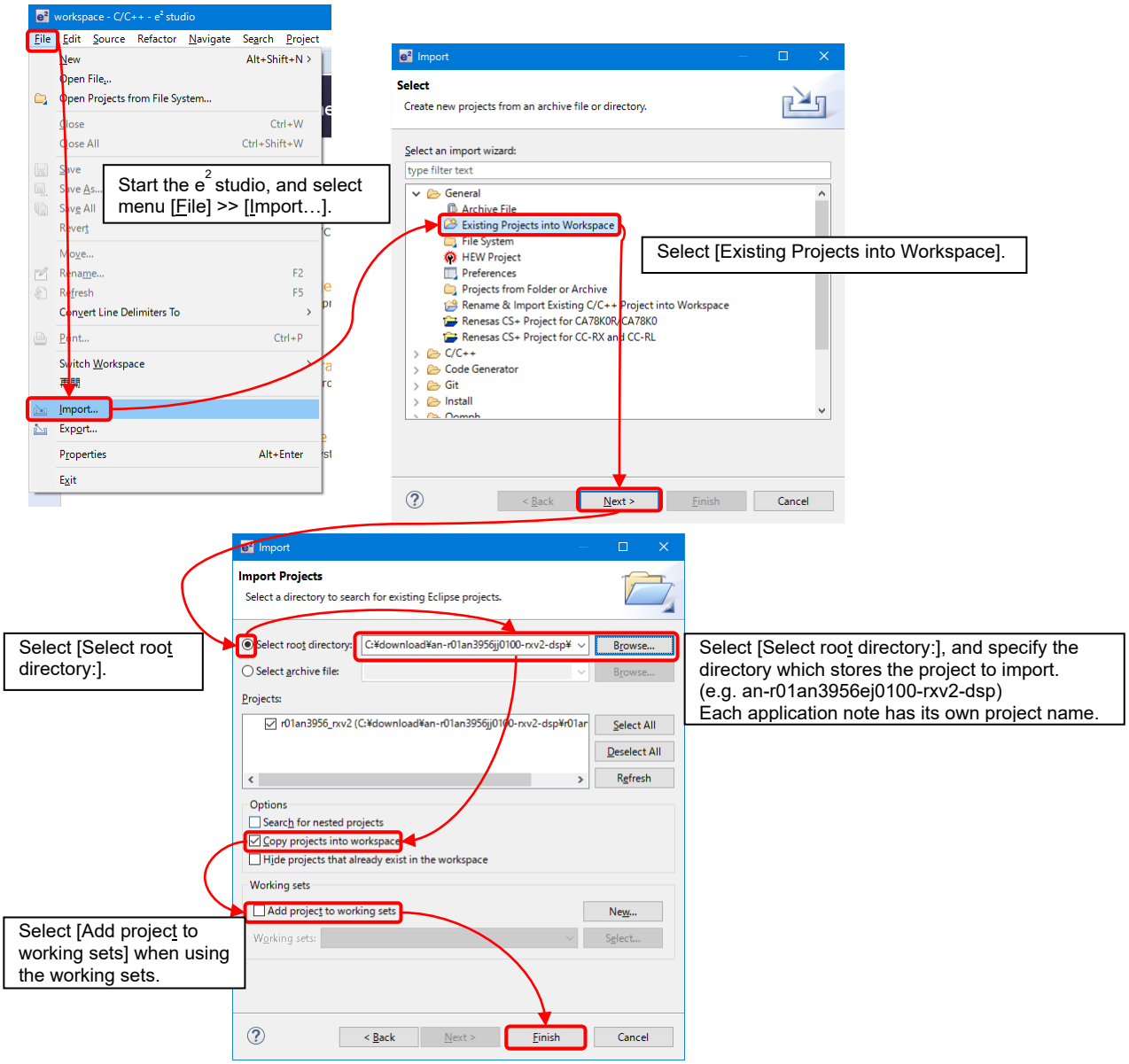


Figure 4.1 Importing a Project into the e² studio

4.2 Importing a Project into CS+

Follow the steps below to import your project into CS+.
(Windows/dialogs may differ depending on the CS+ version used.)

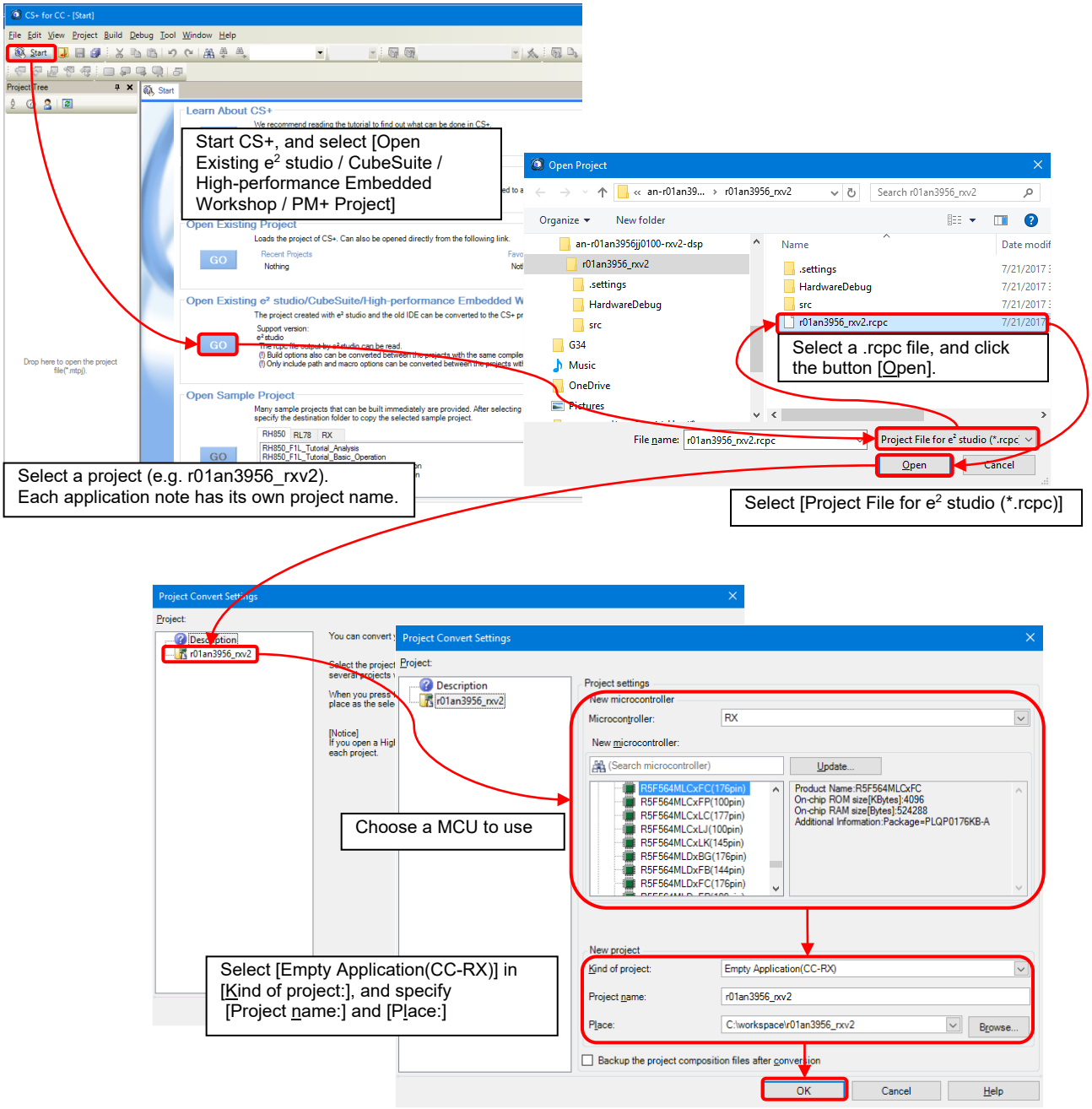


Figure 4.2 Importing a Project into CS+

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware
RX660 Group User's Manual: Hardware (R01UH0937)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

User's Manual: Development Tools
RX Family CC-RX Compiler User's Manual (R20UT3248)
(The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.18.22	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

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