RX65N, H8SX/1668

Watchdog Timer Migration Guide: H8SX/1668 to RX65N

Introduction

This application note describes the differences in the watchdog timer (WDT) module between the RX65N and H8SX/1668 devices.

Target Devices

RX65N

H8SX/1668

Contents

1. Features

Table 1.1 shows the features of the WDT modules of the RX65N and H8SX/1668 devices. Differences between the devices are shaded.

Table 1.1 Features of the WDT Module

Item	Specifications	
	RX65N	**H8SX/1668**
Number of channels	1	1
Clock source	PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, and PCLK/8192	PCLK/2, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, and PCLK/131072
Behavior of counting	Down-counting using a 14-bit down-counter	Up-counting using an 8-bit up-counter
Counter is cleared by	A refresh operation. (Writing “00h” and then “FFh” to the WDTRR register)	A write to the TCNT.
Operating mode	• Auto-start mode • Register start mode	• Watchdog mode • Interval timer
Interrupt source	An interrupt (WUNI) occurs in the following cases: when the WDTRCR.RSTIRQS bit is set to 0 in register start mode; when the WDTRSTIRQS bit of the optional function select register 0 (OFS0) is set to 0 in auto-start mode; and when an underflow or refresh error occurs on the counter. The interrupt WUNI can be used as a non-maskable interrupt or as an ordinary interrupt.	Watchdog overflow interrupt (WOVI) in interval timer mode
Hardware output	Feasible by using a refresh error interrupt by the window function.	The WDTOVF# signal is output when the TCNT counter overflows. At the same time, the LSI is internally reset (whether this reset is to be performed can be selected).

2. General Notes

- Some restrictions are placed on the write operations for the WDT control register (WDTCR) of the RX65N and for the WDT reset control register (WDTRCR) of the RX65N. For details, refer to the hardware manual for the RX65N.
- Peripheral module clock B (PCLKB) is the counting source of the WDT. By accelerating the clock of the RX65N cores, peripheral module clock B can operate at a maximum of 60 MHz. The maximum peripheral clock frequency of the H8SX/1668 is 35 MHz.
- In applications that use the peripheral clock accelerator, the watchdog timer settings must be corrected. As a result, the minimum and maximum allowable delay times may change.

3. References

- Hardware manual for the RX65N:
  R01UH0590EJ0230: RX65N Group, RX651 Group User's Manual: Hardware
- Software manual for the RX65N:
  R01US0071EJ0100: RX Family RXv2 Instruction Set Architecture User's Manual: Software

(The latest versions of the above manuals are available on the Renesas website.)

3.1 Related Chapters in the Hardware Manual

- Clock Generation Circuit
  Provides details on how to set up the peripheral module clocks used for the WDT.
- I/O Registers
  Shows a list of all registers.
- Low Power Consumption
  Provides details on sleep mode and other modes affected by the WDT.
- Interrupt Controller (ICUB)
  Describes how to enable interrupts from the WDT to the interrupt controller.
- Watchdog Timer (WDTA)
  Provides details on the WDT-specific registers and operating modes.
- Independent Watchdog Timer (IWDTa)
  Provides details on the independent watchdog timer (second watchdog timer) of the RX65N.
- Option-Setting Memory (OFSM)
  Provides details on how to set up the option-setting memory used for the WDT.
- Resets
  Provides details on a watchdog timer reset caused by an underflow or refresh error occurring on the WDT.

3.2 Related Registers

The following table lists the registers that are related to the operation of the watchdog timer (WDTA) of the RX65N.

Table 3.1 Registers Related to the Operation of the Watchdog Timer

Name	Description	Chapter in the Hardware Manual
SYSTEM.SCKCR	System clock control register	Clock Generation Circuit
ICU.IR096	Interrupt request register	Interrupt Controller (ICUB)
ICU.IER0C.IEN0	Interrupt request enable register	
ICU.IPR096	Interrupt request priority register	
WDT.WDTRR	WDT refresh register	Watchdog Timer (WDTA)
WDT.WDTCR	WDT control register	
WDT.WDTSR	WDT status register	
WDT.WDTRCR	WDT reset control register	
OFSM.OFS0	Optional function select register 0	Option-Setting Memory (OFSM)

4. Summary of Differences in the Watchdog Timer Function

4.1 WDT Modes

For the watchdog timer of the H8SX/1668 device, watchdog timer mode and interval timer mode are available.

- Watchdog timer mode
  When the TCNT overflows, the WDTOVF# signal is output externally. At this time, if the RSTE bit of the RSTCSR register is 1, an internal reset signal is generated for the entire LSI.
  On the RX65N device, auto-start mode and register start mode are equivalent to the two watchdog timer modes available on the H8SX/1668 device.
  — Auto-start mode
    After a reset is canceled, the timer counter automatically starts.
  — Register start mode
    The timer counter starts when a refresh operation is performed.

- Interval timer mode
  An interval timer interrupt (WOVI) is generated when the TCNT overflows.
  The RX65N device does not provide a function that is equivalent to the interval timer mode available on the H8SX/1668 device.
  On the H8SX/1668 device, the WT/IT# bit of the TCSR register is used to select watchdog timer mode or interval timer mode.
  On the RX65N device, the WDTSTRT bit of the OFS0 register is used to select auto-start mode or register start mode.
  If auto-start mode is selected, the settings of the WDTCR and WDTRCR registers are invalidated and the OFS0 settings take effect.
  If register start mode is selected, the OFS0 settings are invalidated and the settings of the WDTCR and WDTRCR registers take effect.

4.2 WDT Hardware Output

On the H8SX/1668 device, while the WDT is operating as a watchdog timer, the WDTOVF# signal is output when the TCNT overflows. At this time, if the RSTE bit of the RSTCSR register is 1, an internal reset signal is generated for the entire LSI.

On the RX65N device, a reset signal is output for one count cycle due to an underflow of the down-counter or a refresh error in the following cases: when the RSTIRQS bit of the WDTRCR register is set to 1 in register start mode; or when the WDTRSTIRQS bit of the OFS0 register is set to 1 in auto-start mode.

The RX65N device does not provide a function equivalent to WDTOVF# pin output available on the H8SX/1668 device. However, an equivalent function can be achieved by using a refresh interrupt of the window function.

On the RX651 device, the range in which a counter refresh is prohibited can be set. This function is referred to as the “window function”. A refresh error interrupt can be generated when an attempt is made to perform a refresh operation in this prohibition range. Set the range up to 75 percent of the threshold at which a counter underflow occurs as the prohibition range, and generate a refresh error interrupt within the range. By controlling the I/O port in the processing of the interrupt, a signal equivalent to WDTOVF# can be output.

Furthermore, by using the event link controller supported by the independent watchdog timer, a refresh error interrupt and I/O output can be automatically linked without using interrupt processing. This method will achieve an operation that is more similar to the operation based on the WDTOVF# specifications.

4.3 Setting the WDT Overflow/Underflow Cycle

On the H8SX/1668 device, the clock to be input to the TCNT is selected by using the CKS[2:0] bits of the TCSR register, and the cycle at which the TCNT overflows is set by the counter value (“00h”, normally) written to the TCNT.

On the RX65N device in auto-start mode, the division ratio of the clock to be used for the down-counter is selected by using the WDTCKS[3:0] bits of the OFS0 register, and the timeout period before the down-counter underflows is set by using the WDTTOPS[1:0] bits of the OFS0 register.

On the RX65N device in register start mode, the division ratio of the clock to be used for the down-counter is selected by using the CKS[3:0] bits of the WDTCR register, and the timeout period before the down-counter underflows is set by using the TOPS[1:0] bits of the WDTCR register.

On the RX65N device, the start and end positions of the window that indicates the refresh permission period can be set. In auto-start mode, the window start position is set by using the WDTRPSS[1:0] bits of the OFS0 register. In reset start mode, the window start position is set by using the RPSS[1:0] bits of the WDTCR register. In auto-start mode, the window end position is set by using the WDTRPES[1:0] bits of the OFS0 register. In reset start mode, the window end position is set by using the RPWS[1:0] bits of the WDTCR register.

4.4 Conditions Under Which the WDT Starts/Stops Counting

On the H8SX/1668 device, the TCNT starts counting when the TME bit of the TCSR register is set to 1. If the TME bit of the TCSR register is cleared to 0, the TCNT stops the counting operation and is initialized to 00h.

On the RX65N device in auto-start mode, the counting automatically starts according to the OFS0 settings after a reset is canceled. In register start mode, the counting starts when a refresh operation is performed after the registers are set after a reset is canceled. The counting stops when an underflow or refresh error occurs in the case where the device is reset and placed in a power-down state in register start mode.

4.5 Sources That Trigger Issuance of a WDT Reset Signal

On the H8SX/1668 device, if the RSTE bit of the RSTCSR register is 1 when the TCNT overflows in watchdog timer mode, a signal that internally resets the LSI is generated at the same time when the WDTOVF# signal is output.

On the RX65N device, a reset signal is output for one count cycle due to an underflow of the down-counter or a refresh error in the following cases: when the RSTIRQS bit of the WDTCR register is set to 1 in register mode; or when the WDTRSTIRQS bit of the OFS0 register is set to 1 in auto-start mode.

4.6 Interrupt Sources

On the H8SX/1668 device, an interval timer interrupt (WOVI) is generated when an overflow occurs in interval timer mode.

On the RX65N device, an interrupt (WUNI) occurs in the following cases: when the RSTIRQS bit of the WDTRCR register is set to 0 in register start mode; when the WDTRSTIRQS bit of the OFS0 register is set to 0 in auto-start mode; and when an underflow or refresh error occurs on the counter. This interrupt can be used as a non-maskable interrupt or as an ordinary interrupt.

5. Register Details

Table 5.1 lists the registers for the watchdog timers of the RX65N and H8SX/1668 devices. Differences between the devices are shaded.

This chapter provides detailed descriptions of only the registers related to the functions of the H8SX/1668 device. For details on the other registers, refer to the hardware manual for the RX65N.

Table 5.1 Watchdog Timer Registers

RX65N		
Auto-start mode	**Register start mode**	**H8SX/1668**
WDTRR		
OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]	
OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]	
OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]	TCSR.CKS[2:0]
OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]	
WDTSR.REFEF		
WDTSR.UNDFF		RSTCSR.WOVF
WDTSR.CNTVAL[13:0]		TCNT
OFS0.WDTRSTIRQS	WDTRCR.ISTIRQS	RSTCSR.RSTE
OFS0.WDTSTRT		
		TCSR.OVF
		TCSR.WT/IT#
		TCSR.TME

5.1 WDT Control Register (WDTCR) and Optional Function Select Register (OFS0)

5.1.1 WDT Control Register (WDTCR) of the RX65N

The WDTCR register is used to select the timeout period, the clock division ratio, and the start and end position of the window that indicates the refresh permission period. Some restrictions are placed on the write operations for the WDTCR register. For details, refer to the hardware manual for the RX65N.

The timeout period before the down-counter underflows is represented by the number of cycles of the frequency dividing clock set by using the CKS[3:0] bits. 1024, 4096, 8192, or 16348 (cycles) can be selected. The time period (number of PCLK cycles) before an underflow occurs after a refresh is performed is determined by the combination of the CKS[3:0] and TOPS[1:0] bit settings. For details on the relationships among the CKS[3:0] and TOPS[1:0] settings, the timeout period, and the number of PCLK cycles, refer to the hardware manual for the RX65N.

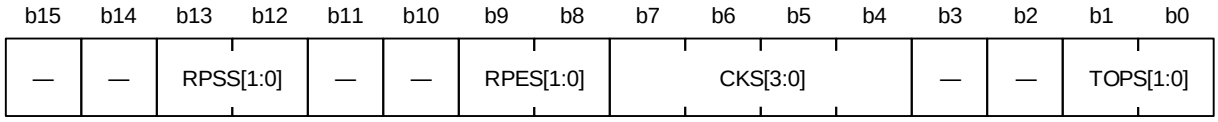


Table 5.2 WDT Control Register (WDTCR) of the RX65N

Bit	Description
[13:12]	RPSS[1:0]: Window start position select bits 00: 25% 01: 50% 10: 75% 11: 100% (Sets no window start position.)
[9:8]	RPES[1:0]: Window end position select bits 00: 75% 01: 50% 10: 25% 11: 0% (Sets no window end position.)
[7:4]	CKS[3:0]: Clock division ratio select bits 0001: 1/4 0100: 1/64 1111: 1/128 0110: 1/512 0111: 1/2048 1000: 1/8192 Settings other than the above are prohibited.
[1:0]	TOPS[1:0]: Timeout period select bits 00: 1024 cycles (03FFh) 01: 4096 cycles (0FFFh) 10: 8192 cycles (1FFFh) 11: 16384 cycles (3FFFh)

5.1.2 Optional Function Select Register 0 (OFS0) of the RX65N

The OFS0 register is used in auto-start mode (WDTSTRT=0) to select the timeout period, the clock division ratio, and the start and end position of the window that indicates the refresh permission period.

The timeout period before the down-counter underflows is represented by the number of cycles of the frequency dividing clock set by using the WDTCKS[3:0] bits. 1024, 4096, 8192, or 16348 (cycles) can be selected. The time period (number of PCLK cycles) before an underflow occurs after a refresh is performed is determined by the combination of the WDTCKS[3:0] and WDTTOPS[1:0] bit settings. For details on the relationships among the WDTCKS[3:0] and WDTTOPS[1:0] settings, the timeout period, and the number of PCLK cycles, refer to the hardware manual for the RX65N.

This section describes WDTTOPS[1:0], WDTCKS[3:0], and WDTSTRT.

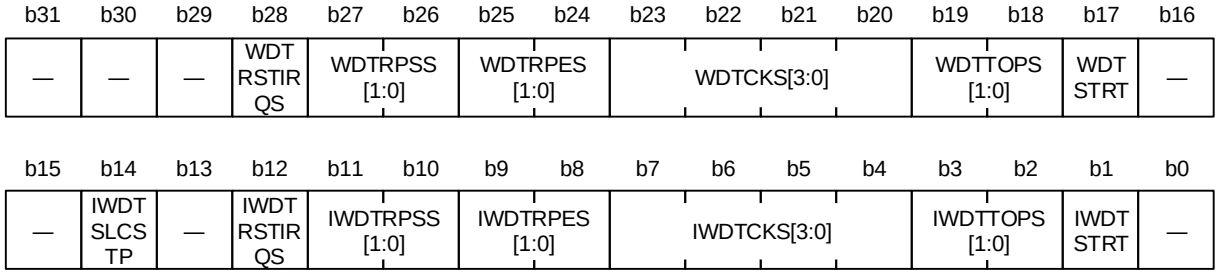


Table 5.3 Optional Function Select Register 0 (OFS0) of the RX65N

Bit	Description
[23:20]	WDTCKS[3:0]: WDT clock division ratio select bits 0001: 1/4 0100: 1/64 1111: 1/128 0110: 1/512 0111: 1/2048 1000: 1/8192 Settings other than the above are prohibited.
[19:18]	WDTTOPS[1:0]: Timeout period select bits 00: 1024 cycles (03FFh) 01: 4096 cycles (0FFFh) 10: 8192 cycles (1FFFh) 11: 16384 cycles (3FFFh)
17	WDTSTRT: WDT start mode select bit 0: After a reset occurs, the WDT automatically starts in auto-start mode. 1: After a reset occurs, the WDT stops.

5.1.3 Timer Control/Status Register (TCSR) of the H8SX/1668

The TCSR register is used to select the clock to be input to the TCNT, specify the TCNT counter control settings, and set the timer mode. It also indicates that the TCNT overflowed in interval timer mode.

Make sure that a data read from the TCSR is performed in units of 8 bits. Also make sure that a data write to the TCSR is performed in words.

This section describes the CKS[2:0] bits.

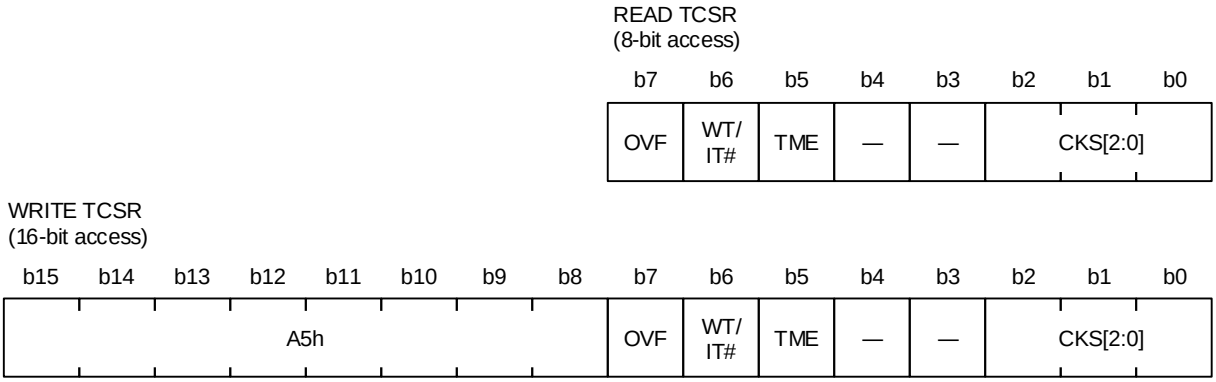


Table 5.4 Timer Control/Status Register (TCSR) of the H8SX/1668

Bit	Description
[2:0]	CKS[2:0]: Clock select bits 2 to 0 000: PCLK/2 (cycle: 25.6 µs) 001: PCLK/64 (cycle: 819.2 µs) 010: PCLK/128 (cycle: 1.6 ms) 011: PCLK/512 (cycle: 6.6 ms) 100: PCLK/2048 (cycle: 26.2 ms) 101: PCLK/8192 (cycle: 104.9 ms) 110: PCLK/32768 (cycle: 419.4 ms) 111: PCLK/131072 (cycle: 1.68 s) Note: The value enclosed in parentheses indicates the overflow cycle when Pφ is 20 MHz.

5.2 WDT Status Register (WDTSR)

5.2.1 WDT Status Register (WDTSR) of the RX65N

The WDTSR register indicates the value of the down-counter, the underflow occurrence status of the down-counter, and the refresh error occurrence status.

This section describes UNDFF and CNTVAL[13:0].

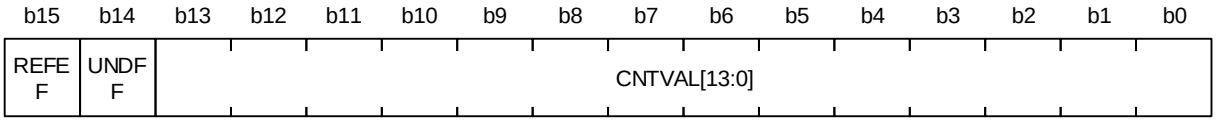


Table 5.5 WDT Status Register (WDTSR) of the RX65N

Bit	Description
14	UNDFF: Underflow flag 0: No underflow occurred. 1: An underflow occurred.
[13:0]	CNTVAL[13:0]: Down-counter value bits Value of the down-counter.

5.2.2 Reset Control/Status Register (RSTCSR) of the H8SX/1668

The RSTCSR register is used to control generation of an internal reset signal that is generated when the TCNT overflows and select the type of the internal reset signal. The RSTCSR register is initialized to 1Fh by a reset signal from the RES# pin. It is not initialized by an internal reset signal generated when the WDT overflows.

This section describes WOVF.

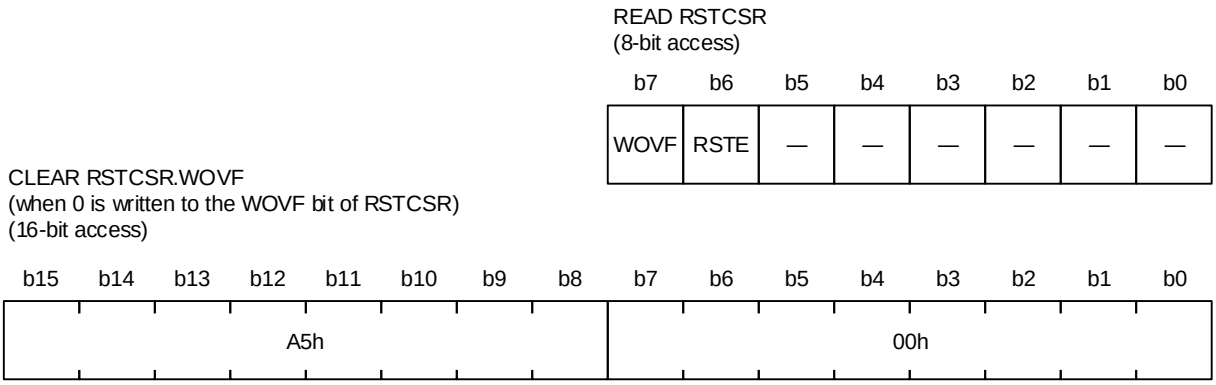


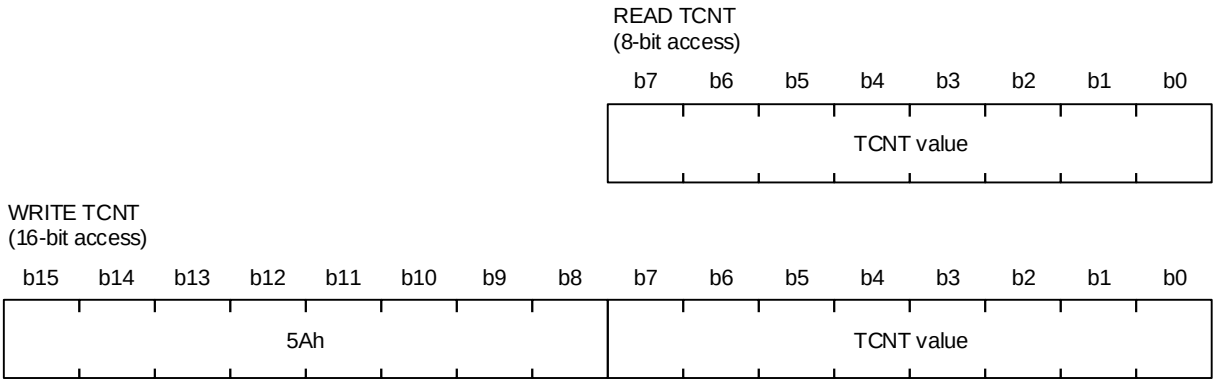
Table 5.6 WDT Status Register (WDTSR) of the RX65N

Bit	Description
7	WOVF: Watchdog timer overflow flag This flag is set when the TCNT overflows in watchdog timer mode. This flag is not set in interval timer mode. It is possible to write only 0. [Setting condition] The TCNT overflows (FFh to 00h) in watchdog timer mode. [Clearing condition] The status 1 is read, and then 0 is written.

5.2.3 Timer Counter (TCNT) of the H8SX/1668

The TCNT is a read/write-enabled 8-bit up-counter. The TCNT is initialized to “00h” when the TME bit of the timer control/status register (TCSR) is 0.

Make sure that a data read from the TCNT is performed in units of 8 bits. Also make sure that a data write to the TCNT is performed in words.



5.3 WDT Reset Control Register (WDTRCR) and Optional Function Select Register (OFS0)

5.3.1 WDT Reset Control Register (WDTRCR) of the RX65N

The WDTRCR register is used to select the reset interrupt request. In auto-start mode, the WDTRCR settings are invalid and the settings of the optional function select register 0 (OFS0) take effect. Some restrictions are placed on the write operations for the WDTRCR register. For details, refer to the hardware manual for the RX65N.

b7	b6	b5	b4	b3	b2	b1	b0
RSTIRQS	—	—	—	—	—	—	—

Table 5.7 WDT Reset Control Register (WDTRCR) of the RX65N

Bit	Description
7	RSTIRQS: Reset interrupt request select bit 0: Enables output of non-maskable interrupt requests or ordinary interrupt requests. 1: Enables output of reset signals.
[6:0]	Reserved bits

5.3.2 Optional Function Select Register 0 (OFS0) of the RX65N

The OFS0 register is used to select the reset interrupt request in auto-start mode (WDTSTRT = 0).

This section describes WDTRSTIRQS.

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	IWDTSLCSTP	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—

Table 5.8 Optional Function Select Register 0 (OFS0) of the RX65N

Bit	Description
28	WDTRSTIRQS: WDT reset interrupt request select bit 0: Enables output of non-maskable interrupt requests or ordinary interrupt requests. 1: Enables output of reset signals.

5.3.3 Reset Control/Status Register (RSTCSR) of the H8SX/1668

The RSTCSR register is used to control generation of an internal reset signal that is generated when the TCNT overflows and select the type of the internal reset signal. The RSTCSR register is initialized to 1Fh by a reset signal from the RES# pin. It is not initialized by an internal reset signal generated when the WDT overflows. This section describes the reset enable bit (RSTE).

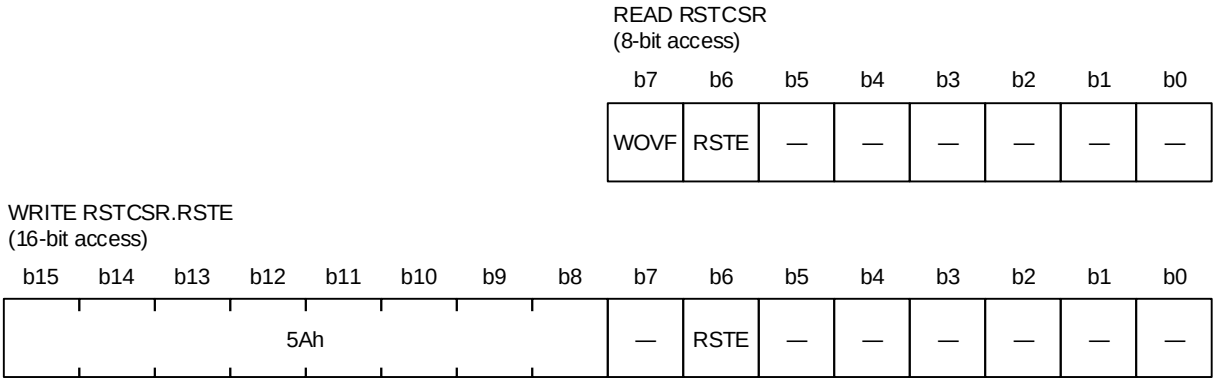


Table 5.9 WDT Status Register (WDTSR) of the RX65N

Bit	Description
7	WOVF: Watchdog timer overflow flag
6	RSTE: Reset enable bit 0: Does not internally reset the LSI even when the TCNT overflows in watchdog timer mode. (The TCNT and TCSR are reset.) 1: Internally resets the LSI when the TCNT overflows in watchdog timer mode.
[5:0]	Reserved bits

6. Usage Notes

6.1 RX Smart Configurator

On an RX-family device, RX Smart Configurator can be used when creating code for the watchdog timer. With RX Smart Configurator, when a user selects or sets the watchdog timer function from the GUI, the corresponding driver code is automatically generated. When you migrate to an RX-family device, we recommend that you use Smart Configurator.

6.2 Difference in the Operating Frequency Between the H8SX/1668 and RX65N

The RX65N can operate at a higher peripheral clock frequency than the H8SX/1668 can operate. The peripheral clock (PCLK) is used to drive the WDT subsystem. If the PCLK frequency is changed, one or more of the following conditions must be changed:

1. The clock division ratio select bit and timeout period select bit of the WDTCR register
2. An interrupt handler designed to ensure that a timer interrupt is generated at a certain frequency
3. Application code that handles the watchdog timer to prevent an underflow from occurring. Note that increasing the operating frequency may shorten the time before the watchdog timer underflows.

6.3 I/O Register Macros

With new macros defined in the iodefine.h file for RX family members, the ICU control register and interrupt vector numbers can easily be referenced by using the logical name associated with a peripheral module. These macros allow specific registers and vector numbers to be hidden, thus achieving migration between RX family members. For details, refer to the code contained in iodefine.h.

Table 6.1 Usage Examples of I/O Register Macros

Macro	Usage Example
IR(<module-name>, <bit-name>)	if (IR(WDT, WUNI) == 1)…
IEN(<module-name>, <bit-name>)	IEN(WDT, WUNI) = 1U;
IPR(<module-name>, <bit-name>)	IPR(WDT, WUNI) = 0x02;

VECT(<module-name>, <bit-name>)	#pragma interrupt
	INT_WDT(vect=VECT(WDT, WUNI))

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 27, 2023	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

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