RX65N, H8SX/1668

DTC Migration Guide: H8SX/1668 to RX65N

Introduction

This application note describes the differences in the data transfer controller (DTC) between the RX65N and H8SX/1668 devices.

Target Devices

RX65N

H8SX/1668

Contents

1. Features

Table 1.1 shows the features of the DTC modules of the RX65N and H8SX/1668 devices. Differences between the modules are shaded.

Table 1.1 Features of the DTC Module (1/2)

Item	Specifications	
	RX65N	**H8SX/1668**
Transfer mode	• Normal transfer mode Each time the module is activated, it transfers a single piece of data. • Repeat transfer mode When the module is activated once, it transfers a single piece of data. Returns control to the transfer start address each time the module transfers data of a specified size (repeat size). A maximum of 256 can be set as the repeat count. A maximum of 1,024 bytes (256 × 32 bits) can be transferred in total. • Block transfer mode Each time the module is activated, it transfers a block of data. A maximum of 1,024 bytes (256 × 32 bits) can be set as the block size.	
Transfers via arbitrary channels	• Multiple data transfers (chained transfers) can be triggered by a single trigger source. • The user can select whether another transfer is to be chained after a transfer, and the conditions under which the chained transfer is performed.	
Address mode	• Short address mode 24-bit long address 16-MB address space Data packed into three longwords • Full address mode 32-bit long address 4-GB address space Data packed into four longwords	
Unit of data transfer	• Bit length of one data piece: 1 byte (8 bits) 1 word (16 bits) 1 longword (32 bits) • Block size: 1 to 256 data pieces	
Interrupt source	• An interrupt request can be sent to the CPU by an interrupt that activated the DTC. • An interrupt request can be sent to the CPU after completion of a single data transfer. • An interrupt request can be sent to the CPU after completion of the specified number of data transfers.	
Read skip	If identical transfers occur in succession, reading of the transfer information can be omitted.	
Write-back skip	If the transfer source or destination address is fixed, writing back of the transfer information that is not updated can be omitted.	
Low power consumption function	The module can be placed in the stopped state.	
Event linkage function	An event linkage request is issued each time a single data piece (or block) is transferred.	—

Table 1.1 Features of the DTC Module (2/2)

Item	Specifications	
	RX65N	**H8SX/1668**
Disabling write-back	Disabling writing back of transfer information can be set.	—
Sequence transfer	If complicated transfers need to be performed in a predetermined order, the ordering of the transfers can be registered as a single sequence. A registered sequence can be selected according to the data to be transferred. • Only one trigger source for a sequence of transfers can be selected concurrently. • A maximum of 256 sequences can be registered for one trigger source. • The first data piece transferred by a transfer request determines the sequence. • A sequence of transfers started by a single transfer request can be continued until all transfers are completed or can be stopped before completion and resumed by the next transfer request (sequence division).	—
Addition of a displacement	A displacement can be added to the transfer source address. (Whether to add a displacement can be selected according to the transfer information.)	—

2. General Notes

- The memory layout of the transfer descriptors for the DTC differs depending on whether the MCU adopts the big-endian or little-endian format.
- The main system clock (ICLK) provides the clock for the DTC.
- Unlike most other peripheral modules, the DTC is not placed in the stopped state after a reset. While the DTC is not in use, to reduce its power consumption, place it in the stopped mode by using module stop control register A.
- For the RX65N, the DTC enable registers are located inside the interrupt controller (ICU). For the H8SX/1668, they are located inside the DTC module.
- Although the iodefine.h header file contains the definitions of DTCER registers for 256 potential DTC trigger sources, not all of the trigger sources are always available. For details on the trigger sources that are available as triggers to perform DTC transfers, refer to the interrupt vector table in the chapter on the interrupt controller in the hardware manual.
- This application note provides a summary of the changes made to the DTC. For details on the DTC, refer to the relevant hardware manual.

3. References

- Hardware manual for the RX65N:
  R01UH0590EJ0230: RX65N Group, RX651 Group User's Manual: Hardware
- Software manual for the RX65N:
  R01US0071EJ0100: RX Family RXv2 Instruction Set Architecture User's Manual: Software

(The latest versions of the above manuals are available on the Renesas website.)

3.1 Related Chapters in the Hardware Manual

- Clock Generation Circuit
  Provides details on how to set up the system clock used for the DTC.
- I/O Registers
  Shows a list of all registers.
- Low Power Consumption
  Provides details on the low-power mode of the DTC.
- Interrupt Controller
  Provides details on the settings for the interrupt sources that can trigger DTC transfers (DTCERn register settings).
- Data Transfer Controller (DTCb)
  Provides details on the DTC-specific registers and operating modes.

3.2 Related Registers

The following table lists the registers that are related to the operation of the data transfer controller (DTCb) of the RX65N.

Table 3.1 Registers Related to the Operation of the DTC

Name	Description	Chapter in the Hardware Manual
SYSTEM.SCKCR	System clock control register	Clock Generation Circuit
SYSTEM.MSTPCRA	Module stop control register A	Low Power Consumption
ICU.DTCERn	DTC transfer request enable register	Interrupt Controller (ICUB)
ICU.IERn	Interrupt request enable registers (for each DTC trigger source)	
DTC.MRA	DTC mode register A	Data Transfer Controller (DTCb)
DTC.MRB	DTC mode register B	
DTC.MRC	DTC mode register C	
DTC.SAR	DTC transfer source register	
DTC.DAR	DTC transfer destination register	
DTC.CRA	DTC transfer counting register A	
DTC.CRB	DTC transfer counting register B	
DTC.DTCCR	DTC control register	
DTC.DTCVBR	DTC vector base register	
DTC.DTCADMOD	DTC address mode register	
DTC.DTCST	DTC module activation register	
DTC.DTCSTS	DTC status register	
DTC.DTCIBR	DTC index table base register	
DTC.DTCOR	DTC operation register	
DTC.DTCSQE	DTC sequence transfer enable register	
DTC.DTCDISP	DTC address displacement register	

4. Summary of Differences of Registers

Table 4.1 shows the registers for the data transfer controllers of the RX65N and H8SX/1668 devices. The registers added or modified on the RX65N are shaded in the table. For details on the added or modified registers, refer to the relevant sections in this chapter.

Table 4.1 Differences of Registers

Register Name	Symbolic Name
DTC mode register A	MRA
DTC mode register B	MRB
[New] DTC mode register C	MRC
DTC transfer source register	SAR
DTC transfer destination register	DAR
DTC transfer counting register A	CRA
DTC transfer counting register B	CRB
DTC control register	DTCCR
DTC vector base register	DTCVBR
[New] DTC address mode register	DTCADMOD
[New] DTC module activation register	DTCST
[New] DTC status register	DTCSTS
[New] DTC index table base register	DTCIBR
[New] DTC operation register	DTCOR
[New] DTC sequence transfer enable register	DTCSQE
[New] DTC address displacement register	DTCDISP
DTC transfer request enable register	DTCERn

4.1 Changes to DTC Mode Register A (MRA)

For DTC mode register A (MRA), the write-back disable bit (WBDIS) was added. This bit is used to select whether to write back the transfer information after completion of a data transfer. If the WBDIS bit is 0, the updated transfer information is written back. If the bit is 1, the transfer information is not written back.

- MRA (for the RX65N)

Address (that cannot be directly accessed by the CPU)

b7	b6	b5	b4	b3	b2	b1	b0
MD[1:0]		SZ[1:0]		SM[1:0]		—	WBDIS

- MRA (for the H8SX/1668)

Address (that cannot be directly accessed by the CPU)

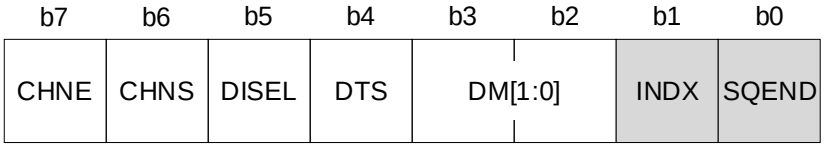
b7	b6	b5	b4	b3	b2	b1	b0
MD[1:0]		SZ[1:0]		SM[1:0]		—	—

4.2 Changes to DTC Mode Register B (MRB)

For DTC mode register B (MRB), the sequence transfer end bit (SQEND) and index table reference bit (INDX) were added. For details on the SQEND and INDX bits, refer to Table 4.2.

- MRB (for the RX65N)

Address (that cannot be directly accessed by the CPU)



- MRB (for the H8SX/1668)

Address (that cannot be directly accessed by the CPU)

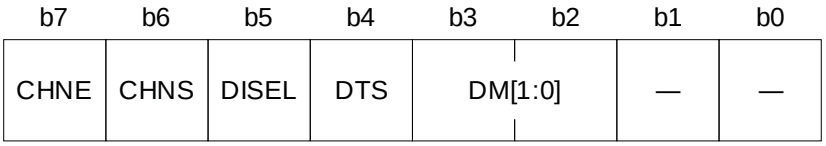


Table 4.2 Settings of the CHNE, SQEND, and INDX bits and DTC Operations in a Sequence Transfer

CHNE	SQEND	INDX	Operation	What the Settings Are Used for
0	0	1	Starts a sequence transfer.	These bit settings are used for the information about the first transfer read by a transfer request triggered by the source set in the DTCSQE register.
1	0	0	Resumes the sequence transfer.	These bit settings are used for the information about the first or a subsequent transfer in the sequence.
0	0	0	Suspends the sequence transfer.	These bit settings are used for the information about the first or a subsequent transfer in the sequence.
0	1	0	Ends the sequence transfer.	These bit settings are used for the information about the last transfer in the sequence.
0	1	1	Ends the sequence transfer and starts a new sequence transfer.	These bit settings are used for the information about the last transfer in the sequence.

Note: Settings other than the above are prohibited.
If you do not use sequence transfers, set the SQEND and INDX bits to 0.

4.3 [New Register] DTC Mode Register C (MRC)

The MRC register is used to select the DTC operating mode. This register cannot be accessed directly from the CPU. This register can be used in full address mode only. Because this register cannot be used in short address mode, to use the displacement addition function, set the DTCADMOD.SHORT bit to 0 (full address mode). If the displacement addition bit (DISPE) is 0, no displacement value is added to the transfer source address. Conversely, if this bit is 1, a displacement value is added.

- MRC (for the RX65N)

Address (that cannot be directly accessed by the CPU)

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	DISPE

4.4 Changes to DTC Control Register (DTCCR)

The following bits were deleted from the DTC control register (DTCCR): RCHNE (the bit for a DTC repeat transfer to be followed by a chained transfer) and ERR (the transfer termination flag bit). To check whether a bus error or non-maskable interrupt occurred on the RX65N, check the DTCST bit of the DTCST register. For the H8SX/1668, this status is reflected on the ERR bit.

- DTCCR (for the RX65N)

Address: DTC.DTCCR 0008 2400h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	RRS	—	—	—	—

- DTCCR (for the H8SX/1668)

Address: DTC.DTCCR 000F FF30h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	RRS	RCHNE	—	—	ERR

4.5 [New register] DTC Address Mode Register (DTCADMOD)

The DTC address mode register (DTCADMOD) is used to set the area that can be accessed by the DTC. If the short address mode setting bit (SHORT) is 0, full address mode is set. If the bit is 1, short address mode is set.

- DTCADMOD (for the RX65N)

Address: DTC.DTCADMOD 0008 2408h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	SHORT

4.6 [New Register] DTC Module Activation Register (DTCST)

The DTC module activation register (DTCST) is used to set whether to operate or stop the DTC module. If the DTC module activation bit (DTCST) is 0, the DTC module terminates and accepts no more transfer requests. If the bit is 1, the DTC module accepts transfer requests. If the bit setting is changed to 0 during a data transfer, the accepted transfer request is valid until the current processing is completed. When a bus error or non-maskable interrupt occurs, this bit is cleared to 0 (DTC module stoppage). To enable transmission when the module is stopped or all module clocks are stopped or when the module is in software standby mode or deep software standby mode, clear the DTCST bit to 0.

- DTCST (for the RX65N)

Address: DTC.DTCST 0008 240Ch

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	DTCST

4.7 [New Register] DTC Status Register (DTCSTS)

The DTC status register (DTCSTS) indicates the transfer operation status of the DTC. While the DTC is transferring data, the DTC active flag bit (ACT) is set to 1. The DTC active vector number monitoring flag bit (VECN) is valid and indicates the vector number of the trigger source only when the ACT bit is 1.

- DTCSTS (for the RX65N)

Address: DTC.DTCSTS 0008 240Eh

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ACT	—	—	—	—	—	—	—	VECN[7:0]							

4.8 [New Register] DTC Index Table Base Register (DTCIBR)

The DTC index table base register (DTCIBR) sets the base address that is used to calculate the address at which to allocate a DTC index. For the highest four bits, write operations are ignored. The value written to b27 is also written to these bits. The lowest 10 bits are reserved bits. The values of these bits are fixed to 0. It is only possible to write 0 to these bits. A value in the range from 0000 0000h to 07FF FC00h or the range from F800 0000h to FFFF FC00h can be set in K units.

- DTCIBR (for the RX65N)

Address: DTC.DTCIBR 0008 2410h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

4.9 [New Register] DTC Operation Register (DTCOR)

The DTC operation register (DTCOR) sets the operation of the DTC module. If the sequence transfer end bit (SQTFRL) is set to 1, the currently running sequence transfer ends. Be careful if the DTCSQE.ESPSEL bit is set to 1 (enable sequence transfers). In this case, disable the DTC transfer request triggered by the relevant interrupt (by setting IERm.IENj to 0). If the relevant data transfer is in progress, wait until it ends and then forcibly terminate the sequence transfer by the DTC. If 1 is written to the SQTFRL bit when no sequence transfer is being performed, nothing happens.

- DTCOR (for the RX65N)

Address: DTC.DTCOR 0008 2414h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	SQTFRL

4.10 [New Register] DTC Sequence Transfer Enable Register (DTCSQE)

The DTC sequence transfer enable register (DTCSQE) is used to specify the settings for sequence transfers by the DTC. For the sequence transfer vector number specification bit (VECN), specify the number of the vector that uses sequence transfers. Sequence transfers can operate by only one trigger source. The sequence transfer enable bit (ESPSEL) specifies whether to use sequence transfers. To use sequence transfers by setting the ESPSEL bit to 1, make sure that the DTCADMOD.SHORT bit is 0 (full address mode).

- DTCSQE (for the RX65N)

Address: DTC.DTCSQE 0008 2416h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ESPSEL	—	—	—	—	—	—	—	VECN[7:0]							

4.11 [New Register] DTC Address Displacement Register (DTCDISP)

The DTC address displacement register (DTCDISP) specifies the displacement value to be added to the transfer source address of the DTC. If the MRC.DISPE bit is 1, the result of adding the DTCDISP value to the SAR value becomes the transfer source address.

- DTCDISP (for the RX65N)

Address: DTC.DTCDISP 0008 2418h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

4.12 DTC Transfer Request Enable Register (DTCERn)

On both the H8SX/1668 and RX65N devices, the DTC transfer request enable register (DTCERn) is used to select the interrupt source that activates the DTC. For the H8SX/1668 device, the DTCERn registers are built into the DTC module. Each of these registers has multiple interrupt source bits. For the RX65N device, the DTCERn registers are built into the interrupt controller (ICU). A separate DTCERn register is provided for each interrupt source. Check the valid interrupt numbers for DTC trigger sources in the interrupt vector table. Then, set the relevant DTC transfer request enable bit (DTCE) to 1 to enable the interrupt.

- DTCERn (for the RX65N)

Address: ICU.DTCER026 0008 711Ah to ICU.DTCER255 0008 71FFh

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	DTCE

- DTCERn (for the H8SX/1668)

Address: DTC.DTCERF 000F FF20h to DTC.DTCERF 000F FF2Ah

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
DTCE 15	DTCE 14	DTCE 13	DTCE 12	DTCE 11	DTCE 10	DTCE 9	DTCE 8	DTCE 7	DTCE 6	DTCE 5	DTCE 4	DTCE 3	DTCE 2	DTCE 1	DTCE 0

5. Usage Notes

5.1 RX Smart Configurator

On an RX-family device, RX Smart Configurator can be used when creating code for the DTC. With RX Smart Configurator, when a user selects or sets the DTC function from the GUI, the corresponding driver code is automatically generated. When you migrate to an RX-family device, we recommend that you use Smart Configurator.

5.2 I/O Register Macros

With new macros defined in the iodefine.h file for RX family members, the ICU control register, module stop register, DTC enable register, and interrupt vector numbers can easily be referenced by using the logical name associated with a peripheral module. These macros allow specific registers and vector numbers to be hidden, thus achieving migration between RX family members. For details, refer to the code contained in iodefine.h.

Table 5.1 Usage Examples of I/O Register Macros

Macro	Usage Example
IR(<module-name>, <bit-name>)	if (IR(SCI0, TXI0) == 1)…
IEN(<module-name>, <bit-name>)	IEN(SCI0, TXI0) = 1;
IPR(<module-name>, <bit-name>)	IPR(SCI0, TXI0) = 0x02;
MSTP(<module-name>)	MSTP(DTC) = 0;
VECT(<module-name>, <bit-name>)	#progma interrupt (MySciTxIsr(vect=VECT(SCI0,TXI0)))

5.3 DTC Enable Register

With the latest version of Renesas Toolchain for RX family devices, a C header file that contains macros for greatly simplifying the code for the DTC enable register is created. The created code can be reused between RX family members that share the same peripheral modules. These macros are defined in the iodefine.h file.

Examples:

```
DTCE(SCI0, RXI0) = 1 ; /* Enables DTC activation on SCI0 data reception */
DTCE(ADC0, ADI0) = 1 ; /* Enables DTC activation on AD0 conversion complete */
```

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 27, 2023	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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