RX65N, H8SX/1668

ADC Migration Guide: H8SX/1668 to RX65N

Introduction

This application note describes the differences in the A/D converter module between the RX65N and H8SX/1668 devices.

Target Devices

RX65N

H8SX/1668

Contents

1. Features 4
2. General Notes 6
3. References 6
3.1 Related Chapters in the Hardware Manual 6
3.2 Related Registers 7
4. Hardware Details 9
5. Register Details 10
5.1 A/D Data Register: ADDRy 12
5.1.1 RX65N 12
5.1.2 H8SX/1668 12
5.2 A/D Control Registers: ADCSR and ADCR 13
5.2.1 RX65N 13
5.2.2 H8SX/1668 14
5.3 A/D Control/Status Register: ADCSR 15
5.3.1 RX65N 15
5.3.2 H8SX/1668 15
5.4 A/D Channel Select Register A0: ADANSA0 17
5.4.1 RX65N 17
5.4.2 H8SX/1668 17
5.5 A/D Channel Select Register A1: ADANSA1 18
5.5.1 RX65N 18
5.5.2 H8SX/1668 18
5.6 A/D Control Extended Register: ADCER 19
5.6.1 RX65N 19
5.6.2 H8SX/1668 19
5.7 A/D Conversion Start Trigger Select Register: ADSTRGR 20
5.7.1 RX65N 20
5.7.2 H8SX/1668 21
5.8 A/D Sampling State Register n: ADSSTRn (n = 0 to 15, L, T, or O) 22
5.8.1 RX65N 22
5.8.2 H8XS/1668 22
5.9 A/D Sample-and-Hold Circuit Control Register: ADSHCR 23
5.9.1 RX65N 23
5.9.2 H8SX/1668 23
5.10 A/D Sample-and-Hold Operating Mode Select Register: ADSHMSR 24
5.10.1 RX65N 24
5.10.2 H8SX/1668 24

6. Usage Notes 25
6.1 RX Smart Configurator 25
6.2 I/O Register Macros 25
6.3 Polling to Check for the End of A/D Conversion 25
6.4 Differences in the Timing of A/D Conversion Between the H8SX/1668 and RX65N 26

Revision History 27

1. Features

Table 1.1 shows the features of the A/D converters of the RX65N and H8SX/1668 devices. Differences between the devices are shaded.

Table 1.1 Features of the A/D Converter (1/2)

Item	Specifications	
	RX65N	**H8SX/1668**
Resolution	12 bits	10 bits
Number of units	Two units: Units 0 and 1	
Input channels	30 channels in total 8 channels: Unit 0 22 channels: Unit 1	8 channels in total 4 channels: Unit 0 4 channels: Unit 1 or 8 channels: Unit 0 0 channels: Unit 1
Conversion time per channel	0.48 µs 12-bit conversion mode 0.45 µs 10-bit conversion mode 0.42 µs 8-bit conversion mode (when the A/D conversion clock ADCLK is operating at 60 MHz)	2.7 µs (when the peripheral clock PCLK is operating at 35 MHz)
Maximum signal source impedance for full-speed conversion	1.0 kΩ	5.0 kΩ
A/D conversion clocks	4 types:*1 PCLK PCLK/2 PCLK/4 PCLK/8 The operating clock can be set for each unit. (Unit 0 can operate using PCLKC and unit 1 can operate using PCLKD.)	1 type: Pφ (peripheral clock)
Operating mode	• Single-scan mode • Continuous-scan mode • Group-scan mode	Single mode Scan mode
Conversion is started by	• Software • Trigger signal from the TPU, MTU, TMR, or ELC • External trigger: #ADTRG pin	• Software • Trigger by TPU or TMR • External trigger: #ADTRG pin

Table 1.1 Features of the A/D Converter (2/2)

Item	Specifications	
	RX65N	**H8SX/1668**
Function	• Sample-and-hold • Channel-specific sample-and-hold: 3 channels (available with unit 0 only) • Variable number of sampling states (can be set for each channel) • Self-diagnosis for 12-bit A/D converter • Addition mode or averaging mode can be selected for A/D conversion values • Analog input disconnection detection assist (discharge/pre-charge function) • Double-trigger mode (A/D-converted data duplication function) • Conversion mode switchover (12/10/8-bit mode) • A/D data register automatic clearing • Extended analog input • Compare (windows A and B)	• Sample-and-hold
Interrupt source	• A/D conversion end interrupt (S12ADI) • Group-B A/D conversion end interrupt (S12GBADI) • Group-C A/D conversion end interrupt (S12GCADI) • Compare interrupt (S12CMPAI) • DMAC can be triggered • DTC can be triggered	• A/D conversion end interrupt (ADI) • DMAC can be triggered • DTC can be triggered (unit 0 only)
Event linkage	• ELC event can be generated when all scans end. • Scans can be started by a trigger signal from the ELC.	
Low power consumption	The module can be placed in the stopped state.	The module can be placed in the stopped state.

Note: 1. The clock source for unit 0 is PCLKC and the clock source for unit 1 is PCLKD. “PCLK” refers to PCLKB.

2. General Notes

- As a result of improvement in the conversion speed, the external signal regulator may need to be modified. The new clock generation circuit and conversion option can minimize such modification or can make such modification unnecessary.
- For the result register, left-justification or right-justification can be selected to maintain compatibility with the existing software. For the number of bits, 12, 10, or 8 can be selected.
  For the RX65N device, by default, the result is right-justified and the value that is read is stored in the lowest 12 bits of the 16-bit register. Data is left-justified by setting “b'1” for the ADRFMT bit of the A/D control extended register (ADCER) for compatibility with the application code ported from the H8SX device. 10-bit conversion mode is set by setting “b'01” for the ADPRC[1:0] bits.
- The new diagnosis register makes it possible to check whether the ADC is normally operating by reading the internal reference voltage.
  On the RX65N device, single-cycle scan mode is available with both units 0 and 1 (note that this mode has been renamed to “single-scan mode” in the RX65N device). On the H8SX/1668, the mode is available with only unit 1.

3. References

- Hardware manual for the RX65N:
  R01UH0590EJ0230: RX65N Group, RX651 Group User’s Manual: Hardware
- Software manual for the RX65N:
  R01US0071EJ0100: RX Family RXv2 Instruction Set Architecture User’s Manual: Software

(The latest versions of the above manuals are available on the Renesas website.)

3.1 Related Chapters in the Hardware Manual

- Clock Generation Circuit
  Provides details on how to set up the peripheral clocks used for the ADC.
- I/O Registers
  Shows a list of all registers.
- Low Power Consumption
  Provides details on the module stop control registers.
- Interrupt Controller
  Describes how to enable interrupts from the ADC to the interrupt controller.
- Event Link Controller
  Provides details on the ADC event link setting register.
- Multi-Function Pin Controller
  Provides details on the pin function control registers related to ADC-related pins.
- 12-Bit A/D Converter
  Provides details on the ADC-specific registers and operating modes.

3.2 Related Registers

The following table lists the registers that are related to the operation of the A/D converter module (S12ADFa) of the RX65N.

Table 3.1 Registers Related to the Operation of the A/D Converter (1/2)

Name	Description	Chapter in the Hardware Manual
SYSTEM.SCKCR	System clock control register	Clock Generation Circuit
SYSTEM.MSTPCRA	Module stop control register A	Low Power Consumption
ICU.IRn	Interrupt request register	Interrupt Controller
ICU.IERm	Interrupt request enable register	
ICU.IPRr	Interrupt source priority register	
ICU.SLIBRx	Software configurable interrupt B source select register	
ICU.GRPBLx	Group-BLx interrupt request register	
ICU.GENBLx	Group-BLx interrupt request enable register	
ELC.ELSRn	Event link setting register	Event Link Controller
MPC.PmnPFS	Pmn pin function control register	Multi-Function Pin Controller
S12ADx.ADDRy	A/D data register	12-Bit A/D Converter
S12ADx.ADDRBLDR	A/D data duplication register	
S12ADx.ADDRBLDRA	A/D data duplication register A	
S12ADx.ADDRBLDRB	A/D data duplication register B	
S12ADx.ADTSDR	A/D temperature sensor data register	
S12ADx.ADOCDR	A/D internal reference voltage data register	
S12ADx.ADRD	A/D self-diagnosis data register	
S12ADx.ADCSR	A/D control register	
S12ADx.ADANSA0	A/D channel select register A0	
S12ADx.ADANSA1	A/D channel select register A1	
S12ADx.ADANSB0	A/D channel select register B0	
S12ADx.ADANSB1	A/D channel select register B1	
S12ADx.ADANSC0	A/D channel select register C0	
S12ADx.ADANSC1	A/D channel select register C1	
S12ADx.ADADS0	A/D-converted value addition/averaging function channel select register 0	
S12ADx.ADADS1	A/D-converted value addition/averaging function channel select register 1	
S12ADx.ADADC	A/D-converted value addition/averaging count select register	
S12ADx.ADCER	A/D control extended register	
S12ADx.ADSTRGR	A/D conversion start trigger select register	
S12ADx.ADEXICR	A/D conversion extended input control register	
S12ADx.ADGCEXCR	A/D group-C extended input control register	
S12ADx.ADGCTRGR	A/D group-C trigger select register	
S12ADx.ADSSTR	A/D sampling state register	
S12ADx.ADSHCR	A/D sample-and-hold circuit control register	
S12ADx.ADSHMSR	A/D sample-and-hold operating mode select register	
S12ADx.ADDISCR	A/D disconnection detection control register	
S12ADx.ADGSPCR	A/D group-scan priority control register	
S12ADx.ADCMPCR	A/D compare function control register	

Table 3.1 Registers Related to the Operation of the A/D Converter (2/2)

Name	Description	Chapter in the Hardware Manual
S12ADx.ADCMPANSR0	A/D compare function window-A channel select register 0	12-Bit A/D Converter
S12ADx.ADCMPANSR1	A/D compare function window-A channel select register 1	
S12ADx.ADCMPANSER	A/D compare function window-A extended input select register	
S12ADx.ADCMPLR0	A/D compare function window-A comparison condition setting register 0	
S12ADx.ADCMPLR1	A/D compare function window-A comparison condition setting register 1	
S12ADx.ADCMPLER	A/D compare function window-A extended input comparison condition setting register	
S12ADx.ADCMPDR0	A/D compare function window-A lower-bit level setting register	
S12ADx.ADCMPDR1	A/D compare function window-A upper-bit level setting register	
S12ADx.ADCMPSR0	A/D compare function window-A channel status register 0	
S12ADx.ADCMPSR1	A/D compare function window-A channel status register 1	
S12ADx.ADCMPSER	A/D compare function window-A extended input channel status register	
S12ADx.ADWINMON	A/D compare function window-A/B status monitor register	
S12ADx.ADCMPBNSR	A/D compare function window-B channel select register	
S12ADx.ADWINLLB	A/D compare function window-B lower-bit level setting register	
S12ADx.ADWINULB	A/D compare function window-B upper-bit level setting register	
S12ADx.ADCMPBSR	A/D compare function window-B channel status register	
S12ADx.ADSAM	A/D sequential conversion time setting register	
S12ADx.ADSAMPR	A/D sequential conversion time setting protection release register	

4. Hardware Details

The RX65N device has the VREFL0 pin but the H8SX/1668 device does not have its equivalent pin. The reference supply for unit 0 can be input from the VREFH0 or VREFL0 pin. The reference voltage of the RX651 device is shared with the AVCC and AVSS pins. Separate AVCC and AVSS pins are available to each unit. (Unit 0: AVCC0 and AVSS0, unit 1: AVCC1 and AVSS1)

Table 4.1 Analog Pins for the RX65N and H8SX/1668 Devices

Unit	RX65N	H8SX/1668
Unit 0	AVCC0	AVCC
	AVSS0	AVSS
	VREFH0	VREF
	VREFL0	—
Unit 1	AVCC1	AVCC
	AVSS1	AVSS
	—	VREF

For details on ground connection, power supplies, and bypassing, refer to the data sheet for the RX65N device. The valid voltage for the VREFH0 pin is from 2.7 V to AVCC.

To take advantage of the accelerated ADC of the RX65N device, signal conditioning circuitry connected to the analog inputs must be of suitably low impedance.

Table 4.2 Signal Source Impedances of the RX65N and H8SX/1668 Devices

Name	RX65N	H8SX/1668
Maximum peripheral clock	ADCLK: 60 MHz	PCLK: 35 MHz
Maximum conversion speed	0.48 µs/channel (12-bit conversion mode) 0.45 µs/channel (10-bit conversion mode) 0.42 µs/channel (8-bit conversion mode)	2.7 µs/channel
Maximum signal source impedance	1.0 kΩ	5.0 kΩ

New clock generation circuit and conversion options can be used to minimize or eliminate the need for external circuit hardware modification. For details, refer to section 6.4, “Differences in the Timing of A/D Conversion Between the H8SX/1668 and RX65N”.

5. Register Details

Table 5.1 lists the registers for the A/D converters of the RX65N and H8SX/1668 devices. The registers related to the functions of the H8SX/1668 device are shaded. For details on the other registers, refer to the hardware manual for the RX65N.

Table 5.1 List of Registers for the A/D Converter (1/2)

RX65N	H8SX/1668
A/D data register y (ADDRy) (y = 0 to 7: unit 0, y = 0 to 20: unit 1)	A/D data register y (y = A to H: unit 0, y = E to H: unit 1)
A/D data duplication register (ADDRBLDR)	
A/D data duplication register A (ADDRBLDRA)	
A/D data duplication register B (ADDRBLDRB)	
A/D temperature sensor data register (ADTSDR)	
A/D internal reference voltage data register (ADOCDR)	
A/D self-diagnosis data register (ADRD)	
A/D control register (ADCSR)	A/D control register (ADCR)
	A/D control/status register (ADCSR)
A/D channel select register A0 (ADANSA0)	
A/D channel select register A1 (ADANSA1)	
A/D channel select register B0 (ADANSB0)	
A/D channel select register B1 (ADANSB1)	
A/D channel select register C0 (ADANSC0)	
A/D channel select register C1 (ADANSC1)	
A/D-converted value addition/averaging function channel select register 0 (ADADS0)	
A/D-converted value addition/averaging function channel select register 1 (ADADS1)	
A/D-converted value addition/averaging count select register (ADADC)	
A/D control extended register (ADCER)	
A/D conversion start trigger select register (ADSTRGR)	
A/D conversion extended input control register (ADEXICR)	
A/D group-C extended input control register (ADGCEXCR)	
A/D group-C trigger select register (ADGCTRGR)	
A/D sampling state register (ADSSTRn) (n = 0 to 15, L, T, or O)	
A/D sample-and-hold circuit control register (ADSHCR)	
A/D sample-and-hold operating mode select register (ADSHMSR)	
A/D disconnection detection control register (ADDISCR)	
A/D group-scan priority control register (ADGSPCR)	
A/D compare function control register (ADCMPCR)	
A/D compare function window-A channel select register 0 (ADCMPANSR0)	
A/D compare function window-A channel select register 1 (ADCMPANSR1)	

Table 5.1 List of Registers for the A/D Converter (2/2)

RX65N	H8SX/1668
A/D compare function window-A extended input select register (ADCMPANSER)	
A/D compare function window-A comparison condition setting register 0 (ADCMPLR0)	
A/D compare function window-A comparison condition setting register 1 (ADCMPLR1)	
A/D compare function window-A extended input comparison condition setting register (ADCMPLER)	
A/D compare function window-A lower-bit level setting register (ADCMPDR0)	
A/D compare function window-A upper-bit level setting register (ADCMPDR1)	
A/D compare function window-A channel status register 0 (ADCMPSR0)	
A/D compare function window-A channel status register 1 (ADCMPSR1)	
A/D compare function window-A extended input channel status register (ADCMPSER)	
A/D compare function window-A/B status monitor register (ADWINMON)	
A/D compare function window-B channel select register (ADCMPBNSR)	
A/D compare function window-B lower-bit level setting register (ADWINLLB)	
A/D compare function window-B upper-bit level setting register (ADWINULB)	
A/D compare function window-B channel status register (ADCMPBSR)	
A/D sequential conversion time setting register (ADSAM)	
A/D sequential conversion time setting protection release register (ADSAMPR)	

5.1 A/D Data Register: ADDRy

The ADDRy register is a 16-bit read-only register that stores A/D conversion results.

On the RX65N device, the number of bits and justification format (left-justification or right-justification) for A/D conversion results can be specified by using the register described in section 5.6, “A/D Control Extended Register: ADCER”.

On the H8SX/1668 device, A/D conversion results are stored in 10-bit format in the ADDRy[15:6] bits.

5.1.1 RX65N

ADCER.ADRFMT = 0,
ADCER.ADPRC[1:0] = b’01

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	–	ADDRy[9:0]									

ADCER.ADRFMT = 1,
ADCER.ADPRC[1:0] = b’01

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ADDRy[15:6]										–	–	–	–	–	–

5.1.2 H8SX/1668

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ADDRy[15:6]										–	–	–	–	–	–

5.2 A/D Control Registers: ADCSR and ADCR

5.2.1 RX65N

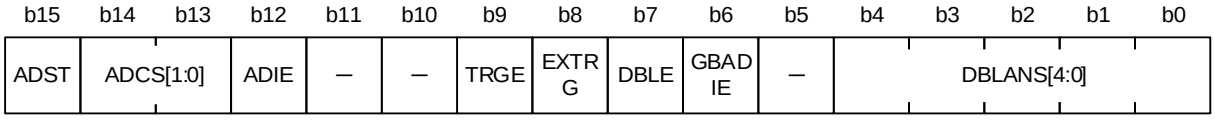

Table 5.2 ADCSR Register of the RX65N Device

Bit	Description	Remarks
15	A/D conversion start bit 0: Stops A/D conversion. 1: Starts A/D conversion.	
[14:13]	Scan mode select bits 00: Single-scan mode 01: Group-scan mode 10: Continuous-scan mode 11: Setting prohibited	
12	Scan end interrupt enable bit 0: Disables occurrence of an interrupt after the end of a scan. 1: Enables occurrence of an interrupt after the end of a scan.	
[11:10]	Reserved bits	
9	Trigger-based start enable bit 0: Disables start of A/D conversion by a synchronization or asynchronization trigger. 1: Enables start of A/D conversion by a synchronization or asynchronization trigger.	
8	Trigger select bit 0: Uses a synchronization trigger for starting A/D conversion. 1: Uses an asynchronous trigger for starting A/D conversion.	
7	Double trigger mode select bit 0: Does not select double trigger mode. 1: Selects double trigger mode.	
6	Group-B scan end interrupt enable bit 0: Disables occurrence of an interrupt after the end of a scan for group B. 1: Enables occurrence of an interrupt after the end of a scan for group B.	
5	Reserved bit	
[4:0]	Double-trigger target channel select bits Select the analog input channel for which double-trigger mode is applied. The settings of these bits take effect only when double-trigger mode is selected.	

5.2.2 H8SX/1668

For the H8SX/1668 device, the A/D control register equivalent to ADCSR is ADCR.

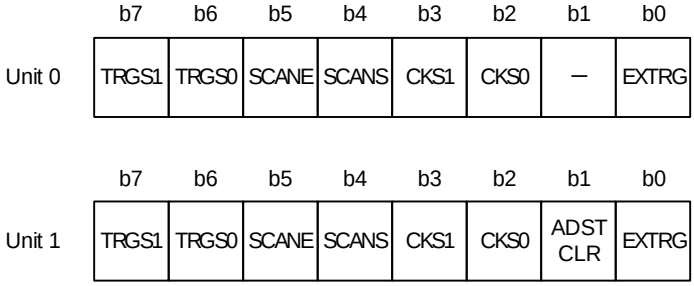

Table 5.3 DCR Register of the H8SX/1668 Device

Bit	Description	Remarks
[7:6], 0	Timer trigger select bits 1 and 0, and extended trigger select bit 000: Disables start of A/D conversion by an external trigger. 010: Starts A/D conversion by the conversion trigger signal from the TPU (unit 0). 100: Starts A/D conversion by the conversion trigger signal from the TMR (unit 0/1). 110: Starts A/D conversion by ADTRG0. 001: Disables external triggers. 011: Setting prohibited 101: Setting prohibited 111: Starts A/D conversion by ADTRG0 (both units are started simultaneously).	
[5:4]	Scan mode 0X: Single mode 10: Scan mode (continuous A/D conversion for 1 to 4 channels) 11: Scan mode (continuous A/D conversion for 1 to 8 channels)	
[3:2]	Clock select bits 1 and 0 (unit 0) 00: Conversion time = 528 states 01: Conversion time = 268 states 10: Conversion time = 138 states 11: Conversion time = 73 states Extended clock select bit, and clock select bits 1 and 0 (unit 1) 000: Conversion time = 528 states 001: Conversion time = 268 states 010: Conversion time = 138 states 011: Conversion time = 73 states 100: Conversion time = 336 states 101: Conversion time = 172 states 110: Conversion time = 90 states 111: Conversion time = 49 states	For unit 1, the ADCSR1. EXCKS value is used.
1	A/D conversion start bit clearing bit 0: Disables automatic clearing of the ADST bit in scan mode. 1: Clears the ADST bit in scan mode when A/D conversion for all selected channels ends.	This is a reserved bit for unit 0.

5.3 A/D Control/Status Register: ADCSR

5.3.1 RX65N

The RX65N device has the A/D control register (ADCSR). Some item names and register specifications are different than the corresponding registers of the H8SX/1668 device. For details on the ADCSR register of the RX65N device, refer to section 5.2.1, “RX65N”.

5.3.2 H8SX/1668

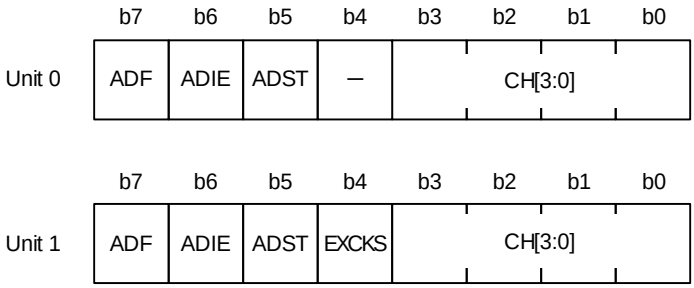

Table 5.4 ADCSR Register of the H8SX/1668 Device (1/2)

Bit	Description	Remarks
7	A/D end flag Status flag indicating whether A/D conversion ended	
6	A/D interrupt enable bit Setting this bit to 1 enables ADF to generate ADI interrupts.	
5	A/D start bit 0: Stops A/D conversion and places the device in a standby state. 1: Starts A/D conversion.	
4	Extended clock select bit Sets the A/D conversion time in combination with the CKS1/0 bit of the ADCR register.	This is a reserved bit for unit 0.

Table 5.4 ADCSR Register of the H8SX/1668 Device (2/2)

<table>
<tr><th>Bit</th><th>Description</th><th>Remarks</th></tr>
<tr><td>[3:0]</td><td>Channel select bits 3 to 0
These bits are used to select the analog input in combination with the SCANE and SCANS bits of the ADCR register.
• Unit 0
<table>
<tr><th>Single mode
(ADCR.SCANE = 0)</th><th>Scan mode: 4 channels
(ADCR.SCANE = 1 and
ADCR.SCANS = 0)</th></tr>
<tr><td rowspan="2">0000: AN0
0001: AN1
0010: AN2
0011: AN3
0100: AN4
0101: AN5
0110: AN6
0111: AN7
1XXX: Setting prohibited</td><td>0000: AN0
0001: AN0 and AN1
0010: AN0 to AN2
0011: AN0 to AN3
0100: AN4
0101: AN4 and AN5
0110: AN4 to AN6
0111: AN4 to AN7
1XXX: Setting prohibited</td></tr>
<tr><td>Scan mode: 8 channels
(ADCR.SCANE = 1 and
ADCR.SCANS = 1)</td></tr>
<tr><td></td><td>0000: AN0
0001: AN0 and AN1
0010: AN0 to AN2
0011: AN0 to AN3
0100: AN0 to AN4
0101: AN0 to AN5
0110: AN0 to AN6
0111: AN0 to AN7
1XXX: Setting prohibited</td></tr>
</table>
• Unit 1
<table>
<tr><th>Single mode
(ADCR.SCANE = 0)</th><th>Scan mode: 4 channels
(ADCR.SCANE = 1 and
ADCR.SCANS = 0)</th></tr>
<tr><td rowspan="2">00XX: Setting prohibited
0100: AN4
0101: AN5
0110: AN6
0111: AN7
1XXX: Setting prohibited</td><td>00XX: Setting prohibited
0100: AN4
0101: AN4 and AN5
0110: AN4 to AN6
0111: AN4 to AN7
1XXX: Setting prohibited</td></tr>
<tr><td>Scan mode: 8 channels
(ADCR.SCANE = 1 and
ADCR.SCANS = 1)</td></tr>
<tr><td></td><td>XXXX: Setting prohibited</td></tr>
</table>
</td><td>The settings on unit 0 are different from those on unit 1.</td></tr>
</table>

5.4 A/D Channel Select Register A0: ADANSA0

5.4.1 RX65N

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Unit 0	–	–	–	–	–	–	–	–	ANSA 007	ANSA 006	ANSA 005	ANSA 004	ANSA 003	ANSA 002	ANSA 001	ANSA 000

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Unit 1	ANSA 015	ANSA 014	ANSA 013	ANSA 012	ANSA 011	ANSA 010	ANSA 009	ANSA 008	ANSA 007	ANSA 006	ANSA 005	ANSA 004	ANSA 003	ANSA 002	ANSA 001	ANSA 000

Table 5.5 ADANSA0 Register of the RX65N Device (Unit 0)

Bit	Description	Remarks
[15:8]	Reserved bits	
[7:0]	A/D conversion channel select bits The ANSA000 bit corresponds to the AN100 bit and the ANSA015 bit corresponds to the AN115 bit. 0: The channel is not subject to conversion. 1: The channel is subject to conversion.	On unit 0, bits 7 to 0 are effective.

Table 5.6 ADANSA0 Register of the RX65N Device (Unit 1)

Bit	Description	Remarks
[15:0]	A/D conversion channel select bits The ANSA000 bit corresponds to the AN100 bit and the ANSA015 bit corresponds to the AN115 bit. 0: The channel is not subject to conversion. 1: The channel is subject to conversion.	On unit 1, bits 15 to 0 are effective.

5.4.2 H8SX/1668

On the H8SX/1668 device, A/D channel select register A0 is not present. Channel selection is performed by using the CH[3:0] bits of the ADCR register.

5.5 A/D Channel Select Register A1: ADANSA1

5.5.1 RX65N

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Unit 1	–	–	–	–	–	–	–	–	–	–	–	ANSA 104	ANSA 103	ANSA 102	ANSA 101	ANSA 100

Table 5.7 ADANSA1 Register of the RX65N Device (Unit 1)

Bit	Description	Remarks
[15:5]	Reserved bits	
[4:0]	A/D conversion channel select bits The ANSA100 bit corresponds to the AN116 bit and the ANSA104 bit corresponds to the AN120 bit. 0: The channel is not subject to conversion. 1: The channel is subject to conversion.	These bits are effective on only unit 1.

5.5.2 H8SX/1668

On the H8SX/1668 device, A/D channel select register A1 is not present. Channel selection is performed by using the CH[3:0] bits of the ADCR register.

5.6 A/D Control Extended Register: ADCER

5.6.1 RX65N

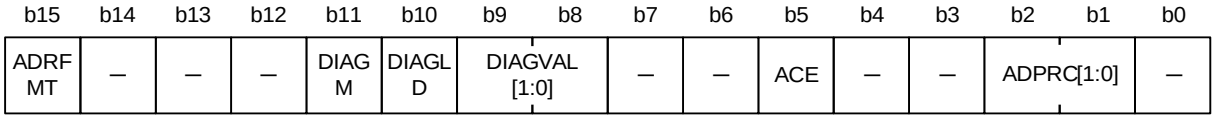

Table 5.8 ADCER Register of the RX65N Device

Bit	Description	Remarks
15	A/D data register format select bit 0: Sets right-justification for the A/D data register. 1: Sets left-justification for the A/D data register.	
[14:12]	Reserved bits	
11	Self-diagnosis enable bit 0: Disables self-diagnosis of the 12-bit A/D converter. 1: Enables self-diagnosis of the 12-bit A/D converter.	
10	Self-diagnosis mode select bit 0: Voltage-rotation self-diagnosis mode 1: Fixed-voltage self-diagnosis mode	
[9:8]	Self-diagnosis conversion voltage select bits 00: Setting prohibited in fixed-voltage self-diagnosis mode 01: Makes self-diagnosis by using a voltage of 0 V. 10: Makes self-diagnosis by using the 1/2 voltage of the reference supply. 11: Makes self-diagnosis by using the voltage of the reference supply.	
[7:6]	Reserved bits	
5	A/D data register automatic clearing enable bit 0: Disables automatic clearing. 1: Enables automatic clearing.	
[4:3]	Reserved bits	
[2:1]	A/D conversion accuracy specification bits 00: Performs A/D conversion at an accuracy of 12 bits. 01: Performs A/D conversion at an accuracy of 10 bits. 10: Performs A/D conversion at an accuracy of 8 bits. 11: Setting prohibited	
0	Reserved bit	

5.6.2 H8SX/1668

On the H8SX/1668 device, A/D control extended register is not present. Data is always stored in ADDRy[15:6]. A/D conversion is always performed at an accuracy of 10 bits.

5.7 A/D Conversion Start Trigger Select Register: ADSTRGR

5.7.1 RX65N

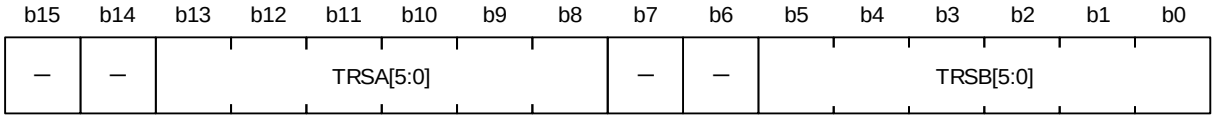

Table 5.9 DSTRGR Register of the RX65N Device (1/2)

Bit	Description	Remarks
[15:14]	Reserved bits	
[13:8]	A/D conversion start trigger select bits 111111: Trigger source not selected 000001: Compare match/input capture of MTU0.TGRA 000010: Compare match/input capture of MTU1.TGRA 000011: Compare match/input capture of MTU2.TGRA 000100: Compare match/input capture of MTU3.TGRA 000101: Compare match/input capture of MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode 000110: Compare match/input capture of MTU6.TGRA 000111: Compare match/input capture of MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode 001000: Compare match of MTU0.TGRE 001001: Compare match of MTU4.TADCORA and MTU4.TCNT 001010: Compare match of MTU4.TADCORB and MTU4.TCNT 001011: Compare match of MTU4.TADCORA and MTU4.TCNT, or compare match of MTU4.TADCORB and MTU4.TCNT 001100: Compare match of MTU4.TADCORA and MTU4.TCNT, and compare match of MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used) 001101: Compare match of MTU7.TADCORA and MTU7.TCNT 001110: Compare match of MTU7.TADCORB and MTU7.TCNT 001111: Compare match of MTU7.TADCORA and MTU7.TCNT, or compare match of MTU7.TADCORB and MTU7.TCNT 010000: Compare match of MTU7.TADCORA and MTU7.TCNT, and compare match of MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used) 011101: Compare match of TMR0.TCORA and TMR0.TCNT 011110: Compare match of TMR2.TCORA and TMR2.TCNT 011111: Compare match/input capture of TPUn.TGRAn (n = 0 to 5) 100000: Compare match/input capture of TPU0.TGRA0 110000: Event linkage	
[7:6]	Reserved bits	

Table 5.9 DSTRGR Register of the RX65N Device (2/2)

Bit	Description	Remarks
[5:0]	Group-B dedicated A/D conversion start trigger select bits 111111: Trigger source not selected 000001: Compare match/input capture of MTU0.TGRA 000010: Compare match/input capture of MTU1.TGRA 000011: Compare match/input capture of MTU2.TGRA 000100: Compare match/input capture of MTU3.TGRA 000101: Compare match/input capture of MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode 000110: Compare match/input capture of MTU6.TGRA 000111: Compare match/input capture of MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode 001000: Compare match of MTU0.TGRE 001001: Compare match of MTU4.TADCORA and MTU4.TCNT 001010: Compare match of MTU4.TADCORB and MTU4.TCNT 001011: Compare match of MTU4.TADCORA and MTU4.TCNT, or compare match of MTU4.TADCORB and MTU4.TCNT 001100: Compare match of MTU4.TADCORA and MTU4.TCNT, and compare match of MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used) 001101: Compare match of MTU7.TADCORA and MTU7.TCNT 001110: Compare match of MTU7.TADCORB and MTU7.TCNT 001111: Compare match of MTU7.TADCORA and MTU7.TCNT, or compare match of MTU7.TADCORB and MTU7.TCNT 010000: Compare match of MTU7.TADCORA and MTU7.TCNT, and compare match of MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used) 011101: Compare match of TMR0.TCORA and TMR0.TCNT 011110: Compare match of TMR2.TCORA and TMR2.TCNT 011111: Compare match/input capture of TPUn.TGRAn (n = 0 to 5) 100000: Compare match/input capture of TPU0.TGRA0 110000: Event linkage	

5.7.2 H8SX/1668

On the H8SX/1668 device, the A/D conversion start trigger select register is not present. Trigger selection is performed by using the TRGS1, TRGS0, and EXTRGS bits of the ADCR register.

5.8 A/D Sampling State Register n: ADSSTRn (n = 0 to 15, L, T, or O)

5.8.1 RX65N

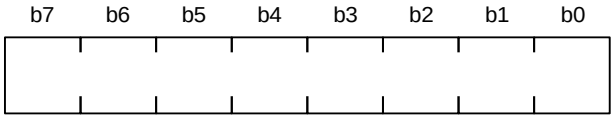

Table 5.10 ADSSTR Register of the RX65N Device

Bit	Description	Remarks
[7:0]	These bits are used to set the sampling time.	

The ADSSTRn register is used to set the sampling time of analog input.

If 1 state is the width of a single cycle of ADCLK (A/D conversion clock) where the clock speed of ADCLK is 60 MHz, 1 state = 16.7 ns. The initial value is 11 states. If the impedance of the analog input signal source is too high to secure a sufficient sampling time or the ADCLK clock is too slow, the sampling time can be adjusted. The lower limit of the sampling time that can be set differs depending on the frequency ratio of PCLK and ADCLK.

If the frequency ratio of PCLK to ADCLK is 1:0, 2:1, 4:1, or 8:1, set 5 or more states.

The relationships among the sampling time, ADSSTR, and ADCLK are as follows:

Sampling time = Value set in ADSSTRn (n = 0 to 15, L, T, or O) × ADCLK
(Initial value of ADSSTRn: 0Bh)

5.8.2 H8XS/1668

On the H8SX/1668 device, the A/D sampling state register is not present.

5.9 A/D Sample-and-Hold Circuit Control Register: ADSHCR

5.9.1 RX65N

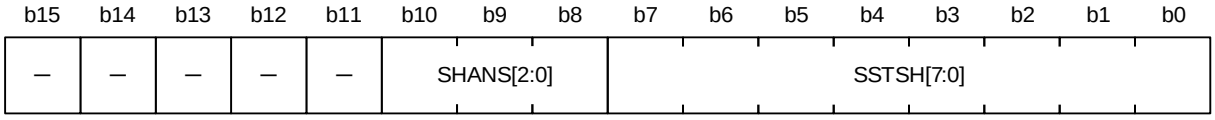

Table 5.11 ADSHCR Register of the RX65N Device

Bit	Description	Remarks
[15:11]	Reserved bits	
[10:8]	Channel-dedicated sample-and-hold circuit bypass select bits These bits are used to select whether the sample-and-hold circuits dedicated to channels AN000 to AN002 should be used or bypassed. 0: Bypasses the channel-dedicated sample-and-hold circuits. 1: Uses the channel-dedicated sample-and-hold circuits.	
[7:0]	Channel-dedicated sample-and-hold circuit sampling time setting bits These bits are used to set the sampling time in the range from 4 to 255 states.	

If 1 state is the width of a single cycle of the ADCLK clock (A/D conversion clock) where the clock speed of ADCLK is 60 MHz, 1 state = 16.7 ns. The initial value is 24 states. If the impedance of the analog input signal source is too high to secure a sufficient sampling time or the ADCLK clock is too slow, the sampling time can be adjusted. For the sampling time, set the number of states in the range from 4 to 255. Make sure that the resulting sampling time is at least 0.4 µs.

For example, when the ADCLK is operating at 60 MHz, at least 24 must be set as the number of sampling states.

The relationships among the sampling time, ADSSTR, and ADCLK are as follows:

Sampling time = Value set in ADSHCR.SSTSH[7:0] × ADCLK
(Initial value of ADSHCR.SSTSH[7:0]: 18h)

5.9.2 H8SX/1668

On the H8SX/1668 device, A/D sample-and-hold circuit control register is not present. This device provides an A/D converter with a sample-and-hold circuit.

5.10 A/D Sample-and-Hold Operating Mode Select Register: ADSHMSR

5.10.1 RX65N

b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	–	–	SHMD

Table 5.12 ADSHCR Register of the RX65N Device

Bit	Description	Remarks
[7:1]	Reserved bits	
0	Channel-dedicated sample-and-hold circuit operating mode setting bit 0: Disables continuous sampling of the channel-dedicated sample-and-hold circuit. 1: Enables continuous sampling of the channel-dedicated sample-and-hold circuit.	

5.10.2 H8SX/1668

On the H8SX/1668 device, the A/D sample-and-hold operating mode select register is not present. This device provides an A/D converter with a sample-and-hold circuit.

6. Usage Notes

6.1 RX Smart Configurator

On an RX-family device, RX Smart Configurator can be used when creating code for the A/D converter. With RX Smart Configurator, when a user selects or sets the function of the A/D converter from the GUI, the corresponding driver code is automatically generated. When you migrate to an RX-family device, we recommend that you use Smart Configurator.

6.2 I/O Register Macros

With new macros defined in the iodefine.h file for RX family members, the ICU control register, module stop register, DTC enable register, and interrupt vector numbers can easily be referenced by using the logical name associated with a peripheral module. These macros allow specific registers and vector numbers to be hidden, thus achieving migration between RX family members. For details, refer to the code contained in iodefine.h.

Table 6.1 Macro Usage Examples (if S12ADI is assigned to vector number 186)

Macro	Usage Example
IR(<module-name>, <bit-name>)	if (IR(PERIB, INTB186) == 1)…
IEN(<module-name>, <bit-name>)	IEN(PERIB, INTB186) = 1U;
IPR(<module-name>, <bit-name>)	IPR(PERIB, INTB186) = 0xF;
MSTP(<module-name>)	MSTP(S12AD) = 0U;
VECT(<module-name>, <bit-name>)	#pragma interrupt r_Config_S12AD0_interrupt(vect=VECT(PERIB,INTB186))

6.3 Polling to Check for the End of A/D Conversion

An H8SX device can wait until the ADF bit of the A/D control/status register is set to 1. This allows the device to stand by while checking for the end of A/D conversion. With this function, the software can perform polling to check for the end of A/D conversion without using interrupts.

The ADF bit is not present on the RX65N device. However, polling can be performed by using the following procedure.

- Set the ADIE bit of the ADCSR register to 1 to enable A/D interrupts for the A/D converter. As a result, the IR flag of the interrupt controller (ICU) becomes effective.
- For the ICU, do not enable A/D interrupts. (Make sure that the corresponding bit of the IER register is cleared.)
- Before A/D conversion starts, clear the interrupt request flag by writing “0” to the corresponding interrupt request register (IRn) of the ICU.
- Start A/D conversion.
- When A/D conversion ends, an interrupt request is sent to the ICU and the IR bit of the interrupt request register is set. No interrupt occurs.
- The software can wait until the IR bit is set to 1, which indicates that A/D conversion is completed and the conversion result is stored in the A/D data register (ADDRy).

The above procedure allows the software to perform polling to check for the end of A/D conversion without using the A/D conversion end interrupt.

6.4 Differences in the Timing of A/D Conversion Between the H8SX/1668 and RX65N

The A/D conversion speed is dictated by the following conditions.

1 Signal source impedance
2 A/D conversion clock (ADCLK) speed setting (for the RX65N) or peripheral clock (PCLK) speed setting (for the H8SX/1668)
3 Configuration settings of the ADC subsystem

When porting an application from the H8SX/1668 device to the RX65N device, the effects of the above conditions must be considered. Generally, as the peripheral clock speed increases, the conversion time decreases. As the conversion time decreases, the signal source impedance must be decreased accordingly.

For the H8SX/1668 device with the peripheral clock operating at a maximum of 35 MHz, conversion takes 2.7 µs per channel. For the RX65N device, the maximum frequency of ADCLK is 60 MHz. Because the clock frequency is higher and the internal capacitance of the ADC is reduced, the conversion of the RX65N device has been speeded up to 0.45 µs per channel in 10-bit conversion mode.

This improvement, however, requires that external signal conditioning circuitry meets certain design criteria. For the RX65N device, to achieve the conversion time of 0.45 µs per channel, the input signal source impedance must be 1 kΩ or less.

Table 6.2 Signal Source Impedances of the RX65N and H8SX/1668 Devices

Name	RX65N	H8SX/1668
Maximum peripheral clock	ADCLK: 60 MHz	PCLK: 35 MHz
Maximum conversion speed	0.48 µs/channel (12-bit conversion mode) 0.45 µs/channel (10-bit conversion mode) 0.42 µs/channel (8-bit conversion mode)	2.7 µs/channel
Maximum signal source impedance	1.0 kΩ	5.0 kΩ

As an alternative to modifying the signal conditioning circuitry driving the analog inputs, it is possible to adjust the RX65N's ADC timing through software so that legacy hardware remains unaffected. ADC timing may be adjusted by changing the Peripheral Clock (PCLK) base frequency, by using a post-scaled PCLK as the AD timing reference, and by changing the number of timing states that make up an ADC sample.

The base PCLK frequency is set in the system clock control register (SCKCR) of the clock generation circuit. The A/D sampling state register n (ADSSTRn) offers a final adjustment over the AD sampling time, allowing the sampling time to grow to accommodate higher impedance circuits or to shrink to account for slow PCLK settings.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 27, 2023	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.