RX65N, H8SX/1668

8-Bit Timer (TMR) Migration Guide: H8SX/1668 to RX65N

Introduction

This application note describes the differences between the 8-bit timer (TMR) modules for the RX65N and H8SX/1668 devices, respectively.

Target Devices

RX65N

H8SX/1668

Contents

1. Features

Table 1.1 shows the features of the TMR modules* of the RX65N and H8SX/1668 devices. Differences between the devices are shaded.

Table 1.1 Features of the 8-Bit Timer (1/2)

Item	Specifications	
	RX65N	**H8SX/1668**
Number of units	2	4
Number of channels per unit	2	
Total number of channels	4	8
Clock source	Units 0 and 1: • Internal clocks: PCLK, PCLK/2, PCLK/8, CLK/32, PCLK/64, PCLK/1024, and PCLK/8192 • External clock: External count clock	Units 0 and 1: • Internal clocks: Pφ/2, Pφ/8, Pφ/32, Pφ/64, Pφ/1024, and Pφ/8192 (Pφ: peripheral clock) • External clock: External count clock Units 2 and 3: • Internal clocks only: Pφ, Pφ/2, Pφ/8, Pφ/32, Pφ/64, Pφ/1024, and Pφ/8192 (Pφ: peripheral clock)
Compare match	8-bit mode and 16-bit mode	
Counter is cleared by	• Units 0 and 1: Compare match A, compare match B, or external reset signal	• Units 0 and 1: Compare match A, compare match B, or external reset signal • Units 2 and 3: Compare match A or compare match B
Timer output	Pulse or PWM output at a desired duty cycle	
Dual-channel cascade connection	16-bit counting mode: 16-bit timer using TMR0 for the upper bits and TMR1 for the lower bits (16 bits × 2 channels available). Compare match counting mode: TMR1 counts the compare matches of TMR0 (TMR3 counts the compare matches of TMR2).	16-bit counting mode: 16-bit timer using TMR_0 for the upper bits and TMR_1 for the lower bits (16 bits × 4 channels available). Compare match counting mode: TMR_1 counts the compare matches of TMR_0 (TMR_3 counts the compare matches of TMR_2).
Interrupt source	• Units 0 and 1: Compare match A, compare match B, or overflow	• Units 0 and 1: • Compare match A, compare match B, or overflow • Units 2 and 3: Compare match A or compare match B

Table 1.1 Features of the 8-Bit Timer (2/2)

Item	Specifications	
	RX65N	**H8SX/1668**
DTC activation	The DTC can be activated by a compare match A interrupt or compare match B interrupt.	• Units 0 and 1: The DTC can be activated by a compare match A interrupt or compare match B interrupt (for only units 0 and 1).
ADC activation trigger	Compare match A of TMR0/TMR2	Compare match A of TMR_0/TMR_2/TMR_4/TMR_6
SCI baud rate generation	The baud rate clock is generated for SCI5, SCI6, and SCI12.	The baud rate clock is generated for SCI5 and SCI6 (for units 2 and 3 only).
Event linkage function (output)	Compare match A, compare match B, or overflow (TMR0 to TMR3)	—
Event linkage function (input)	One of three operations can be performed upon acceptance of an event: (1) Count-start operation (TMR0 to TMR3) (2) Event-counter operation (TMR0 to TMR3) (3) Count-restart operation (TMR0 to TMR3)	—
Low power consumption	The module-stop state can be set for each unit.	

Note: * The RX65N does not have timer units 2 and 3, which the H8SX/1668 has. However, the RX65N has the TPU and MTU, which are upward-compatible timers. If more timers are necessary on the RX65N, use the TPU and/or MTU.

2. General Notes

- The peripheral clock provides the TMR's time base. The improved high-speed core of the RX65N allows the peripheral clock to run at speeds of up to 60 MHz. The maximum peripheral clock speed on the H8SX/1668 is 35 MHz.
- For an application to take advantage of the increased performance of the peripheral clock, the timer settings of the application must be adjusted accordingly. As a result of adjustment, the minimum and maximum allowable time delays may change.
- The clock source select bit and clock select bit on the RX65N are contained in the timer counter control register (TCCR). On the H8SX/1668, these bits are separately allocated to the TCCR and TCR registers.
- Local interrupt flag bits CMFA, CMFB, and OVF are no longer available. The equivalents of these flags are available with the software configurable interrupt B request register (PIBR) in the ICU (refer to section 7.2, "Polling to Check for a Timer Compare or Overflow").

3. References

- Hardware manual for the RX65N:
  R01UH0590EJ0230: RX65N Group, RX651 Group User's Manual: Hardware
- Software manual for the RX65N:
  R01US0071EJ0100: RX Family RXv2 Instruction Set Architecture User's Manual: Software
- RX-Family Device Application Note:
  R01AN2178EJ0110: RX Family Using the Exception Vector Table and Software Configurable Interrupts

(The latest versions of the above manuals are available on the Renesas website.)

3.1 Related Chapters in the Hardware Manual

- I/O Registers
  Shows a list of all registers.
- Clock Generation Circuit
  Provides details on how to set up the peripheral clocks used for the TMR.
- Low Power Consumption
  Provides details on the module stop control registers.
- Interrupt Controller (ICUB)
  Describes how to enable interrupts from the TMR to the interrupt controller.
- I/O Ports
  Provides details on the TMR-related port settings.
- Multi-Function Pin Controller (MPC)
  Describes the allocation of the TMR-related ports.
- 8-Bit Timer (TMR)
  Provides details on the TMR-specific registers and operating modes.
- Event Link Controller (ELC)
  Provides details on the TMR-related event link options.

The TMR not only can provide a basic timing function, but also can be used to generate the baud rate for the SCI and to sample the clock for the A/D converter. To use these functions, also refer to the following chapters:

- Serial Communications Interface (SCIg, SCIi, SCIh)
  Provides details on how to use the TMR to generate the baud rate.
- 12-Bit A/D Converter
  Provides details on how to use the TMR to adjust the converter trigger.

3.2 Related Registers

The following table lists the registers that are related to the operation of the 8-bit timer (TMR) of the RX65N.

Table 3.1 Registers Related to the Operation of the TMR

Name	Description	Chapter in the Hardware Manual
SYSTEM.SCKCR	System clock control register	Clock Generation Circuit
SYSTEM.MSTPCRA	Module stop control register A	Low Power Consumption
ICU.IRn	Interrupt request register	Interrupt Controller
ICU.IERm	Interrupt request enable register	
ICU.IPRr	Interrupt source priority register	
ICU.PIBRx	Software configurable interrupt B request register	
ICU.SLIBXRn	Software configurable interrupt B source select register Xn	
ICU.SLIBRn	Software configurable interrupt B source select register n	
ICU.SLIPRCR	Write-protection register for the software configurable interrupt source select register	
PORTx.PDR	Port direction register	I/O Ports
PORTx.PMR	Port mode register	
ELC.ELSRn	Event link setting register n	Event Link Controller
ELC.ELOPD	Event link option setting register D	
MPC.PWPR	Write protection register	Multi-Function Pin Controller
MPC.P0nPFS	P0n pin function control register	
MPC.P1nPFS	P1n pin function control register	
MPC.P2nPFS	P2n pin function control register	
MPC.P3nPFS	P3n pin function control register	
MPC.P5nPFS	P5n pin function control register	
MPC.PAnPFS	PAn pin function control register	
MPC.PBnPFS	PBn pin function control register	
MPC.PCnPFS	PCn pin function control register	
TMRn.TCNT	Timer counter	8-Bit Timer
TMRn.TCORA	Time constant register A	
TMRn.TCORB	Time constant register B	
TMRn.TCR	Timer control register	
TMRn.TCCR	Timer counter control register	
TMRn.TCSR	Timer control/status register	
TMRn.TCSTR	Timer count start register	

4. Hardware Details

Some timer channels present on the H8SX/1668 are not present on the RX65N.

Table 4.1 Timer Channels

Unit	Channel	Timer channel present?	
		RX65N	H8SX/1668
0	TMR0	Yes	Yes
	TMR1	Yes	Yes
1	TMR2	Yes	Yes
	TMR3	Yes	Yes
2	TMR4	No	Yes
	TMR5	No	Yes
3	TMR6	No	Yes
	TMR7	No	Yes

5. Summary of Differences of Registers

Table 5.1 lists the registers for the 8-bit timers of the RX65N and H8SX/1668 devices. A register set consisting of 6 registers is provided for each timer channel. The registers modified on the RX65N are shaded in the table. For details on the modified registers, refer to the relevant sections in this chapter.

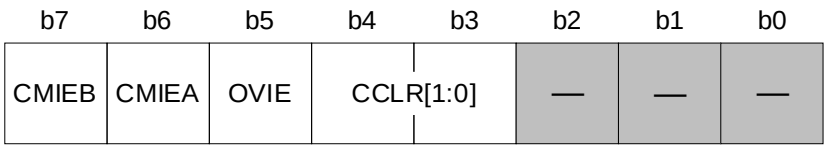
Table 5.1 TMR Registers

Register Name	Symbolic Name
Timer counter	TCNT
Time constant register A	TCORA
Time constant register B	TCORB
Timer control register	TCR
Timer counter control register	TCCR
Timer control/status register	TCSR
[New] Timer counter start register	TCSTR

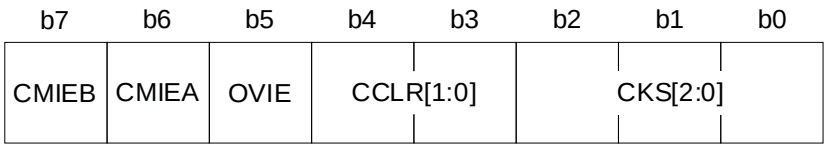
5.1 Changes to the Timer Control Register (TCR)

On the RX65N, the clock select bits CKS[2:0] have been moved to the TCCR register.

- TCR (for the RX65N)



- TCR (for the H8SX/1668)

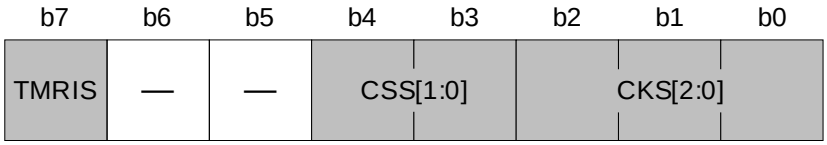


5.2 Changes to the Timer Counter Control Register (TCCR)

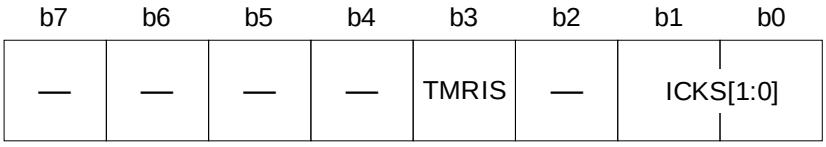
The TMRIS bit has been moved to b7.

The field named “ICKS” (internal clock select) has been renamed to “CCS” (clock source select).

- TCCR (for the RX65N)



- TCCR (for the H8SX/1668)

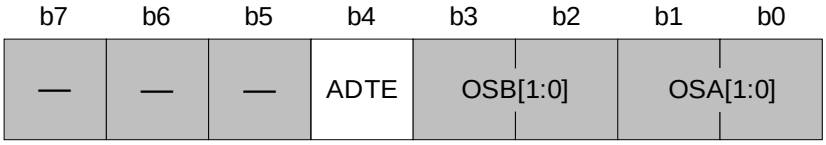


5.3 Changes to the Timer Control/Status Register (TCSR)

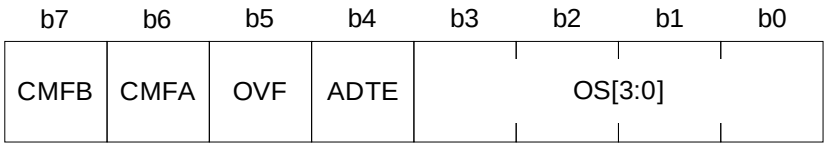
The compare A (CMFA), compare B (CMFB), and timer overflow flag (OVF) bits have been deleted. The equivalents of these bits are available with the software configurable interrupt B request register (PIBR) on the RX65N in the ICU. For details, refer to section 7.2, “Polling to Check for a Timer Compare or Overflow”.

The OS[3:0] field has been split into the OSB[1:0] and OSA[1:0] fields. The functionality has not been changed.

- TCSR (for the RX65N)



- TCSR (for the H8SX/1668)



6. Register Details

6.1 Timer Counter Register (TCNT)

The TCNT is an 8-bit read/write-enabled up-counter.

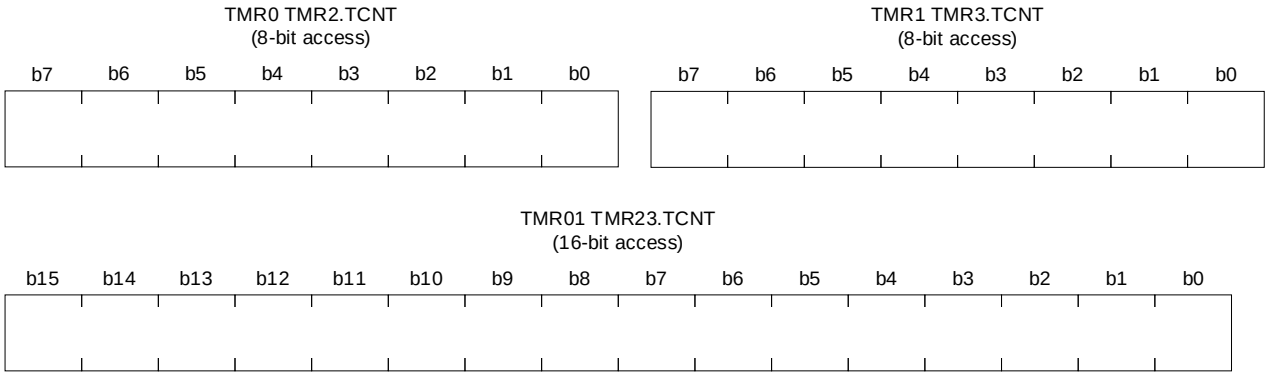
The TMR0.TCNT and TMR1.TCNT counters (or the TMR2.TCNT and TMR3.TCNT counters) can be combined into a single 16-bit counter that can be accessed by word.

- RX65N
  The TCCR.CSS[1:0] and CKS[2:0] bits are used to select the clock.
- H8SX/1668
  The TCR.CKS[2:0] and TCCR.ICKS[1:0] bits are used to select the clock.

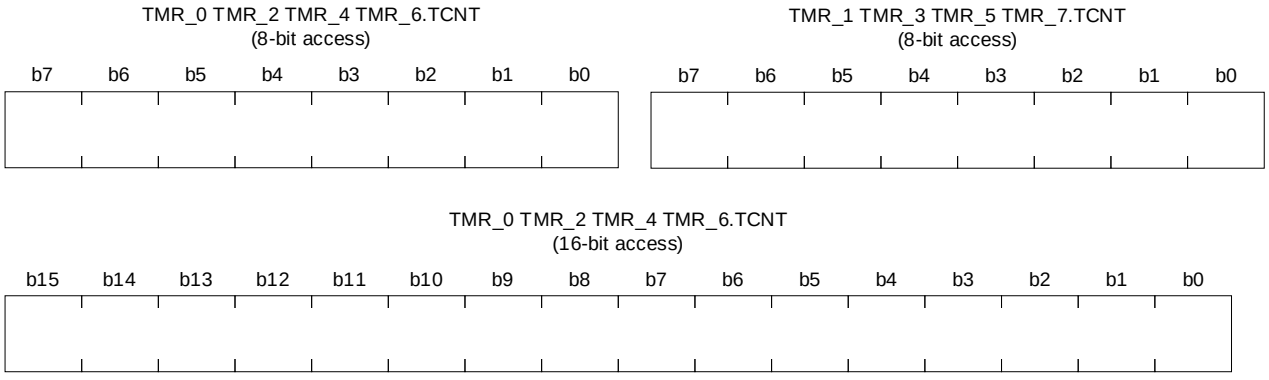
The TCNT can be cleared by an external reset input signal, compare match A signal, or compare match B signal. The signal used to clear the counter is selected by using the TCR.CCLR[1:0] bits.

- RX65N
  If TCR.OVIE is set, an interrupt flag is set in the interrupt controller (ICU) when the TCNT overflows (when the value changes from FFh to 00h).
- H8SX/1668
  The OVF bit of the TCSR register is set when the TCNT overflows (when the value changes from FFh to 00h).

6.1.1 RX65N



6.1.2 H8SX/1668



6.2 Time Constant Register A (TCORA)

The TCORA is an 8-bit read/write-enabled register.

The TMR0.TCORA and TMR1.TCORA registers (or the TMR2.TCORA and TMR3.TCORA registers) can be combined into a single 16-bit register that can be accessed by word.

The value of the TCORA register is continually compared with the value of the TCNT counter.

When a match is detected, the corresponding compare match A signal is set to 1. Note, however, that comparison is not performed during writing to the TCORA register. The timer output from the TMOn pin can be controlled by a combination of this compare match A signal and the TCSR register settings.

- RX65N
  The compare match state is stored in the ICU.PIBRx register of the timer (for this to happen, TCR.CMIEA must be set). For details, refer to section 7.2, “Polling to Check for a Timer Compare or Overflow”.
- H8SX/1668
  The compare match state is stored in TCSR.CMFA.

6.2.1 RX65N

TMR0 TMR2.TCORA
(8-bit access)

b7	b6	b5	b4	b3	b2	b1	b0

TMR1 TMR3.TCORA
(8-bit access)

b7	b6	b5	b4	b3	b2	b1	b0

TMR01 TMR23.TCORA
(16-bit access)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

6.2.2 H8SX/1668

TMR_0 TMR_2 TMR_4 TMR_6.TCORA
(8-bit access)

b7	b6	b5	b4	b3	b2	b1	b0

TMR_1 TMR_3 TMR_5 TMR_7.TCORA
(8-bit access)

b7	b6	b5	b4	b3	b2	b1	b0

TMR_0 TMR_2 TMR_4 TMR_6.TCORA
(16-bit access)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

6.3 Time Constant Register B (TCORB)

The TCORB is an 8-bit read/write-enabled register.

The TMR0.TCORB and TMR1.TCORB registers (or the TMR2.TCORB and TMR3.TCORB registers) can be combined into a single 16-bit register that can be accessed by word.

The value of the TCORB register is continually compared with the value of the TCNT counter.

When a match is detected, the corresponding compare match B signal is set to 1. Note, however, that comparison is not performed during writing to the TCORB register. The timer output from the TMOn pin can be controlled by a combination of this compare match B signal and the TCSR register settings.

- RX65N
  The compare match state is stored in the ICU.PIBRx register of the timer (for this to happen, TCR.CMIEB must be set). For details, refer to section 7.2, “Polling to Check for a Timer Compare or Overflow”.
- H8SX/1668
  The compare match state is stored in TCSR.CMFB.

6.3.1 RX65N

TMR_0 TMR_2.TCORB
(8-bit access)

b7	b6	b5	b4	b3	b2	b1	b0

TMR_1 TMR_3.TCORB
(8-bit access)

b7	b6	b5	b4	b3	b2	b1	b0

TMR_01 TMR_23.TCORB
(16-bit access)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

6.3.2 H8SX/1668

TMR_0 TMR_2 TMR_4 TMR_6.TCORB
(8-bit access)

b7	b6	b5	b4	b3	b2	b1	b0

TMR_1 TMR_3 TMR_5 TMR_7.TCORB
(8-bit access)

b7	b6	b5	b4	b3	b2	b1	b0

TMR_0 TMR_2 TMR_4 TMR_6.TCORB
(16-bit access)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

6.4 Timer Control Register (TCR)

6.4.1 RX65N

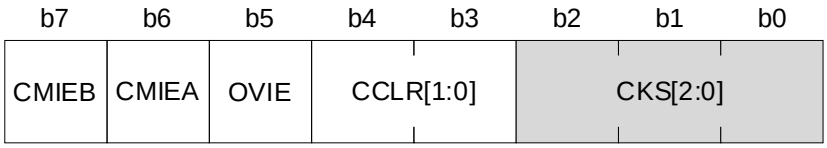
TMR0 TMR1 TMR2 TMR3.TCR

b7	b6	b5	b4	b3	b2	b1	b0
CMIEB	CMIEA	OVIE	CCLR[1:0]		—	—	—

Bit	Description
7	CMIEB: Compare match interrupt enable B bit 0: Disables issuance of an interrupt request by compare match B (CMIBn). 1: Enables issuance of an interrupt request by compare match B (CMIBn).
6	CMIEA: Compare match interrupt enable A bit 0: Disables issuance of an interrupt request by compare match A (CMIAn). 1: Enables issuance of an interrupt request by compare match A (CMIAn).
5	OVIE: Timer overflow interrupt enable bit 0: Disables issuance of an interrupt request by an overflow (OVIn). 1: Enables issuance of an interrupt request by an overflow (OVIn).
[4:3]	CCLR[1:0]: Counter clearing bits [1:0] 0 0: Disables clearing of the counter. 0 1: Clears the counter by compare match A. 1 0: Clears the counter by compare match B. 1 1: Clears the counter by an external counter reset signal. (Whether to use the edge or level is selected by using the TCCR.TMRIS bit.)
[2:0]	Reserved bits: 0 is always read. It is only permitted to write 0.

6.4.2 H8SX/1668

TMR_0 TMR_1 TMR_2 TMR_3
TMR_4 TMR_5 TMR_6 TMR_7.TCR

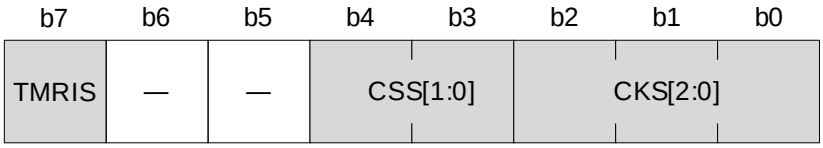


Bit	Description
7	CMIEB: Compare match interrupt enable B bit 0: Disables issuance of an interrupt request by CMFB (CMIB). 1: Enables issuance of an interrupt request by CMFB (CMIB).
6	CMIEA: Compare match interrupt enable A bit 0: Disables issuance of an interrupt request by CMFA (CMIA). 1: Enables issuance of an interrupt request by CMFA (CMIA).
5	OVIE: Timer overflow interrupt enable bit 0: Disables issuance of an interrupt request by OVF (OVI). 1: Enables issuance of an interrupt request by OVF (OVI).
[4:3]	CCLR[1:0]: Counter clearing bits 1 and 0 [1:0] 0 0: Disables clearing of the counter. 0 1: Clears the counter by compare match A. 1 0: Clears the counter by compare match B. 1 1: Clears the counter by the rising edge (if TCCR.TMRIS = 0) or the High level (if TCCR.TMRIS = 1) of the external reset input.
[2:0]	CKS[2:0]: Clock select bits 2 to 0 These bits are used to select the clock to be input to the TCNT and the counting conditions (refer to Table 6.2).

6.5 Timer Counter Control Register (TCCR)

6.5.1 RX65N

TMR0 TMR1 TMR2 TMR3.TCCR



Bit	Description
7	TMRIS: Timer reset detection condition select bit 0: Clears the counter by the rising edge of the external counter reset signal. 1: Clears the counter by the High level of the external counter reset signal.
[6:5]	Reserved bits: 0 is always read. It is only permitted to write 0.
[4:0]	CSS[1:0]: Clock source select bits CKS[2:0]: Clock select bits For details, refer to Table 6.1.

Table 6.1 Clock Input to the TCNT Counter and Counting Conditions (1/2)

Channel	TCCR register					Description
	CSS[1:0]		CKS[2:0]			
	B4	B3	B2	B1	B0	
TMR0 (TMR2)	0	0	—	0	0	Disables clock input.
					1	Counts by the rising edge of the external count clock.*1
				1	0	Counts by the falling edge of the external count clock.*1
					1	Counts by both the rising and falling edges of the external count clock.*1
	0	1	0	0	0	Internal clock: Counts at PCLK.
					1	Internal clock: Counts at PCLK/2.
				1	0	Internal clock: Counts at PCLK/8.
					1	Internal clock: Counts at PCLK/32.
			1	0	0	Internal clock: Counts at PCLK/64.
					1	Internal clock: Counts at PCLK/1024.
				1	0	Internal clock: Counts at PCLK/8192.
					1	Disables clock input.
	1	0	—	—	—	Setting prohibited
	1	1	—	—	—	Counts by the overflow signal for TMR1.TCNT (or TMR3.TCNT).*2

Table 6.1 Clock Input to the TCNT Counter and Counting Conditions (2/2)

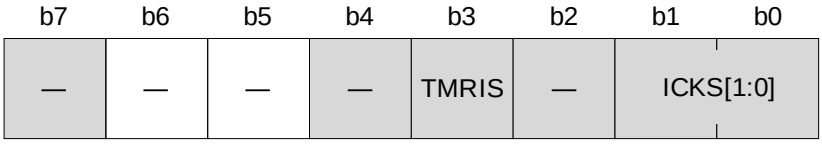
Channel	TCCR register					Description
	CSS[1:0]		CKS[2:0]			
	B4	B3	B2	B1	B0	
TMR1 (TMR3)	0	0	—	0	0	Disables clock input.
					1	Counts by the rising edge of the external count clock.*1
				1	0	Counts by the falling edge of the external count clock.*1
					1	Counts by both the rising and falling edges of the external count clock.*1
	0	1	0	0	0	Internal clock: Counts at PCLK.
					1	Internal clock: Counts at PCLK/2.
				1	0	Internal clock: Counts at PCLK/8.
					1	Internal clock: Counts at PCLK/32.
			1	0	0	Internal clock: Counts at PCLK/64.
					1	Internal clock: Counts at PCLK/1024.
				1	0	Internal clock: Counts at PCLK/8192.
					1	Disables clock input.
	1	0	—	—	—	Setting prohibited
	1	1	—	—	—	Counts by compare match A of TMR0.TCNT (or TMR2.TCNT).

Notes: 1. To use an external count clock, the corresponding pin settings must be specified. For details, refer to Chapter 22, “I/O Ports” and Chapter 23, “Multi-Function Pin Controller (MPC)”, in the manual “RX65N Group, RX651 Group User’s Manual: Hardware”.

2. It is impossible to set the CSS[1:0] bits to “11” in both the TMR0 and TMR1 registers (or in both the TMR2 and TMR3 registers).

6.5.2 H8SX/1668

TMR_0 TMR_1 TMR_2 TMR_3
TMR_4 TMR_5 TMR_6 TMR_7.TCCR



Bit	Description
[7:4]	Reserved bits
3	TMRIS: Timer reset input select bit 0: Clears the timer by the rising edge of the external reset signal. 1: Clears the timer by the High level of the external reset signal.
2	Reserved bits
[1:0]	ICKS[1:0]: Internal clock select bits 1 and 0 The ICKS[1:0] bits are used, together with the CKS[2:0] bits of the TCR register, to select the internal clock (refer to Table 6.2).

Table 6.2 H8SX/1668 Clock Input to the TCNT and Counting Conditions (Units 0 and 1)

Channel	TCR CKS[2:0] B2	B1	B0	TCCR ICKS[1:0] B1	B0	Description
TMR_0 (TMR_2)	0	0	0	—	—	Disables clock input.
	0	0	1	0	0	Internal clock: Counts by the rising edge at Pφ/8.
				0	1	Internal clock: Counts by the rising edge at Pφ/2.
				1	0	Internal clock: Counts by the falling edge at Pφ/8.
				1	1	Internal clock: Counts by the falling edge at Pφ/2.
	0	1	0	0	0	Internal clock: Counts by the rising edge at Pφ/64.
				0	1	Internal clock: Counts by the rising edge at Pφ/32.
				1	0	Internal clock: Counts by the falling edge at Pφ/64.
				1	1	Internal clock: Counts by the falling edge at Pφ/32.
	0	1	1	0	0	Internal clock: Counts by the rising edge at Pφ/8192.
				0	1	Internal clock: Counts by the rising edge at Pφ/1024.
				1	0	Internal clock: Counts by the falling edge at Pφ/8192.
				1	1	Internal clock: Counts by the falling edge at Pφ/1024.
	1	0	0	—	—	Counts by the overflow signal for TCNT_1 (or TCNT_3).*1
TMR_1 (TMR_3)	0	0	0	—	—	Disables clock input.
	0	0	1	0	0	Internal clock: Counts by the rising edge at Pφ/8.
				0	1	Internal clock: Counts by the rising edge at Pφ/2.
				1	0	Internal clock: Counts by the falling edge at Pφ/8.
				1	1	Internal clock: Counts by the falling edge at Pφ/2.
	0	1	0	0	0	Internal clock: Counts by the rising edge at Pφ/64.
				0	1	Internal clock: Counts by the rising edge at Pφ/32.
				1	0	Internal clock: Counts by the falling edge at Pφ/64.
				1	1	Internal clock: Counts by the falling edge at Pφ/32.
	0	1	1	0	0	Internal clock: Counts by the rising edge at Pφ/8192.
				0	1	Internal clock: Counts by the rising edge at Pφ/1024.
				1	0	Internal clock: Counts by the falling edge at Pφ/8192.
				1	1	Internal clock: Counts by the falling edge at Pφ/1024.
	1	0	0	—	—	Counts by compare match A of TCNT_0 (or TCNT_2).*1
All	1	0	1	—	—	Counts by the rising edge of the external clock.*2
	1	1	0	—	—	Counts by the falling edge of the external clock.*2
	1	1	1	—	—	Counts by both the rising and falling edges of the external clock.*2

Notes: 1. No count-up clock is generated if the clock input to channel 0 (or channel 2) is used as an overflow signal for TCNT_1 (or TCNT_3) and the clock input to channel 1 (or channel 3) is used as a compare match signal for TCNT_0 (or TCNT_2). Do not use these settings.

2. To use an external clock, set the bit of the DDR register for the corresponding pin to 0 and the bit of the ICR register to 1. For details, refer to the “I/O Ports” section in the data sheet.

Table 6.3 H8SX/1668 Clock Input to the TCNT and Counting Conditions (Units 2 and 3)

Channel	TCR CKS[2:0] B2	B1	B0	TCCR ICKS[1:0] B1	B0	Description
TMR_4 (TMR_6)	0	0	0	—	—	Disables clock input.
	0	0	1	0	0	Internal clock: Counts by the rising edge at Pφ/8.
				0	1	Internal clock: Counts by the rising edge at Pφ/2.
				1	0	Internal clock: Counts by the falling edge at Pφ/8.
				1	1	Internal clock: Counts by the falling edge at Pφ/2.
	0	1	0	0	0	Internal clock: Counts by the rising edge at Pφ/64.
				0	1	Internal clock: Counts by the rising edge at Pφ/32.
				1	0	Internal clock: Counts by the falling edge at Pφ/64.
				1	1	Internal clock: Counts by the falling edge at Pφ/32.
	0	1	1	0	0	Internal clock: Counts by the rising edge at Pφ/8192.
				0	1	Internal clock: Counts by the rising edge at Pφ/1024.
				1	0	Internal clock: Counts by the falling edge at Pφ/8192.
				1	1	Internal clock: Counts by the falling edge at Pφ/1024.
	1	0	0	—	—	Counts by the overflow of TMR_5 (or TMR_7).*1
TMR_5 (TMR_7)	0	0	0	—	—	Disables clock input.
	0	0	1	0	0	Internal clock: Counts by the rising edge at Pφ/8.
				0	1	Internal clock: Counts by the rising edge at Pφ/2.
				1	0	Internal clock: Counts by the falling edge at Pφ/8.
				1	1	Internal clock: Counts by the falling edge at Pφ/2.
	0	1	0	0	0	Internal clock: Counts by the rising edge at Pφ/64.
				0	1	Internal clock: Counts by the rising edge at Pφ/32.
				1	0	Internal clock: Counts by the falling edge at Pφ/64.
				1	1	Internal clock: Counts by the falling edge at Pφ/32.
	0	1	1	0	0	Internal clock: Counts by the rising edge at Pφ/8192.
				0	1	Internal clock: Counts by the rising edge at Pφ/1024.
				1	0	Internal clock: Counts by the falling edge at Pφ/8192.
				1	1	Internal clock: Counts by the falling edge at Pφ/1024.
	1	0	0	—	—	Counts by compare match A of TMR_4 (or TMR_6).*1
All	1	0	1	—	—	Setting prohibited
	1	1	0	—	—	Setting prohibited
	1	1	1	—	—	Setting prohibited

Note: 1. No count-up clock is generated if the clock input to channel 4 (or channel 6) is used as an overflow signal for TCNT_5 (or TCNT7) and the clock input to channel 5 (or channel 7) is used as a compare match signal for TCNT_4 (or TCNT_6). Do not use these settings.

6.6 Timer Control/Status Register (TCSR)

6.6.1 RX65N

TMR0 TMR2.TCSR

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	ADTE	OSB[1:0]		OSA[1:0]	

TMR1 TMR3.TCSR

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	OSB[1:0]		OSA[1:0]	

Bit	Description
[7:5]	Reserved bits: Undefined values are read. It is only permitted to write 1.
4	• TMR0 and TMR2 ADTE: A/D conversion trigger enable bit 0: Disables issuance of an A/D conversion start request by compare match A. 1: Enables issuance of an A/D conversion start request by compare match A. • TMR1 and TMR3 Reserved bit: 1 is always read. It is only permitted to write 1.
[3:2]	OSB[1:0]: Output select bits B [1:0] 0 0: Does not change the output level. 0 1: Selects the Low-level output. 1 0: Selects the High-level output. 1 1: Inverts (toggles) the output level.
[1:0]	OSA[1:0]: Output select bits A [1:0] 0 0: Does not change the output level. 0 1: Selects the Low-level output. 1 0: Selects the High-level output. 1 1: Inverts (toggles) the output level.

6.6.2 H8SX/1668

TMR_0 TMR_2 TMR_4 TMR_6.TCSR

b7	b6	b5	b4	b3	b2	b1	b0
CMFB	CMFA	OVF	ADTE	OS[1:0]		OS[1:0]	

TMR_1 TMR_3 TMR_5 TMR_7.TCSR

b7	b6	b5	b4	b3	b2	b1	b0
CMFB	CMFA	OVF	—	OS[1:0]		OS[1:0]	

Bit	Description
7	CMFB: Compare match flag B*1 [Setting condition] The TCNT and TCORB values match. [Clearing conditions] • CMFB is read while CMFB = 1, and then 0 is written to CMFB. (If the CPU uses an interrupt to clear the flag, make sure that the flag is read after 0 is written.) • The DTC is started by a CMIB interrupt when the DISEL bit of the MRB register for the DTC is 0.*3
6	CMFA: Compare match flag A*1 [Setting condition] The TCNT and TCORA values match. [Clearing conditions] • CMFA is read while CMFA = 1, and then 0 is written to CMFA. (If the CPU uses an interrupt to clear the flag, make sure that the flag is read after 0 is written.) • The DTC is started by a CMIA interrupt when the DISEL bit of the MRB register for the DTC is 0.*3
5	OVF: Timer overflow flag*1 Timer overflow flag [Setting condition] The TCNT overflows (the TCNT value changes from H'FF to H'00). [Clearing condition] OVF is read while OVF = 1, and then 0 is written to OVF. (If the CPU uses an interrupt to clear the flag, make sure that the flag is read after 0 is written.)
4	• TMR_0, TMR_2, TMR_4, and TMR_6 ADTE: A/D conversion trigger enable bit This bit is used to select whether to enable or disable issuance of an A/D conversion start request by compare match A. 0: Disables issuance of an A/D conversion start request by compare match A. 1: Enables issuance of an A/D conversion start request by compare match A. • TMR_1, TMR_3, TMR_5, and TMR_7 Reserved bit: 1 is always read. This bit cannot be modified.

Bit	Description
[3:2]	OS[1:0]: Output select bits 3 and 2*2 These bits are used to select the value output from the TMO pin by compare match B of TCORB and TCNT. [1:0] 0 0: Does not change the output value. 0 1: Selects output of “0”. 1 0: Selects output of “1”. 1 1: Inverts (toggles) the output value.
[1:0]	OS[1:0]: Output select bits 1 and 2*2 These bits are used to select the value output from the TMO pin by compare match A of TCORA and TCNT. [1:0] 0 0: Does not change the output value. 0 1: Selects output of “0”. 1 0: Selects output of “1”. 1 1: Inverts (toggles) the output value.

Notes: 1. It is only permitted to write 0 in order to clear the flag.
2. Timer output is prohibited if all of bits OS3 to OS0 are 0. After a reset occurs, 0 is output as the timer output value until the first compare match occurs.

6.7 Timer Count Start Register (TCSTR)

6.7.1 RX65N

TMR0 TMR1 TMR2 TMR3.TCSTR

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	TCS

Bit	Description
[7:1]	Reserved bits: Undefined values are read. It is only permitted to write 0.
0	TCS: Timer counter status bit 0: The counter was stopped by the event link controller (ELC). 1: The counter was started by the event link controller (ELC).

7. Usage Notes

7.1 RX Smart Configurator

On an RX-family device, RX Smart Configurator can be used when creating code for the TMR. With RX Smart Configurator, when a user selects or sets the TMR function from the GUI, the corresponding driver code is automatically generated. When you migrate to an RX-family device, we recommend that you use Smart Configurator.

7.2 Polling to Check for a Timer Compare or Overflow

An H8SX device can wait until the CMFB, CMFA, or OVF bit of the timer control/status register (TCSR) is set to 1. This allows the device to stand by while checking for timer events.

These bits are not present on the RX65N device. However, polling mode becomes available by using software configurable interrupt B*[1].

For polling mode to be available, first, use the following procedure to configure the interrupt settings:

- Set 0 for the IERm.IENj bit of the target software configurable interrupt to disable the interrupt request (for example, if the target interrupt is software configurable interrupt B, m is 10h to 19h and j is 0 to 7). (This step is unnecessary if the value of the bit has not been changed after a reset was performed.)
- Set the interrupt source number for the SLIBXRn register (n: 128 to 143) or the SLIBRn register (n: 144 to 207). For the numbers of the interrupt sources for software configurable interrupt B, refer to Table 15.3, “Interrupt Sources for Software Configurable Interrupt B”, in the hardware manual for the RX65N.
- To use a software configurable interrupt as a trigger to activate the EXDMAC, set values for the bits of the SELEXDR register as described below.
- Set the SLIPRCR.WPRC bit to “1” so that writing to SLIBXRn or SLIBRn is disabled.
- Select the interrupt request destination (CPU, DTC, or DMAC). For details on the configuration procedure, refer to section 15.7.3.1, “Interrupt Request Destination Setting Procedure”, in the manual “RX65N Group, RX651 Group User’s Manual: Hardware”.
- Set the IRn.IR flag to “0” (for example, if the target interrupt is software configurable interrupt B, n is 128 to 207).
- Set the IERm.IENj bit to “1” to enable the interrupt request.

Then, use the following procedure to perform polling to check for interrupt requests by referencing the PIRj flag of the PIBKk register:

- Write “1” to the PIRj flag of the polling-target PIBRk register to clear the flag.*[2]
- Set the CMIEB, CMIEA, and OVIE bits of the TCR register to enable the timer compare or overflow interrupts.
- Read the PIRj flag of the PIBRk register at appropriate intervals to check the value.
- To clear a PIRj flag of a PIBRk register, write “1” to the flag.*[2]
- Repeat read and clear operations for the necessary PIRj flags subsequently.

Notes: 1. For a software configurable interrupt, one of the interrupt vector numbers 128 to 255 can be assigned any one of interrupt sources for multiple peripheral modules. These interrupt sources are categorized into those for software configurable interrupt B and those for software configurable interrupt A, according to the operating clocks of the peripheral modules. TMR compare matches and overflows are categorized into the interrupt sources for software configurable interrupt B.

2. Do not use bit-manipulation instructions. Using bit-manipulation instructions may cause multiple status flags to be cleared. To clear a flag, write “1” to the flag and write “0” to all other flags on a byte basis.

7.3 Difference in the Operating Frequency Between the H8SX/1668 and RX65N

The RX65N can operate at a higher peripheral clock frequency than the H8SX/1668 can operate. The peripheral clock (PCLK) is used to drive the TMR subsystem. If the PCLK frequency is changed, the settings must be changed for one or more of the following items:

- TCSR clock source select bit
- Timer constant registers (TCORA and TCORB)
- An interrupt handler designed to ensure that a timer interrupt is generated at a certain frequency

7.4 I/O Register Macros

With new macros defined in the iodefine.h file for RX-family devices, The ICU control register, module stop register, DTC enable register, and interrupt vector numbers can easily be referenced by using the logical name associated with a peripheral module. These macros allow specific registers and vector numbers to be hidden, thus achieving migration between RX-family devices. For details, refer to the document contained in iodefine.h.

Table 7.1 Macro Usage Examples (if CMIA is assigned to vector number 146)

Macro	Usage Example
IR(<module-name>, <bit-name>)	if (IR(PERIB, INTB146) == 1)
IEN(<module-name>, <bit-name>)	IEN(PERIB, INTB146) = 1;
IPR(<module-name>, <bit-name>)	IPR(PERIB, INTB146) = 0x02;
MSTP(<module-name>)	MSTP(TMR0) = 0;
VECT(<module-name>, <bit-name>)	#pragma interrupt r_Config_TMR0_cmia0_interrupt vect=VECT(PERIB,INTB146))

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 27, 2023	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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