RX64M Group, RX71M Group

Ethernet Hardware Design Guide

R01AN3342EJ0100
Rev.1.00
Nov 11, 2016

Summary

This application note describes precautions when designing boards that use the Ethernet functions of the RX64M Group and RX71M Group. Note that the information in this document is based on the corresponding information for the Ethernet communication board developed at Renesas for internal evaluation.

Target Devices

- RX64M Group 177/176-pin version ROM capacity: 2 MB to 4 MB
- RX71M Group 177/176-pin version ROM capacity: 2 MB to 4 MB

Contents

1. Board Design

1.1 Layer Structure

An RX64M or RX71M, as well as a physical layer chip (PHY-LSI), an SDRAM, etc. are mounted on the Ethernet communication board. Taking into consideration the large number of wiring patterns, the need for noise suppression for specific signals, the size of the board, and the like, the board was designed with a six-layer structure.

The layer structure of the Ethernet communication board is shown in Table 1. Note that, in order to perform noise suppression for specific signals*[1], layer L2 has been made the ground layer, and layer L5 has been made the power supply layer.

Note 1. Refers to the MII/RMII signals in Table 2 and the SDRAM address/data bus and control signals

Table 1 Ethernet Communication Board Layer Structure

Layer	Usage
L1	Component surface (signal layer)
L2	Ground layer
L3	Signal layer
L4	Signal layer
L5	Power supply layer
L6	Solder surface (signal layer)

Table 2 MII/RMII Signals

MII	RMII
ETn_TX_CLK	—
ETn_RX_CLK	REF50CKn
ETn_ERXD3 to ETn_ERXD0	RMIIn_RXD1 to RMIIn_RXD0
ETn_ETXD3 to ETn_ETXD0	RMIIn_TXD1 to RMIIn_TXD0

1.2 Component Layout

The component layout of the Ethernet communication board is shown in Figure 1, and precautions during layout are described below.

- The maximum SDCLK frequency of the SDRAM is 60 MHz, so when mounting the SDRAM, give priority to placing it in the vicinity of the RX64M/RX71M.
- Lay out the components such that the SDRAM data bus and the media independent interface (MII) or reduced media independent interface (RMII) signals (particularly ET1_RX_CLK on MII channel 1) are as short as possible and do not run alongside one another. In particular, be sure that the signal patterns of ET1_RX_CLK and D5/D6 (of the SDRAM data bus) do not run parallel to one another. (See Figure 1.)
- Lay out the components such that other lines do not run alongside the data bus and the MII or RMII signals either.

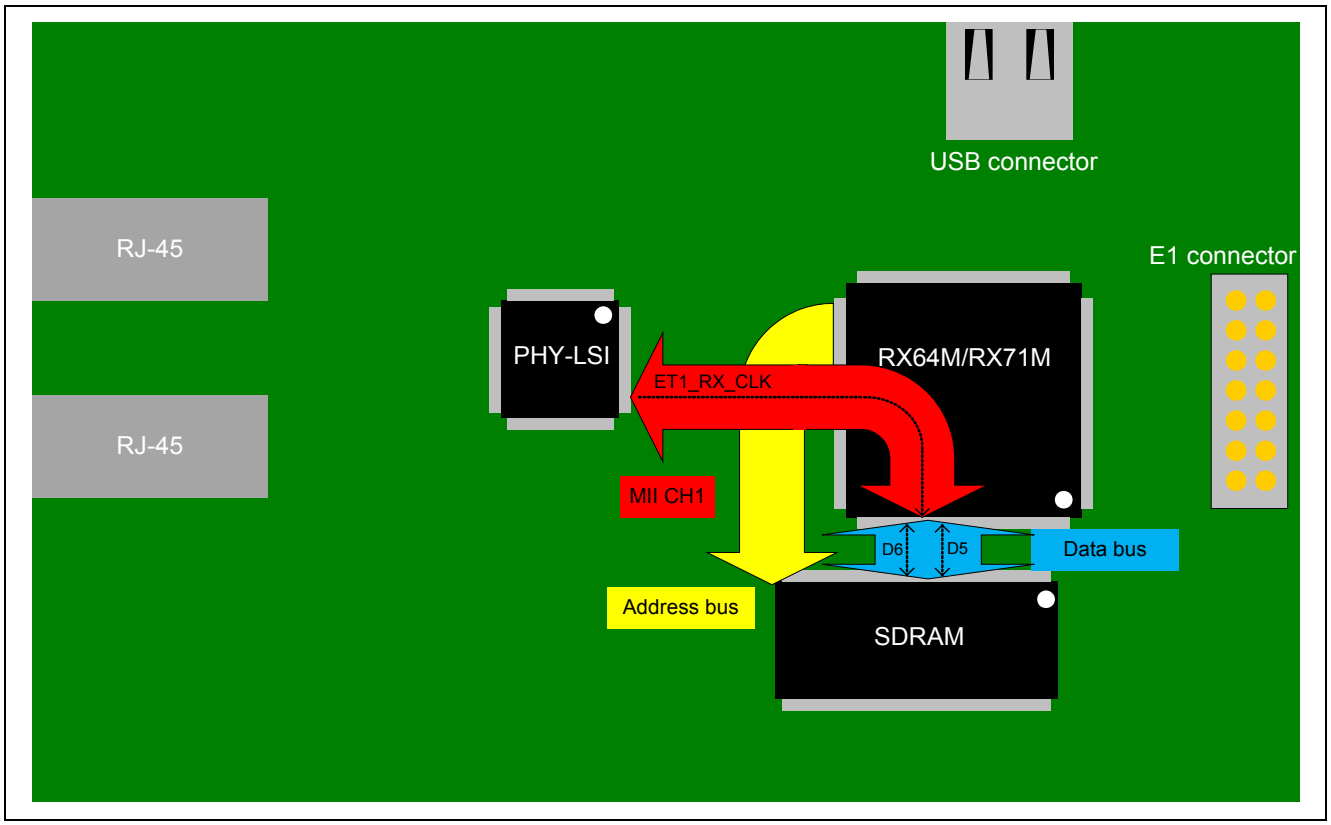


Figure 1 Component Layout

1.3 Pattern Design

1.3.1 MII/RMII/SDRAM Signal Patterns

The following are some precautions for when designing MII, RMII, and SDRAM signal patterns. Note that the MII and RMII signals in this section refer to the signals shown in Table 2.

1. Give priority to wiring D7 to D0 (particularly D5 and D6) of the data bus of the SDRAM on layer L1, and to making it as short as possible. (See (1) in Figure 2.)
2. In order to allow the return current from the SDRAM and MII/RMII signals to readily return, make layer L2 the ground layer.
3. As a result of having given priority to D7 to D0 of the data bus of the SDRAM, it will not be possible to wire the MII signals (particularly ET1_RX_CLK) on layer L1 alone. For this reason, wire it on layers L1 and L3 instead. Note that when layer L3 is used, the return current can readily return since the ground layer (layer L2) is immediately above. (See (2) in Figure 2.)
4. The components have been laid out with priority given to wiring D7 to D0 of the data bus of the SDRAM. As a result, it will not be possible to wire D15 to D8 of the data bus on layer L1 alone. For this reason, wire it on layers L1 and L3 instead. Note that when layer L3 is used, the return current can readily return since the ground layer (layer L2) is immediately above. (See (3) in Figure 2.)
5. As a result of having wired the SDRAM data bus and the MII signals on layers L1 and L3, it will not be possible to wire the SDRAM address bus on those layers. For this reason, wire it on layers L1 and L4 instead. (See (4) in Figure 2.)
6. Wire the signals other than those mentioned above on layer L6.
7. Design the inter-layer thicknesses, with the exception of that between layers L3 and L4, to be one-third the distance (H) between patterns running alongside one another (i.e., to be 1/3H) in order to allow return currents to readily return. (See Figure 3.) In addition, the inter-layer thickness affects impedance, so if there are signals subject to impedance control, take this into account when designing the board thicknesses. In the case of the Ethernet communication control board, based on impedance control and the board thicknesses that were possible for the board manufacturer that was asked to do the design, an inter-layer thickness of 0.1 mm was used, except for between layers L3 and L4.
8. Make the thickness between layers L3 and L4 substantial in order to prevent the effects of coupling. In the case of the Ethernet communication board, this thickness was decided by subtracting the inter-layer thickness between layers L1 and L3 and that between layers L4 and L6 from the board thickness. Given that the board thickness was 1.4 mm, an inter-layer thickness of 0.8 mm between layers L3 and L4 was used.
9. Design the distance between the SDRAM signal pattern and the MII/RMII signal pattern based on the 3W rule (i.e., a distance of at least 2W+α for a line width of W). (See Figure 4.)
10. Impedance control is necessary for the SDRAM and MII/RMII signals. Design the board with a characteristic impedance of 50Ω ±10%. In the case of the Ethernet communication board, a line width of 0.16 mm was used for layers L1 and L6, and a line width of 0.12 mm was used for layers L3 and L4.
11. When wiring the MII channel 1 signal from the RX64M/RX71M, avoid having the lines run alongside those of the SDRAM signals. In particular, be sure to lay out the patterns from the RX64M/RX71M such that the ET1_RX_CLK and D5 and D6 signals run in the opposite directions. (See Figure 5.)
12. Design the board such that, on the ground layer (power supply layer) along the return current path, there are no GND (power supply) slits or ground (power supply) separations. (See Figure 6.)

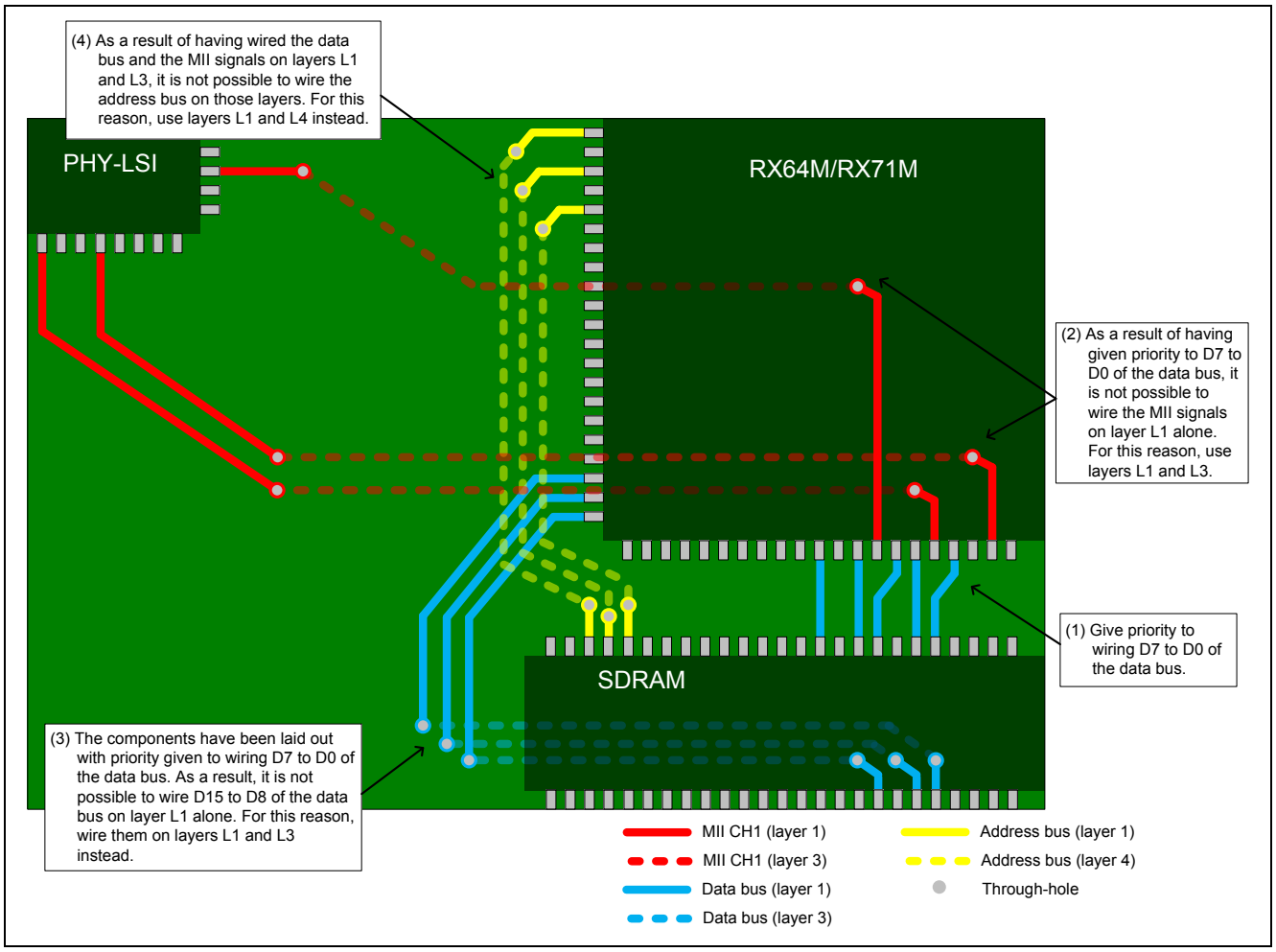


Figure 2 Pattern Layout Image (Transparency Diagram from Perspective of Layer L1)

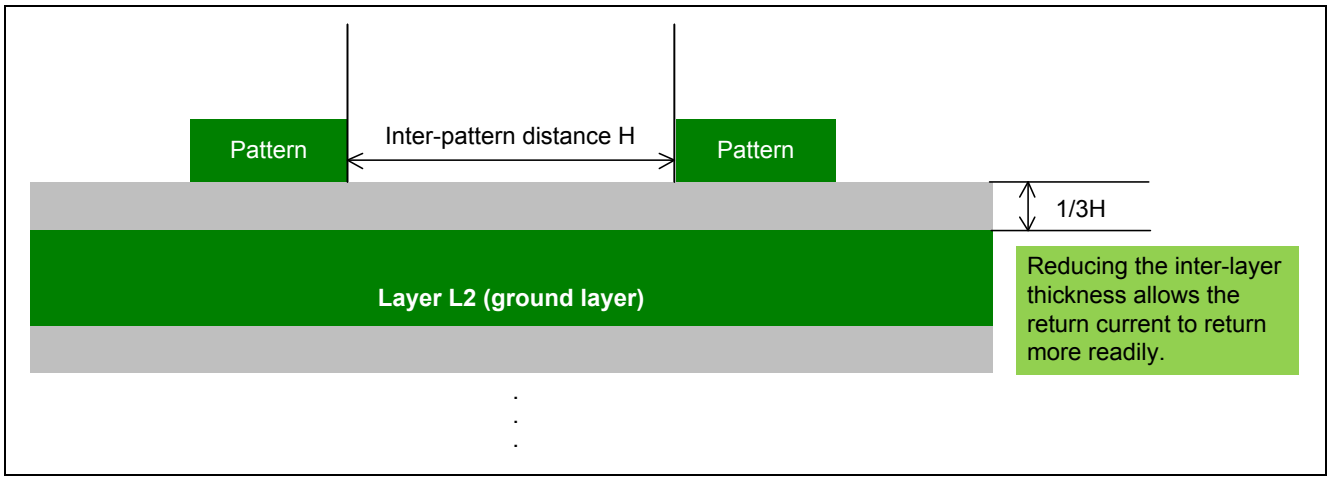


Figure 3 Return Current (Inter-layer Distance)

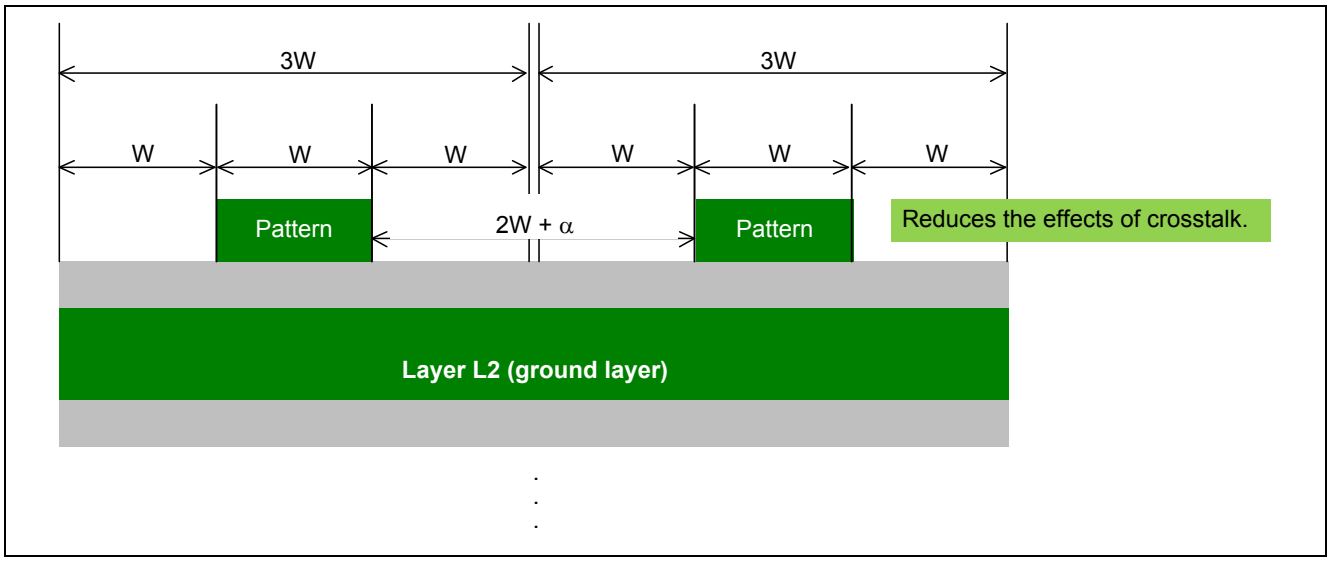


Figure 4 The 3W Rule

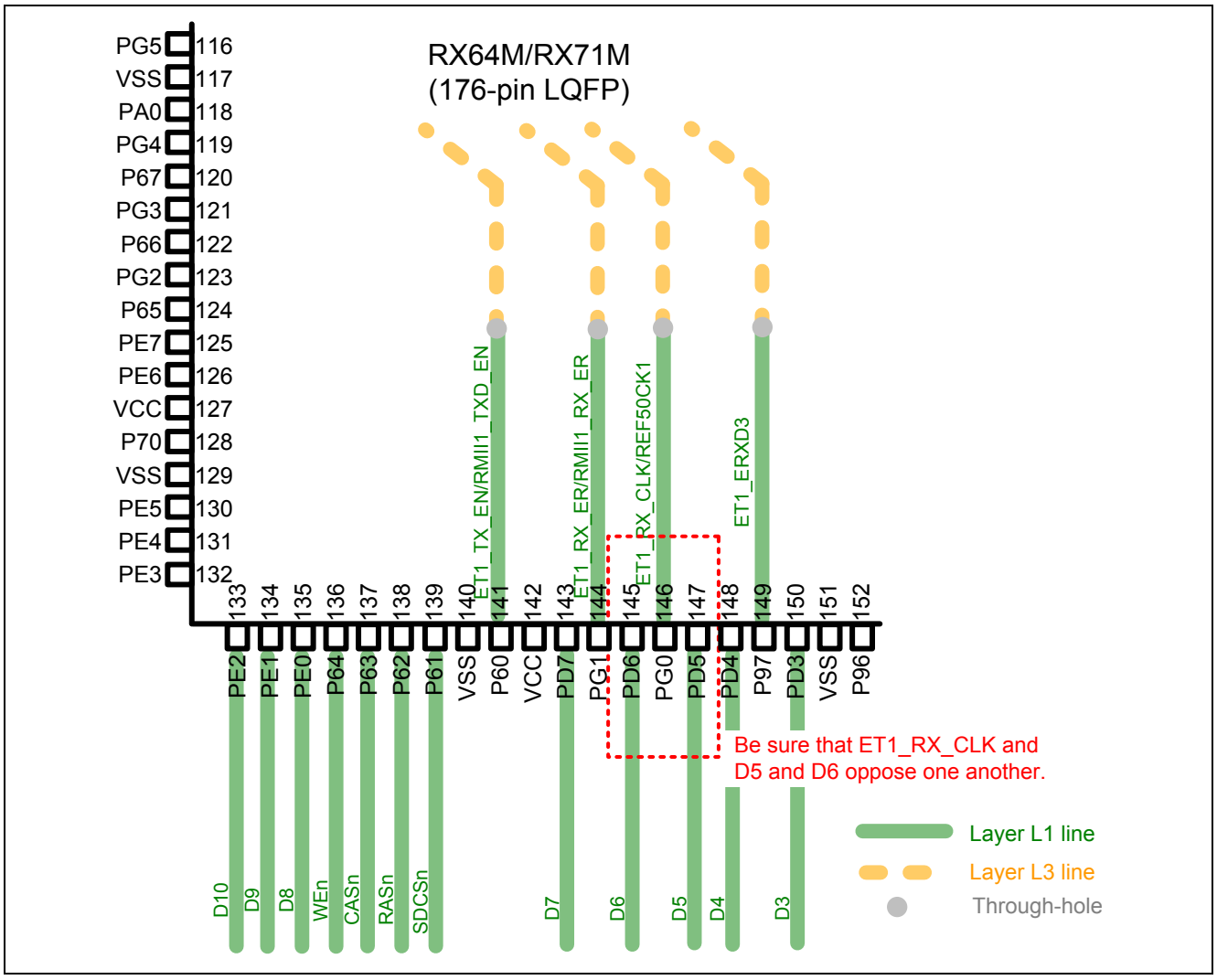
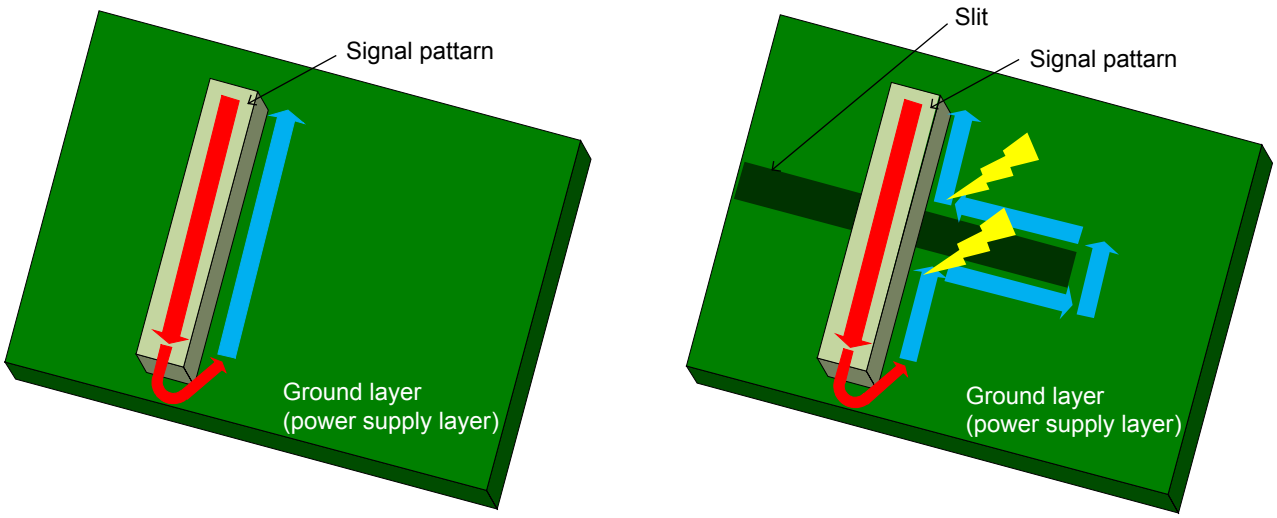


Figure 5 Wiring Example



(a) If there are no obstructions on the return current path, disturbances will not arise in the magnetic field and noise will be suppressed

(b) If there are obstructions on the return current path, the magnetic field will be disturbed and noise will arise due to the presence of slits and separations

Figure 6 Return Current (Facilitated by Ground Layer)

1.3.2 MDI Signals

The following are some precautions for when designing patterns for the media dependent interface signal (MDI signal).

- Do not place the MDI signal lines near any other signals (both on the same layer and on different layers).
- Make the MDI signal lines as short as possible.
- Impedance control is necessary for the MDI signals. For the characteristic impedance required by the MDI transmission path, follow the guidelines of the manufacturer of the PHY chip being used.
- Make all differential signals isometric using differential pairs.
- Lay out components on the MDI signals such that the differential pairs are symmetric. (See Figure 7.)
- Lay out the termination network in accordance with the guidelines of the hardware manufacturer.

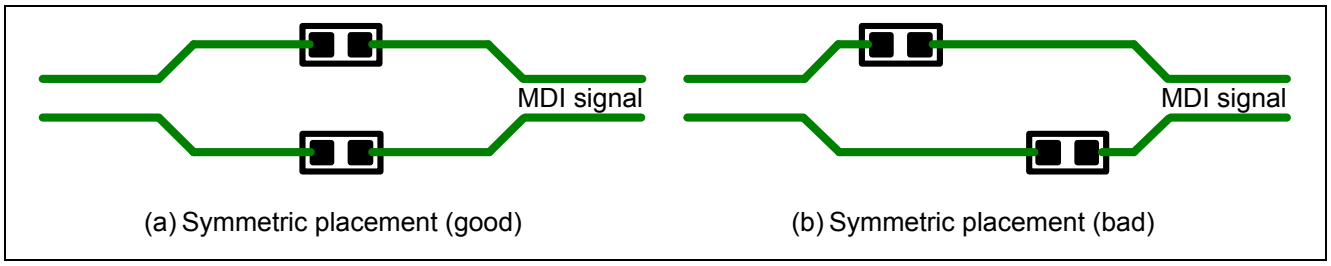


Figure 7 Layout of Components on Differential Signal Transmission Paths

2. Board Specifications

The following are the board specifications for the Ethernet communication board developed in accordance with this guide.

- Board layers: 6
- Board thickness: 1.43 mm
- Per-layer signal details:
  Layer L1 Ethernet signals (MII/RMII/MDI), data bus,*1 address bus,*1 strobe signal*1
  Layer L2 Ground layer
  Layer L3 Ethernet signals (MII/RMII), data bus,*1 strobe signal*1
  Layer L4 Power supply, address bus*1
  Layer L5 Power supply layer
  Layer L6 Ethernet signals (MDI), strobe signal*1

Note 1. SDRAM signals

- Pattern specifications
  — Normal pattern width is 0.15 mm.
  — Pattern width of specific MII/RMII/SDRAM signals that are noise-suppressed is 0.16 mm for layers L1 and L6, and 0.12 mm for layers L3 and L4.
  — Pattern width of specific MDI signals that are noise-suppressed is 0.1 mm.

- Layer structure:

Layer	Thickness (mm)	Material
1	0.025	Copper plating
	0.018	Copper foil
	0.100	Prepreg
2	0.035	Copper foil
	0.100	Core material
3	0.035	Copper foil
	0.800	Prepreg
4	0.035	Copper foil
	0.100	Core material
5	0.035	Copper foil
	0.100	Prepreg
6	0.018	Copper foil
	0.025	Copper plating

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Nov. 11, 2016	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.
   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 5.0