RX63T Group, RX24T Group, RX24U Group

Migrating from the RX63T Group to the RX24T Group or RX24U Group

R01AN4020EJ0100
Rev.1.00
Oct 17, 2017

Summary

This application note describes guidelines for migrating microcontroller code from the RX63T Group to the RX24T Group or RX24U Group.

Information is included for comparing specifications and confirming points of difference between microcontrollers in the RX63T Group and in the RX24T Group or RX24U Group with the package pin count indicated below.

100-pin package

The RX24T Group is available in two versions: A and B. The differences between these versions are summarized below. (Version B is available in a 100-pin package only.)

Function			Version B	Version A
Memory	ROM		256 KB/384 KB/512 KB	128 KB/256 KB
	RAM		32 KB	16 KB
Multi-function pin controller		MTU inverted I/O	Yes	No
Timer	Port output enable 3 • Version B: POE3A • Version A: POE3b		High-impedance control for MTU3 and GPT output pins	High-impedance control for MTU3 output pin
		I/O port switching control	Yes	No
		Independent setting of comparator sources	Yes	No
	GPT		16-bit × 4 channels	No
Communication	RSCAN		1 channel	No
Comparator		External reference voltage	No	CVREFC0 or CVREFC1 pin
		Internal reference voltage	DA0 or DA1 output selectable	Comparator C dedicated D/A converter
8-bit D/A			2 channels	1 channel
		External output	Yes	No (dedicated comparator C reference voltage generator)

The description of the RX24T Group contained in this application note applies mainly to version B.

This application note provides guidelines for smooth migration from the RX63T Group to the RX24T Group or RX24U Group. It does not cover all the details of the differences in the specifications of the above products.

Refer to the User's Manual: Hardware of each of the above products when migrating program code.

Target Devices

RX63T Group, RX24T Group, and RX24U Group

When not otherwise indicated, descriptions refer to the 100-pin package version of the RX63T Group, RX24T Group, and RX24U Group. The RX63T Group is available in a version equipped with an optional CAN module.

Contents

1. Overview for Migration Design

Compared to the RX63T Group, the RX24T Group and RX24U Group incorporate improvements that increase processing power and reduce power consumption.

There are some points to keep in mind about hardware and software when migrating from the RX63T Group to the RX24T Group or RX24U Group.

Section 2, Notes on the Pin Design describes notes on hardware. Section 3, Notes on the Function Settings describes notes on software.

2. Notes on the Pin Design

The range of frequencies to which the XTAL and EXTAL pins can be connected differs on the RX24T Group and RX24U Group. Notes on 100-pin package versions are presented below. For notes on 144-pin and 64-pin packages, refer to the tables listing the differences in pin functions and the differences in power supply, clock, and system control pins for the respective package pin counts in 4.2, Points of Difference between Pin Functions.

2.1 Main Clock Oscillator

On the RX24T Group and RX24U Group an oscillator (ceramic resonator or crystal oscillator) with an oscillation frequency of 1 MHz to 20 MHz may be connected to the EXTAL or XTAL pin. (This covers the entire allowable oscillation frequency range of the RX63T Group, which is 8 MHz to 12.5 MHz.)

In the crystal oscillator connection examples for the RX63T Group and for the RX24T Group and RX24U Group, the capacitor and damping resistor reference values differ. For detailed information on connecting a crystal oscillator, refer to the User's Manual: Hardware of the RX24T Group and of the RX24U Group, which are listed in 5, Reference Documents.

2.2 PLL Circuit Power Supply Pin

The RX63T Group has a dedicated power supply pin for the PLL circuit, but on the RX24T Group and RX24U Group no such pin is provided.

2.3 VCL Pin (External Capacity)

On the RX24T Group and RX24U Group, connect a 4.7μF smoothing capacitor to the VCL pin for internal power supply stabilization.

2.4 General I/O Ports

Note that on the RX63T Group port 4 is an AVCC0-dependent input port and ports 5 and 6 are AVCC-dependent input ports, but on the RX24T Group and RX24U Group P40 to P43 are AVCC0-dependent I/O ports, P44 to P47 are AVCC1-dependent I/O ports, and ports 5 and 6 are AVCC2-dependent I/O ports. If these pins will not be used, either set them to input and connect each to the pin corresponding to the target port (AVCC0, AVCC1, or AVCC2) via a resistor (pull-up), or connect each to the pin corresponding to the target port (AVSS0, AVSS1, or AVSS2) via a resistor (pull-down).

2.5 Comparator

The RX63T Group integrates comparator functionality into the 12-bit A/D converter, but the 12-bit A/D converter of the RX24T Group and RX24U Group does not include comparator functionality. Comparator C can be used instead. To accomplish this, use CMPCnm (n = channel number, m = 0 to 3) for analog input.

In addition, on the RX63T Group it is possible to select between using pin input (low side: AN003/CVREFL, high side: AN103/CVREFH) and using an internal voltage source (1/8 × AVCC0 to 7/8 × AVCC0) for reference voltages. On the RX24T Group and RX24U Group, in contrast, the reference voltage source is selectable between the output of on-chip D/A converter 0 and the output of on-chip D/A converter 1. Note that on version A of the RX24T Group either the input on the CVREFC0 or CVREFC1 pin or the output of on-chip D/A converter 0 may be selected as the reference voltage source.

2.6 Inputting an External Clock

On the RX63T Group it is permissible to input on the XTAL pin a signal that is the antiphase of the external clock signal input on the EXTAL pin. On the RX24T Group and RX24U Group, however, this is not allowed. Keep this in mind when designing your system.

When inputting an external clock to the RX24T Group or RX24U Group, it is necessary to set the main clock oscillator switch bit (MOSEL) in the main clock oscillator forced oscillation control register (MOFCR) to 1.

3. Notes on the Function Settings

Points related to function settings that differ between the RX63T Group and the RX24T Group and RX24U Group, which should be kept in mind when writing software, are touched on below.

For details on points of difference in modules and functions, see 4.3, Points of Difference between Modules and Functions.

When making use of this application note, make sure to perform thorough evaluation on the target system.

3.1 Memory Wait Cycle

RX24T Group and RX24U Group microcontrollers have a memory wait cycle setting register (MEMWAIT), but RX63T Group microcontrollers do not. To select a high-speed ICLK clock frequency of 32 MHz or higher on the RX24T Group or RX24U Group, set the MEMWAIT bits to 01b (wait states (ICLK ≤ 64 MHz)) or 10b (wait states (ICLK ≤ 80 MHz)). For details, refer to the User's Manual: Hardware of the RX24T Group and of the RX24U Group, which are listed in 5, Reference Documents.

3.2 Low Power Consumption

Change deep software standby mode in the RX63T Group to software standby mode in the RX24T Group and RX24U Group. Current consumption of software standby mode is equal to that of deep software standby mode.

Change all-module clock stop mode in the RX63T Group to deep sleep mode in the RX24T Group and RX24U Group. Current consumption of deep sleep mode is equal to that of all-module clock stop mode.

3.3 Comparator

The RX63T Group integrates comparator functionality into the 12-bit A/D converter, but the 12-bit A/D converter of the RX24T Group and RX24U Group does not include comparator functionality. Comparator C can be used instead.

3.4 Supplemental Information on RAM Self-Diagnostics

The RX24T Group and RX24U Group provide a buffer to enable fast access between the RAM and CPU. When a write to RAM is followed by a read access to the same address, the data may be read not from the RAM but from the buffer in some cases. Such read and write operations present no problems in a buffered configuration, but programs that expect to actually read from the RAM the previously written data (for example, software that performs self-diagnostics on on-chip RAM) may not operate as expected (because the data is read from the buffer instead).

To ensure that data is actually read from the RAM, do the following.

When reading data from an address in RAM aligned with a 4-byte boundary*[1] after a write to RAM completes, first perform a write to another address that is different from that address aligned with a 4-byte boundary that you wish to read, then start the read from the desired address in RAM.

Note 1. An address aligned with a 4-byte boundary refers to an address whose lowest two bits have a value of 00b to 11b.

3.5 Flash Memory

The programming and erase time and unit for the flash memory in the RX63T Group differ from those for the flash memory in the RX24T Group or RX24U Group. Therefore, software that performs self-programming in single-chip mode will require changes.

On the RX63T Group programming and erasing of the flash memory is accomplished by issuing commands to the FCU, which is a dedicated sequencer. On the RX24T Group and RX24U Group, in contrast, programming and erasing of the flash memory is accomplished by first transitioning to the dedicated sequencer mode for programming and erasing the ROM and then issuing software commands.

Table 3.1 compares the specifications of FCU commands and software commands.

Table 3.1 Comparison of FCU Command and Software Command Specifications

Item	FCU Command (RX63T)	Software Command (RX24T and RX24U)
Command issue area	Program/erase address (00F8 0000h to 00FF FFFFh)	Program/erase address (FC18 0000h to FC1F FFFFh)
Usable commands	• Transition to program/erase normal mode • Transition to status read mode • Transition to lock bit read mode • Peripheral clock notify • Program • Block erase • Program/erase suspend • Program/erase resume • Status register clear • Lock bit read 2 • Program lock bit • Blank check	• Program • Block erase • All-block erase • Blank check • Program startup area information • Program access window information

4. Points of Difference

4.1 Points of Difference between Specifications in Outline

Table 4.1 lists points of difference between the specifications of the RX63T Group and of the RX24T Group and RX24U Group in outline. The specifications of 100-pin package products are listed. The number of channels of each peripheral module varies with the pin count of the package.

Specifications that apply only to one group or the other are indicated in blue. Specifications that are different between groups are indicated in red. Specifications that apply to both groups are indicated in black.

Table 4.1 Points of Difference between Specifications in Outline

Item		RX63T	RX24T RX24U
CPU	Central processing unit	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Min. instruction execution time: 1 clock cycle per instruction • Address space: 4 GB, linear addressing • Register 16 general-purpose registers (32 bits) 9 control registers (32 bits) 1 accumulator (64 bits) • Basic instructions: 73 • 8 floating-point instructions • 9 DSP instructions • 10 addressing modes • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • 32-bit multiplier: 32-bit × 32-bit → 64 bits • Divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits —	• Maximum operating frequency: 80 MHz • 32-bit RX CPU (RXv2) • Min. instruction execution time: 1 clock cycle per instruction • Address space: 4 GB, linear addressing • Register 16 general-purpose registers (32 bits) 10 control registers (32 bits) 2 accumulators (72 bits) • Basic instructions: 75, variable instruction length • 11 floating-point instructions • 23 DSP instructions • 11 addressing modes • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • 32-bit multiplier: 32-bit × 32-bit → 64 bits • Divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits • ROM cache: 2 KB (disabled by default)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard

Item		RX63T	RX24T RX24U
Memory	ROM	• ROM Capacity: 32, 48, 64, 256, 384, 512 KB	• ROM Capacity: (RX24T) 128, 256, 384, 512 KB (RX24U) 256, 384, 512 KB
		• 100 MHz, no-wait memory access	• 32 MHz or less: no-wait memory access 32 to 80 MHz: Wait states
		• 3 on-board programming modes Boot mode (SCI interface) — User boot mode Self-programming (single-chip mode)	• 3 on-board programming modes Boot mode (SCI interface) Boot mode (FINE interface) — Self-programming (single-chip mode)
		• Off-board programming (144-, 120-, 112-, and 100-pin versions only) Programming method: Programming using a parallel writer supported	• Off-board programming Programming using a compatible flash programmer supported
	RAM	• Capacity: 8, 24, 32, 48 KB	• Capacity: (RX24T) 16, 32 KB (RX24U) 32 KB
		• 100 MHz, no-wait memory access	• 80 MHz, no-wait memory access
	E2 DataFlash	• Data ROM capacity: 32, 8 KB • Program/erase cycles: 100,000 • Background operation (BGO) supported	• Data ROM capacity: 8 KB • Program/erase cycles: 1,000,000 • Background operation (BGO) supported
MCU operating mode		[144-, 120-, 112-, and 100-pin versions] Single-chip mode, On-chip ROM enabled extended mode, on-chip ROM disabled extended mode (software switchable) [46- and 48-pin versions] Single-chip mode	Single-chip mode — —

Item	RX63T	RX24T RX24U
Clock generation circuits	• Main clock oscillator • Low-speed on-chip oscillators — • PLL frequency synthesizer • IWDT-dedicated on-chip oscillator • Main clock oscillation stop detection: Yes • Clock frequency accuracy measurement circuit (CAC): Yes • Ability to independently set system clock (ICLK), peripheral module clock (PCLKA), peripheral module clock (PCLKB), AD clock (PCLKC), FlashIF clock (FCLK), and S12AD clock (PCLKD) • The CPU and system sections such as bus masters run in synchronization with the ICLK: 100 MHz max. • PCLKA synchronization of multi-function timer pulse unit 3 and general PWM timer: 100 MHz max. • PCLK synchronization of peripheral module: 50 MHz max. • FCLK synchronization of flash interface: 50 MHz max. • BCLK synchronization of devices connected to the external bus: 50 MHz max. • PCLKC synchronization of 10-bit A/D converter: 100 MHz max. • PCLKD synchronization of 12-bit A/D converter: 50 MHz max.	• Main clock oscillator • Low-speed on-chip oscillators • High-speed on-chip oscillators • PLL frequency synthesizer • IWDT-dedicated on-chip oscillator • Main clock oscillation stop detection: Yes • Clock frequency accuracy measurement circuit (CAC): Yes • Ability to independently set system clock (ICLK), peripheral module clock (PCLKA), peripheral module clock (PCLKB), FlashIF clock (FCLK), and S12AD clock (PCLKD) • The CPU and system sections such as bus masters run in synchronization with the ICLK: 80 MHz max. • PCLKA synchronization of MTU3 and GPT: Max. 80 MHz • PCLKB synchronization of peripheral modules other than MTU3 and GPT: Max. 40 MHz • The flash memory peripheral circuit runs in synchronization with the FCLK: 32 MHz max. — — • PCLKD synchronization of ADCLK of S12AD: Max. 40 MHz

Item	RX63T	RX24T RX24U
Resets	RES# pin reset Power-on reset Voltage monitoring reset Independent watchdog timer reset Watchdog timer reset Deep software standby reset Software reset	RES# pin reset Power-on reset Voltage monitoring reset Independent watchdog timer reset — — Software reset
Voltage detection	LVDA • Generation of internal reset or internal interrupt when VCC drops below voltage detection level (Vdet)	LVDAb • Generation of internal reset or internal interrupt when VCC drops below voltage detection level (Vdet) Voltage detection 0: Ability to select voltage from among 3 detection voltage levels Voltage detection 1: Ability to select voltage from among 9 detection voltage levels Voltage detection 2: Ability to select voltage from among 4 detection voltage levels
Low power consumption functions	• Module stop function • 4 low-power states: Sleep mode All-module clock stop mode Software standby mode Deep software standby mode —	• Module stop function • 3 low-power states: Sleep mode — Software standby mode — Deep sleep mode
Function for lower operating power consumption	Not available	Operating power control modes • High-speed operating mode • Middle-speed operating mode

Item	RX63T	RX24T	RX24U
Interrupt controller	• Peripheral function interrupts: 169 (max.) sources • External interrupts: 9 source (NMI, IRQ0 to IRQ7 pins)	• Interrupt vectors: 163 • External interrupts: 9 source (NMI, IRQ0 to IRQ7 pins)	• Interrupt vectors: 175 • External interrupts: 9 source (NMI, IRQ0 to IRQ7 pins)
	• Software interrupt: 1 source	—	—
	• Non-maskable interrupts: 6 source (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt)	• Non-maskable interrupts: 5 source (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, IWDT interrupt)	• Non-maskable interrupts: 5 source (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, IWDT interrupt)
	• 16 levels specifiable for the order of priority	• 16 levels specifiable for the order of priority	• 16 levels specifiable for the order of priority
External bus extension	• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 1 MB (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area selectable between 8-bit bus space and 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility	Not available	

Item		RX63T	RX24T	RX24U
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupt, peripheral function interrupt	Not available	
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupt, peripheral function interrupt • Chain transfer function	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupt, peripheral function interrupt • Chain transfer function	
I/O ports		144-, 120-, 112-, 100-, 64-, 48-pin • I/O: 81/72/69/57/39/25 • Input: 29/21/21/21/9/7 — • Open-drain outputs: 27/26/20/16/10/8 • Large-current output: 12/12/12/12/0/0 • 5-V tolerant: 0/0/0/0/39/25 • Pin states are always readable.	100-, 80-, 64-pin • I/O: 80/60/48 Input: 1/1/1 • Pull-up resistors: 80/64/48 • Open-drain outputs: 60/45/37 • Large-current output: 15/14/14 • 5-V tolerant: 2/2/2 • Pin states are always readable.	144-, 100-pin • I/O: 110/79 Input: 1/1 • Pull-up resistors: 110/79 • Open-drain outputs: 90/61 • Large-current output: 15/15 • 5-V tolerant: 2/2 • Pin states are always readable.
Multi-function pin controller		Capable of selecting the input/output function from multiple pins	Capable of selecting the input/output function from multiple pins	
Timers	Multi-function timer pulse unit 3	MTU3 • 16 bits × 8 channels • Support for max. 16 pulse I/O and 3 pulse input lines • Ability to select 8 among 10 count clocks (PCLKA/1, PCLKA/4, PCLKA/16, PCLKA/64, PCLKA/256, PCLK/1,024, MTCLKA, MTCLKB, MTCLKC, and MTCLKD) for each channel (7 count clocks for channel 1, 4 count clocks for channel 5, and 6 count clocks for channels 6 and 7)	MTU3d • 16 bits × 9 channels • Support for max. 28 pulse I/O and 3 pulse input lines • Ability to select among 14 count clocks (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLK/32, PCLK/64, PCLKA/256, PCLK/1,024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, and MTIOC1A) for each channel (11 count clocks for channels 1, 3, 4, 6, and 7, 12 count clocks for channel 2, and 10 count clocks for channel 5)	

Item		RX63T	RX24T RX24U
Timers	Multi-function timer pulse unit 3	• 35 general registers (Of these, 24 function as output compare and input capture registers.) • Counter clear operation (support for simultaneous clearing at compare match or input capture) • Writing synchronized with multiple timer counters (TCNT) • Counter-synchronous I/O with each register • Buffer operation • Operation with cascade connection • 38 interrupt sources • Automatic transfer of register data • Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronous PWM • Complementary PWM mode Non-overlapping waveform output for 3-phase inverter control Automatic dead time setting Ability to set PWM duty ratio to 0 to 100% Delayed A/D conversion request function Peak/trough interrupt skipping function Double buffer function • Reset-synchronous PWM mode 3-phase output of forward- and reverse-phase PWM waveforms with user-defined duty ratio • Phase counting mode • Dead time compensation counter function • A/D converter conversion start trigger generation • A/D conversion start skipping function —	• 43 general registers (Of these, 28 function as output compare and input capture registers.) • Counter clear operation (support for simultaneous clearing at compare match or input capture) • Writing synchronized with multiple timer counters (TCNT) • Counter-synchronous I/O with each register • Buffer operation • Operation with cascade connection • 45 interrupt sources • Automatic transfer of register data • Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronous PWM • Complementary PWM mode Non-overlapping waveform output for 3-phase inverter control Automatic dead time setting Ability to set PWM duty ratio to 0 to 100% Delayed A/D conversion request function Peak/trough interrupt skipping function Double buffer function • Reset-synchronous PWM mode 3-phase output of forward- and reverse-phase PWM waveforms with user-defined duty ratio • Phase counting mode • Dead time compensation counter function • A/D converter conversion start trigger generation • A/D conversion start skipping function • Digital filtering of input capture and external count clock pins

Item		RX63T	RX24T RX24U
Timers	Port output enable 3	POE3 • High-impedance control for MTU3 and GPT waveform output pins • Activation by 6 input pins: POE0, POE4, POE8, POE10, POE11, and POE12 • Activation by short-circuited output detection (detection of state in which PWM outputs are active level simultaneously) • Activation by oscillation stop detection, comparator detection, or software • Programmable addition of pins subject to output control	POE3A • MTU3 and GPT waveform output pin high-impedance/general I/O port switching control • Activation by 6 input pins: POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# • Activation by short-circuited output detection (detection of state in which PWM outputs are active level simultaneously) • Activation by oscillation stop detection, comparator detection, or software • Programmable addition of pins subject to output control
	General PWM timer	GPT • 16 bits × 8 channels — • Ability to select up-count or down-count (sawtooth wave) or up-down-count (triangular wave) operation on each counter • Ability to select among 4 count clock sources for each channel (PCLKA/1, PCLKA/4, PCLKA/8, PCLKA/16) • 2 I/O pins per channel • 2 output compare/input capture registers per channel • For each channel, 4 registers that function as buffer register for the 2 output compare/input capture registers and that can be used as compare registers when buffering is not used • Generation of asymmetrical left/right PWM waveforms allowing peak and trough buffering during output compare operation	GPTB • 16 bits × 4 channels • Support for cascade connection on 2 channels as a 32-bit timer • Ability to select up-count or down-count (sawtooth wave) or up-down-count (triangular wave) operation on each counter • Ability to select among 13 count clock sources for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLKA/32, PCLKA/64, PCLKA/256, PCLKA/1024, GTECLKA, GTECLKB, GTECLKC, GTECLKD) • 2 I/O pins per channel • 2 output compare/input capture registers per channel • For each channel, 4 registers that function as buffer register for the 2 output compare/input capture registers and that can be used as compare registers when buffering is not used • Generation of asymmetrical left/right PWM waveforms allowing peak and trough buffering during output compare operation

Item		RX63T	RX24T RX24U
Timers	General PWM timer	• Frame cycle registers for each channel (ability to generate interrupts at overflow/ underflow) • Support for synchronous operation of each counter • Synchronous operation mode (synchronous or precisely at user-defined timing (phase shifting support) • Ability to generate dead time during PWM operation • Ability to combine 3 counters to generate 3-phase PWM waveforms with dead time • Support for count start, clear, or stop by external or internal trigger • Ability to use comparator detection, software, or compare match as internal trigger source — • Ability to generate A/D converter start trigger • Ability to count edges of the frequency-divided IWDT dedicated clock using the count clock function of the main clock (oscillation error detection) • Rise/fall timing control at a resolution equal to 1/32 the system clock (ICLK) for 2 PWM output pins among channel 0 to channel 3 (PWM delay generation function)	• Frame cycle registers for each channel (ability to generate interrupts at overflow/ underflow) • Support for synchronous operation of each counter • Synchronous operation mode (synchronous or precisely at user-defined timing (phase shifting support) • Ability to generate dead time during PWM operation • Ability to combine 3 counters to generate 3-phase PWM waveforms with dead time • Support for count start, clear, or stop by external or internal trigger • Ability to use comparator detection, MTU3 count start, software, or compare match as internal trigger source • Noise filtering function activated by input capture, external trigger pin, or external count clock pin • Ability to generate A/D converter start trigger — —
	Compare match timer	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer	• 14 bits × 1 channel • Select from among six count clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)	Not available
	Independent watchdog timer	• 14 bits × 1 channel • Count clock: IWDT-dedicated on-chip oscillator	• 14 bits × 1 channel • Count clock: IWDT-dedicated on-chip oscillator

Item		RX63T	RX24T RX24U
Timers	8-bit timer	Not available	• (8 bits × 2 channels) × 4 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer • Ability to generate A/D converter start trigger • Ability to generate baud rate clock for SCI5 and SCI6
Communication function	Serial communications interfaces	SCIc • 3 channels • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor function • Ability to select any bit rate using on-chip baud rate generator • Choice of LSB-first or MSB-first transfer — — • Simple I^2C • Simple SPI — — — SCId (functions below in addition to those of SCIc) • 1 channel • Support for serial communication protocol consisting of start frame and information frame • Support for LIN format	SCIg • 3 channels (RX24T) 4 channels (RX24U) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor function • Ability to select any bit rate using on-chip baud rate generator • Choice of LSB-first or MSB-first transfer • Noise canceling function (enabled only during asynchronous operation) • Average transfer rate clock can be input from TMR timers for SCI5 and SCI6 • Simple I^2C • Simple SPI • Start-bit detection: Level or edge detection is selectable. • Support for 9-bit transfer mode • Support for bit rate modulation —

Item		RX63T	RX24T RX24U
Communication function	I²C bus interface	RIIC • 1 channel • Communications formats: I²C bus format/SMBus format Master mode or slave mode selectable Multi-master support Fast mode support	RIICa • 1 channel • Communications formats: I²C bus format/SMBus format Master mode or slave mode selectable Multi-master support Fast mode support
	CAN module	CAN • 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes	RSCAN • 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 16 mailboxes
	Serial peripheral interface	RSPI • 2 channels • RSPI transfer facility • Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock synchronous operation (three lines) • Support for serial communication in master or slave mode • Data formats • Ability to switch between MSB-first and LSB-first bit order • The number of bits in each transfer can be changed to 8 to 16, 20, 24, or 32 bits. • 128-bit buffers for transmission and reception • Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffer configuration Double buffers for both transmission and reception	RSPIb • 1 channel • RSPI transfer facility • Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock synchronous operation (three lines) • Support for serial communication in master or slave mode • Data formats • Choice of LSB-first or MSB-first transfer • The number of bits in each transfer can be changed to 8 to 16, 20, 24, or 32 bits. • 128-bit buffers for transmission and reception • Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffer configuration Double buffers for both transmission and reception

Item		RX63T	RX24T	RX24U
A/D converter	12-bit A/D converter	S12ADB	S12ADF	
		• 12 bits (4 channels × 2 units)	• 12 bits (RX24T): 5 channels × 2 units, 12 channels × 1 unit (RX24U): 5 channels × 2 units, 10 channels × 1 unit	
		• 12-bit resolution	• 12-bit resolution	
		• Conversion time: 1.0 μs per channel (when S12ADB clock PCLKD (A/D converter clock ADCLK) = 50 MHz and AVCC0 = 4.0 to 5.5 V) 2.0 μs per channel (when S12ADB clock PCLKD (A/D converter clock ADCLK) = 25 MHz and AVCC0 = 3.0 to 3.6 V)	• Conversion time: 1.0 μs per channel (when ADCLK = 40 MHz)	
		• Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode)	• Operating modes Scan mode (single scan mode, continuous scan mode, and 3-group scan mode) Group A priority control (only for 3-group scan mode)	
		—	• Sampling variable Sampling time can be set up for each channel.	
		• Sample-and-hold function Sample and hold circuit common to all units Individual sample and hold circuit in addition to the above (3 channels/1 unit)	• Sample-and-hold function Sample and hold circuit common to all units Individual sample and hold circuit in addition to the above (3 channels/1 unit)	
		• Self-diagnostic function Ability to generate 3 analog input voltages (VREFL0, VREFH0 × 1/2, and VREFH0) for use by self-diagnostic function	• Self-diagnostic function For each unit, ability to generate 3 analog input voltages (VREFL0 to VREFL2, VREFH0 to VREFH2 × 1/2, and VREFH0 to VREFH2) for use by self-diagnostic function	
		• Double-trigger mode (duplication of A/D conversion data)	• Double-trigger mode (duplication of A/D conversion data)	
		—	• Analog input cutoff detection assist function	
		• Input signal amplification function using programmable gain amplifier (3 channels/unit 1)	• Input signal amplification function using programmable gain amplifier (1 channel/unit 0, 3 channels/unit 1)	

Item		RX63T	RX24T RX24U
A/D converter	12-bit A/D converter	• Amplification ratio: 2.0×, 2.5×, 3.077×, 3.636×, 4.0×, 4.444×,5.0×, 5.714×, 6.667×, 10.0×, or 13.333× (total 11 steps) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU3, GPT), an external trigger signal	• Amplification ratio: (RX24T): 2.0×, 2.5×, 3.077×, 3.636×, 4.0×, or 4.444× (total 6 steps) (RX24U): 2.0×, 2.5×, 3.077×, 3.636×, 4.0×, 4.444×, 5.0×, 6.667×, 8×, 10.0×, or 13.333× (total 11 steps) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU3, GPT, TMR), an external trigger signal
	10-bit A/D converter	10 bits (12 channels × 1 unit) • 10-bit resolution • Conversion time: 0.5 µs per channel (when A/D converter clock ADCLK = 100 MHz) • 2 operating modes Single mode and scan mode • Scan mode 1-cycle scan mode Continuous scan mode • Sample and hold function Sample and hold circuit common to all units • 3 A/D conversion start methods Software trigger, timer (MTU3 or GPT) trigger, and external trigger • Support for 8-bit precision output Ability to select 2-bit right-shifting of conversion result output • Self-diagnostic function Ability to generate 3 analog input voltages (VSS, VREF × 1/2, and VREF) for use by self-diagnostic function	Not available
Comparator C		Not available	• 4 channels • Reference voltage and analog input voltage comparison function • Reference voltage: Selectable among 2 • Analog input voltage: Selectable among 4 inputs

Item	RX63T	RX24T	RX24U
D/A converter (DAa)	2 channels • 10-bit resolution • Output voltage: 0 V to VREF —	2 channels • 8-bit resolution • Output voltage: 0 V to VREF • Support for external output, support for use as comparator C reference voltage	2 channels • 8-bit resolution • Output voltage: 0 V to AVCC2 • Support for external output, support for use as comparator C reference voltage
Memory protection unit	• Protected areas: Ability to specify up to 8 areas within range from 0000 0000h to FFFF FFFFh • Minimum protection unit: 16 bytes • Ability to specify read, write, or run access for each area • Generation of access exception when access to a non-specified area is detected	• Protected areas: Ability to specify up to 8 areas within range from 0000 0000h to FFFF FFFFh • Minimum protection unit: 16 bytes • Ability to specify read, write, or run access for each area • Generation of access exception when access to a non-specified area is detected	
Register write protection	Ability to prohibit write access to important registers to protect against program runaway	Ability to prohibit write access to important registers to protect against program runaway	
CRC calculator	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.	
Clock frequency accuracy measurement circuit	Ability to measure the following clock frequencies • Main clock oscillator output clock (CACMCLK) — — — • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock (PCLK)	Ability to measure the following clock frequencies • Main clock oscillator • High-speed on-chip oscillators • Low-speed on-chip oscillators • PLL frequency synthesizer • IWDT-dedicated on-chip oscillator • Output clock frequency based on PCLKB	

Item	RX63T	RX24T	RX24U
Data Operation Circuit (DOC)	Ability to compare, add, or subtract user-defined data in 16-bit units	Function for comparing, adding, or subtracting 16 bits of data	
Digital power supply controller (DPC)	• Control parameter calculation unit of the digital switching power supply system • Robust control algorithm with high control stability • Calculation of control parameters in coordination with 10-bit A/D converter	Not available	
Operating frequencies	100 MHz max.	80 MHz max.	
Power supply voltages	• 3 V product VCC = PLLVCC = VCC_USB = 2.7 to 3.6V AVCC0 = AVCC = VREF = 3.0 to 3.6V, or 4.0 to 5.5V VREFH0 = 3.0 V to AVCC0, or 4.0 V to AVCC0 • 5 V product VCC = PLLVCC = 4.0 to 5.5V VCC_USB = 3.0 to 3.6V AVCC0 = AVCC =VREF = 4.0 to 5.5V VREFH0 = 4.0 to AVCC0	VCC = 2.7 to 5.5V	
Operating ambient temperature	D version: –40 to +85°C G version: –40 to +105°C	D version: –40 to +85°C —	
Packages	144-pin LFQFP 0.5 mm pitch 120-pin LFQFP 0.5 mm pitch 112-pin LFQFP 0.5 mm pitch 100-pin LFQFP 0.5 mm pitch 64-pin LFQFP 0.5 mm pitch 48-pin LFQFP 0.5 mm pitch	100-pin LFQFP 0.5 mm pitch 80-pin LQFP 0.65 mm pitch 80-pin LFQFP 0.5 mm pitch 64-pin LFQFP 0.5 mm pitch	144-pin LFQFP 0.5 mm pitch 100-pin LQFP 0.5 mm pitch

4.2 Points of Difference between Pin Functions

Points of difference between pin functions and between pins for power supplies, clocks, and system control are listed below. Items that apply only to one group or the other are indicated in blue. Items that are different between groups are indicated in red. Items that apply to both groups are indicated in black.

4.2.1 100-Pin Package

Table 4.2 lists points of difference between the pin functions for the 100-pin package. Table 4.3 lists points of difference between pins for power supplies, clocks, and system control for the 100-pin package.

Table 4.2 Points of Difference between Pin Functions for 100-Pin Package

I/O Port	RX63T	RX24T	RX24U
P00	CS1#, CACREF, IRQ2, ADST1	IRQ2, ADST1	IRQ2, ADST1
P01	RD#, CTS0#, RTS0#, SS0#	POE12#, IRQ4, ADST2	POE12#, IRQ4, ADST2
P02	— (No I/O port)	MTIOC9D, MTIOC9D#, CTS1#, RTS1#, SS1#, IRQ5, ADST0	MTIOC9D, MTIOC9D#, CTS1#, RTS1#, SS1#, IRQ5, ADST0
P10	MTCLKD, IRQ0-DS	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#, CTS6#, RTS6#, SS6#, IRQ0	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#, CTS6#, RTS6#, SS6#, IRQ0
P11	ALE, MTCLKC, IRQ1-DS	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3, IRQ1	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3, IRQ1
P20	D15, [A15/D15], MTCLKB, IRQ7-DS, ADTRG0#	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4, IRQ7, ADTRG0#, AN016	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4, IRQ7, ADTRG0#, AN016
P21	D14, [A14/D14], MTCLKA, IRQ6-DS, ADTRG1#	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4, IRQ6, ADTRG1#, AN116	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4, IRQ6, ADTRG1#, AN116
P22	D13, [A13/D13], RXD0, SMISO0, SSCL0, MISOA, MISOB, CRX1, ADTRG#	MTIC5W, MTIC5W#, TMRI2, TMO4, MISOA, ADTRG2#, COMP2	MTIC5W, MTIC5W#, TMRI2, TMO4, MISOA, ADTRG2#, COMP2
P23	D12, [A12/D12], CACREF, TXD0, SMOSI0, SSDA0, MOSIA, MOSIB, CTX1	MTIC5V, MTIC5V#, TMO2, CACREF, MOSIA, COMP1, DA1	MTIC5V, MTIC5V#, TMO2, CACREF, MOSIA, COMP1, DA1
P24	D11, [A11/D11], CTS0#, RTS0#, SS0#, RSPCKA, RSPCKB, IRQ4	MTIC5U, MTIC5U#, TMCI2, TMO6, RSPCKA, COMP0, DA0	MTIC5U, MTIC5U#, TMCI2, TMO6, RSPCKA, COMP0, DA0
P27	— (No I/O port)	— (No I/O port)	MTIOC1A, MTIOC1A#
P30	D10, [A10/D10], MTIOC0B, MTCLKD, SCK0, SSLA0, SSLB0	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6, SSLA0, IRQ7, COMP3	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6, SSLA0, IRQ7, COMP3
P31	D9, [A9/D9], MTIOC0A, MTCLKC, SSLA1, SSLB1	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6, SSLA1, IRQ6	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6, SSLA1, IRQ6
P32	D8, [A8/D8], MTIOC3C, MTCLKB, SSLA2, SSLB2	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6, SSLA2	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6, SSLA2

I/O Port	RX63T	RX24T	RX24U
P33	D7, [A7/D7], MTIOC3A, MTCLKA, SSLA3, SSLB3	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0, SSLA3	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0, SSLA3
P36	— (No I/O port)	—	—
P37	— (No I/O port)	—	—
P40	AN000	AN000, CMPC00, CMPC01, CMPC22, CMPC23	AN000, CMPC00, CMPC01, CMPC22, CMPC23
P41	AN001	AN001	AN001
P42	AN002	AN002	AN002
P43	AN003, CVREFL	AN003	AN003
P44	AN100	AN100, CMPC10, CMPC11, CMPC32, CMPC33	AN100, CMPC10, CMPC11, CMPC32, CMPC33
P45	AN101	AN101, CMPC02, CMPC03, CMPC20, CMPC21	AN101, CMPC02, CMPC03, CMPC20, CMPC21
P46	AN102	AN102, CMPC12, CMPC13, CMPC30, CMPC31	AN102, CMPC12, CMPC13, CMPC30, CMPC31
P47	AN103, CVREFH	AN103	AN103
P50	AN6	AN206	— (No I/O port)
P51	AN7	AN207	— (No I/O port)
P52	A7, AN8	AN208, IRQ0	AN208, IRQ0
P53	A6, AN9	AN209, IRQ1	AN209, IRQ1
P54	AN10, DA0	AN210, IRQ2	AN210, IRQ2
P55	AN11, DA1	AN211, IRQ3	AN211, IRQ3
P60	A5, AN0	AN200, IRQ4	AN200, IRQ4
P61	A4, AN1	AN201, IRQ5	AN201, IRQ5
P62	A3, AN2	AN202, IRQ6	AN202, IRQ6
P63	A2, AN3	AN203, IRQ7	AN203, IRQ7
P64	A1, AN4	AN204	AN204
P65	A0, BC0#, AN5	AN205	AN205
P70	D6, [A6/D6], POE0#, CTS1#, RTS1#, SS1#, IRQ5-DS	POE0#, IRQ5	POE0#, IRQ5
P71	D5, [A5/D5], MTIOC3B, GTIOC0A	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#
P72	D4, [A4/D4], MTIOC4A, GTIOC1A	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#
P73	D3, [A3/D3], MTIOC4B, GTIOC2A	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#
P74	D2, [A2/D2], MTIOC3D, GTIOC0B	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#
P75	D1, [A1/D1], MTIOC4C, GTIOC1B	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#
P76	D0, [A0/D0], MTIOC4D, GTIOC2B	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#
P80	A9, MTIC5W, RXD12, SMISO12, SSCL12, RXDX12, IRQ5	MTIC5W, MTIC5W#, TMRI4, RXD6, SMISO6, SSCL6	MTIC5W, MTIC5W#, TMRI4, RXD6, SMISO6, SSCL6
P81	A8, MTIC5V, TXD12, SMOSI12, SSDA12, TXDX12, SIOX12	MTIC5V, MTIC5V#, TMCI4, TXD6, SMOSI6, SSDA6	MTIC5V, MTIC5V#, TMCI4, TXD6, SMOSI6, SSDA6
P82	WAIT#, MTIC5U, SCK12, IRQ3	MTIC5U, MTIC5U#, TMO4, SCK6	MTIC5U, MTIC5U#, TMO4, SCK6

I/O Port	RX63T	RX24T	RX24U
P90	MTIOC7D, GTIOC6B	MTIOC7D, MTIOC7D#	MTIOC7D, MTIOC7D#
P91	MTIOC7C, GTIOC5B	MTIOC7C, MTIOC7C#	MTIOC7C, MTIOC7C#
P92	MTIOC6D, GTIOC4B	MTIOC6D, MTIOC6D#	MTIOC6D, MTIOC6D#
P93	MTIOC7B, GTIOC6A, CTS2#, RTS2#, SS2#	MTIOC7B, MTIOC7B#	MTIOC7B, MTIOC7B#
P94	MTIOC7A, GTIOC5A, CTS1#, RTS1#, SS1#	MTIOC7A, MTIOC7A#	MTIOC7A, MTIOC7A#
P95	MTIOC6B, GTIOC4A, TXD1, SMOSI1, SSDA1	MTIOC6B, MTIOC6B#	MTIOC6B, MTIOC6B#
P96	A13, POE4#, RXD1, SMISO1, SSCL1, IRQ4-DS	POE4#, IRQ4	POE4#, IRQ4
PA0	MTIOC6C, SCK2, SSLA3, SSLB3	MTIOC6C, MTIOC6C#, TMO2, SSLA3, CTXD0	MTIOC6C, MTIOC6C#, TMO2, SSLA3, CTXD0
PA1	MTIOC6A, TXD2, SMOSI2, SSDA2, SSLA2, SSLB2	MTIOC6A, MTIOC6A#, TMO4, SSLA2, CRXD0, ADTRG0#	MTIOC6A, MTIOC6A#, TMO4, SSLA2, CRXD0, ADTRG0#
PA2	MTIOC2B, RXD2, SMISO2, SSCL2, SSLA1, SSLB1	MTIOC2B, MTIOC2B#, TMO7, GTADSM1, CTS6#, RTS6#, SS6#, SSLA1	MTIOC2B, MTIOC2B#, TMO7, GTADSM1, CTS6#, RTS6#, SS6#, SSLA1
PA3	MTIOC2A, SCK0, SSLA0, SSLB0	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0, SSLA0	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0, SSLA0
PA4	MTIOC1B, TXD0, SMOSI0, SSDA0, RSPCKA, RSPCKB, ADTRG0#	MTIOC1B, MTIOC1B#, TMCI7, SCK6, RSPCKA, ADTRG0#	MTIOC1B, MTIOC1B#, TMCI7, SCK6, RSPCKA, ADTRG0#
PA5	MTIOC1A, RXD0, SMISO0, SSCL0, MISOA, MISOB, ADTRG1#	MTIOC1A, MTIOC1A#, TMCI3, RXD6, SMISO6, SSCL6, MISOA, IRQ1, ADTRG1#	MTIOC1A, MTIOC1A#, TMCI3, RXD6, SMISO6, SSCL6, MISOA, IRQ1, ADTRG1#
PB0	A14, MTIOC0D, MOSIA, MOSIB	MTIOC0D, MTIOC0D#, TMO0, TXD6, SMOSI6, SSDA6, MOSIA, ADTRG2#	MTIOC0D, MTIOC0D#, TMO0, TXD6, SMOSI6, SSDA6, MOSIA, ADTRG2#
PB1	MTIOC0C, RXD0, SMISO0, SSCL0, SCL0, IRQ4	MTIOC0C, MTIOC0C#, TMCI0, ADSM1, RXD6, SMISO6, SSCL6, SCL0	MTIOC0C, MTIOC0C#, TMCI0, ADSM1, RXD6, SMISO6, SSCL6, SCL0
PB2	MTIOC0B, TXD0, SMOSI0, SSDA0, SDA0	MTIOC0B, MTIOC0B#, TMRI0, ADSM0, TXD6, SMOSI6, SSDA6, SDA0	MTIOC0B, MTIOC0B#, TMRI0, ADSM0, TXD6, SMOSI6, SSDA6, SDA0
PB3	A15, MTIOC0A, CACREF, SCK0	MTIOC0A, MTIOC0A#, CACREF, SCK6, RSPCKA	MTIOC0A, MTIOC0A#, CACREF, SCK6, RSPCKA
PB4	A16, POE8#, GTETRG0, IRQ3-DS	POE8#, GTETRG, GTECLKD, CTS5#, RTS5#, SS5#, IRQ3	POE8#, GTETRG, GTECLKD, CTS5#, RTS5#, SS5#, IRQ3
PB5	A17, TXD12, SMOSI12, SSDA12, TXDX12, SIOX12, CTX1	GTIOC2B, GTIOC2B#, TXD5, SMOSI5, SSDA5	GTIOC2B, GTIOC2B#, TXD5, SMOSI5, SSDA5
PB6	A18, RXD12, SMISO12, SSCL12, RXDX12, CRX1, IRQ2	GTIOC2A, GTIOC2A#, RXD5, SMISO5, SSCL5, IRQ5	GTIOC2A, GTIOC2A#, RXD5, SMISO5, SSCL5, IRQ5
PB7	A19, SCK12	GTIOC1B, GTIOC1B#, SCK5	GTIOC1B, GTIOC1B#, SCK5
PD0	A12, GTIOC3B, RSPCKA, RSPCKB	TMO6, GTIOC1A, GTIOC1A#, RSPCKA	TMO6, GTIOC1A, GTIOC1A#, RSPCKA
PD1	CS0#, GTIOC3A, MISOA, MISOB	TMO2, GTIOC0B, GTIOC0B#, MISOA	TMO2, GTIOC0B, GTIOC0B#, MISOA
PD2	CS2#, GTIOC2B, MOSIA, MOSIB	TMCI1, TMO4, GTIOC0A, GTIOC0A#, SCK5, MOSIA	TMCI1, TMO4, GTIOC0A, GTIOC0A#, SCK5, MOSIA

I/O Port	RX63T	RX24T	RX24U
PD3	GTIOC2A, TXD1, SMOSI1, SSDA1	TMO0, GTECLKC, TXD1, SMOSI1, SSDA1	TMO0, GTECLKC, TXD1, SMOSI1, SSDA1, TXD11, SMOSI11, SSDA11
PD4	GTIOC1B, SCK1	TMCI0, TMCI6, GTECLKB, SCK1, IRQ2	TMCI0, TMCI6, GTECLKB, SCK1, SCK11, IRQ2
PD5	GTIOC1A, RXD1, SMISO1, SSCL1, IRQ6	TMRI0, TMRI6, GTECLKA, RXD1, SMISO1, SSCL1, IRQ3	TMRI0, TMRI6, GTECLKA, RXD1, SMISO1, SSCL1, RXD11, SMISO11, SSCL11, IRQ3
PD6	GTIOC0B, SSLA0, SSLB0	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#, CTS1#, RTS1#, SS1#, SSLA0, IRQ5, ADST0	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#, CTS1#, RTS1#, SS1#, CTS11#, RTS11#, SS11#, SSLA0, IRQ5, ADST0
PD7	GTIOC0A, CTS0#, RTS0#, SS0#, SSLA1, SSLB1, CTX1	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#, TXD5, SMOSI5, SSDA5, SSLA1	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#, TXD5, SMOSI5, SSDA5, SSLA1
PE0	WR1#, BC1#, WAIT#, SSLA2, SSLB2, CRX1, IRQ7	MTIOC9B, MTIOC9B#, TMCI1, TMCI5, RXD5, SMISO5, SSCL5, SSLA2	MTIOC9B, MTIOC9B#, TMCI1, TMCI5, RXD5, SMISO5, SSCL5, SSLA2
PE1	WR0#, WR#, CTS12#, RTS12#, SS12#, SSLA3, SSLB3	MTIOC9D, MTIOC9D#, TMO5, CTS5#, RTS5#, SS5#, SSLA3	MTIOC9D, MTIOC9D#, TMO5, CTS5#, RTS5#, SS5#, SSLA3
PE2	POE10#, NMI	POE10#, NMI	POE10#, NMI
PE3	A11, POE11#, MTCLKD, IRQ2-DS	MTCLKD, MTCLKD#, POE11#, IRQ2	MTCLKD, MTCLKD#, POE11#, IRQ2
PE4	A10, POE10#, MTCLKC, IRQ1	MTCLKC, MTCLKC#, POE10#, IRQ1	MTCLKC, MTCLKC#, POE10#, IRQ1
PE5	BCLK, IRQ0	IRQ0	IRQ0

Table 4.3 Points of Difference between Pins for Power Supplies, Clocks, and System Control for 100-Pin Package

Pin Number	RX63T	RX24T	RX24U
2	EMLE	— (P02)	— (P02)
3	VSS	VSS	VSS
5	VCL	VCL	VCL
6	— (P00)	MD	MD
7	MD, FINED	— (P01)	— (P01)
10	RES#	RES#	RES#
11	XTAL	XTAL (P37)	XTAL (P37)
12	VSS	VSS	VSS
13	EXTAL	EXTAL (P36)	EXTAL (P36)
14	VCC	VCC	VCC
29	PLLVCC	VCC	VCC
31	PLLVSS	VSS	VSS
42	VCC	VCC	VCC
44	VSS	VSS	VSS
60	VCC	VCC	VCC
62	VSS	VSS	VSS
71	AVCC	AVCC2	— (P64)
72	VREF	VREF	AVCC2
73	AVSS	AVSS2	AVSS2
86	— (P45)	— (P45)	PGAVSS1
91	— (P40)	— (P40)	PGAVSS0
92	AVCC0	AVCC1	AVCC1
93	VREFH0	AVCC0	AVCC0
94	VREFL0	AVSS0	AVSS0
95	AVSS0	AVSS1	AVSS1

4.2.2 144-Pin Package

Table 4.4 lists points of difference between the pin functions for the 144-pin package. Table 4.5 lists points of difference between pins for power supplies, clocks, and system control for the 144-pin package.

Table 4.4 Points of Difference between Pin Functions for 144-Pin Package

I/O Port	RX63T	RX24U
P00	CS1#, CACREF	IRQ2, ADST1
P01	RD#, CTS0#, RTS0#, SS0#, USB0_DRPD	POE12#, IRQ4, ADST2
P02	TXD2, SMOSI2, SSDA2	MTIOC9D, MTIOC9D#, CTS1#, RTS1#, SS1#, IRQ5, ADST0
P03	RXD2, SMISO2, SSCL2, IRQ7	— (No I/O port)
P04	—	— (No I/O port)
P05	CS2#, WAIT#	— (No I/O port)
P10	MTCLKD, IRQ0-DS	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#, CTS6#, RTS6#, SS6#, IRQ0
P11	ALE, MTCLKC, IRQ1-DS	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3, IRQ1
P12	CS3#, USB0_DPRPD	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#
P13	CTS2#, RTS2#, SS2#, USB0_VBUSEN	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#
P14	SCK2	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#
P15	— (No I/O port)	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#
P16	— (No I/O port)	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#
P17	— (No I/O port)	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#
P20	D15, [A15/D15], MTCLKB, IRQ7-DS, ADTRG0#	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4, IRQ7, ADTRG0#, AN016
P21	D14, [A14/D14], MTCLKA, IRQ6-DS, ADTRG1#	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4, IRQ6, ADTRG1#, AN116
P22	D13, [A13/D13], RXD0, SMISO0, SSCL0, MISOA, MISOB, CRX1, ADTRG#	MTIC5W, MTIC5W#, TMRI2, TMO4, MISOA, ADTRG2#, COMP2
P23	D12, [A12/D12], CACREF, TXD0, SMOSI0, SSDA0, MOSIA, MOSIB, CTX1	MTIC5V, MTIC5V#, TMO2, CACREF, MOSIA, COMP1, DA1
P24	D11, [A11/D11], CTS0#, RTS0#, SS0#, RSPCKA, RSPCKB, IRQ4	MTIC5U, MTIC5U#, TMCI2, TMO6, RSPCKA, COMP0, DA0
P25	CS1#, SCK1, SCL1	MTIOC9C, MITOC9C#, SCK1, ADST1
P26	CS0#, TXD1, SMOSI1, SSDA1, SDA1	MTIOC9A, MITOC9A#, CTS1#, RTS1#, SS1#, ADST0
P27	— (No I/O port)	MTIOC1A, MTIOC1A#
P30	D10, [A10/D10], MTIOC0B, MTCLKD, SCK0, SSLA0, SSLB0	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6, SSLA0, IRQ7, COMP3
P31	D9, [A9/D9], MTIOC0A, MTCLKC, SSLA1, SSLB1	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6, SSLA1, IRQ6
P32	D8, [A8/D8], MTIOC3C, MTCLKB, SSLA2, SSLB2	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6, SSLA2
P33	D7, [A7/D7], MTIOC3A, MTCLKA, SSLA3, SSLB3	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0, SSLA3
P36	— (No I/O port)	—
P37	— (No I/O port)	—
P40	AN000	AN000, CMPC00, CMPC01, CMPC22, CMPC23
P41	AN001	AN001
P42	AN002	AN002

I/O Port	RX63T	RX24U
P43	AN003, CVREFL	AN003
P44	AN100	AN100, CMPC10, CMPC11, CMPC32, CMPC33
P45	AN101	AN101, CMPC02, CMPC03, CMPC20, CMPC21
P46	AN102	AN102, CMPC12, CMPC13, CMPC30, CMPC31
P47	AN103, CVREFH	AN103
P50	AN6	AN206
P51	AN7	AN207
P52	A7, AN8	AN208, IRQ0
P53	A6, AN9	AN209, IRQ1
P54	AN10, DA0	AN210, IRQ2
P55	AN11, DA1	AN211, IRQ3
P56	AN12	— (No I/O port)
P57	AN13	— (No I/O port)
P60	A5, AN0	AN200, IRQ4
P61	A4, AN1	AN201, IRQ5
P62	A3, AN2	AN202, IRQ6
P63	A2, AN3	AN203, IRQ7
P64	A1, AN4	AN204
P65	A0, BC0#, AN5	AN205
P70	D6, [A6/D6], POE0#, CTS1#, RTS1#, SS1#, IRQ5-DS	POE0#, CTS9#, RTS9#, SS9#, IRQ5
P71	D5, [A5/D5], MTIOC3B, GTIOC0A	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#
P72	D4, [A4/D4], MTIOC4A, GTIOC1A	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#
P73	D3, [A3/D3], MTIOC4B, GTIOC2A	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#
P74	D2, [A2/D2], MTIOC3D, GTIOC0B	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#
P75	D1, [A1/D1], MTIOC4C, GTIOC1B	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#
P76	D0, [A0/D0], MTIOC4D, GTIOC2B	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#
P80	A9, MTIC5W, RXD12, SMISO12, SSCL12, RXDX12, IRQ5	MTIC5W, MTIC5W#, TMRI4, RXD6, SMISO6, SSCL6
P81	A8, MTIC5V, TXD12, SMOSI12, SSDA12, TXDX12, SIOX12	MTIC5V, MTIC5V#, TMCI4, TXD6, SMOSI6, SSDA6
P82	WAIT#, MTIC5U, SCK12, IRQ3	MTIC5U, MTIC5U#, TMO4, SCK6
P83	— (No I/O port)	RXD8, SMISO8, SSCL8
P84	— (No I/O port)	TXD8, SMOSI8, SSDA8
P90	MTIOC7D, GTIOC6B	MTIOC7D, MTIOC7D#
P91	MTIOC7C, GTIOC5B	MTIOC7C, MTIOC7C#
P92	MTIOC6D, GTIOC4B	MTIOC6D, MTIOC6D#
P93	MTIOC7B, GTIOC6A, CTS2#, RTS2#, SS2#	MTIOC7B, MTIOC7B#
P94	MTIOC7A, GTIOC5A, CTS1#, RTS1#, SS1#	MTIOC7A, MTIOC7A#
P95	MTIOC6B, GTIOC4A, TXD1, SMOSI1, SSDA1	MTIOC6B, MTIOC6B#
P96	A13, POE4#, RXD1, SMISO1, SSCL1, IRQ4-DS	POE4#, CTS8#, RTS8#, SS8#, IRQ4
PA0	MTIOC6C, SCK2, SSLA3, SSLB3	MTIOC6C, MTIOC6C#, TMO2, SSLA3, CTXD0
PA1	MTIOC6A, TXD2, SMOSI2, SSDA2, SSLA2, SSLB2	MTIOC6A, MTIOC6A#, TMO4, SSLA2, CRXD0, ADTRG0#
PA2	MTIOC2B, RXD2, SMISO2, SSCL2, SSLA1, SSLB1	MTIOC2B, MTIOC2B#, TMO7, GTADSM1, CTS6#, RTS6#, SS6#, SSLA1

I/O Port	RX63T	RX24U
PA3	MTIOC2A, SCK0, SSLA0, SSLB0	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0, SSLA0
PA4	MTIOC1B, TXD0, SMOSI0, SSDA0, RSPCKA, RSPCKB, ADTRG0#	MTIOC1B, MTIOC1B#, TMCI7, SCK6, RSPCKA, ADTRG0#
PA5	MTIOC1A, RXD0, SMISO0, SSCL0, MISOA, MISOB, ADTRG1#	MTIOC1A, MTIOC1A#, TMCI3, RXD6, SMISO6, SSCL6, MISOA, IRQ1, ADTRG1#
PA6	CS3#, CTS3#, RTS3#, SS3#	TMO6, ADSM1
PA7	— (No I/O port)	TMO2, ADSM0
PB0	A14, MTIOC0D, MOSIA, MOSIB	MTIOC0D, MTIOC0D#, TMO0, TXD6, SMOSI6, SSDA6, MOSIA, ADTRG2#
PB1	MTIOC0C, RXD0, SMISO0, SSCL0, SCL0, IRQ4	MTIOC0C, MTIOC0C#, TMCI0, ADSM1, RXD6, SMISO6, SSCL6, SCL0
PB2	MTIOC0B, TXD0, SMOSI0, SSDA0, SDA0	MTIOC0B, MTIOC0B#, TMRI0, ADSM0, TXD6, SMOSI6, SSDA6, SDA0
PB3	A15, MTIOC0A, CACREF, SCK0	MTIOC0A, MTIOC0A#, CACREF, SCK6, RSPCKA
PB4	A16, POE8#, GTETRG0, IRQ3-DS	POE8#, GTETRG, GTECLKD, CTS5#, RTS5#, SS5#, IRQ3
PB5	A17, TXD12, SMOSI12, SSDA12, TXDX12, SIOX12, CTX1	GTIOC2B, GTIOC2B#, TXD5, SMOSI5, SSDA5
PB6	A18, RXD12, SMISO12, SSCL12, RXDX12, CRX1, IRQ2	GTIOC2A, GTIOC2A#, RXD5, SMISO5, SSCL5, IRQ5
PB7	A19, SCK12	GTIOC1B, GTIOC1B#, SCK5
PC0	AN14	RXD8, SMISO8, SSCL8, COMP3
PC1	AN15	ADSM1, GTADSM1, TXD8, SMOSI8, SSDA8
PC2	AN16	ADSM0, GTADSM0, SCK8
PC3	AN17	RXD1, SMISO1, SSCL1
PC4	AN18	TXD1, SMOSI1, SSDA1, ADST2
PC5	AN19	MTIOC1B, MTIOC1B#, TXD11, SMOSI11, SSDA11
PC6	— (No I/O port)	MTIOC1A, MTIOC1A#, RXD11, SMISO11, SSCL11
PD0	A12, GTIOC3B, RSPCKA, RSPCKB	TMO6, GTIOC1A, GTIOC1A#, RSPCKA
PD1	CS0#, GTIOC3A, MISOA, MISOB, USB0_EXICEN	TMO2, GTIOC0B, GTIOC0B#, MISOA
PD2	CS2#, GTIOC2B, MOSIA, MOSIB, USB0_ID	TMCI1, TMO4, GTIOC0A, GTIOC0A#, SCK5, MOSIA
PD3	GTIOC2A, TXD1, SMOSI1, SSDA1	TMO0, GTECLKC, TXD1, SMOSI1, SSDA1, TXD11, SMOSI11, SSDA11
PD4	GTIOC1B, SCK1	TMCI0, TMCI6, GTECLKB, SCK1, SCK11, IRQ2
PD5	GTIOC1A, RXD1, SMISO1, SSCL1, IRQ6	TMRI0, TMRI6, GTECLKA, RXD1, SMISO1, SSCL1, RXD11, SMISO11, SSCL11, IRQ3
PD6	GTIOC0B, SSLA0, SSLB0	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#, CTS1#, RTS1#, SS1#, CTS11#, RTS11#, SS11#, SSLA0, IRQ5, ADST0
PD7	GTIOC0A, CTS0#, RTS0#, SS0#, SSLA1, SSLB1, CTX1	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#, TXD5, SMOSI5, SSDA5, SSLA1
PE0	WR1#, BC1#, WAIT#, SSLA2, SSLB2, CRX1, USB_OVRCURB, IRQ7	MTIOC9B, MTIOC9B#, TMCI1, TMCI5, RXD5, SMISO5, SSCL5, SSLA2

I/O Port	RX63T	RX24U
PE1	WR0#, WR#, CTS12#, RTS12#, SS12#, SSLA3, SSLB3, USB_OVRCURA	MTIOC9D, MTIOC9D#, TMO5, CTS5#, RTS5#, SS5#, SSLA3
PE2	POE10#, NMI	POE10#, NMI
PE3	A11, POE11#, MTCLKD, IRQ2-DS	MTCLKD, MTCLKD#, POE11#, IRQ2
PE4	A10, POE10#, MTCLKC, IRQ1	MTCLKC, MTCLKC#, POE10#, IRQ1
PE5	BCLK, USB_VBUS, IRQ0	IRQ0
PE6	— (No I/O port)	POE10#, IRQ3
PF0	—	TMO1, TXD11, SMOSI11, SSDA11, COMP3
PF1	—	TMO5, RXD11, SMISO11, SSCL11, COMP2
PF2	CS1#, RXD1, SMISO1, SSCL1, IRQ5	TMO3, SCK11, CTXD0, COMP1
PF3	TXD1, SMOSI1, SSDA1	TMO7, CTS11#, RTS11#, SS11#, CRXD0, COMP0
PF4	CS3#	— (No I/O port)
PG0	GTIOC7A, TXD2, SMOSI2, SSDA2, IRQ0	RXD9, SMISO9, SSCL9, COMP2
PG1	GTIOC7B, RXD2, SMISO2, SSCL2, IRQ1	TXD9, SMOSI9, SSDA9, COMP1
PG2	SCK2, IRQ2	GTETRG, SCK9, COMP0
PG3	GTIOC6A, TXD3, SMOSI3, SSDA3	— (No I/O port)
PG4	GTIOV6B, RXD3, SMISO3, SSCL3, IRQ6	— (No I/O port)
PG5	POE12#, SCK3, ADTRG#	— (No I/O port)
PG6	CS2#, SCK1	— (No I/O port)

Table 4.5 Points of Difference between Pins for Power Supplies, Clocks, and System Control for 144-Pin Package

Pin Number	RX63T	RX24U
1	VCC_USB	— (P14)
3	EMLE	— (P12)
6	VSS	VCC
8	VCL	VSS
9	— (P00)	VSS
10	MD, FINED	— (P00)
12	— (PE3)	MD
14	VCC	— (PE4)
16	RES#	RES#
17	XTAL	XTAL (P37)
18	VSS	VSS
19	EXTAL	EXTAL (P36)
20	VCC	VCC
21	— (PE2)	VCC
27	VSS	— (PD5)
40	— (PB5)	VCC
41	PLLVCC	— (PB4)
42	— (PB4)	VSS
43	PLLVSS	VSS
60	VCC	— (P34)
63	VSS	VCC
65	— (P94)	VSS
66	— (P93)	VSS
85	VCC	VCC
86	— (P31)	VCC
87	VSS	— (P31)
88	— (P30)	VSS
89	— (P26)	VSS
102	AVCC	— (P64)
103	VREF	VREFH
104	AVSS	AVCC2
105	— (PC1)	AVSS2
106	— (PC0)	VREFL2
121	— (P45)	PGAVSS1
126	— (P40)	PGAVSS0
127	AVCC0	AVCC1
128	VREFH0	VREFH1
129	VREFL0	AVCC0
130	AVSS0	VREFH0
131	— (P82)	AVSS0
132	— (P81)	VREFL0
133	VSS	AVSS1
134	— (P80)	VREFL1
139	VCC	— (P80)
142	VSS_USB	— (P17)

4.2.3 64-Pin Package

Table 4.6 lists points of difference between the pin functions for the 64-pin package. Table 4.7 lists points of difference between pins for power supplies, clocks, and system control for the 64-pin package.

Table 4.6 Points of Difference between Pin Functions for 64-Pin Package

I/O Port	RX63T	RX24T
P00	GTIOC3A, CTS0#, RTS0#, SS0#, IRQ2-DS	IRQ2, ADST1
P01	GTIOC3B, CACREF, IRQ4-DS	POE12#, IRQ4, ADST2
P02	— (No I/O port)	MTIOC9D, CTS1#, RTS1#, SS1#, IRQ5, ADST0
P10	MTCLKD, IRQ0-DS	— (No I/O port)
P11	MTCLKC, IRQ1-DS	MTIOC3A, MTCLKC, TMO3, IRQ1
P21	— (No I/O port)	MTCLKA, MTIOC9A, TMCI4, IRQ6, ADTRG1#, AN116, CVREFC1
P22	MTIC5W, MTCLKA, CTS0#, RTS0#, SS0#, MISOA	MTIC5W, TMRI2, TMO4, MISOA, ADTRG2#, COMP2
P23	MTIC5V, MTCLKB, CACREF, SCK0, MOSIA	MTIC5V, TMO2, CACREF, MOSIA, COMP1
P24	MTIC5U, MTCLKC, RXD0, SMISO0, SSCL0, RSPCKA	MTIC5U, TMCI2, TMO6, RSPCKA, COMP0
P30	MTIOC0B, MTCLKD, TXD0, SMOSI0, SSDA0, SSLA0	MTIOC0B, MTCLKD, TMCI6, SSLA0, IRQ7, COMP3
P31	MTIOC0A, SSLA1	MTIOC0A, MTCLKC, TMRI6, SSLA1, IRQ6
P32	MTIOC3C, MTIOC6C, SSLA2	— (No I/O port)
P33	MTIOC3A, MTIOC6A, SSLA3	— (No I/O port)
P36	— (No I/O port)	—
P37	— (No I/O port)	—
P40	AN000	AN000, CMPC00, CMPC01, CMPC22, CMPC23
P41	AN001	AN001
P42	AN002	AN002
P43	AN003, CVREFL	— (No I/O port)
P44	AN004	AN100, CMPC10, CMPC11, CMPC32, CMPC33
P45	AN005	AN101, CMPC02, CMPC03, CMPC20, CMPC21
P46	AN006	AN102, CMPC12, CMPC13, CMPC30, CMPC31
P47	AN007, CVREFH	— (No I/O port)
P50	— (No I/O port)	AN206
P51	— (No I/O port)	AN207
P52	— (No I/O port)	AN208, IRQ0
P53	— (No I/O port)	AN209, IRQ1
P54	— (No I/O port)	AN210, IRQ2
P70	POE0#, CTS1#, RTS1#, SS1#, IRQ5-DS	POE0#, IRQ5
P71	MTIOC3B, GTIOC0A, MTIOC6B	MTIOC3B
P72	MTIOC4A, GTIOC1A, MTIOC7B	MTIOC4A
P73	MTIOC4B, GTIOC2A, MTIOC7B	MTIOC4B
P74	MTIOC3D, GTIOC0B, MTIOC6D	MTIOC3D
P75	MTIOC4C, GTIOC1B, MTIOC7C	MTIOC4C
P76	MTIOC4D, GTIOC2B, MTIOC7D	MTIOC4D

I/O Port	RX63T	RX24T
P90	— (No I/O port)	MTIOC7D
P91	CTS1#, RTS1#, SS1#	MTIOC7C
P92	SCK1	MTIOC6D
P93	RXD1, SMISO1, SSCL1, IRQ1	MTIOC7B
P94	TXD1, SMOSI1, SSDA1	MTIOC7A
P95	— (No I/O port)	MTIOC6B
P96	— (No I/O port)	POE4#, IRQ4
PA2	MTIOC2B, SSLA1	— (No I/O port)
PA3	MTIOC2A, SSLA0	— (No I/O port)
PA4	MTIOC1B, RSPCKA, ADTRG0#	— (No I/O port)
PA5	MTIOC1A, MISOA	— (No I/O port)
PB0	MTIOC0D, MOSIA	— (No I/O port)
PB1	MTIOC0C, RXD0, SMISO0, SSCL0, SCL	MTIOC0C, TMCI0, ADSM1, RXD6, SMISO6, SSCL6, SCL0
PB2	MTIOC0B, MTCLKB, TXD0, SMOSI0, SSDA0, SDA	MTIOC0B, TMRI0, ADSM0, TXD6, SMOSI6, SSDA6, SDA0
PB3	MTIOC0A, MTCLKA, CACREF, SCK0	MTIOC0A, CACREF, SCK6, RSPCKA
PB4	POE8#, GTETRG, CTS12#, RTS12#, SS12#, IRQ3-DS	POE8#, CTS5#, RTS5#, SS5#, IRQ3
PB5	POE11#, TXD12, SMOSI12, SSDA12, TXDX12, SIOX12, IRQ0	TXD5, SMOSI5, SSDA5
PB6	GTIOC2B, RXD12, SMISO12, SSCL12, RXDX12	RXD5, SMISO5, SSCL5, IRQ5
PB7	GTIOC2B, SCK12	— (No I/O port)
PD3	GTIOC2A, TXD1, SMOSI1, SSDA1	TMO0, TXD1, SMOSI1, SSDA1
PD4	GTIOC1B, SCK1	TMCI0, TMCI6, SCK1, IRQ2
PD5	GTIOC1A, RXD1, SMISO1, SSCL1	TMRI0, TMRI6, RXD1, SMISO1, SSCL1
PD6	GTIOC0B	MTIOC9C, TMO1, CTS1#, RTS1#, SS1#
PD7	GTIOC0A, CTS0#, RTS0#, SS0#	MTIOC9A, TMRI1, TMRI5, SSLA1
PE2	POE10#, NMI	POE10#, NMI

Table 4.7 Points of Difference between Pins for Power Supplies, Clocks, and System Control for 64-Pin Package

Pin Number	RX63T	RX24T
1	EMLE	— (P02)
3	VCL	VCL
4	— (P01)	MD
5	MD, FINED	— (P01)
6	RES#	RES#
7	XTAL	XTAL (P37)
8	VSS	VSS
9	EXTAL	EXTAL (P36)
10	VCC	VCC
20	VCC	— (PB3)
22	VSS	— (PB1)
23	— (PB3)	VCC
25	— (PB1)	VSS
39	— (P70)	VCC
41	— (P32)	VSS
42	VCC	— (P30)
44	VSS	— (P23)
47	— (P23)	AVCC2/VREF
48	— (P22)	AVSS2
57	AVCC0	— (P42)
58	VREFH0	— (P41)
59	VREFL0	— (P40)
60	AVSS0	AVCC1
61	— (P11)	AVCC0
62	— (P10)	AVSS0
63	— (PA5)	AVSS1

4.3 Points of Difference between Modules and Functions

Table 4.8 lists points of difference between modules and functions. This table lists points of difference for the specifications of the 100-pin package. For points of difference between individual modules and functions refer to 4.4, Points of Difference between Specifications in Detail, and the User's Manual: Hardware of each group, listed in 5, Reference Documents.

Table 4.8 Points of Difference between Modules and Functions

No.	Module or Function Name	RX63T	RX24T	RX24U
1	Operating modes	△	△	△
2	Resets	△	△	△
3	Option-setting memory	△	△	△
4	Voltage detection circuit (LVDA/LVDAb/LVDAb)	△	△	△
5	Clock generation circuit	△	△	△
6	Clock frequency accuracy measurement circuit (CAC)	◎	◎	◎
7	Low power consumption	△	△	△
8	Register write protection function	△	△	△
9	Interrupt controller (ICUb)	△	△	△
10	Buses	△	△	△
11	Memory-protection unit (MPU)	△	△	△
12	DMA controller (DMACA)	○	—	—
13	Data transfer controller (DTCa)	◎	◎	◎
14	I/O ports	△	△	△
15	Multi-function pin controller (MPC)	△	△	△
16	Multi-function timer pulse unit 3 (MTU3/MTU3d/MTU3d)	△	△	△
17	Port output enable 3 (POE3/POE3A*[1]/POE3A)	△	△	△
18	General PWM timer (GPT/GPTB/GPTB)	△	△	△
19	8-bit timer (TMR)	—	○	○
20	Compare match timer (CMT)	◎	◎	◎
21	Watchdog timer (WDT)	○	—	—
22	Independent watchdog timer (IWDTa)	◎	◎	◎
23	USB 2.0 host/function module (USBa)	○	—	—
24	Serial communications interface (SCIc, SCId/SCIg/SCIg)	△	△	△
25	I^2C bus interface (RIIC/RIICa/RIICa)	△	△	△
26	CAN module (CAN/RSCAN/RSCAN)	△	△	△
27	Serial peripheral interface (RSPI/RSPIb/RSPIb)	△	△	△
28	CRC calculator (CRC)	◎	◎	◎
29	12-bit A/D converter (S12ADB/S12ADF/S12ADF)	△	△	△
30	10-bit A/D converter (AD)	○	—	—
31	D/A converter (DAa)	△	△	△
32	Comparator C (CMPC)	—	○	○
33	Data operation circuit (DOC)	◎	◎	◎
34	Digital power supply controller (DPC)	○	—	—
35	RAM	△	△	△
36	Flash memory	△	△	△

Note 1. POE3b on RX24T (version A), POE3A on RX24T (version B)

Legend

◎: All groups have this module or function.

○ or —: Not all groups have this module or function.

○ means that the module or function is available on the group indicated.

— means that the module or function is not available on the group indicated.

△: All groups have this module or function, but the specifications differ between groups.

Where the module symbols differ, indications are as follows: Module or symbol name (symbol for RX63T/symbol for RX24T/symbol for RX24U).

4.4 Points of Difference between Specifications in Detail

Points of difference between specifications in detail are listed below. Specifications that apply only to one group or the other are indicated in blue. Specifications that are different between groups are indicated in red. Specifications that have no difference between the two groups are not described.

4.4.1 CPU

Table 4.9 lists the points of difference between the CPUs.

Table 4.9 Points of Difference between CPUs

Item	RX63T	RX24T and RX24U
Instruction architecture	RXv1	RXv2
CPU register set	• 16 general-purpose registers (32 bits) 9 control registers (32 bits) Interrupt stack pointer (ISP) User stack pointer (USP) Interrupt table register (INTB) Program counter (PC) Processor status word (PSW) Backup PC (BPC) Backup PC (BPSW) Fast interrupt vector register (FINTV) Floating-point status word (FPSW) — • 1 accumulator (64 bits) in single-chip mode (ACC)	• 16 general-purpose registers (32 bits) 10 control registers (32 bits) Interrupt stack pointer (ISP) User stack pointer (USP) Interrupt table register (INTB) Program counter (PC) Processor status word (PSW) Backup PC (BPC) Backup PSW (BPSW) Fast interrupt vector register (FINTV) Floating-point status word (FPSW) Exception table register (EXTB) • 2 accumulators (72 bits) in single-chip mode (ACC0, ACC1)
Addressing modes	10 addressing modes: Immediate Register direct Register indirect Register relative Post-increment register indirect Pre-decrement register indirect Indexed register indirect Control register direct PSW direct Program counter relative —	11 modes Immediate Register direct Register indirect Register relative Post-increment register indirect Pre-decrement register indirect Indexed register indirect Control register direct PSW direct Program counter relative Accumulator direct
Basic instructions	73 basic instructions — —	75 basic instructions Storing with LI flag clear (MOVCO) Loading with LI flag set (MOVLI)
Floating-point instructions	8 floating-point instructions — — —	11 floating-point instructions Floating-point square root (FSQRT) Floating point to integer conversion (FTOU) Integer to floating-point conversion (UTOF)

Item	RX63T	RX24T and RX24U
DSP instructions	9 DSP instructions Multiply-accumulate upper 16 bits (MACHI) Multiply-accumulate lower 16 bits (MACLO) Multiply upper 16 bits (MULHI) Multiply lower 16 bits (MULOL) Move upper 32 bits from accumulator (MVFACHI) Move accumulator middle 32 bits from accumulator (MVFACMI) Move accumulator lower 32 bits from accumulator (MVTACLO) Round 16-bit signed value in accumulator (RACW) — — — — — — — — — — — — — —	23 DSP instructions Multiply-accumulate upper 16 bits (MACHI) Multiply-accumulate lower 16 bits (MACLO) Multiply upper 16 bits (MULHI) Multiply lower 16 bits (MULOL) Move upper 32 bits from accumulator (MVFACHI) Move accumulator middle 32 bits from accumulator (MVFACMI) Move accumulator lower 32 bits from accumulator (MVTACLO) Round 16-bit signed value in accumulator (RACW) 32-bit multiply-accumulate (EMACA) 32-bit multiply-subtract (EMSBA) 32-bit multiply (EMULA) Multiply-accumulate upper 16 bits/lower 16 bits (MACLH) Multiply-accumulate upper 16 bits (MSBHI) Multiply-accumulate upper 16 bits/lower 16 bits (MSBLH) Multiply-accumulate lower 16 bits (MSBLO) Multiply upper 16 bits/lower 16 bits (MULLH) Move guard bits from accumulator (MVFACGU) Move lower 32 bits from accumulator (MVFACLO) Move guard bits to accumulator (MVTACGU) Round signed value in accumulator (RACL) Round signed value in accumulator (RADCL) Round 16-bit signed value in accumulator (RDACW)
Vector table	• Fixed vector table • Relocatable vector table	• Exception vector table • Interrupt vector table

4.4.2 Operating Modes

Table 4.10 lists the points of difference between the operating modes, and Table 4.11 lists the points of difference between the I/O registers related to the operating modes.

Table 4.10 Points of Difference between Operating Modes

Item	RX63T	RX24T and RX24U
Operating mode differences	• Single-chip mode • Boot mode SCI interface • User boot mode	• Single-chip mode • Boot mode SCI interface FINE interface —
Pins for setting a mode	MD	MD

Table 4.11 Points of Difference between I/O Registers Related to Operating Modes

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
MDSR	—	Mode status register	Register not available
SYSCR0	—	System control register 0	Register not available

4.4.3 Resets

Table 4.12 lists the points of difference between the resets, and Table 4.13 lists the points of difference between the I/O registers related to the resets.

Table 4.12 Points of Difference between Resets

Reset Name	RX63T	RX24T and RX24U
Types of resets	RES# pin reset	RES# pin reset
	Power-on reset	Power-on reset
	Voltage monitoring 0 reset	Voltage monitoring 0 reset
	Voltage monitoring 1 reset	Voltage monitoring 1 reset
	Voltage monitoring 2 reset	Voltage monitoring 2 reset
	Deep software standby reset	—
	Independent watchdog timer reset	Independent watchdog timer reset
	Watchdog timer reset	—
	Software reset	Software reset

Table 4.13 Points of Difference between I/O Registers Related to Resets

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
RSTSR0	DPSRSTF	Deep software standby reset flag	Reserved
RSTSR2	WDTRF	Watchdog timer reset detect flag	Reserved

4.4.4 Option-Setting Memory

Table 4.14 lists the points of difference between the option-setting memory modules, and Table 4.15 lists the points of difference between the I/O registers related to the option-setting memory modules.

Table 4.14 Points of Difference between Option-Setting Memory Modules

Item	RX63T	RX24T and RX24U
For user boot mode	UB code A UB code B Endian select register B	Not available
For single-chip mode	Endian select register S	Endian select register

Table 4.15 Points of Difference between I/O Registers Related to Option-Setting Memory Modules

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
OFS0	WDTTOPS[1:0]	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby mode, and deep sleep mode
	WDTSTRT	WDT start mode select bit	Reserved
	WDTTOPS[1:0]	WDT timeout period select bits	Reserved
	WDTCKS[3:0]	WDT clock frequency division select bits	Reserved
	WDTRPES[1:0]	WDT window end position select bits	Reserved
	WDTRPSS[1:0]	WDT window start position select bits	Reserved
	WDTRSTIRQS	WDT reset interrupt request select bit	Reserved
OFS1	VDSEL[1:0]	Reserved	Voltage detection 0 level select bits
	FASTSTUP	Reserved	HOCO oscillation enable bit

4.4.5 Voltage Detection Circuit

Table 4.16 lists the points of difference between the voltage detection circuits, and Table 4.17 lists the points of difference between the I/O registers related to the voltage detection circuits.

Table 4.16 Points of Difference between Voltage Detection Circuits

Item		RX63T	RX24T and RX24U
Voltage monitoring 0	Detection voltage	Fixed at 1 level	Selectable from 3 levels
Voltage monitoring 1	Detection voltage	Selectable from 3 levels	Selectable from 9 levels
Voltage monitoring 2	Detection voltage	Selectable from 3 levels	Selectable from 4 levels

Table 4.17 Points of Difference between I/O Registers Related to Voltage Detection Circuits

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
LVD1CR1	LVD1IRQSEL	Reserved	Voltage monitoring 1 interrupt generation condition select bit
LVD2CR1	LVD2IRQSEL	Reserved	Voltage monitoring 2 interrupt generation condition select bit
LVD1CR0	LVD1FSAMP [1:0]	Sampling clock select bits	Reserved
LVD2CR0	LVD2FSAMP [1:0]	Sampling clock select bits	Reserved

4.4.6 Clock Generation Circuit

Table 4.18 lists the points of difference between the clock generation circuits, and Table 4.19 lists the points of difference between the I/O registers related to the clock generation circuits.

Table 4.18 Points of Difference between Clock Generation Circuits

Item	RX63T	RX24T and RX24U
Uses	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the MTU3, GPT, and DPC. • Generates the peripheral module clocks (PCLKB) to be supplied to the peripheral modules. • Generates the AD clock (PCLKC) to be supplied the AD. • Generates the S12AD clock (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the CAC clock (CACMCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the MTU3 and GPT. • Generates the peripheral module clocks (PCLKB) to be supplied to the peripheral modules. — • Generates the S12AD clock (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. — — • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN. • Generates the CAC clock (CACMCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. —
Operating frequencies	ICLK: 100 MHz (max.) PCLKA: 100 MHz (max.) PCLKB: 50 MHz (max.) PCLKC: 100 MHz (max.) PCLKD: 50 MHz (max.) FCLK: 4 MHz to 50 MHz (ROM or E2 DataFlash program/erase) — — CANMCLK: 14 MHz (max.)	ICLK: 80 MHz (max.) PCLKA: 80 MHz (max.) PCLKB: 40 MHz (max.) — PCLKD: 40 MHz (max.) FCLK: 1 MHz to 32 MHz (ROM) CACCLK: Same frequency as each oscillator IWDTCLK: 15 kHz CANMCLK: 20 MHz (max.)
Main clock oscillator	Oscillation frequency: 8 MHz to 12.5 MHz	Oscillation frequency: 1 MHz to 20 MHz

Item	RX63T	RX24T and RX24U
PLL circuit	• Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, 25, and 50 • VCO oscillation frequency: 104 MHz to 200 MHz	• Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • VCO oscillation frequency: 40 MHz to 80 MHz
High-speed on-chip oscillator (HOCO)	—	Oscillation frequency: 32 MHz, 64 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 15 kHz

Table 4.19 Points of Difference between I/O Registers Related to Clock Generation Circuits

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
SCKCR	PCKD[3:0]	S12AD clock (PCLKD) select bits	Peripheral module clock D (PCLKD) select bits
	PCKC[3:0]	AD clock (PCLKC) select bits	Reserved
	BCK [3:0]	External bus clock (BCLK) select bits	Reserved
	PSTOP1	BCLK pin output control bit	Reserved
SCKCR2	—	System clock control register 2	Register not available
SCKCR3	CKSEL[2:0]	Clock source select bits 0 0 0: LOCO — 0 1 0: Main clock oscillator 1 0 0: PLL circuit	Clock source select bits 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 1 0 0: PLL circuit

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
PLLCR	PLLSRCSEL	Register not available	PLL Clock source select bit
	STC[5:0]	Frequency multiplication factor select bits [5:0] 0 0 0 1 1 1: ×8 — 0 0 1 0 0 1: ×10 — 0 0 1 0 1 1: ×12 — — — 0 0 1 1 1 1: ×16 — — — 0 1 0 0 1 1: ×20 — — — 0 1 0 1 1 1: ×24 0 1 1 0 0 0: ×25 1 1 0 0 0 1: ×50 — — — — —	Frequency multiplication factor select bits [5:0] 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15 0 1 1 1 1 0: ×15.5
BCKCR	—	External bus clock control register	Register not available
HOCOCR	—	Register not available	High-speed on-chip oscillator control register
HOCOCR2	—	Register not available	High-speed on-chip oscillator control register 2
HOCOWTCR	—	Register not available	High-speed on-chip oscillator wait control register
OSCOVFSR	—	Register not available	Oscillation stabilization flag register
MOFCR	MOFXIN	Main clock oscillator forced oscillation bit	Reserved
	MODRV21	Reserved	Main clock oscillator drive capability switch bit
	MOSEL	Reserved	Main clock oscillator switch bit
MEMWAIT	—	Register not available	Memory wait cycle setting register

4.4.7 Low Power Consumption

Table 4.20 lists the points of difference between the low power consumption functions, and Table 4.21 lists the points of difference between the I/O registers related to the low power consumption functions.

Table 4.20 Points of Difference between Low Power Consumption Functions

Item	RX63T	RX24T and RX24U
Reducing power consumption by switching clock signals	Clocks for which the frequency division ratio is settable independently • System clock (ICLK) • Timer module clock (PCLKA) • Peripheral module clock (PCLKB) • AD clock (PCLKC) • S12AD clock (PCLKD) • External bus clock (BCLK) • FlashIF clock (FCLK)	Clocks for which the frequency division ratio is settable independently • System clock (ICLK) • High-speed peripheral module clock (PCLKA) • Peripheral module clock (PCLKB) — • S12AD clock (PCLKD) — • FlashIF clock (FCLK)
BCLK output control function	Selectable between BCLK output and high output	—
Low power consumption modes	Sleep mode All-module clock stop mode Software standby mode Deep software standby mode —	Sleep mode — Software standby mode — Deep sleep mode
Function for lower operating power consumption	—	Two operating power control modes • High-speed operating mode • Middle-speed operating mode

Table 4.21 Points of Difference between I/O Registers Related to Low Power Consumption Functions

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
SBYCR	OPE	Output port enable bit	Reserved
	SSBY	Software standby bit 0: Shifts to sleep mode or all-module clock stop mode after the WAIT instruction is executed 1: Shifts to software standby mode after the WAIT instruction is executed	Software standby bit 0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed
MSTPCRA	MSTPA2	Reserved	8-bit timer 7 and 6 (unit 3) module stop bit
	MSTPA3	Reserved	8-bit timer 5 and 4 (unit 2) module stop bit
	MSTPA4	Reserved	8-bit timer 3 and 2 (unit 1) module stop bit
	MSTPA5	Reserved	8-bit timer 1 and 0 (unit 0) module stop bit
	MSTPA6	General PWM timer (unit 1) module stop bit	Reserved
	MSTPA7	General PWM timer (unit 0) module stop bit	General PWM timer module stop bit
	MSTPA16	12-bit A/D converter (unit 1) module stop bit	12-bit A/D converter 1 module stop bit
	MSTPA17	12-bit A/D converter (unit 0) module stop bit	12-bit A/D converter module stop bit
	MSTPA19	Reserved	Comparator C reference voltage generation dedicated D/A converter module stop bit
	MSTPA23	10-bit A/D converter module stop bit	12-bit A/D converter 2 module stop bit
	MSTPA24	12-bit A/D converter control section module stop bit	Reserved
	ACSE	All-module clock stop mode enable bit	Reserved

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
MSTPCRB	MSTPB0	CAN module stop bit	RSCAN module stop bit
	MSTPB4	Serial communication interface SCId module stop bit	Reserved
	MSTPB6	Data operation circuit module stop bit	DOC module stop bit
	MSTPB10	Reserved	Comparator C module stop bit
	MSTPB16	Serial peripheral interface 1 module stop bit	Reserved
	MSTPB19	Universal serial bus interface (port 0) module stop bit	Reserved
	MSTPB21	I^2C bus interface module stop bit	I^2C bus interface 0 module stop bit
	MSTPB25	Reserved	Serial communication interface 6 module stop bit
	MSTPB26	Reserved	Serial communication interface 5 module stop bit
	MSTPB28	Serial communication interface 3 module stop bit	Reserved
	MSTPB29	Serial communication interface 2 module stop bit	Reserved
	MSTPB31	Serial communication interface 0 module stop bit	Reserved
MSTPCRC	MSTPC24	Reserved	(RX24U only) serial communication interface 11 module stop bit
	MSTPC31 (RX63T) DSLPE (RX24T/24U)	Digital power supply control circuit module stop bit (MSTPC31)	Deep sleep mode enable bit (DSLPE)
MOSCWTCR	—	Main clock oscillator wait control register	Register not available
PLLWTCR	—	PLL wait control register	Register not available
DPSBYCR	—	Deep standby control register	Register not available
DPSIER0	—	Deep standby interrupt enable register 0	Register not available
DPSIER2	—	Deep standby interrupt enable register 2	Register not available
DPSIFR0	—	Deep standby interrupt flag register 0	Register not available
DPSIFR2	—	Deep standby interrupt flag register 2	Register not available
DPSIEGR0	—	Deep standby interrupt edge register 0	Register not available
DPSIEGR2	—	Deep standby interrupt edge register 2	Register not available
DPSBKRy (y = 0 to 31)	—	Deep standby backup register	Register not available
OPCCR	—	Register not available	Operating power control register

4.4.8 Register Write Protection Function

Table 4.22 lists the points of difference between the register write protection functions, and Table 4.23 lists the points of difference between the I/O registers related to the register write protection functions.

Table 4.22 Points of Difference between Register Write Protection Functions

Item	RX63T	RX24T and RX24U
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, LOCOCR, ILOCOCR, OSTDCR, OSTDSR	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, MEMWAIT
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2 • Registers related to clock generation circuit: MOFCR • Software reset register SWRR	• Registers related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to clock generation circuit: HOCOWTCR • Software reset register SWRR
PRC2 bit	—	• Registers related to clock generation circuit: HOCOWTCR

Table 4.23 Points of Difference between I/O Registers Related to Register Write Protection Functions

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
PRCR	PRC1	Protect bit 1 Enables writing to registers related to operating modes, low-power-consumption functionality, and software resets.	Protect bit 1 Enables writing to registers related to operating modes, low-power-consumption functionality, the clock generation circuit, and software resets.
	PRC2	Reserved	Protect bit 2 Enables writing to registers related to the clock generation circuit.

4.4.9 Interrupt Controller

Table 4.24 the points of difference between the interrupt controllers, and Table 4.25 lists the points of difference between the I/O registers related to the interrupt controllers.

Table 4.24 Points of Difference between Interrupt Controllers

Item		RX63T	RX24T and RX24U
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Sources: 169 • Interrupt detection: Edge detection/level detection • Edge detection or level detection is fixed for each source of the connected peripheral modules. • Interrupt grouping: Multiple interrupt requests can be allocated to a single interrupt vector. Number of groups for edge detection interrupts: 1 (group 0) Number of groups for level detection interrupts: 1 (group 12)	• Interrupts from peripheral modules • Sources: 163 (RX24T), 175 (RX24U) • Interrupt detection: Edge detection/level detection • Edge detection or level detection is fixed for each source of the connected peripheral modules. —
	DTC control	DTC activation sources: 124 (115 peripheral function interrupts + 8 external pin interrupts + 1 software interrupt)	DTC activation sources: 118 (RX24T), 124 (RX24U) (109 (RX24T) or 115 (RX24U) peripheral function interrupts + 8 external pin interrupts + 1 software interrupt)
	DMAC control	DMAC activation sources: 119 (111 peripheral function interrupts + 8 external pin interrupts)	Not available
Non-maskable interrupts	WDT underflow/ refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error	Not available
Return from low power consumption modes		• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. —	• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source.
		• All-module clock stop mode: Return by means of non-maskable interrupt, IRQ0 to IRQ7 interrupt, or USB resume interrupt	—
		• Software standby mode: Return by means of non-maskable interrupt, IRQ0 to IRQ7 interrupt, or USB resume interrupt	• Software standby mode: Return by means of non-maskable interrupt, IRQ0 to IRQ7 interrupt

Table 4.25 Points of Difference between I/O Registers Related to Interrupt Controllers

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
DTCERn n = interrupt vector number	DTCE	DTC activation enable bit	DTC transfer request enable bit
DMRSRm m = DMAC channel number	—	DMAC activation request select register	Register not available
NMISR	WDTST	WDT underflow/refresh error status flag	Reserved
NMIER	WDTEN	WDT underflow/refresh error enable bit	Reserved
NMICLR	WDTCLR	WDT clear bit	Reserved
GRPm m = group number	—	Group m interrupt source register	Register not available
GENm m = group number	—	Group m interrupt enable register	Register not available
GCRm m = group number	—	Group m interrupt clear register	Register not available

Headings in Table 4.26 indicate as follows.

- Vector No.: Vector number for the interrupt
- RX63T/RX24T/RX24U: Applies to RX63T Group, RX24T Group, or RX24U Group, as indicated.
- Source of interrupt request generation: Name of the source for generation of the interrupt request
- Name: Name of the interrupt
- Interrupt detection: “Edge” or “level” as the method for detection of the interrupt
- CPU interrupt: “○” in this column indicates that the source can be used for the CPU interrupt.
- DTC activation: “○” in this column indicates that the source can be used for DTC activation.
- DMAC activation: “○” in this column indicates that the source can be used for DMAC activation.
- sstb return: “○” in this column indicates that the source can be used for return from software-standby mode.
- sacs return: “○” in this column indicates that the source can be used for return from all-module clock stop mode.
- IER: IER register and bit corresponding to the vector number
- IPR: IPR register corresponding to the interrupt source
- DTCER: DTCER register corresponding to the DTC activation source

Table 4.26 Points of differences between Interrupt Vector Tables

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
21	RX63T	FCUIF	FIFERR	Level	○	×	×	×	×	IER02.IEN5	IPR001	—
	RX24T RX24U	—	Reserved	—	×					—	—	
32	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	CAC	FERRF	Level	○					IER04.IEN0	IPR032	
33	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	CAC	MENDF	Level	○					IER04.IEN1	IPR033	
34	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	CAC	OVFF	Level	○					IER04.IEN2	IPR034	
36	RX63T	CAC	FERRF	Level	○	×	×	×	×	—	—	—
	RX24T RX24U	—	Reserved	—	×					IER04.IEN4	IPR036	
37	RX63T	CAC	MENDF	Level	○	×	×	×	×	—	—	—
	RX24T RX24U	—	Reserved	—	×					IER04.IEN5	IPR036	
38	RX63T	CAC	OVFF	Level	○	×	×	×	×	—	—	—
	RX24T RX24U	—	Reserved	—	×					IER04.IEN6	IPR036	
39	RX63T	RSPI0	SPRI0	Edge	○	○	○	×	×	IER04.IEN7	IPR039	DTCER039
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
40	RX63T	RSPI0	SPTI0	Edge	○	○	○	×	×	IER05.IEN0	IPR040	DTCER040
	RX24T RX24U	GPT	ETGIN			×	×					—
41	RX63T	RSPI0	SPII0	Level	○	×	×	×	×	IER05.IEN1	IPR041	—
	RX24T RX24U	GPT	ETGIP	Edge								
42	RX63T	RSPI1	SPRI1	Edge	○	○	○	×	×	IER05.IEN2	IPR042	DTCER042
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
43	RX63T	RSPI1	SPTI1	Edge	○	○	○	×	×	IER05.IEN3	IPR043	DTCER043
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
44	RX63T	RSPI1	SPII1	Level	○	×	×	×	×	IER05.IEN4	IPR044	—
	RX24T RX24U	RSPI0	SPEI0									
45	RX63T	CAN1	RXF1	Edge	○	×	×	×	×	IER05.IEN5	IPR045	—
	RX24T RX24U	RSPI0	SPRI0			○					IPR044	DTCER045
46	RX63T	CAN1	TXF1	Edge	○	×	×	×	×	IER05.IEN6	IPR045	—
	RX24T RX24U	RSPI0	SPTI0			○					IPR044	DTCER046
47	RX63T	CAN1	RXM1	Edge	○	×	×	×	×	IER05.IEN7	IPR045	—
	RX24T RX24U	RSPI0	SPII0	Level							IPR044	
48	RX63T	CAN1	TXM1	Edge	○	×	×	×	×	IER06.IEN0	IPR045	—
	RX24T RX24U	GPT0	GTCIA0			○					IPR048	DTCER048
49	RX63T	GPT7	GTCIA7	Edge	○	○	○	×	×	IER06.IEN1	IPR049	DTCER049
	RX24T RX24U	GPT0	GTCIB0				×					
50	RX63T	GPT7	GTCIB7	Edge	○	○	○	×	×	IER06.IEN2	IPR049	DTCER050
	RX24T RX24U	GPT0	GTCIC0				×				IPR050	
51	RX63T	GPT7	GTCIC7	Edge	○	○	○	×	×	IER06.IEN3	IPR049	DTCER051
	RX24T RX24U	GPT0	GTCID0				×				IPR051	
52	RX63T	GPT7	GTCIE7	Edge	○	○	○	×	×	IER06.IEN4	IPR052	DTCER052
	RX24T RX24U	GPT0	GDTE0			×	×					—
53	RX63T	GPT7	GTCIV7	Edge	○	○	○	×	×	IER06.IEN5	IPR052	DTCER053
	RX24T RX24U	GPT0	GTCIE0				×				IPR053	

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
54	RX63T	Comparator	CMP4	Edge	○	○	○	×	×	IER06.IEN6	IPR054	DTCER054
	RX24T RX24U	GPT0	GTCIF0				×					
55	RX63T	Comparator	CMP5	Edge	○	○	○	×	×	IER06.IEN7	IPR055	DTCER055
	RX24T RX24U	GPT0	GTCIV0				×					
56	RX63T	Comparator	CMP6	Edge	○	○	○	×	×	IER07.IEN0	IPR056	DTCER056
	RX24T RX24U	GPT0	GTCIU0				×					
58	RX63T	DPC	RBI0	Edge	○	○	○	×	×	IER07.IEN2	IPR058	DTCER058
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
59	RX63T	DPC	RBI1	Edge	○	○	○	×	×	IER07.IEN3	IPR059	DTCER059
	RX24T RX24U	RSCAN	COMFRXINT				×					
60	RX63T	DPC	RBI2	Edge	○	○	○	×	×	IER07.IEN4	IPR060	DTCER060
	RX24T RX24U	RSCAN	RXFINT	Level		×	×					—
61	RX63T	DPC	RBI3	Edge	○	○	○	×	×	IER07.IEN5	IPR061	DTCER061
	RX24T RX24U	RSCAN	TXINT	Level		×	×					—
62	RX63T	DPC	RBI4	Edge	○	○	○	×	×	IER07.IEN6	IPR062	DTCER062
	RX24T RX24U	RSCAN	CHERRINT	Level		×	×					—
63	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	RSCAN	GLERRINT	Level	○					IER07.IEN7	IPR063	
64	RX63T	ICU	IRQ0	Edge/ Level	○	○	○	○	○	IER08.IEN0	IPR064	DTCER064
	RX24T RX24U	ICU					×		×			
65	RX63T	ICU	IRQ1	Edge/ Level	○	○	○	○	○	IER08.IEN1	IPR065	DTCER065
	RX24T RX24U	ICU					×		×			
66	RX63T	ICU	IRQ2	Edge/ Level	○	○	○	○	○	IER08.IEN2	IPR066	DTCER066
	RX24T RX24U	ICU					×		×			
67	RX63T	ICU	IRQ3	Edge/ Level	○	○	○	○	○	IER08.IEN3	IPR067	DTCER067
	RX24T RX24U	ICU					×		×			
68	RX63T	ICU	IRQ4	Edge/ Level	○	○	○	○	○	IER08.IEN4	IPR068	DTCER068
	RX24T RX24U	ICU					×		×			

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
69	RX63T	ICU	IRQ5	Edge/	○	○	○	○	○	IER08.IEN5	IPR069	DTCER069
	RX24T	ICU		Level			×		×			
	RX24U											
70	RX63T	ICU	IRQ6	Edge/	○	○	○	○	○	IER08.IEN6	IPR070	DTCER070
	RX24T	ICU		Level			×		×			
	RX24U											
71	RX63T	ICU	IRQ7	Edge/	○	○	○	○	○	IER08.IEN7	IPR071	DTCER071
	RX24T	ICU		Level			×		×			
	RX24U											
88	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T	LVD	LVD1	Edge	○			○		IER0B.IEN0	IPR088	
	RX24U											
89	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T	LVD	LVD2	Edge	○			○		IER0B.IEN1	IPR089	
	RX24U											
98	RX63T	AD	ADI0	Edge	○	○	○	×	×	IER0C.IEN2	IPR098	DTCER098
	RX24T	GPT1	GTCIA1				×					
	RX24U											
99	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T	GPT1	GTCIB1	Edge	○	○				IER0C.IEN3	IPR099	DTCER099
	RX24U											
100	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T	GPT1	GTCIC1	Edge	○	○				IER0C.IEN4	IPR100	DTCER100
	RX24U											
101	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T	GPT1	GTCID1	Edge	○	○				IER0C.IEN5	IPR101	DTCER101
	RX24U											
102	RX63T	S12AD	S12ADI	Edge	○	○	○	×	×	IER0C.IEN6	IPR102	DTCER102
	RX24T						×					
	RX24U											
103	RX63T	S12AD	S12GBADI	Edge	○	○	○	×	×	IER0C.IEN7	IPR103	DTCER103
	RX24T		GBADI				×					
	RX24U											
104	RX63T	S12AD1	S12ADI1	Edge	○	○	○	×	×	IER0D.IEN0	IPR104	DTCER104
	RX24T	S12AD	GCADI				×					
	RX24U											
105	RX63T	S12AD1	S12GBADI1	Edge	○	○	○	×	×	IER0D.IEN1	IPR105	DTCER105
	RX24T		S12ADI1				×					
	RX24U											
106	RX63T	ICU	GROUP0	Level	○	×	×	×	×	IER0D.IEN2	IPR106	—
	RX24T	S12AD1	GBADI1	Edge		○						DTCER106
	RX24U											

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
107	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	S12ADI1	GCADI1	Edge	○	○				IER0D.IEN3	IPR107	DTCER107
108	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	CMPC0	CMPC0	Edge	○	○				IER0D.IEN4	IPR108	DTCER108
109	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	CMPC1	CMPC1	Edge	○	○				IER0D.IEN5	IPR109	DTCER109
110	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	CMPC2	CMPC2	Edge	○	○				IER0D.IEN6	IPR110	DTCER110
111	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	S12AD2	S12ADI2	Edge	○	○				IER0D.IEN7	IPR111	DTCER111
112	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	S12AD2	GBADI2	Edge	○	○				IER0E.IEN0	IPR112	DTCER112
113	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	S12AD2	GCADI2	Edge	○	○				IER0E.IEN1	IPR113	DTCER113
114	RX63T	ICU	GROUP12	Level	○	×	×	×	×	IER0E.IEN2	IPR114	—
	RX24T RX24U	MTU0	TGIA0	Edge		○						DTCER114
115	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	MTU0	TGIB0	Edge	○	○				IER0E.IEN3	IPR114	DTCER115
116	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	MTU0	TGIC0	Edge	○	○				IER0E.IEN4	IPR114	DTCER115
117	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	MTU0	TGID0	Edge	○	○				IER0E.IEN5	IPR114	DTCER115
118	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	MTU0	TCIV0	Edge	○					IER0E.IEN6	IPR118	
119	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	MTU0	TGIE0	Edge	○					IER0E.IEN7	IPR118	
120	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	MTU0	TGIF0	Edge	○					IER0F.IEN0	IPR118	

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
121	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	MTU1	TGIA1	Edge	○	○				IER0F.IEN1	IPR121	DTCER121
122	RX63T	SCI12	SCIX0	Level	○	×	×	×	×	IER0F.IEN2	IPR122	—
	RX24T RX24U	MTU1	TGIB1	Edge		○					IPR121	DTCER122
123	RX63T	SCI12	SCIX1	Level	○	×	×	×	×	IER0F.IEN3	IPR122	—
	RX24T RX24U	MTU1	TCIV1	Edge							IPR123	
124	RX63T	SCI12	SCIX2	Level	○	×	×	×	×	IER0F.IEN4	IPR122	—
	RX24T RX24U	MTU1	TCIU1	Edge							IPR123	
125	RX63T	SCI12	SCIX3	Level	○	×	×	×	×	IER0F.IEN5	IPR122	—
	RX24T RX24U	MTU2	TGIA2	Edge		○					IPR125	DTCER125
126	RX63T	MTU0	TGIA0	Edge	○	○	○	×	×	IER0F.IEN6	IPR126	DTCER126
	RX24T RX24U	MTU2	TGIB2				×				IPR125	
127	RX63T	MTU0	TGIB0	Edge	○	○	○	×	×	IER0F.IEN7	IPR126	DTCER127
	RX24T RX24U	MTU2	TCIV2			×	×				IPR127	—
128	RX63T	MTU0	TGIC0	Edge	○	○	○	×	×	IER10.IEN0	IPR126	DTCER128
	RX24T RX24U	MTU2	TCIU2			×	×				IPR127	—
129	RX63T	MTU0	TGID0	Edge	○	○	○	×	×	IER10.IEN1	IPR126	DTCER129
	RX24T RX24U	MTU3	TGIA3				×				IPR129	
130	RX63T	MTU0	TCIV0	Edge	○	×	×	×	×	IER10.IEN2	IPR130	—
	RX24T RX24U	MTU3	TGIB3			○					IPR129	DTCER130
131	RX63T	MTU0	TGIE0	Edge	○	×	×	×	×	IER10.IEN3	IPR130	—
	RX24T RX24U	MTU3	TGIC3			○					IPR129	DTCER131
132	RX63T	MTU0	TGIF0	Edge	○	×	×	×	×	IER10.IEN4	IPR130	—
	RX24T RX24U	MTU3	TGID3			○					IPR129	DTCER132
133	RX63T	MTU1	TGIA1	Edge	○	○	○	×	×	IER10.IEN5	IPR133	DTCER133
	RX24T RX24U	MTU3	TCIV3			×	×					—
134	RX63T	MTU1	TGIB1	Edge	○	○	○	×	×	IER10.IEN6	IPR133	DTCER134
	RX24T RX24U	MTU4	TGIA4				×				IPR134	

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
135	RX63T	MTU1	TCIV1	Edge	○	×	×	×	×	IER10.IEN7	IPR135	—
	RX24T RX24U	MTU4	TGIB4			○					IPR134	DTCER135
136	RX63T	MTU1	TCIU1	Edge	○	×	×	×	×	IER11.IEN0	IPR135	—
	RX24T RX24U	MTU4	TGIC4			○					IPR134	DTCER136
137	RX63T	MTU2	TGIA2	Edge	○	○	○	×	×	IER11.IEN1	IPR137	DTCER137
	RX24T RX24U	MTU4	TGID4				×				IPR134	
138	RX63T	MTU2	TGIB2	Edge	○	○	○	×	×	IER11.IEN2	IPR137	DTCER138
	RX24T RX24U	MTU4	TCIV4				×				IPR138	
139	RX63T	MTU2	TCIV2	Edge	○	×	×	×	×	IER11.IEN3	IPR139	—
	RX24T RX24U	MTU5	TGIU5			○						DTCER139
140	RX63T	MTU2	TCIU2	Edge	○	×	×	×	×	IER11.IEN4	IPR139	—
	RX24T RX24U	MTU5	TGIV5			○						DTCER140
141	RX63T	MTU3	TGIA3	Edge	○	○	○	×	×	IER11.IEN5	IPR141	DTCER141
	RX24T RX24U	MTU5	TGIW5				×				IPR139	
142	RX63T	MTU3	TGIB3	Edge	○	○	○	×	×	IER11.IEN6	IPR141	DTCER142
	RX24T RX24U	MTU6	TGIA6				×				IPR142	
143	RX63T	MTU3	TGIC3	Edge	○	○	○	×	×	IER11.IEN7	IPR141	DTCER143
	RX24T RX24U	MTU6	TGIB6				×				IPR142	
144	RX63T	MTU3	TGID3	Edge	○	○	○	×	×	IER12.IEN0	IPR141	DTCER144
	RX24T RX24U	MTU6	TGIC6				×				IPR142	
145	RX63T	MTU3	TCIV3	Edge	○	×	×	×	×	IER12.IEN1	IPR145	—
	RX24T RX24U	MTU6	TGID6			○					IPR142	DTCER145
146	RX63T	MTU4	TGIA4	Edge	○	○	○	×	×	IER12.IEN2	IPR146	DTCER146
	RX24T RX24U	MTU6	TCIV6			×	×				IPR146	—
147	RX63T	MTU4	TGIB4	Edge	○	○	○	×	×	IER12.IEN3	IPR146	DTCER147
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
148	RX63T	MTU4	TGIC4	Edge	○	○	○	×	×	IER12.IEN4	IPR146	DTCER148
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
149	RX63T	MTU4	TGID4	Edge	○	○	○	×	×	IER12.IEN5	IPR146	DTCER149
	RX24T RX24U	MTU7	TGIA7				×				IPR149	
150	RX63T	MTU4	TCIV4	Edge	○	○	○	×	×	IER12.IEN6	IPR150	DTCER150
	RX24T RX24U	MTU7	TGIB7				×				IPR149	
151	RX63T	MTU5	TGIU5	Edge	○	○	○	×	×	IER12.IEN7	IPR151	DTCER151
	RX24T RX24U	MTU7	TGIC7				×					
152	RX63T	MTU5	TGIV5	Edge	○	○	○	×	×	IER13.IEN0	IPR151	DTCER152
	RX24T RX24U	MTU7	TGID7				×					
153	RX63T	MTU5	TGIW5	Edge	○	○	○	×	×	IER13.IEN1	IPR151	DTCER153
	RX24T RX24U	MTU7	TCIV7				×				IPR153	
154	RX63T	MTU6	TGIA6	Edge	○	○	○	×	×	IER13.IEN2	IPR154	DTCER154
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
155	RX63T	MTU6	TGIB6	Edge	○	○	○	×	×	IER13.IEN3	IPR154	DTCER155
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
156	RX63T	MTU6	TGIC6	Edge	○	○	○	×	×	IER13.IEN4	IPR154	DTCER156
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
157	RX63T	MTU6	TGID6	Edge	○	○	○	×	×	IER13.IEN5	IPR154	DTCER157
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
158	RX63T	MTU6	TCIV6	Edge	○	×	×	×	×	IER13.IEN6	IPR158	—
	RX24T RX24U	—	Reserved	—	×					—	—	
159	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	MTU9	TGIA9	Edge	○	○				IER13.IEN7	IPR159	DTCER159
160	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	MTU9	TGIB9	Edge	○	○				IER14.IEN0	IPR159	DTCER160
161	RX63T	MTU7	TGIA7	Edge	○	○	○	×	×	IER14.IEN1	IPR161	DTCER161
	RX24T RX24U	MTU9	TGIC9				×				IPR159	
162	RX63T	MTU7	TGIB7	Edge	○	○	○	×	×	IER14.IEN2	IPR161	DTCER162
	RX24T RX24U	MTU9	TGID9				×				IPR159	

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
163	RX63T	MTU7	TGIC7	Edge	○	○	○	×	×	IER14.IEN3	IPR163	DTCER163
	RX24T RX24U	MTU9	TCIV9			×	×					—
164	RX63T	MTU7	TGID7	Edge	○	○	○	×	×	IER14.IEN4	IPR163	DTCER164
	RX24T RX24U	MTU9	TGIE9			×	×					—
165	RX63T	MTU7	TCIV7	Edge	○	○	○	×	×	IER14.IEN5	IPR165	DTCER165
	RX24T RX24U	MTU9	TGIF9			×	×				IPR163	—
166	RX63T	POE	OEI1	Level	○	×	×	×	×	IER14.IEN6	IPR166	—
	RX24T RX24U	—	Reserved	—	×					—	—	
167	RX63T	POE	OEI2	Level	○	×	×	×	×	IER14.IEN7	IPR166	—
	RX24T RX24U	—	Reserved	—	×					—	—	
168	RX63T	POE	OEI3	Level	○	×	×	×	×	IER15.IEN0	IPR166	—
	RX24T RX24U		OEI1								IPR168	
169	RX63T	POE	OEI4	Level	○	×	×	×	×	IER15.IEN1	IPR166	—
	RX24T RX24U		OEI2								IPR168	
170	RX63T	POE	OEI5	Level	○	×	×	×	×	IER15.IEN2	IPR166	—
	RX24T RX24U		OEI3								IPR168	
171	RX63T	Comparator	CMP0	Edge	○	○	○	×	×	IER15.IEN3	IPR171	DTCER171
	RX24T RX24U	POE	OEI4	Level		×	×				IPR168	—
172	RX63T	Comparator	CMP1	Edge	○	○	○	×	×	IER15.IEN4	IPR172	DTCER172
	RX24T RX24U	POE	OEI5	Level		×	×				IPR168	—
173	RX63T	Comparator	CMP2	Edge	○	○	○	×	×	IER15.IEN5	IPR173	DTCER173
	RX24T RX24U	CMPC3	CMPC3				×					
174	RX63T	GPT4	GTCIA4	Edge	○	○	○	×	×	IER15.IEN6	IPR174	DTCER174
	RX24T RX24U	TMR0	CMIA0				×					
175	RX63T	GPT4	GTCIB4	Edge	○	○	○	×	×	IER15.IEN7	IPR174	DTCER175
	RX24T RX24U	TMR0	CMIB0				×					
176	RX63T	GPT4	GTCIC4	Edge	○	○	○	×	×	IER16.IEN0	IPR174	DTCER176
	RX24T RX24U	TMR0	OVI0			×	×					—

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
177	RX63T	GPT4	GTCIE4	Edge	○	○	○	×	×	IER16.IEN1	IPR177	DTCER177
	RX24T RX24U	TMR1	CMIA1				×					
178	RX63T	GPT4	GTCIV4	Edge	○	○	○	×	×	IER16.IEN2	IPR177	DTCER178
	RX24T RX24U	TMR1	CMIB1				×					
179	RX63T	GPT4	LOCOI4	Edge	○	○	○	×	×	IER16.IEN3	IPR177	DTCER179
	RX24T RX24U	TMR1	OVI1			×	×					—
180	RX63T	GPT5	GTCIA5	Edge	○	○	○	×	×	IER16.IEN4	IPR180	DTCER180
	RX24T RX24U	TMR2	CMIA2				×					
181	RX63T	GPT5	GTCIB5	Edge	○	○	○	×	×	IER16.IEN5	IPR180	DTCER181
	RX24T RX24U	TMR2	CMIB2				×					
182	RX63T	GPT5	GTCIC5	Edge	○	○	○	×	×	IER16.IEN6	IPR180	DTCER182
	RX24T RX24U	TMR2	OVI2			×	×					—
183	RX63T	GPT5	GTCIE5	Edge	○	○	○	×	×	IER16.IEN7	IPR183	DTCER183
	RX24T RX24U	TMR3	CMIA3				×					
184	RX63T	GPT5	GTCIV5	Edge	○	○	○	×	×	IER17.IEN0	IPR183	DTCER184
	RX24T RX24U	TMR3	CMIB3				×					
185	RX63T	GPT6	GTCIA6	Edge	○	○	○	×	×	IER17.IEN1	IPR185	DTCER185
	RX24T RX24U	TMR3	OVI3			×	×				IPR183	—
186	RX63T	GPT6	GTCIB6	Edge	○	○	○	×	×	IER17.IEN2	IPR185	DTCER186
	RX24T RX24U	TMR4	CMIA4				×				IPR186	
187	RX63T	GPT6	GTCIC6	Edge	○	○	○	×	×	IER17.IEN3	IPR185	DTCER187
	RX24T RX24U	TMR4	CMIB4				×				IPR186	
188	RX63T	GPT6	GTCIE6	Edge	○	○	○	×	×	IER17.IEN4	IPR188	DTCER188
	RX24T RX24U	TMR4	OVI4			×	×				IPR186	—
189	RX63T	GPT6	GTCIV6	Edge	○	○	○	×	×	IER17.IEN5	IPR188	DTCER189
	RX24T RX24U	TMR5	CMIA5				×				IPR189	
190	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	TMR5	CMIB5	Edge	○	○				IER17.IEN6	IPR189	DTCER190

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
191	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	TMR5	OVI5	Edge	○					IER17.IEN7	IPR189	
192	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	TMR6	CMIA6	Edge	○	○				IER18.IEN0	IPR192	DTCER192
193	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	TMR6	CMIB6	Edge	○	○				IER18.IEN1	IPR192	DTCER193
194	RX63T	RIIC0	EEI0	Level	○	×	×	×	×	IER18.IEN2	IPR194	—
	RX24T RX24U	TMR6	OVI6	Edge							IPR192	
195	RX63T	RIIC0	RXI0	Edge	○	○	○	×	×	IER18.IEN3	IPR194	DTCER195
	RX24T RX24U	TMR7	CMIA7				×				IPR195	
196	RX63T	RIIC0	TXI0	Edge	○	○	○	×	×	IER18.IEN4	IPR194	DTCER196
	RX24T RX24U	TMR7	CMIB7				×				IPR195	
197	RX63T	RIIC0	TEI0	Level	○	×	×	×	×	IER18.IEN5	IPR194	—
	RX24T RX24U	TMR7	OVI7	Edge							IPR195	
198	RX63T	DMAC	DMAC0I	Edge	○	○	×	×	×	IER18.IEN6	IPR198	DTCER198
	RX24T RX24U	—	Reserved	—	×	×				—	—	—
199	RX63T	DMAC	DMAC1I	Edge	○	○	×	×	×	IER18.IEN7	IPR199	DTCER199
	RX24T RX24U	—	Reserved	—	×	×				—	—	—
200	RX63T	DMAC	DMAC2I	Edge	○	○	×	×	×	IER19.IEN0	IPR200	DTCER200
	RX24T RX24U	—	Reserved	—	×	×				—	—	—
201	RX63T	DMAC	DMAC3I	Edge	○	○	×	×	×	IER19.IEN1	IPR201	DTCER201
	RX24T RX24U	—	Reserved	—	×	×				—	—	—
202	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GDTE1	Edge	○					IER19.IEN2	IPR202	
203	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIE1	Edge	○	○				IER19.IEN3	IPR203	DTCER203
204	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIF1	Edge	○	○				IER19.IEN4	IPR204	DTCER204

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
205	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIV1	Edge	○	○				IER19.IEN5	IPR205	DTCER205
206	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIU1	Edge	○	○				IER19.IEN6	IPR206	DTCER206
207	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIA2	Edge	○	○				IER19.IEN7	IPR207	DTCER207
208	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIB2	Edge	○	○				IER1A.IEN0	IPR208	DTCER208
209	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIC2	Edge	○	○				IER1A.IEN1	IPR209	DTCER209
210	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCID2	Edge	○	○				IER1A.IEN2	IPR210	DTCER210
211	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GDTE2	Edge	○					IER1A.IEN3	IPR211	
212	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIE2	Edge	○	○				IER1A.IEN4	IPR212	DTCER212
213	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIF2	Edge	○	○				IER1A.IEN5	IPR213	DTCER213
214	RX63T	SCI0	RXI0	Edge	○	○	○	×	×	IER1A.IEN6	IPR214	DTCER214
	RX24T RX24U	GPT2	GTCIV2				×					
215	RX63T	SCI0	TXI0	Edge	○	○	○	×	×	IER1A.IEN7	IPR214	DTCER215
	RX24T RX24U	GPT2	GTCIU2				×				IPR215	
216	RX63T	SCI0	TEI0	Level	○	×	×	×	×	IER1B.IEN0	IPR214	—
	RX24T RX24U	GPT3	GTCIA3	Edge		○					IPR216	DTCER216
217	RX63T	SCI1	RXI1	Edge	○	○	○	×	×	IER1B.IEN1	IPR217	DTCER217
	RX24T RX24U	GPT3	GTCIB3				×					
218	RX63T	SCI1	TXI1	Edge	○	○	○	×	×	IER1B.IEN2	IPR217	DTCER218
	RX24T RX24U		ERI1	Level		×	×				IPR218	—

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
219	RX63T	SCI1	TEI1	Level	○	×	×	×	×	IER1B.IEN3	IPR217	—
	RX24T RX24U		RXI1	Edge		○					IPR218	DTCER219
220	RX63T	SCI2	RXI2	Edge	○	○	○	×	×	IER1B.IEN4	IPR220	DTCER220
	RX24T RX24U	SCI1	TXI1				×				IPR218	
221	RX63T	SCI2	TXI2	Edge	○	○	○	×	×	IER1B.IEN5	IPR220	DTCER221
	RX24T RX24U	SCI1	TEI1	Level		×	×				IPR218	—
222	RX63T	SCI2	TEI2	Level	○	×	×	×	×	IER1B.IEN6	IPR220	—
	RX24T RX24U	SCI5	ERI5								IPR222	
223	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	SCI5	RXI5	Edge	○	○				IER1B.IEN7	IPR222	DTCER223
224	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	SCI5	TXI5	Edge	○	○				IER1C.IEN0	IPR222	DTCER224
225	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	SCI5	TEI5	Level	○					IER1C.IEN1	IPR222	
226	RX63T	GPT0	GTCIA0	Edge	○	○	○	×	×	IER1C.IEN2	IPR226	DTCER226
	RX24T RX24U	SCI6	ERI6	Level		×	×					—
227	RX63T	GPT0	GTCIB0	Edge	○	○	○	×	×	IER1C.IEN3	IPR226	DTCER227
	RX24T RX24U	SCI6	RXI5				×					
228	RX63T	GPT0	GTCIC0	Edge	○	○	○	×	×	IER1C.IEN4	IPR226	DTCER228
	RX24T RX24U	SCI6	TXI6				×					
229	RX63T	GPT0	GTCIE0	Edge	○	○	○	×	×	IER1C.IEN5	IPR229	DTCER229
	RX24T RX24U	SCI6	TEI6	Level		×	×				IPR226	—
230	RX63T	GPT0	GTCIV0	Edge	○	○	○	×	×	IER1C.IEN6	IPR229	DTCER230
	RX24T/ RX24U	—	Reserved	—	×	×	×			—	—	—
231	RX63T	GPT0	LOCOI0	Edge	○	○	○	×	×	IER1C.IEN7	IPR229	DTCER231
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
232	RX63T	GPT1	GTCIA1	Edge	○	○	○	×	×	IER1D.IEN0	IPR232	DTCER232
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
233	RX63T	GPT1	GTCIB1	Edge	○	○	○	×	×	IER1D.IEN1	IPR232	DTCER233
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
234	RX63T	GPT1	GTCIC1	Edge	○	○	○	×	×	IER1D.IEN2	IPR232	DTCER234
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
235	RX63T	GPT1	GTCIE1	Edge	○	○	○	×	×	IER1D.IEN3	IPR235	DTCER235
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
236	RX63T	GPT1	GTCIV1	Edge	○	○	○	×	×	IER1D.IEN4	IPR235	DTCER236
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
238	RX63T	GPT2	GTCIA2	Edge	○	○	○	×	×	IER1D.IEN6	IPR238	DTCER238
	RX24T RX24U	GPT3	GTCIC3				×					
239	RX63T	GPT2	GTCIB2	Edge	○	○	○	×	×	IER1D.IEN7	IPR238	DTCER239
	RX24T RX24U	GPT3	GTCID3				×				IPR239	
240	RX63T	GPT2	GTCIC2	Edge	○	○	○	×	×	IER1E.IEN0	IPR238	DTCER240
	RX24T RX24U	GPT3	GDTE3			×	×				IPR240	—
241	RX63T	GPT2	GTCIE2	Edge	○	○	○	×	×	IER1E.IEN1	IPR241	DTCER241
	RX24T RX24U	GPT3	GTCIE3				×					
242	RX63T	GPT2	GTCIV2	Edge	○	○	○	×	×	IER1E.IEN2	IPR241	DTCER242
	RX24T RX24U	GPT3	GTCIF3				×				IPR242	
243	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	GPT3	GTCIV3	Edge	○	○				IER1E.IEN3	IPR243	DTCER243
244	RX63T	GPT3	GTCIA3	Edge	○	○	○	×	×	IER1E.IEN4	IPR244	DTCER244
	RX24T RX24U	GPT3	GTCIU3				×					
245	RX63T	GPT3	GTCIB3	Edge	○	○	○	×	×	IER1E.IEN5	IPR244	DTCER245
	RX24T RX24U	—	Reserved	—	×	×	×			—	—	—
246	RX63T	GPT3	GTCIC3	Edge	○	○	○	×	×	IER1E.IEN6	IPR244	DTCER246
	RX24T RX24U	RIIC0	EEI0	Level		×	×				IPR246	
247	RX63T	GPT3	GTCIE3	Edge	○	○	○	×	×	IER1E.IEN7	IPR247	DTCER247
	RX24T RX24U	RIIC0	RXI0				×					

Vector No.	RX63T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER
248	RX63T	GPT3	GTCIV3	Edge	○	○	○	×	×	IER1F.IEN0	IPR247	DTCER248
	RX24T RX24U	RIIC0	TXI0				×				IPR248	
249	RX63T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24T RX24U	RIIC0	TEI0	Level	○					IER1F.IEN1	IPR249	
250	RX63T	SCI12	RXI12	Edge	○	○	○	×	×	IER1F.IEN2	IPR250	DTCER250
	RX24T	—	Reserved	—	×	×	×			—	—	—
	RX24U	SCI11	ERI11	Level	○	×	×			IER1F.IEN2	IPR250	
251	RX63T	SCI12	TXI12	Edge	○	○	○	×	×	IER1F.IEN3	IPR250	DTCER251
	RX24T	—	Reserved	—	×	×	×			—	—	—
	RX24U	SCI11	RXI11	Edge	○	○	×			IER1F.IEN3	IPR250	DTCER251
252	RX63T	SCI12	TEI12	Level	○	×	×	×	×	IER1F.IEN4	IPR250	—
	RX24T	—	Reserved	—	×					—	—	
	RX24U	SCI11	TXI11	Edge	○	○				IER1F.IEN4	IPR250	DTCER252
253	RX63T RX24T	—	Reserved	—	×	×	×	×	×	—	—	—
	RX24U	SCI11	TEI11	Level	○					IER1F.IEN5	IPR250	

4.4.10 Buses

Table 4.27 lists the points of difference between the buses, and Table 4.28 lists the points of difference in between the I/O registers related to the buses.

Table 4.27 Points of Difference between Buses

Item	RX63T	RX24T and RX24U
Internal main bus 2	• Connected to DTC and DMAC • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to DTC • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).
Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4). • Operates in synchronization with the peripheral module clock (PCLKB).
Internal peripheral bus 3	• Connected to peripheral modules (USB). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (RSCAN and CMPC). • Operates in synchronization with the peripheral module clock (PCLKB).
Internal peripheral bus 4	• Connected to peripheral modules (MTU3, GPT, and DPC) • Operates in synchronization with the peripheral module clock (PCLKA).	• Connected to peripheral modules (MTU3, GPT, and SCI11 (RX24U)) • Operates in synchronization with the peripheral module clock (PCLKA).
Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash. • Operates in synchronization with the FlashIF clock (FCLK).	• Connected to the flash control module and E2 DataFlash. • Operates in synchronization with the FlashIF clock (FCLK).
CS area	• Connected to external device • Operates in synchronization with the external-bus clock (BCLK)	Not available

Table 4.28 Points of Difference between I/O Registers Related to Buses

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
CSnCR n = 0 to 3	—	CSn control register	Register not available
CSnREC n = 0 to 3	—	CSn recovery cycle register	Register not available
CSRECEN	—	CS recovery cycle insertion enable register	Register not available
CSnMOD n = 0 to 3	—	CSn mode register	Register not available
CSnWCR1 n = 0 to 3	—	CSn wait control register 1	Register not available
CSnWCR2 n = 0 to 3	—	CSn wait control register 2	Register not available
BERSR1	MST[2:0]	Bus master code bits 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPEB[1:0]	External bus priority control bits	Reserved

4.4.11 Memory-Protection Unit

Table 4.29 lists the I/O registers related to the memory-protection unit.

Table 4.29 Points of difference between I/O Registers Related to the Memory-Protection Units

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
MPESTS	IA (RX63T) IMPER (RX24T and RX24U)	Instruction memory-protection error generated bit	Instruction memory-protection error generated bit
	DA (RX63T) DMPER (RX24T and RX24U)	Data memory-protection error generated bit	Data memory-protection error generated bit

4.4.12 I/O Ports

Table 4.30 lists the points of difference between the I/O ports and Table 4.31 lists the points of difference between the I/O registers related to the I/O ports.

Table 4.30 Points of Difference between I/O Ports

Item	Port Symbol	RX63T	RX24T	RX24U
Ports	PORT0	P00, P01, —	P00, P01, P02	
	PORT2	P20, P21, P22, P23, P24, —		P20, P21, P22, P23, P24, P27
	PORT3	P30, P31, P32, P33	P30, P31, P32, P33, P36, P37	
	PORT5	P50, P51, P52, P53, P54, P55		—, —, P52, P53, P54, P55
Input pull-up function	PORT0	P00, P01, — Not available	P00, P01, P02 Available	
	PORT1	P10, P11 Not available	P10, P11 Available	
	PORT2	P20 to P24, — Not available	P20 to P24, — Available	P20 to P24, P27 Available
	PORT3	P30 to P33, —, — Not available	P30 to P33, P36, P37 Available	
	PORT4	P40 to P47 Not available	P40 to P47 Available	
	PORT5	P50, P51, P52 to P55 Not available	P50, P51, P52 to P55 Available	—, —, P52 to P55 Available
	PORT6	P60 to P65 Not available	P60 to P65 Available	
	PORT7	P70 to P76 Not available	P70 to P76 Available	
	PORT8	P80 to P82 Not available	P80 to P82 Available	
	PORT9	P90 to P96 Not available	P90 to P96 Available	
	PORTA	PA0 to PA5 Not available	PA0 to PA5 Available	

Item	Port Symbol	RX63T	RX24T	RX24U
Input pull-up function	PORTB	PB0 to PB7 Not available	PB0 to PB7 Available	
	PORTD	PD0 to PD7 Not available	PD0 to PD7 Available	
	PORTE	PE0, PE1, PE3 to PE5 Not available	PE0, PE1, PE3 to PE5 Available	
Open drain output	PORT0	P00, P01, — Not available	P00, P01, P02 Available	
	PORT1	P10, P11 Not available	P10, P11 Available	
	PORT2	P20, P21, P24, — Not available	P20, P21, P24, — Available	P20, P21, P24, P27 Available
	PORT3	P30 to P33, —, — Not available	P30 to P33, P36, P37 Available	
	PORT7	P70 to P76 Not available	P70 to P76 Available	
	PORT8	P82 Not available	P82 Available	
	PORT9	P90 to P94 Not available	P90 to P94 Available	
	PORTA	PA0, PA3 Not available	PA0, PA3 Available	
	PORTB	PB0, PB3, PB4, PB7 Not available	PB0, PB3, PB4, PB7 Available	
	PORTD	PD0 to PD2, PD4, PD6, PD7 Not available	PD0 to PD2, PD4, PD6, PD7 Available	
	PORTE	PE0, PE1, PE3 to PE5 Not available	PE0, PE1, PE3 to PE5 Available	
Drive Capacity Switching	PORT1	P10 Not available	P10 Available	
	PORT8	P81 Available P82 Not available	P81 Not available P82 Available	
	PORTB	PB5 Available	PB5 Not available	
	PORTD	PD4, PD5 Not available	PD4, PD5 Available	
Large-current pins	PORT8	P81 Not available	P81 Available	
	PORTB	PB5 Not available	PB5 Available	
	PORTD	PD3 Not available	PD3 Available	
5 V tolerant	PORTB	PB1, PB2 Not available	PB1, PB2 Available	

Table 4.31 Points of Difference between I/O Registers Related to I/O Ports

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
DSCR1	—	Drive capacity control register 1	Register not available
DSCR2	—	Drive capacity control register 2	Register not available
PCR	—	Register not available	Pull-up control register
DSCR	—	Register not available	Drive capacity control register

4.4.13 Multi-Function Pin Controller

Table 4.32 lists points of difference between multi-function pin assignments, and Table 4.33 lists points of difference between I/O registers related to the multi-function pin controller.

Table 4.32 Points of Difference between Multi-Function Pin Assignment

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
Interrupts		NMI (input)	PE2	PE2	PE2
	IRQ0	IRQ0-DS (input)	P10	—	—
		IRQ0 (input)	—	P10	P10
			—	P52	P52
			PE5	PE5	PE5
	IRQ1	IRQ1-DS (input)	P11	—	—
		IRQ1 (input)	—	P11	P11
			—	P53	P53
			—	PA5	PA5
			PE4	PE4	PE4
	IRQ2	IRQ2-DS (input)	PE3	—	—
		IRQ2 (input)	—	P00	P00
			—	P54	P54
			PB6	—	—
			—	PD4	PD4
			—	PE3	PE3
	IRQ3	IRQ3-DS (input)	PB4	—	—
		IRQ3 (input)	—	P55	P55
			P82	—	—
			—	PB4	PB4
			—	PD5	PD5
	IRQ4	IRQ4-DS (input)	P96	—	—
		IRQ4 (input)	—	P01	P01
			P24	—	—
			—	P60	P60
			—	P96	P96
			PB1	—	—
	IRQ5	IRQ5-DS (input)	P70	—	—
		IRQ5 (input)	—	P02	P02
			—	P61	P61
			—	P70	P70
			P80	—	—
			—	PB6	PB6
			—	PD6	PD6
	IRQ6	IRQ6-DS (input)	P21	—	—
		IRQ6 (input)	—	P21	P21
			—	P31	P31
			—	P62	P62
			PD5	—	—

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
Interrupts	IRQ7	IRQ7-DS (input)	P20	—	—
		IRQ7 (input)	—	P20	P20
			—	P30	P30
			—	P63	P63
			PE0	—	—
Multi-function timer unit 3	MTU0	MTIOC0A (input/output) (RX63T) MTIOC0A/MTIOC0A# (input/output) (RX24T/24U)	P31	P31	P31
			PB3	PB3	PB3
		MTIOC0B (input/output) (RX63T) MTIOC0B/MTIOC0B# (input/output) (RX24T/24U)	P30	P30	P30
			PB2	PB2	PB2
		MTIOC0C (input/output) (RX63T) MTIOC0C/MTIOC0C# (input/output) (RX24T/24U)	PB1	PB1	PB1
		MTIOC0D (input/output) (RX63T) MTIOC0D/MTIOC0D# (input/output) (RX24T/24U)	PB0	PB0	PB0
	MTU1	MTIOC1A (input/output) (RX63T)	—	—	P27
		MTIOC1A/MTIOC1A# (input/output) (RX24T/24U)	PA5	PA5	PA5
		MTIOC1B (input/output) (RX63T) MTIOC1B/MTIOC1B# (input/output) (RX24T/24U)	PA4	PA4	PA4
	MTU2	MTIOC2A (input/output) (RX63T) MTIOC2A/MTIOC2A# (input/output) (RX24T/24U)	PA3	PA3	PA3
		MTIOC2B (input/output) (RX63T) MTIOC2B/MTIOC2B# (input/output) (RX24T/24U)	PA2	PA2	PA2
	MTU3	MTIOC3A (input/output) (RX63T)	—	P11	P11
		MTIOC3A/MTIOC3A# (input/output) (RX24T/24U)	P33	P33	P33
		MTIOC3B (input/output) (RX63T) MTIOC3B/MTIOC3B# (input/output) (RX24T/24U)	P71	P71	P71
		MTIOC3C (input/output) (RX63T) MTIOC3C/MTIOC3C# (input/output) (RX24T/24U)	P32	P32	P32
		MTIOC3D (input/output) (RX63T) MTIOC3D/MTIOC3D# (input/output) (RX24T/24U)	P74	P74	P74

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
Multi-function timer unit 3	MTU4	MTIOC4A (input/output) (RX63T) MTIOC4A/MTIOC4A# (input/output) (RX24T/24U)	P72	P72	P72
		MTIOC4B (input/output) (RX63T) MTIOC4B/MTIOC4B# (input/output) (RX24T/24U)	P73	P73	P73
		MTIOC4C (input/output) (RX63T) MTIOC4C/MTIOC4C# (input/output) (RX24T/24U)	P75	P75	P75
		MTIOC4D (input/output) (RX63T) MTIOC4D/MTIOC4D# (input/output) (RX24T/24U)	P76	P76	P76
	MTU5	MTIC5U (input) (RX63T)	—	P24	P24
		MTIC5U/MTIC5U# (input) (RX24T/24U)	P82	P82	P82
		MTIC5V (input) (RX63T)	—	P23	P23
		MTIC5V/MTIC5V# (input) (RX24T/24U)	P81	P81	P81
		MTIC5W (input) (RX63T)	—	P22	P22
		MTIC5W/MTIC5W# (input) (RX24T/24U)	P80	P80	P80
	MTU6	MTIOC6A (input/output) (RX63T) MTIOC6A/MTIOC6A# (input/output) (RX24T/24U)	PA1	PA1	PA1
		MTIOC6B (input/output) (RX63T) MTIOC6B/MTIOC6B# (input/output) (RX24T/24U)	P95	P95	P95
		MTIOC6C (input/output) (RX63T) MTIOC6C/MTIOC6C# (input/output) (RX24T/24U)	PA0	PA0	PA0
		MTIOC6D (input/output) (RX63T) MTIOC6D/MTIOC6D# (input/output) (RX24T/24U)	P92	P92	P92
	MTU7	MTIOC7A (input/output) (RX63T) MTIOC7A/MTIOC7A# (input/output) (RX24T/24U)	P94	P94	P94
		MTIOC7B (input/output) (RX63T) MTIOC7B/MTIOC7B# (input/output) (RX24T/24U)	P93	P93	P93
		MTIOC7C (input/output) (RX63T) MTIOC7C/MTIOC7C# (input/output) (RX24T/24U)	P91	P91	P91
		MTIOC7D (input/output) (RX63T) MTIOC7D/MTIOC7D# (input/output) (RX24T/24U)	P90	P90	P90

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
Multi-function timer unit 3	MTU9	MTIOC9A/MTIOC9A# (input/output)	—	P21	P21
			—	PD7	PD7
		MTIOC9B/MTIOC9B# (input/output)	—	P10	P10
			—	PE0	PE0
		MTIOC9C/MTIOC9C# (input/output)	—	P20	P20
			—	PD6	PD6
		MTIOC9D/MTIOC9D# (input/output)	—	P02	P02
			—	PE1	PE1
	MTU	MTCLKA (input) (RX63T) MTCLKA/MTCLKA# (input) (RX24T/24U)	P21	P21	P21
			P33	P33	P33
		MTCLKB (input) (RX63T) MTCLKB/MTCLKB# (input) (RX24T/24U)	P20	P20	P20
			P32	P32	P32
		MTCLKC (input) (RX63T) MTCLKC/MTCLKC# (input) (RX24T/24U)	P11	P11	P11
			P31	P31	P31
			PE4	PE4	PE4
		MTCLKD (input) (RX63T) MTCLKD/MTCLKD# (input) (RX24T/24U)	P10	P10	P10
			P30	P30	P30
			PE3	PE3	PE3
		ADSM0 (output)	—	PB2	PB2
		ADSM1 (output)	—	PB1	PB1
Port output enable 3	POE0	POE0# (input)	P70	P70	P70
	POE4	POE4# (input)	P96	P96	P96
	POE8	POE8# (input)	PB4	PB4	PB4
	POE10	POE10# (input)	PE2	PE2	PE2
			PE4	PE4	PE4
	POE11	POE11# (input)	PE3	PE3	PE3
	POE12	POE12# (input)	—	P01	P01
			—	P10	P10
General PWM timer	GPT0	GTIOC0A (input/output) (RX63T) GTIOC0A/GTIOC0A# (input/output) (RX24T/24U)	P71	P71	P71
			—	PD2	PD2
			PD7	—	—
		GTIOC0B (input/output) (RX63T) GTIOC0B/GTIOC0B# (input/output) (RX24T/24U)	P74	P74	P74
			—	PD1	PD1
			PD6	—	—
	GPT1	GTIOC1A (input/output) (RX63T) GTIOC1A/GTIOC1A# (input/output) (RX24T/24U)	P72	P72	P72
			—	PD0	PD0
			PD5	—	—
		GTIOC1B (input/output) (RX63T) GTIOC1B/GTIOC1B# (input/output) (RX24T/24U)	P75	P75	P75
			—	PB7	PB7
			PD4	—	—
	GPT2	GTIOC2A (input/output) (RX63T) GTIOC2A/GTIOC2A# (input/output) (RX24T/24U)	P73	P73	P73
			—	PB6	PB6
			PD3	—	—
		GTIOC2B (input/output) (RX63T) GTIOC2B/GTIOC2B# (input/output) (RX24T/24U)	P76	P76	P76
			—	PB5	PB5
			PD2	—	—

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
General PWM timer	GPT3	GTIOC3A (input/output) (RX63T)	PD1	—	—
		GTIOC3A/GTIOC3A# (input/output) (RX24T/24U)	—	PD7	PD7
		GTIOC3B (input/output) (RX63T)	PD0	—	—
		GTIOC3B/GTIOC3B# (input/output) (RX24T/24U)	—	PD6	PD6
	GPT4	GTIOC4A (input/output)	P95	—	—
		GTIOC4B (input/output)	P92	—	—
	GPT5	GTIOC5A (input/output)	P94	—	—
		GTIOC5B (input/output)	P91	—	—
	GPT6	GTIOC6A (input/output)	P93	—	—
		GTIOC6B (input/output)	P90	—	—
	GPT	GTECLKA (input)	—	PD5	PD5
		GTECLKB (input)	—	PD4	PD4
		GTECLKC (input)	—	PD3	PD3
		GTECLKD (input)	—	PB4	PB4
		GTETRG/GTETRG0 (RX63T) GTETRG (input) (RX24T/24U)	PB4	PB4	PB4
		GTADSM0 (output)	—	PA3	PA3
		GTADSM1 (output)	—	PA2	PA2
8-bit timer	TMR0	TMO0 (output)	—	P33	P33
			—	PB0	PB0
			—	PD3	PD3
		TMCI0 (input)	—	PB1	PB1
			—	PD4	PD4
		TMRI0 (input)	—	PB2	PB2
			—	PD5	PD5
	TMR1	TMO1 (output)	—	PD6	PD6
		TMCI1 (input)	—	PD2	PD2
			—	PE0	PE0
		TMRI1 (input)	—	PD7	PD7
	TMR2	TMO2 (output)	—	P23	P23
			—	PA0	PA0
			—	PD1	PD1
		TMCI2 (input)	—	P24	P24
		TMRI2 (input)	—	P22	P22
	TMR3	TMO3 (output)	—	P11	P11
		TMCI3 (input)	—	PA5	PA5
		TMRI3 (input)	—	P10	P10
	TMR4	TMO4 (output)	—	P22	P22
			—	P82	P82
			—	PA1	PA1
			—	PD2	PD2
		TMCI4 (input)	—	P21	P21
			—	P81	P81
		TMRI4 (input)	—	P20	P20
			—	P80	P80

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
8-bit timer	TMR5	TMO5 (output)	—	PE1	PE1
		TMCI5 (input)	—	PE0	PE0
		TMRI5 (input)	—	PD7	PD7
	TMR6	TMO6 (output)	—	P24	P24
			—	P32	P32
			—	PD0	PD0
		TMCI6 (input)	—	P30	P30
			—	PD4	PD4
		TMRI6 (input)	—	P31	P31
			—	PD5	PD5
	TMR7	TMO7 (output)	—	PA2	PA2
		TMCI7 (input)	—	PA4	PA4
		TMRI7 (input)	—	PA3	PA3
Serial communications interface	SCI0	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P22	—	—
			PA5	—	—
			PB1	—	—
		TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P23	—	—
			PA4	—	—
			PB2	—	—
		SCK0 (input/output)	P30	—	—
			PA3	—	—
			PB3	—	—
		CTS0# (input)/RTS0# (output)/ SS0# (input)	P01	—	—
			P24	—	—
			PD7	—	—
	SCI1	RXD1 (input)/ SMISO01 (input/output)/ SSCL1 (input/output)	P96	—	—
			PD5	PD5	PD5
		TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P95	—	—
			PD3	PD3	PD3
		SCK1 (input/output)	PD4	PD4	PD4
		CTS1# (input)/RTS1# (output)/ SS1# (input)	P70	—	—
			P94	—	—
			—	P02	P02
			—	PD6	PD6
	SCI2	RXD2 (input)/ SMISO02 (input/output)/ SSCL2 (input/output)	PA2	—	—
		TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	PA1	—	—
		SCK2 (input/output)	PA0	—	—
		CTS2# (input)/RTS2# (output)/ SS2# (input)	P93	—	—

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
Serial communications interface	SCI5	RXD5 (input)/ SMISO05 (input/output)/ SSCL5 (input/output)	—	PB6	PB6
			—	PE0	PE0
		TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	—	PB5	PB5
			—	PD7	PD7
		SCK5 (input/output)	—	PB7	PB7
			—	PD2	PD2
		CTS5# (input)/RTS5# (output)/ SS5# (input)	—	PB4	PB4
			—	PE1	PE1
	SCI6	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	—	P80	P80
			—	PA5	PA5
			—	PB1	PB1
		TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	—	P81	P81
			—	PB0	PB0
			—	PB2	PB2
		SCK6 (input/output)	—	P82	P82
			—	PA4	PA4
			—	PB3	PB3
		CTS6# (input)/RTS6# (output)/ SS6# (input)	—	P10	P10
			—	PA2	PA2
	SCI11	RXD11 (input)/ SMISO011 (input/output)/ SSCL11 (input/output)	—	—	PD5
		TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	—	—	PD3
		SCK11 (input/output)	—	—	PD4
		CTS11# (input)/RTS11# (output)/ SS11# (input)	—	—	PD6
	SCI12	RXD12 (input)/ SMISO012 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P80	—	—
			PB6	—	—
		TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	P81	—	—
			PB5	—	—
		SCK12 (input/output)	P82	—	—
			PB7	—	—
		CTS12# (input)/RTS12# (output)/ SS12# (input)	PE1	—	—

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
I^2C bus interface	RIIC0	SCL0 (input/output)	PB1	PB1	PB1
		SDA0 (input/output)	PB2	PB2	PB2
CAN module	CAN (RX63T) RSCAN0 (RX24T/24U)	CRX1 (input) (RX63T) CRXD0 (input) (RX24T/24U)	P22	—	—
			PB6	—	—
			PE0	—	—
			—	PA1	PA1
		CTX1 (output) (RX63T) CTXD0 (output) (RX24T/24U)	P23	—	—
			PB5	—	—
			PD7	—	—
			—	PA0	PA0
Serial peripheral interface	RSPI0	RSPCKA (input/output)	P24	P24	P24
			PA4	PA4	PA4
			—	PB3	PB3
			PD0	PD0	PD0
		MOSIA (input/output)	P23	P23	P23
			PB0	PB0	PB0
			PD2	PD2	PD2
		MISOA (input/output)	P22	P22	P22
			PA5	PA5	PA5
			PD1	PD1	PD1
		SSLA0 (input/output)	P30	P30	P30
			PA3	PA3	PA3
			PD6	PD6	PD6
		SSLA1 (output)	P31	P31	P31
			PA2	PA2	PA2
			PD7	PD7	PD7
		SSLA2 (output)	P32	P32	P32
			PA1	PA1	PA1
			PE0	PE0	PE0
		SSLA3 (output)	P33	P33	P33
			PA0	PA0	PA0
			PE1	PE1	PE1

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
Serial peripheral interface	RSPI1	RSPCKB (input/output)	P24	—	—
			PA4	—	—
			PD0	—	—
		MOSIB (input/output)	P23	—	—
			PB0	—	—
			PD2	—	—
		MISOB (input/output)	P22	—	—
			PA5	—	—
			PD1	—	—
		SSLB0 (input/output)	P30	—	—
			PA3	—	—
			PD6	—	—
		SSLB1 (output)	P31	—	—
			PA2	—	—
			PD7	—	—
		SSLB2 (output)	P32	—	—
			PA1	—	—
			PE0	—	—
		SSLB3 (output)	P33	—	—
			PA0	—	—
			PE1	—	—
12-bit A/D converter		AN000 (input)	P40	P40	P40
		AN001 (input)	P41	P41	P41
		AN002 (input)	P42	P42	P42
		AN003 (input)	P43	P43	P43
		AN016 (input)	—	P20	P20
		AN100 (input)	P44	P44	P44
		AN101 (input)	P45	P45	P45
		AN102 (input)	P46	P46	P46
		AN103 (input)	P47	P47	P47
		AN116 (input)	—	P21	P21
		AN200 (input)	—	P60	P60
		AN201 (input)	—	P61	P61
		AN202 (input)	—	P62	P62
		AN203 (input)	—	P63	P63
		AN204 (input)	—	P64	P64
		AN205 (input)	—	P65	P65
		AN206 (input)	—	P50	—
		AN207 (input)	—	P51	—
		AN208 (input)	—	P52	P52
		AN209 (input)	—	P53	P53
		AN210 (input)	—	P54	P54
		AN211 (input)	—	P55	P55
		ADTRG0# (input)	P20	P20	P20
			—	PA1	PA1
			PA4	PA4	PA4
		ADTRG1# (input)	P21	P21	P21
			PA5	PA5	PA5

Module/Function	Channel	Pin Function	RX63T	RX24T	RX24U
12-bit A/D converter		ADTRG2# (input)	—	P22	P22
			—	PB0	PB0
		ADST0 (output)	—	P02	P02
			—	PD6	PD6
		ADST1 (output)	—	P00	P00
		ADST2 (output)	—	P01	P01
10-bit A/D converter		AN0 (input)	P60	—	—
		AN1 (input)	P61	—	—
		AN2 (input)	P62	—	—
		AN3 (input)	P63	—	—
		AN4 (input)	P64	—	—
		AN5 (input)	P65	—	—
		AN6 (input)	P50	—	—
		AN7 (input)	P51	—	—
		AN8 (input)	P52	—	—
		AN9 (input)	P53	—	—
		AN10 (input)	P54	—	—
		AN11 (input)	P55	—	—
		ADTRG# (input)	P22	—	—
D/A converter		DA0 (output)	P54	P24	P24
		DA1 (output)	P55	P23	P23
Clock frequency accuracy measurement circuit		CACREF (input)	P00	—	—
			P23	P23	P23
			PB3	PB3	PB3
Comparator		COMP0 (output)	—	P24	P24
		COMP1 (output)	—	P23	P23
		COMP2 (output)	—	P22	P22
		COMP3 (output)	—	P30	P30
		CMPC00 (input)	—	P40	P40
		CMPC01 (input)	—	P40	P40
		CMPC02 (input)	—	P45	P45
		CMPC03 (input)	—	P45	P45
		CMPC10 (input)	—	P44	P44
		CMPC11 (input)	—	P44	P44
		CMPC12 (input)	—	P46	P46
		CMPC13 (input)	—	P46	P46
		CMPC20 (input)	—	P45	P45
		CMPC21 (input)	—	P45	P45
		CMPC22 (input)	—	P40	P40
		CMPC23 (input)	—	P40	P40
		CMPC30 (input)	—	P46	P46
		CMPC31 (input)	—	P46	P46
		CMPC32 (input)	—	P44	P44
		CMPC33 (input)	—	P44	P44

Table 4.33 Points of Difference between I/O Registers Related to Multi-Function Pin Controllers

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
PX2nPFS (n = 0 to 4) (RX63T) (n = 0 to 4) (RX24T) (n = 0 to 4, 7) (RX24U)	ASEL	Reserved	Analog input function select bit
PX5nPFS (n = 0 to 5) (RX63T) (n = 0 to 5) (RX24T) (n=2 to 5) (RX24U)	ISEL	Reserved	Interrupt input function select bit
PX6nPFS (n = 0 to 5)	ISEL	Reserved	Interrupt input function select bit
PX8nPFS (n = 0 to 2)	ISEL	Interrupt input function select bit	Reserved
PXAnPFS (n = 0 to 5)	ISEL	Reserved	Interrupt input function select bit

4.4.14 Multi-Function Timer Pulse Unit 3

Table 4.34 lists the points of difference between the multi-function timer pulse unit 3 modules, and Table 4.35 lists the points of difference between the I/O registers related to the multi-function timer pulse unit 3 modules.

Table 4.34 Points of Difference between Multi-Function Timer Pulse Unit 3 Modules

Item	RX63T	RX24T and RX24U
Pulse input/output	Maximum 24	Maximum 28
Count clocks	6 to 8 clocks for each channel (4 clocks for channel 5)	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and 4 clocks for MTU1 and MTU2 (LWA = 1))
Operating frequency	8 to 100 MHz	Up to 80MHz
Available operations	[MTU0 to MTU4, MTU6, and MTU7] • Waveform output on compare match • Input capture function • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, and MTU9] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, and MTU7] Buffer operation specifiable	[MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9] Buffer operation specifiable
	[MTU1 and MTU2] • Phase counting mode can be specified independently. — • Cascade connection operation available	[MTU1 and MTU2] • Phase counting mode can be specified independently. • MTU1 and MTU2 interlocked operation in 32-bit phase counting mode is available (TMDR3.LWA = 1). • Cascade connection operation available

Item	RX63T	RX24T and RX24U
Available operations	[MTU3, MTU4, MTU6, and MTU7] • Through interlocked operation of MTU3/MTU4 and MTU6/MTU7, the positive and negative signals in three phases, for a total of 6 phases, can be output in complementary PWM and reset PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers is supported at peaks and troughs of the timer-counter values or when writing to the buffer registers (MTU4.TGRD and MTU7.TGRD). • Double-buffering is selectable in complementary PWM mode.	[MTU3, MTU4, MTU6, and MTU7] • Through interlocked operation of MTU3/MTU4 and MTU6/MTU7 the positive and negative signals in six phases, for a total of 12 phases, can be output in complementary PWM or reset PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers is supported at peaks and troughs of the timer-counter values or when writing to the buffer registers (MTU4.TGRD and MTU7.TGRD). • Double-buffering is selectable in complementary PWM mode.
	—	[MTU6 and MTU7] An AC asynchronous motor (brushless DC motor) drive mode using interlocked operation with MTU9 in complementary PWM or reset PWM operation is available, selectable between two types of waveform output (chopping or level).
Interrupt sources	38	45

Table 4.35 Points of Difference between I/O Registers Related to Multi-Function Timer Pulse Unit 3 Modules

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
TCR2	—	Register not available	Timer control register 2
TMDR1	BFE	Buffer operation E bit 0: MTU0.TGRE and MTU0.TGRF operate normally. 1: MTU0.TGRE and MTU0.TGRF are used together for buffer operation.	Buffer operation E bit 0: MTU0.TGRE and MTU9.TGRE, and MTU0.TGRF and TU9.TGRF operate normally. 1: MTU0.TGRE and MTU9.TGRE, and MTU0.TGRF and TU9.TGRF are used together for buffer operation.
TMDR3	—	Register not available	Timer mode register 3
TSR	TGFA	Input capture/output compare flag A	Reserved
	TGFB	Input capture/output compare flag B	Reserved
	TGFC	Input capture/output compare flag C	Reserved
	TGFD	Input capture/output compare flag D	Reserved
	TCFV	Overflow flag	Reserved
	TCFU	Underflow flag	Reserved
TSR2	—	Timer status register 2	Register not available
TBTM	TTSE	Timing select E bit 0: When compare match E occurs in MTU0, data is transferred from MTU0.TGRF to MTU0.TGRE 1: When MTU0.TCNT is cleared, data is transferred from MTU0.TGRF to MTU0.TGRE.	Timing select E bit 0: When compare match E occurs in MTU0 or MTU9, data is transferred from MTU0.TGRF to MTU0.TGRE or MTU9.TGRF to MTU9.TGRE. 1: When MTU0.TCNT or MTU9.TCNT is cleared, data is transferred from MTU0.TGRF to MTU0.TGRE or MTU9.TGRF to MTU9.TGRE.
TCNTLW	—	Register not available	Timer longword counter
TGRnLW (n = A or B)	—	Register not available	Timer longword general register
TSTRA	CST9	Reserved	Counter start 9 bit
TSYRA	SYNC9	Reserved	Timer sync 9 bit
TCSYSTR	SCH9	Reserved	Synchronous start 9 bit
TGCRB	—	Register not available	Timer gate control register B
NFCRn (n = 0 to 4, 6, 7, 9, C)	—	Register not available	Noise filter control register n
NFCR5	—	Register not available	Noise filter control register 5
TADSTRGR0	—	Register not available	A/D conversion start request select register 0
TADSTRGR1	—	Register not available	A/D conversion start request select register 1

4.4.15 Port Output Enable 3

Table 4.36 lists the points of difference between the port output enable 3 modules, and Table 4.37 lists the points of difference between the I/O registers related to the port output enable 3 modules.

Table 4.36 Points of Difference between Port Output Enable 3 Modules

Item	RX63T	RX24T and RX24U
Target pins to be placed in high-impedance state (POE3A also selectable as general I/O)	• MTU output pins MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) MTU3 pins (MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D) MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) MTU6 pins (MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D) MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) • GPT output pins GPT0 pins (GTIOC0A, GTIOC0B) GPT1 pins (GTIOC1A, GTIOC1B) GPT2 pins (GTIOC2A, GTIOC2B) GPT3 pins (GTIOC3A, GTIOC3B) GPT4 pins (GTIOC4A, GTIOC4B) GPT5 pins (GTIOC5A, GTIOC5B) GPT6 pins (GTIOC6A, GTIOC6B) GPT7 pins (GTIOC7A, GTIOC7B)	• MTU output pins MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) MTU3 pins (MTIOC3B, MTIOC3D) MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) MTU6 pins (MTIOC6B, MTIOC6D) MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPT output pins (not available on RX24T version A) GPT0 pins (GTIOC0A, GTIOC0B) GPT1 pins (GTIOC1A, GTIOC1B) GPT2 pins (GTIOC2A, GTIOC2B) GPT3 pins (GTIOC3A, GTIOC3B)

Item	RX63T	RX24T and RX24U
Conditions for high-impedance state (POE3A also selectable as general I/O)	• Change to input pin When input is received on POE0#, POE4#, POE8#, POE10#, POE11#, or POE12#*[1] • Shorting of output pins When a match (short circuit) occurs between the output signal levels (active level) over one or more cycles on the following combination of pins: 1. MTIOC3B and MTIOC3D 2. MTIOC4A and MTIOC4C 3. MTIOC4B and MTIOC4D 4. MTIOC6B and MTIOC6D 5. MTIOC7A and MTIOC7C 6. MTIOC7B and MTIOC7D 7. GTIOC0A and GTIOC0B 8. GTIOC1A and GTIOC1B 9. GTIOC2A and GTIOC2B 10.GTIOC4A and GTIOC4B 11.GTIOC5A and GTIOC5B 12.GTIOC6A and GTIOC6B • When a register setting is made • When clock generation circuit oscillation stop is detected • When comparator detection occurs in the comparator (S12ADB)	• Change to input pin When input is received on POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# • Shorting of output pins When a match (short circuit) occurs between the output signal levels (active level) over one or more cycles on the following combination of pins: 1. MTIOC3B and MTIOC3D 2. MTIOC4A and MTIOC4C 3. MTIOC4B and MTIOC4D 4. MTIOC6B and MTIOC6D 5. MTIOC7A and MTIOC7C 6. MTIOC7B and MTIOC7D 7. GTIOC0A and GTIOC0B 8. GTIOC1A and GTIOC1B 9. GTIOC2A and GTIOC2B (7 to 9 not available on RX24T version A) — — — • When a register setting is made • When clock generation circuit oscillation stop is detected • When comparator detection occurs in the comparator (CMPC)
Functions	• Each of the POE0#, POE4#, POE8#, POE10#, POE11# or POE12#*[1] input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in the high-impedance state by the POE0#, POE4#, POE8#, POE10#, POE11# or POE12#*[1] pin falling-edge or low-level sampling. • Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in the high-impedance state when the oscillation-stop detection circuit in the clock pulse generator detects stopped oscillation.	• Each of the POE0#, POE4# POE8#, POE10#, POE11#, or POE12# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • Each of the POE0#, POE4# POE8#, POE10#, POE11#, or POE12# input pins can be set for falling edge, or for low-level sampling, halting output on all pins subject to control. • Output can be stopped on all pins subject to control when clock generation circuit oscillation stop is detected.

Item	RX63T	RX24T and RX24U
Functions	• Pins for the MTU complementary PWM output or the GPT output pins can be placed in the high-impedance state when output levels of the MTU complementary PWM output pins or the GPT output pins are compared and simultaneous active-level output continues for one cycle or more.	• Output can be halted on the MTU complementary PWM output pins when simultaneous active-level output continues for 1 cycle or longer by comparing the output level of the MTU complementary PWM output pins or the GPT pins.
		• Output can be halted on the GPT output pins when simultaneous active-level output continues for 1 cycle or longer by comparing the output level of the GPT output pins (GPT0, GPT1, and GPT2).
	• Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in the high-impedance state in response to comparator detection by the 12-bit A/D converter (S12ADB).	• By using comparator C (CMPC) output detection, output can be halted on all pins subject to control.
	• Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in the high-impedance state by modifying settings in the POE3 registers.	• By making settings to the POE3 register, output can be halted on all pins subject to control.
	• Interrupts can be generated by input-level sampling or output-level comparison results.	• Interrupts can be generated by input-level sampling or output-level comparison results.

Note 1. Implemented only on packages with 112 or more pins.

Table 4.37 Points of Difference between I/O Registers Related to Port Output Enable 3 Modules

Register Symbol	Bit Symbol	RX63T	RX24T RX24U
ICSR1	POE0M[1:0]	POE0 mode select bits 0 0: Accepts a high-impedance control request on the falling edge of the POE0# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE0# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE0# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE0# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE0 mode select bits 0 0: Accepts a request on the falling edge of the POE0# pin input. 0 1: Accepts a request when the low level of the POE0# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the low level of the POE0# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the low level of the POE0# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.
	POE0F	POE0 flag 0: Indicates that a high-impedance control request has not been input on the POE0# pin. 1: Indicates that a high-impedance control request has been input on the POE0# pin.	POE0 flag 0: Indicates that an output stop request has not been input on the POE0# pin. 1: Indicates that an output stop request has been input on the POE0# pin.

Register Symbol	Bit Symbol	RX63T	RX24T RX24U
ICSR2	POE0M[1:0]	POE4 mode select bits 0 0: Accepts a high-impedance control request on the falling edge of the POE4# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE4# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE4# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE4# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE4 mode select bits 0 0: Accepts a request on the falling edge of the POE4# pin input. 0 1: Accepts a request when the low level of the POE4# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the low level of the POE4# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the low level of the POE4# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.
	POE0F	POE4 flag 0: Indicates that a high-impedance control request has not been input on the POE4# pin. 1: Indicates that a high-impedance control request has been input on the POE4# pin.	POE4 flag 0: Indicates that an output stop request has not been input on the POE4# pin. 1: Indicates that an output stop request has been input on the POE4# pin.
OCSR1	OCE1	Output short high-impedance enable 1 bit 0: Pins are not placed in high-impedance state. 1: Pins are placed in high-impedance state.	Simultaneous conduction output disable 1 bit 0: Does not disable outputs when they simultaneously go to active level. 1: Does disables outputs when they simultaneously go to active level.
OCSR2	OCE2	Output short high-impedance enable 2 bit 0: Pins are not placed in high-impedance state. 1: Pins are placed in high-impedance state.	Simultaneous conduction output disable 2 bit 0: Does not disable outputs when they simultaneously go to active level. 1: Does disables outputs when they simultaneously go to active level.

Register Symbol	Bit Symbol	RX63T	RX24T	RX24U
ALR1	OLSG0A	MTIOC3B/GTIOC0A active level setting bit	MTIOC3B/GTIOC0A (P71) pin active level setting bit	
	OLSG0B	MTIOC3D/GTIOC0B active level setting bit	MTIOC3D/GTIOC0B (P74) pin active level setting bit	
	OLSG1A	MTIOC4A/GTIOC1A active level setting bit	MTIOC4A/GTIOC1A (P72) pin active level setting bit	
	OLSG1B	MTIOC4C/GTIOC1B active level setting bit	MTIOC4C/GTIOC1B (P75) pin active level setting bit	
	OLSG2A	MTIOC4B/GTIOC2A active level setting bit	MTIOC4B/GTIOC2A (P73) pin active level setting bit	
	OLSG2B	MTIOC4D/GTIOC2B active level setting bit	MTIOC4D/GTIOC2B (P76) pin active level setting bit	
	MTUCHSEL	MTU output active level channel setting bit	Reserved	
ALR2	OLSG4A	MTIOC6B/GTIOC4A active level setting bit	MTIOC6B active level setting bit	
	OLSG4B	MTIOC6D/GTIOC4B active level setting bit	MTIOC6D active level setting bit	
	OLSG5A	MTIOC7A/GTIOC5A active level setting bit	MTIOC7A active level setting bit	
	OLSG5B	MTIOC7C/GTIOC5B active level setting bit	MTIOC7C active level setting bit	
	OLSG6A	MTIOC7B/GTIOC6A active level setting bit	MTIOC7B active level setting bit	
	OLSG6B	MTIOC7D/GTIOC6B active level setting bit	MTIOC7D active level setting bit	
ALR3	—	Register not available		Active level register 3
ICSR3	POE8M[1:0]	POE8 mode select bits 0 0: Accepts a high-impedance control request on the falling edge of the POE8# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE8# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE8# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE8# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE8 mode select bits 0 0: Accepts a request on the falling edge of the POE8# pin input. 0 1: Accepts a request when the low level of the POE8# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the low level of the POE8# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the low level of the POE8# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	

Register Symbol	Bit Symbol	RX63T	RX24T RX24U
ICSR3	POE8E	POE8 high-impedance enable bit	POE8 output disable bit
	POE8F	POE8 flag 0: Indicates that a high-impedance control request has not been input on the POE8# pin. 1: Indicates that a high-impedance control request has been input on the POE8# pin.	POE8 flag 0: Indicates that an output stop request has not been input on the POE8# pin. 1: Indicates that an output stop request has been input on the POE8# pin.
ICSR4	POE10M[1:0]	POE10 mode select bits 0 0: Accepts a high-impedance control request on the falling edge of the POE10# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE10# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE10# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE10# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE10 mode select bits 0 0: Accepts a request on the falling edge of the POE10# pin input. 0 1: Accepts a request when the low level of the POE10# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the low level of the POE10# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the low level of the POE10# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.
	POE10E	POE10 high-impedance enable bit	POE10 output disable bit
	POE10F	POE10 flag 0: Indicates that a high-impedance control request has not been input on the POE10# pin. 1: Indicates that a high-impedance control request has been input on the POE10# pin.	POE10 flag 0: Indicates that an output stop request has not been input on the POE10# pin. 1: Indicates that an output stop request has been input on the POE10# pin.

Register Symbol	Bit Symbol	RX63T	RX24T RX24U
ICSR5	POE11M[1:0]	POE11 mode select bits 0 0: Accepts a high-impedance control request on the falling edge of the POE11# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE11# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE11# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE11# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE11 mode select bits 0 0: Accepts a request on the falling edge of the POE11# pin input. 0 1: Accepts a request when the low level of the POE11# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the low level of the POE11# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the low level of the POE11# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.
	POE11E	POE11 high-impedance enable bit	POE11 output disable bit
	POE11F	POE11 flag 0: Indicates that a high-impedance control request has not been input on the POE11# pin. 1: Indicates that a high-impedance control request has been input on the POE11# pin.	POE11 flag 0: Indicates that an output stop request has not been input on the POE11# pin. 1: Indicates that an output stop request has been input on the POE11# pin.

Register Symbol	Bit Symbol	RX63T	RX24T	RX24U
ICSR7	POE12M[1:0]	POE12 mode select bits 0 0: Accepts a high-impedance control request on the falling edge of the POE12# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE12# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE12# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE12# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE12 mode select bits 0 0: Accepts a request on the falling edge of the POE12# pin input. 0 1: Accepts a request when the low level of the POE12# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the low level of the POE12# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the low level of the POE12# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	
	POE12E	POE12 high-impedance enable bit	POE12 output disable bit	
	POE12F	POE12 flag 0: Indicates that a high-impedance control request has not been input on the POE12# pin. 1: Indicates that a high-impedance control request has been input on the POE12# pin.	POE12 flag 0: Indicates that an output stop request has not been input on the POE12# pin. 1: Indicates that an output stop request has been input on the POE12# pin.	
ICSR6	OSTSTE	OSTST high-impedance enable bit	Oscillation stop output disable bit	
	OSTSTF	OSTST high-impedance flag	Oscillation stop detection flag	
SPOER	MTUCH34HIZ	MTU3 and MTU4 output high-impedance enable bit	MTU3 and MTU4 or GPT0 to GPT2 pin output disable bit	
	MTUCH67HIZ	MTU6 and MTU7 output high-impedance enable bit	MTU6, MTU7 pin output disable bit	
	MTUCH0HIZ	MTU0 output high-impedance enable bit	MTU0 pin output disable bit	
	GPT01HIZ (RX63T) GPT02HIZ (RX24U)	GPT0 and GPT1 output high-impedance enable bit	Reserved	GPT0 to GPT2 or MTU3 and MTU4 pin output disable bit
	GPT23HIZ (RX63T) GPT03HIZ (RX24T/24U)	GPT2 and GPT3 output high-impedance enable bit	GPT0 to GPT3 pin output disable bit	

Register Symbol	Bit Symbol	RX63T	RX24T	RX24U
SPOER	GPT67HIZ (RX63T) MTUCH9HIZ (RX24T/24U)	GPT6 and GPT7 output high-impedance enable bit	MTU9 output disable bit	
POECR1	MTU0AZE	MTU CH0A high-impedance enable bit	MTIOC0A (PB3) pin high-impedance enable bit	
	MTU0BZE	MTU CH0B high-impedance enable bit	MTIOC0B (PB2) pin high-impedance enable bit	
	MTU0CZE	MTU CH0C high-impedance enable bit	MTIOC0C pin high-impedance enable bit	
	MTU0DZE	MTU CH0D high-impedance enable bit	MTIOC0D pin high-impedance enable bit	
	MTU0A1ZE	Reserved	MTIOC0A (P31) pin high-impedance enable bit	
	MTU0B1ZE	Reserved	MTIOC0B (P30) pin high-impedance enable bit	
POECR2	MTU7BDZE	MTU CH7BD high-impedance enable bit	MTIOC7B/MTIOC7D pin high-impedance enable bit	
	MTU7ACZE	MTU CH7AC high-impedance enable bit	MTIOC7A/MTIOC7C pin high-impedance enable bit	
	MTU6BDZE	MTU CH6BD high-impedance enable bit	MTIOC6B/MTIOC6D pin high-impedance enable bit	
	MTU4BDZE	MTU CH4BD high-impedance enable bit	MTIOC4B/MTIOC4D (P73/P76) pin high-impedance enable bit	
	MTU4ACZE	MTU CH4AC high-impedance enable bit	MTIOC4A/MTIOC4C (P72/P75) pin high-impedance enable bit	
	MTU3BDZE	MTU CH3BD high-impedance enable bit	MTIOC3B/MTIOC3D (P71/P74) pin high-impedance enable bit	
POECR3	GPT0ABZE (RX63T) GPT0AZE (RX24U)	GPT CH0AB high-impedance enable bit	Reserved	GTIOC0A (P12) pin high-impedance enable bit
	GPT1ABZE (RX63T) GPT0BZE (RX24U)	GPT CH1AB high-impedance enable bit	Reserved	GTIOC0B (P15) pin high-impedance enable bit
	GPT1AZE	Reserved		GTIOC1A (P13) pin high-impedance enable bit
	GPT1BZE	Reserved		GTIOC1B (P16) pin high-impedance enable bit
	GPT2AZE	Reserved		GTIOC2A (P14) pin high-impedance enable bit

Register Symbol	Bit Symbol	RX63T	RX24T	RX24U
POECR3	GPT2BZE	Reserved		GTIOC2B (P17) pin high-impedance enable bit
	GPT2ABZE (RX63T) GPT0A1ZE (RX24U/24U)	GPT CH2AB high-impedance enable bit	GTIOC0A (PD2) pin high-impedance enable bit	
	GPT3ABZE (RX63T) GPT0B1ZE (RX24U/24U)	GPT CH3AB high-impedance enable bit	GIOC0B (PD1) pin high-impedance enable bit	
	GPT1A1ZE	Reserved	GTIOC1A (PD0) pin high-impedance enable bit	
	GPT1B1ZE	Reserved	GTIOC1B (PB7) pin high-impedance enable bit	
	GPT2A1ZE	Reserved	GTIOC2A (PB6) pin high-impedance enable bit	
	GPT2B1ZE	Reserved	GTIOC2B (PB5) pin high-impedance enable bit	
	GPT3A1ZE	Reserved	GTIOC3A high-impedance enable bit	
	GPT3B1ZE	Reserved	GTIOC3B high-impedance enable bit	
POECR4	CMADDMT34ZE	MTU CH34 high-impedance CFLAG add bit	MTU3, MTU4 output disabling condition CFLAG add bit	
	IC2ADDMT34ZE	MTU CH34 high-impedance POE4F add bit	MTU3, MTU4 output disabling condition POE4F add bit	
	IC3ADDMT34ZE	MTU CH34 high-impedance POE8F add bit	MTU3, MTU4 output disabling condition POE8F add bit	
	IC4ADDMT34ZE	MTU CH34 high-impedance POE10F add bit	MTU3, MTU4 output disabling condition POE10F add bit	
	IC5ADDMT34ZE	MTU CH34 high-impedance POE11F add bit	MTU3, MTU4 output disabling condition POE11F add bit	
	IC6ADDMT34ZE	MTU CH34 high-impedance POE12F add bit	MTU3, MTU4 output disabling condition POE12F add bit	
	CMADOMT67ZE (RX63T) CMADDMT67ZE (RX24U/24U)	MTU CH67 high-impedance CFLAG add bit	MTU6, MTU7 output disabling condition CFLAG add bit	
	IC1ADDMT67ZE	MTU CH67 high-impedance POE0F add bit	MTU6, MTU7 output disabling condition POE0F add bit	
	IC3ADDMT67ZE	MTU CH67 high-impedance POE8F add bit	MTU6, MTU7 output disabling condition POE8F add bit	
	IC4ADDMT67ZE	MTU CH67 high-impedance POE10F add bit	MTU6, MTU7 output disabling condition POE10F add bit	
	IC5ADDMT67ZE	MTU CH67 high-impedance POE11F add bit	MTU6, MTU7 output disabling condition POE11F add bit	
	IC6ADDMT67ZE	MTU CH67 high-impedance POE12F add bit	MTU6, MTU7 output disabling condition POE12F add bit	

Register Symbol	Bit Symbol	RX63T	RX24T	RX24U
POECR5	CMADDMT0ZE	MTU CH0 high-impedance CFLAG add bit	MTU0 output disabling condition CFLAG add bit	
	IC1ADDMT0ZE	MTU CH0 high-impedance POE0F add bit	MTU0 output disabling POE0F add bit	
	IC2ADDMT0ZE	MTU CH0 high-impedance POE4F add bit	MTU0 output disabling POE4F add bit	
	IC4ADDMT0ZE	MTU CH0 high-impedance POE10F add bit	MTU0 output disabling POE10F add bit	
	IC5ADDMT0ZE	MTU CH0 high-impedance POE11F add bit	MTU0 output disabling POE11F add bit	
	IC6ADDMT0ZE	MTU CH0 high-impedance POE12F add bit	MTU0 output disabling POE12F add bit	
POECR6	CMADDGPT01ZE (RX63T) CMADDGPT02ZE (RX24U)	GPT CH01 high-impedance CFLAG add bit	Reserved	GPT0 to GPT2 output disabling condition CFLAG add bit
	IC1ADDGPT01ZE (RX63T) IC1ADDGPT02ZE (RX24U)	GPT CH01 high-impedance POE0F add bit	Reserved	GPT0 to GPT2 output disabling condition POE0F add bit
	IC2ADDGPT01ZE (RX63T) IC2ADDGPT02ZE (RX24U)	GPT CH01 high-impedance POE4F add bit	Reserved	GPT0 to GPT2 output disabling condition POE4F add bit
	IC3ADDGPT01ZE (RX63T) IC3ADDGPT02ZE (RX24U)	GPT CH01 high-impedance POE8F add bit	Reserved	GPT0 to GPT2 output disabling condition POE8F add bit
	IC5ADDGPT01ZE (RX63T) IC5ADDGPT02ZE (RX24U)	GPT CH01 high-impedance POE11F add bit	Reserved	GPT0 to GPT2 output disabling condition POE11F add bit
	IC6ADDGPT01ZE (RX63T) IC6ADDGPT02ZE (RX24U)	GPT CH01 high-impedance POE12F add bit	Reserved	GPT0 to GPT2 output disabling condition POE12F add bit
	CMADDGPT23ZE (RX63T) CMADDGPT03ZE (RX24T/24U)	GPT CH23 high-impedance CFLAG add bit	GPT0 to GPT3 output disabling condition CFLAG add bit	
	IC1ADDGPT23ZE (RX63T) IC1ADDGPT03ZE (RX24T/24U)	GPT CH23 high-impedance POE0F add bit	GPT0 to GPT3 output disabling condition POE0F add bit	

Register Symbol	Bit Symbol	RX63T	RX24T	RX24U
POECR6	IC2ADDGPT23ZE (RX63T) IC2ADDGPT03ZE (RX24T/24U)	GPT CH23 high-impedance POE4F add bit	GPT0 to GPT3 output disabling condition POE4F add bit	
	C3ADDGPT23ZE (RX63T) IC3ADDGPT03ZE (RX24T/24U)	GPT CH23 high-impedance POE8F add bit	GPT0 to GPT3 output disabling condition POE8F add bit	
	IC4ADDGPT23ZE (RX63T) IC4ADDGPT03ZE (RX24T/24U)	GPT CH23 high-impedance POE10F add bit	GPT0 to GPT3 output disabling condition POE10F add bit	
	IC6ADDGPT23ZE (RX63T) IC6ADDGPT03ZE (RX24T/24U)	GPT CH23 high-impedance POE12F add bit	GPT0 to GPT3 output disabling condition POE12F add bit	
POECR7	MTU9AZE	Reserved	MTIOC9A (PD7) pin high-impedance enable bit	
	MTU9BZE	Reserved	MTIOC9B (PE0) pin high-impedance enable bit	
	MTU9CZE	Reserved	MTIOC9C (PD6) pin high-impedance enable bit	
	MTU9DZE	Reserved	MTIOC9D (PE1) pin high-impedance enable bit	
	MTU9A1ZE	Reserved	MTIOC9A (P21) pin high-impedance enable bit	
	MTU9B1ZE	Reserved	MTIOCBA (P10) pin high-impedance enable bit	
	MTU9C1ZE	Reserved	MTIOC9A (P20) pin high-impedance enable bit	
	MTU9D1ZE	Reserved	MTIOC9D (P02) pin high-impedance enable bit	
	GPT6ABZE (RX63T) MTU9A2ZE (RX24U)	GPT6ABZE high-impedance enable bit	Reserved	MTIOC9A (P26) pin high-impedance enable bit
	GPT7ABZE	GPT7ABZE high-impedance enable bit	Reserved	Reserved
	MTU9C2ZE	Reserved		MTIOC9C (P25) pin high-impedance enable bit

Register Symbol	Bit Symbol	RX63T	RX24T	RX24U
POECR8	CMADDGPT67ZE (RX63T) CMADDMT9ZE (RX24T/24U)	GPT CH67 high-impedance CFLAG add bit	MTU9 output disabling condition CFLAG add bit	
	IC1ADDGPT67ZE (RX63T) IC1ADDMT9ZE (RX24T/24U)	GPT CH67 high-impedance POE0F add bit	MTU9 output disabling condition POE0F add bit	
	IC2ADDGPT67ZE (RX63T) IC2ADDMT9ZE (RX24T/24U)	GPT CH67 high-impedance POE4F add bit	MTU9 output disabling condition POE4F add bit	
	IC3ADDGPT67ZE (RX63T) IC3ADDMT9ZE (RX24T/24U)	GPT CH67 high-impedance POE8F add bit	MTU9 output disabling condition POE8F add bit	
	IC4ADDGPT67ZE (RX63T) IC4ADDMT9ZE (RX24T/24U)	GPT CH67 high-impedance POE10F add bit	MTU9 output disabling condition POE10F add bit	
	IC5ADDGPT67ZE (RX63T) IC5ADDMT9ZE (RX24T/24U)	GPT CH67 high-impedance POE11F add bit	MTU9 output disabling condition POE11F add bit	
PMMCR0	—	Register not available	Port mode mask control register 0	
PMMCR1	—	Register not available	Port mode mask control register 1	
PMMCR2	GPT0AME	Register not available	Reserved	GTIOC0A/MTIOC3B (P12) pin port mode mask enable bit
	GPT0BME	Register not available	Reserved	GTIOC0B/MTIOC3D (P15) pin port mode mask enable bit
	GPT1AME	Register not available	Reserved	GTIOC1A/MTIOC4A (P13) pin port mode mask enable bit
	GPT1BME	Register not available	Reserved	GTIOC1B/MTIOC4C (P16) pin port mode mask enable bit

Register Symbol	Bit Symbol	RX63T	RX24T	RX24U
PMMCR2	GPT2AME	Register not available	Reserved	GTIOC2A/MTIOC4B (P14) pin port mode mask enable bit
	GPT2BME	Register not available	Reserved	GTIOC2B/MTIOC4D (P17) pin port mode mask enable bit
PMMCR3	MTU9A2ME	Register not available	Reserved	MTIOC9A (P26) pin port mode mask enable bit
	MTU9C2ME	Register not available	Reserved	MTIOC9C (P25) pin port mode mask enable bit
POECMPFR	—	Register not available	Port output enable comparator output detection flag register	
POECMPSEL	—	Register not available	Port output enable comparator request select register	
POECMPEXm (m = 0 to 2, 4, 5) (RX24T) (m = 0 to 5) (RX24U)	—	Register not available	Port output enable comparator request extended selection register m	

4.4.16 General PWM Timer

Table 4.38 lists the points of difference between the general PWM timers, and Table 4.39 lists the points of difference between the I/O registers related to the general PWM timers.

Table 4.38 Points of Difference between General PWM Timers

Item	RX63T	RX24T and RX24U
Functions	• 16 bits × 8 channels	• Selectable among 16 bits × 4 channels, 16 bits × 2 channels + 32 bits × 1 channel, and 32 bits × 2 channels
	• Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter	• Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter
	• Operating modes Sawtooth-wave PWM mode Sawtooth-wave one-shot pulse mode Triangle-wave PWM mode 1 Triangle-wave PWM mode 2 Triangle-wave PWM mode 3	• Operating modes Sawtooth-wave PWM mode Sawtooth-wave one-shot pulse mode Triangle-wave PWM mode 1 Triangle-wave PWM mode 2 Triangle-wave PWM mode 3
	• Independently selectable clock source for each channel (4 internal clocks and 2 external clocks)	• Independently selectable clock source for each channel (9 internal clocks and 4 external clocks)
	• 2 I/O pins per channel	• 2 I/O pins per channel
	—	• Ability to select noise filter for each input path
	• 2 output compare/input capture registers per channel	• 2 output compare/input capture registers per channel
	• For each channel, 4 registers that function as buffer register for the 2 output compare/input capture registers and that can be used as compare registers when buffering is not used	• For each channel, 4 registers that function as buffer register for the 2 output compare/input capture registers and that can be used as compare registers when buffering is not used
	• Generation of asymmetrical left/right PWM waveforms allowing peak and trough buffering during output compare operation	• Generation of asymmetrical left/right PWM waveforms allowing peak and trough buffering during output compare operation
	• Frame cycle registers for each channel (ability to generate interrupts at overflow/underflow)	• Frame cycle registers for each channel (ability to generate interrupts at overflow/underflow)
	• Support for synchronous operation of each counter	• Support for synchronous operation of each counter
	• Synchronous operation mode (synchronous or precisely at user-defined timing (phase shifting support)	• Synchronous operation mode (synchronous or precisely at user-defined timing (phase shifting support)
	• Ability to generate dead time during PWM operation	• Ability to generate dead time during PWM operation
	• Ability to combine 3 counters to generate 3-phase PWM waveforms with dead time	• Ability to combine 3 counters to generate 3-phase PWM waveforms with dead time
	• Starting, clearing, and stopping counters in response to external or internal trigger (hardware source)	• Starting, stopping, and clearing counters in response to external or internal trigger (hardware source)

Item	RX63T	RX24T and RX24U
Functions	• Ability to use comparator detection, software, or compare match as internal trigger source	• Ability to use comparator detection, MTU count start, software, or compare match as internal trigger source
	• Ability to use frequency-divided timer module clock (PCLKA) as counter clock to measure timing of edges of signals produced by frequency-dividing the IWDT-dedicated clock signal (IWDTCLK) (to detect abnormal oscillation)	—
	• Rise/fall timing control at a resolution equal to 1/32 the system clock (ICLK) for 2 PWM output pins among channel 0 to channel 3 (PWM delay generation function)	—

Table 4.39 Points of Difference between I/O Registers Related to General PWM Timers

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTSTR	CST1	GPT1.GTCNT count start bit	GPT1.GTCNT/GPT01.GTCNT LW count start bit
	CST3	GPT3.GTCNT count start bit	GPT3.GTCNT/GPT23.GTCNT LW count start bit
NFCR	—	Register not available	Noise filter control register
GTHSCR General PWM Timer hardware source start control register (RX63T) General PWM timer hardware source start/stop control register (RX24T/RX24U)	CSHW1[1:0]	GPT1.GTCNT hardware source count start bits	GPT1.GTCNT/GPT01.GTCNT LW hardware source count start bits
	CSHW3[1:0]	GPT3.GTCNT hardware source count start bits	GPT3.GTCNT/GPT23.GTCNT LW hardware source count start bits
	CPHW1[1:0]	GPT1.GTCNT hardware source count stop bits	GPT1.GTCNT/GPT01.GTCNT LW hardware source count stop bits
	CPHW3[1:0]	GPT3.GTCNT hardware source count stop bits	GPT3.GTCNT/GPT23.GTCNT LW hardware source count stop bits
GTHCCR	CCHW1[1:0]	GPT1.GTCNT hardware source counter clear bits	GPT1.GTCNT/GPT01.GTCNT LW hardware source counter clear bits
	CCHW3[1:0]	GPT3.GTCNT hardware source counter clear bits	GPT3.GTCNT/GPT01.GTCNT LW hardware source counter clear bits
	CCSW1	GPT1.GTCNT counter clear bit	GPT1.GTCNT/GPT01.GTCNT LW counter clear bit
	CCSW3	GP30.GTCNT counter clear bit	GPT3.GTCNT/GPT23.GTCNT LW counter clear bit

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTHSSR	CSHSL0[3:0]	GPT0.GTCNT hardware source count start bits b3 b0 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG0 pin input — — Settings other than the above are prohibited.	GPT0.GTCNT hardware source count start bits b3 b0 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTHSSR	CSHSL1[3:0]	GPT1.GTCNT hardware source count start bits b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG0 pin input — — Settings other than the above are prohibited.	GPT1.GTCNT/GPT01.GTCNTLW hardware source count start bits b7 b4 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTHSSR	CSHSL2[3:0]	GPT2.GTCNT hardware counter start source select bits b11 b8 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG0 pin input — — Settings other than the above are prohibited.	GPT2.GTCNT hardware count start source select bits b11 b8 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTHSSR	CSHSL3[3:0]	GPT3.GTCNT hardware counter start source select bits b15 b12 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: GTETRG0 pin input — — Settings other than the above are prohibited.	GPT3.GTCNT/GPT23.GTCNTLW hardware count start source select bits b15 b12 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTHPSR	CSHPL0[3:0]	GPT0.GTCNT hardware count stop/clear source select bits b3 b0 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG0 pin input Settings other than the above are prohibited.	GPT0.GTCNT hardware count stop/clear source select bits b3 b0 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output — 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTHPSR	CSHPL1[3:0]	GPT1.GTCNT hardware count stop/clear source select bits b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG0 pin input Settings other than the above are prohibited.	GPT1.GTCNT/GPT01.GTCNTLW hardware count stop/clear source select bits b7 b4 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output — 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTHPSR	CSHPL2[3:0]	GPT2.GTCNT hardware count stop/clear source select bits b11 b8 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG0 pin input Settings other than the above are prohibited.	GPT2.GTCNT hardware count stop/clear source select bits b11 b8 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output — 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTHPSR	CSHPL3[3:0]	GPT3.GTCNT hardware count stop/clear source select bits b15 b12 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG0 pin input Settings other than the above are prohibited.	GPT3.GTCNT/GPT01.GTCNTLW hardware count stop/clear source select bits b15 b12 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output — 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when count operation is started by a hardware source.
GTWP	WP1	GPT1 register write disable bit	GPT1/GPT01 register write disable bit
	WP3	GPT3 register write disable bit	GPT3/GPT23 register write disable bit
GTSYNC	SYNC0[1:0]	GPT0.GTCNTcounter synchronous clear source select bits b1 b0 0 0: Synchronous clear is not performed. 0 1: GPT0.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT0.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT0.GTCNT is synchronously cleared by a GPT3 clearing source.	GPT0.GTCNTcounter synchronous clear source select bits b1 b0 0 0: Synchronous clear is not performed. 0 1: GPT0.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT0.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT0.GTCNT is synchronously cleared by a GPT3/GPT23 clearing source.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTSYNC	SYNC1[1:0]	GPT1.GTCNT counter synchronous clear source select bits b5 b4 0 0: GPT1.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: Synchronous clear is not performed. 1 0: GPT1.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT1.GTCNT is synchronously cleared by a GPT3 clearing source.	GPT1.GTCNT/GPT01.GTCNTLW counter synchronous clear source select bits b5 b4 0 0: GPT1.GTCNT counter is synchronously cleared by a GPT0 clearing source. 0 1: Synchronous clear is not performed. 1 0: GPT1.GTCNT/GPT01.GTCNTLW counter is synchronously cleared by a GPT2 clearing source. 1 1: GPT1.GTCNT/GPT01.GTCNTLW counter is synchronously cleared by a GPT3/GPT23 clearing source.
	SYNC2[1:0]	GPT2.GTCNT counter synchronous clear source select bits b9 b8 0 0: GPT2.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT2.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: Synchronous clear is not performed. 1 1: GPT2.GTCNT is synchronously cleared by a GPT3 clearing source.	GPT2.GTCNT counter synchronous clear source select bits b9 b8 0 0: GPT2.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT2.GTCNT is synchronously cleared by a GPT1/GPT01 clearing source. 1 0: Synchronous clear is not performed. 1 1: GPT2.GTCNT is synchronously cleared by a GPT3 clearing source.
	SYNC3[1:0]	GPT3.GTCNT counter synchronous clear source select bits b13 b12 0 0: GPT3.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT3.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT3.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: Synchronous clear is not performed.	GPT3.GTCNT/GPT01.GTCNTLW counter synchronous clear source select bits b13 b12 0 0: GPT3.GTCNT/GPT23.GTCNTLW is synchronously cleared by a GPT0 clearing source. 0 1: GPT3.GTCNT/GPT23.GTCNTLW is synchronously cleared by a GPT1/GPT01 clearing source. 1 0: GPT3.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: Synchronous clear is not performed.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTETINT	ETIPF	External trigger rising input interrupt request flag	Reserved
	ETINF	External trigger falling input interrupt request flag	Reserved
	GTETRGEN	Reserved	GTETRG noise filter enable bit
GTBDR	BD0[0](RX63T) BD00(RX24T/24U)	GPT0.GTCCR buffer operation disable bit	GPT0.GTCCR buffer operation disable bit
	BD0[1](RX63T) BD01(RX24T/24U)	GPT0.GTPR buffer operation disable bit	GPT0.GTPR buffer operation disable bit
	BD0[2](RX63T) BD02(RX24T/24U)	GPT0.GTADPR buffer operation disable bit	GPT0.GTADPR buffer operation disable bit
	BD0[3](RX63T) BD03(RX24T/24U)	GPT0.GTDV buffer operation disable bit	GPT0.GTDV buffer operation disable bit
	BD1[0](RX63T) BD10(RX24T/24U)	GPT1.GTCCR buffer operation disable bit	GPT1.GTCCR/ GPT01.GTCCRLW buffer operation disable bit
	BD1[1](RX63T) BD11(RX24T/24U)	GPT1.GTPR/GPT01.GTPRLW buffer operation disable bit	GPT1.GTPR/GPT01.GTPRLW buffer operation disable bit
	BD1[2](RX63T) BD12(RX24T/24U)	GPT1.GTADTR buffer operation disable bit	GPT1.GTADTR/ GPT01.GTADTRLW buffer operation disable bit
	BD1[3](RX63T) BD13(RX24T/24U)	GPT1.GTDV buffer operation disable bit	GPT1.GTDV/ GPT01.GTDVLW buffer operation disable bit
	BD2[0](RX63T) BD20(RX24T/24U)	GPT2.GTCCR buffer operation disable bit	GPT2.GTCCR buffer operation disable bit
	BD2[1](RX63T) BD21(RX24T/24U)	GPT2.GTPR buffer operation disable bit	GPT2.GTPR buffer operation disable bit
	BD2[2](RX63T) BD22(RX24T/24U)	GPT2.GTADPR buffer operation disable bit	GPT2.GTADPR buffer operation disable bit
	BD2[3](RX63T) BD23(RX24T/24U)	GPT2.GTDV buffer operation disable bit	GPT2.GTDV buffer operation disable bit
	BD3[0](RX63T) BD10(RX24T/24U)	GPT3.GTCCR buffer operation disable bit	GPT3.GTCCR/ GPT23.GTCCRLW buffer operation disable bit
	BD3[1](RX63T) BD11(RX24T/24U)	GPT3.GTPR/GPT01.GTPRLW buffer operation disable bit	GPT3.GTPR/GPT23.GTPRLW buffer operation disable bit
	BD3[2](RX63T) BD12(RX24T/24U)	GPT3.GTADTR buffer operation disable bit	GPT3.GTADTR/ GPT23.GTADTRLW buffer operation disable bit
	BD3[3](RX63T) BD33(RX24T/24U)	GPT3.GTDV buffer operation disable bit	GPT3.GTDV/ GPT23.GTDVLW buffer operation disable bit
LCCR	—	LOCO count control register	Register not available
LCST	—	LOCO count status register	Register not available
LCNT	—	LOCO count value register	Register not available
LCNTA	—	LOCO count result average register	Register not available
LCNTn (n = 00 to 15)	—	LOCO count result register n	Register not available
LCNTDU	—	LOCO count upper/lower permissible deviation register	Register not available

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
LCNTDL	—	LOCO count upper/lower permissible deviation register	Register not available
GTCWP	—	Register not available	General PWM timer clearing write-protection register
GTCMNWP	—	Register not available	General PWM timer common register write-protection register
GTMDR	—	Register not available	General PWM timer mode register
GTECNFCR	—	Register not available	General PWM timer external clock noise filter control register
GTADSMR	—	Register not available	General PWM timer A/D conversion start request signal monitor register
GTCR	TPCS[1:0] (RX63T) TPCS[3:0] (RX24T/24U)	Timer prescaler select bits b9 b8 0 0: PCLKA (timer module clock) 0 1: PCLKA/2 (timer module clock/2) 1 0: PCLKA/4 (timer module clock/4) 1 1: PCLKA/8 (timer module clock/8)	Timer prescaler select bits b11 b8 0 0 0 0: PCLKA 0 0 0 1: PCLKA/2 0 0 1 0: PCLKA/4 0 0 1 1: PCLKA/8 0 1 0 0: PCLKA/16 0 1 0 1: PCLKA/32 0 1 1 0: PCLKA/64 0 1 1 1: PCLKA/256 1 0 0 0: PCLKA/1024 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: GTECLKA 1 1 0 1: GTECLKB 1 1 1 0: GTECLKC 1 1 1 1: GTECLKD
GTBER	CCRA[1:0]	GTCCRA buffer operation bits b1 b0 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTCCRA ↔ GTCCRC) 1 x: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD)	GTCCRA(LW) buffer operation bits b1 b0 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTCCRA(LW) register ↔ GTCCRC(LW) register) 1 x: Double buffer operation (GTCCRA(LW) register ↔ GTCCRC(LW) register ↔ GTCCRD(LW) register)

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTBER	CCRB[1:0]	GTCCRB buffer operation bits b3 b2 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) 1 x: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF)	GTCCRB(LW) buffer operation bits b3 b2 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTCCRB(LW) register ↔ GTCCRE(LW) register) 1 x: Double buffer operation (GTCCRB(LW) register ↔ GTCCRE(LW) register ↔ GTCCRF(LW) register)
	PR[1:0]	GTPR buffer operation bits b5 b4 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTPBR → GTPR) 1 x: Double buffer operation (GTPDBR → GTPBR → GTPR)	GTPR(LW) buffer operation bits b5 b4 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTPBR(LW) register → GTPR(LW) register) 1 x: Double buffer operation (GTPDBR(LW) register → GTPBR(LW) register → GTPR(LW) register)
	CCRSWT	GTCCRA and GTCCRB forcible buffer operation bit Writing 1 to this bit forcibly performs buffer transfer of GTCCRA and GTCCRB. This bit is automatically cleared to 0 after 1 is written to it. This bit is read as 0.	GTCCRA(LW) and GTCCRB(LW) forcible buffer operation bit Writing 1 to this bit forcibly performs buffer transfer of GTCCRA(LW) and GTCCRB(LW). This bit is automatically cleared to 0 after 1 is written to it. This bit is read as 0.
	ADTTA[1:0]	GTADTRA buffer transfer timing select bits • Triangle waves b9 b8 0 0: No transfer 0 1: Transfer at peak 1 0: Transfer at trough 1 1: Transfer at both peak and trough • Saw waves b9 b8 0 0: No transfer Value other than 0 0: Transfer at underflow (during down-counting) or overflow (during up-counting)	GTADTRA(LW) buffer transfer timing select bits • Triangle waves b9 b8 0 0: No transfer 0 1: Transfer at peak 1 0: Transfer at trough 1 1: Transfer at both peak and trough • Saw waves b9 b8 0 0: No transfer Value other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clearing

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTBER	ADTDB[1:0]	GTADTRB double buffer operation bits 0: Single buffer operation (GTADTBRA → GTADTRA) 1: Double buffer operation (GTADTDBRA → GTADTBRA → GTADTRA)	GTADTRA(LW) double buffer operation bits 0: Single buffer operation (GTADTBRA(LW) register → GTADTRA(LW) register) 1: Double buffer operation (GTADTDBRA(LW) register → GTADTBRA(LW) register → GTADTRA(LW) register)
	ADTTB[1:0]	GTADTRB buffer transfer timing select bits	GTADTRB(LW) buffer transfer timing select bits
	ADTDB	GTADTRB double buffer operation bit	GTADTRB(LW) double buffer operation bit
GTUDC	UD	Count direction setting bit 0: GTCNT counts down. 1: GTCNT counts up.	Count direction setting bit 0: GTCNT(LW) counts down. 1: GTCNT(LW) counts up.
	OADTY[1:0]	Reserved	GTIOCA pin output duty setting bits
	OADTYF	Reserved	GTIOCA pin output duty forced setting bit
	OADTYR	Reserved	Output after release of GTIOCA pin output 0%/100% duty cycle setting bit
	OBDTY[1:0]	Reserved	GTIOCB pin output duty setting bits
	OBDTYF	Reserved	GTIOCB pin output duty forced setting bit
	OBDTYR	Reserved	Output after release of GTIOCB pin output 0%/100% duty cycle setting bit
GTITC	ITLA	GTCCRA compare match/input capture interrupt link bit 0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	GTCCRA(LW) compare match/input capture interrupt link bit 0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.
	ITLB	GTCCRB compare match/input capture interrupt link bit 0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	GTCCRB(LW) compare match/input capture interrupt link bit 0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.
	ITLC	GTCCRC compare match interrupt link bit 0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	GTCCRC(LW) compare match interrupt link bit 0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTITC	ITLD	GTCCRD compare match interrupt link bit 0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	GTCCRD(LW) compare match interrupt link bit 0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.
	ITLE	GTCCRE compare match interrupt link bit 0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	GTCCRE(LW) compare match interrupt link bit 0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.
	ITLF	GTCCRF compare match interrupt link bit 0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	GTCCRF(LW) compare match interrupt link bit 0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.
	IVTC[1:0]	GTCIV interrupt skipping function select bits	GTCIV/GTCIU interrupt skipping function select bits
	IVTT[2:0]	GTCIV interrupt skipping count select bits	GTCIV/GTCIU interrupt skipping count select bits
	ADTAL	GTADTRA A/D converter start request link bit	GTADTRA(LW) A/D converter start request link bit
	ADTBL	GTADTRB A/D converter start request link bit	GTADTRB(LW) A/D converter start request link bit
GTST	TCFA	Input capture/compare match flag A	Reserved
	TCFB	Input capture/compare match flag B	Reserved
	TCFC	Compare match flag C	Reserved
	TCFD	Compare match flag D	Reserved
	TCFE	Compare match flag E	Reserved
	TCFF	Compare match flag F	Reserved
	TCFPO	Overflow flag	Reserved
	TCFPU	Underflow flag	Reserved
	ITCNT[2:0]	GTCIV interrupt skipping count counter bits	GTCIV/GTCIU interrupt skipping count counter bits
	TUCF	Count direction flag 0: GPTn.GTCNT counts down. 1: GPTn.GTCNT counts up.	Count direction flag 0: GTCNT(LW) counts down. 1: GTCNT(LW) counts up.
GTCNTLW	—	Register not available	General PWM timer longword counter register
GTCCRmLW (m = A to F)	—	Register not available	General PWM timer longword compare capture register
GTPRLW	—	Register not available	General PWM timer longword period setting register
GTPBRLW	—	Register not available	General PWM timer longword period setting buffer register

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTPDBRLW	—	Register not available	General PWM timer longword period setting double buffer register
GTADTRmLW (m = A or B)	—	Register not available	Longword A/D converter start request timing register
GTADTBRmLW (m = A or B)	—	Register not available	Longword A/D converter start request timing buffer register
GTADTDBRmLW (m = A or B)	—	Register not available	Longword A/D converter start request timing double buffer register
GTONCR	NFS[3:0]	GTIOC output negate source select bits b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: GTETRG0 pin input 1 x x x: Software control (control through SWN bit)	GTIOC output negate source select bits b7 b4 0 0 0 1: CMPC1 comparator output 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — — — — 0 1 1 1: GTETRG pin input 1 x x x: Software control (control through SWN bit) Settings other than the above are prohibited when negate control is enabled by the NEA or NEB bit.
GTDTCR	TDE	Negative-phase waveform setting bit 0: The GTCCRB register is set individually without using the GTDVU and GTDVD registers. 1: The GTDVU and GTDVD registers are used to set the compare match value for negative-phase waveforms with dead time automatically in the GTCCRB register.	Negative-phase waveform setting bit 0: The GTCCRB(LW) register is set individually without using the GTDVU(LW) and GTDVD(LW) registers. 1: The GTDVU(LW) and GTDVD(LW) registers are used to set the compare match value for negative-phase waveforms with dead time automatically in the GTCCRB(LW) register.
	TDBUE	GTDVU buffer operation enable bit 0: GTDVU register buffer operation is disabled. 1: GTDVU register buffer operation is enabled.	GTDVU(LW) buffer operation enable bit 0: GTDVU(LW) register buffer operation is disabled. 1: GTDVU(LW) register buffer operation is enabled.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
GTDTCR	TDBDE	GTDVD buffer operation enable bit 0: GTDVD register buffer operation is disabled. 1: GTDVD register buffer operation is enabled.	GTDVD(LW) buffer operation enable bit 0: GTDVD(LW) register buffer operation is disabled. 1: GTDVD(LW) register buffer operation is enabled.
	TDFER	GTDVD setting bit 0: The GTDVU and GTDVD registers are set individually. 1: The value written to the GTDVU register is set automatically in the GTDVD register.	GTDVD(LW) setting bit 0: The GTDVU(LW) and GTDVD(LW) registers are set individually. 1: The value written to the GTDVU(LW) register is set automatically in the GTDVD(LW) register.
GTSOS	SOS [1:0]	Output protection function status bits b1 b0 0 0: Normal operation 0 1: Protected state (GTCCRA = 0 set during transfer at trough or peak) 1 0: Protected state (GTCCRA ≥ GTPR set during transfer at trough) 1 1: Protected state (GTCCRA ≥ GTPR set during transfer at peak)	Output protection function status bits b1 b0 0 0: Normal operation 0 1: Protected state (GTCCRA(LW) = 0 set during transfer at trough or peak) 1 0: Protected state (GTCCRA(LW) ≥ GTPR(LW) set during transfer at trough) 1 1: Protected state (GTCCRA(LW) ≥ GTPR(LW) set during transfer at peak)
GTDVmLW (m = U or D)	—	Register not available	General PWM timer longword dead time value register m
GTDBmLW (m = U or D)	—	Register not available	General PWM timer longword dead time buffer register m
GTDLYCR	—	PWM output delay control register	Register not available
GTDLYRA	—	GTIOCA rising output delay register	Register not available
GTDLYFA	—	GTIOCA falling output delay register	Register not available
GTDLYRB	—	GTIOCB rising output delay register	Register not available
GTDLYFB	—	GTIOCB falling output delay register	Register not available

4.4.17 Independent Watchdog Timer

Table 4.40 lists the points of difference between the independent watchdog timers, and Table 4.41 lists the points of difference between the I/O registers related to the independent watchdog timers.

Table 4.40 Points of Difference between Independent Watchdog Timers

Item	RX63T	RX24T and RX24U
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. Counting restarts. (auto-start mode: automatic, register start mode: refresh)	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. Counting restarts. (In auto-start mode, counting restarts automatically after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after a refresh.)
Non-maskable interrupt sources	• Generation of a non-maskable interrupt (WUNI) when a down counter underflows • Refresh occurring outside the refresh-permitted period (refresh error)	• Down-counter underflow • Refresh occurring outside the refresh-permitted period (refresh error)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)

Item	RX63T	RX24T and RX24U
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

Table 4.41 Points of Difference between I/O Registers Related to Independent Watchdog Timers

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
IWDTCR	TOPS[1:0]	Timeout period selection bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	Timeout period selection bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)

4.4.18 Serial Communications Interface

Table 4.42 lists the points of difference between the serial communications interfaces, and Table 4.43 lists the points of difference between the I/O registers related to the serial communications interfaces.

Table 4.42 Points of Difference between Serial Communications Interfaces

Item		RX63T	RX24T	RX24U
Number of channels		3 channels (SCIc) 1 channel (SCId)	3 channels —	4 channels —
I/O pins		• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK0, RXD0, TXD0, CTS0#/RTS0#, SCK1, RXD1, TXD1, CTS1#/RTS1#, SCK2, RXD2, TXD2, CTS2#/RTS2#, SCK3, RXD3, TXD3, CTS3#/RTS3#, SCK12, RXD12, TXD12, CTS12#/RTS12# • SCI I/O pins (simple I^2C mode) SSCL0, SSDA0, SSCL1, SSDA1, SSCL2, SSDA2, SSCL3, SSDA3, SSCL12, SSDA12 • SCI I/O pins (simple SPI mode) SCK0, SMISO0, SMOSI0, SS0#, SCK1, SMISO1, SMOSI1, SS1#, SCK2, SMISO2, SMOSI2, SS3#, SCK12, SMISO12, SMOSI12, SS12# • SCI I/O pins (extended serial mode) RXDX12, SMISO0, SMOSI0	• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK1, RXD1, TXD1, CTS1#/RTS1#, SCK5, RXD5, TXD5, CTS5#/RTS5#, SCK6, RXD6, TXD6, CTS6#/RTS5# (channel 11 available on RX24U only) SCK11, RXD11, TXD11, CTS11#/RTS11# • SCI I/O pins (simple I^2C mode) SSCL1, SSDA1, SSCL5, SSDA5, SSCL6, SSDA6 (channel 11 available on RX24U only) SSCL11, SSDA11 • SCI I/O pins (simple SPI mode) SCK1, SMISO1, SMOSI1, SS1#, SCK5, SMISO5, SMOSI5, SS5#, SCK6, SMISO6, SMOSI6, SS6# (channel 11 available on RX24U only) SCK11, SMISO11, SMOSI11, SS11#	
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits	
	Start bit detection	—	Selectable between low level and falling edge.	
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the MTU3 can be used.	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.	
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.	

Table 4.43 Points of Difference between I/O Registers Related to Serial Communications Interfaces

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
RDRH	—	Register not available	Receive data register H
RDRL	—	Register not available	Receive data register L
RDRHL	—	Register not available	Receive data register HL
TDRH	—	Register not available	Transmit data register H
TDRL	—	Register not available	Transmit data register L
TDRHL	—	Register not available	Transmit data register HL
SMR (SCMR.SMIF = 0)	CHR	Character length bit (valid only in asynchronous mode) 0: Transmit/receive using 8-bit data length 1: Transmit/receive using 7-bit data length	Character length bit (valid only in asynchronous mode) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive using 9-bit data length 0 1: Transmit/receive using 9-bit data length 1 0: Transmit/receive using 8-bit data length 1 1: Transmit/receive using 7-bit data length
	CM	Communications mode bit 0: Asynchronous mode 1: Clock synchronous mode	Communications mode bit 0: Asynchronous mode or simple I^2C mode 1: Clock synchronous mode or simple SPI mode

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
SCR (SCMR.SMIF = 0)	CKE[1:0]	Clock enable bits (asynchronous mode) 0 0: On-chip baud rate generator SCKn pin can function as I/O port, based on I/O port settings. 0 1: On-chip baud rate generator Clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or MTU3 clock • When an external clock is used, a clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency 8 times the bit rate when the SEMR.ABCS bit is set to 1. • MTU3 clock can be used. The base clock to be input from MTU3 must be set to a frequency no greater than 1/4 that of PCLK. The SCKn pin functions as an I/O port according to the I/O port settings when the MTU3 clock is in use. (Clock synchronous mode) 0 x: Internal clock: SCKn functions as clock output pin. 1 x: External clock SCKn functions as clock input pin.	SCI1 or SCI11*1: Clock enable bits (asynchronous mode) 0 0: On-chip baud rate generator SCKn pin can function as I/O port, based on I/O port settings. 0 1: On-chip baud rate generator Clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock • A clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency 8 times the bit rate when the SEMR.ABCS bit is set to 1. (Clock synchronous mode) 0 x: Internal clock: SCKn functions as clock output pin. 1 x: External clock SCKn functions as clock input pin.

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
SCR (SCMR.SMIF = 0)	CKE[1:0]		SCI5 or SCI6: Clock enable bits (asynchronous mode) 0 0: On-chip baud rate generator SCKn pin can function as I/O port, based on I/O port settings. 0 1: On-chip baud rate generator Clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or TMR clock • When an external clock is used, a clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency 8 times the bit rate when the SEMR.ABCS bit is set to 1. • TMR clock can be used. The SCKn pin functions as an I/O port according to the I/O port settings when the TMR clock is in use. (Clock synchronous mode) 0 x: Internal clock: SCKn functions as clock output pin. 1 x: External clock SCKn functions as clock input pin.
		Clock enable bits (asynchronous mode) 0 0: On-chip baud rate generator SCKn pin can function as I/O port, based on I/O port settings. 0 1: On-chip baud rate generator Clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or MTU3 clock • When an external clock is used, a clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency 8 times the bit rate when the SEMR.ABCS bit is set to 1. • MTU3 clock can be used. The base clock to be input from MTU3 must be set to a frequency no greater than 1/4 that of PCLK. The SCKn pin functions as an I/O port according to the I/O port settings when the MTU3 clock is in use. (Clock synchronous mode) 0 x: Internal clock: SCKn functions as clock output pin. 1 x: External clock SCKn functions as clock input pin.	
SSR (SCMR.SMIF = 1)	RDRF	Reserved Initial value after a reset is different.	Receive data full flag
	TDRE	Reserved Initial value after a reset is different.	Transmit data empty flag

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
SCMR	SMIF	Smart card interface mode select bit 0: Serial communication interface mode 1: Smart card interface mode	Smart card interface mode select bit 0: Non-smart card interface mode (asynchronous mode, clock synchronous mode, simple SPI mode, or simple I^2C mode) 1: Smart card interface mode
	SDIR	Transmitted/received data transfer direction Set the SDIR bit to 1 (MSB first) for operation in simple I^2C mode. 0: Transmit/receive with LSB first 1: Transmit/receive with MSB first	Transmitted/received data transfer direction This bit can be used in the following modes. • Smart card interface mode • Asynchronous mode (multi-processer mode) • Clock synchronous mode • Simple SPI mode Set this bit to 1 for operation in simple I^2C mode. 0: Transmit/receive with LSB first 1: Transmit/receive with MSB first
	CHR1	Reserved	Character length bit 1
SEMR	ACS0	(Only valid in asynchronous mode) 0: External clock input 1: MTU3 clock input (MTIOC6A and MTIOC7A)	(Only valid in asynchronous mode) 0: External clock 1: Logical AND of two compare match outputs from TMR (valid for SCI5 and SCI6 only). Available compare match output varies according to SCI channel.
	BRME	Reserved	Bit rate modulation enable bit
	BGDM	Reserved	Baud rate generator double-speed mode select bit
	RXDESEL	Reserved	Asynchronous start bit edge detection select bit
SIMR1	IICM	Simple I^2C mode select bit 0 0: Serial interface mode (asynchronous mode, clock synchronous mode, or simple SPI mode) 0 1: Simple I^2C mode 1 0: Smart card interface mode 1 1: Setting prohibited	Simple I^2C mode select bit 0 0: Asynchronous mode, multi-processer mode, clock synchronous mode (asynchronous mode, clock synchronous mode, or simple SPI mode) 0 1: Simple I^2C mode 1 0: Smart card interface mode 1 1: Setting prohibited
SPMR	SSE	SS pin function enable bit 0: SS pin function disabled 1: SS pin function enabled	SSn# pin function enable bit 0: SSn# pin function disabled 1: SSn# pin function enabled
ESMER	—	Extended serial module enable register	Register not available

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
CR0	—	Control register 0	Register not available
CR1	—	Control register 1	Register not available
CR2	—	Control register 2	Register not available
CR3	—	Control register 3	Register not available
PCR	—	Port control register	Register not available
ICR	—	Interrupt control register	Register not available
STR	—	Status register	Register not available
STCR	—	Status clear register	Register not available
CF0DR	—	Control field 0 data register	Register not available
CF0CR	—	Control field 0 compare enable register	Register not available
CF0RR	—	Control field 0 receive data register	Register not available
PCF1DR	—	Primary control field 1 data register	Register not available
SCF1DR	—	Secondary control field 1 data register	Register not available
CF1CR	—	Control field 1 compare enable register	Register not available
CF1RR	—	Control field 1 receive data register	Register not available
TCR	—	Timer control register	Register not available
TMR	—	Timer mode register	Register not available
TPRE	—	Timer prescaler register	Register not available
TCNT	—	Timer count register	Register not available

Note 1. Available on RX24U only.

4.4.19 I²C Bus Interface

Table 4.44 lists the points of difference between the I²C bus interfaces, and Table 4.45 lists the points of difference between the I/O registers related to the I²C bus interfaces.

Table 4.44 Points of Difference between I²C Bus Interfaces

Item	RX63T	RX24T and RX24U
Number of channels	2 channels	1 channel

Table 4.45 Points of Difference between I/O Registers Related to I²C Bus Interfaces

Register Symbol	Bit Symbol	RX63T	RX24T/24U
ICCR2	BBSY	Bus busy detection flag 0: I²C bus in released state (bus free state) 1: I²C bus in occupied state (bus busy state or in bus free period)	Bus busy detection flag 0: I²C bus in released state (bus free state) 1: I²C bus in occupied state (bus busy state)
ICMR2	TMWE	Timeout internal counter write enable	Reserved
TMOCNT	—	Timeout internal counter	Register not available

4.4.20 CAN Module

Table 4.46 lists the points of difference between the CAN modules, and Table 4.47 lists the points of difference between the I/O registers related to the CAN modules.

Table 4.46 Points of Difference between CAN Modules

Item	RX63T	RX24T and RX24U
Number of channels	3 channels	1 channel
Bit rate	Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Up to 1 Mbps
Message boxes	32 mailboxes: 2 selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, 4 FIFO stages can be configured for transmission and 4 FIFO stages for reception.	16 message boxes • Each channel dedicated: 4 buffers (4 buffers per channel) Transmit buffer: 4 buffer per channel • Shared among channels: 16 buffers Receive buffers: 0 to 16 buffers Receive FIFO buffers: 2 (up to 16 buffers allocatable to each) Transmit/receive FIFO buffers: 1 per channel (up to 16 buffers allocatable to each)
Reception	• Ability to receive data frames and remote frames • Ability to select ID format used for reception (standard ID only, extended ID only, or both standard and extended IDs) • Selectable one-shot reception function • Ability to select overwrite mode (message overwritten) or overrun mode (message discarded) • Ability to enable or disable receive end interrupt for each mailbox — — —	• Ability to receive data frames and remote frames • Ability to select ID format used for reception (standard ID only, extended ID only, or both) — — — • Ability to enable or disable interrupts for each FIFO • Mirror function (to receive messages transmitted from own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)
Acceptance filtering	• 8 acceptance masks (individual mask for every 4 mailboxes) • Ability to individually enable or disable masks for each mailbox	• Refer to reception filtering function.

Item	RX63T	RX24T and RX24U
Reception filtering function	—	• Ability to select receive messages using a total of 16 receive rules • Ability to set the number of receive rules (0 to 16) for each channel • Acceptance filtering: Ability to set ID and mask for each receive rule • DLC filter processing: Ability to specify DLC filter checking for each receive rule
Receive message transfer function	—	• Routing function Ability to transfer receive messages to user-defined buffers (max. transfer buffers: 2) Transfer destination: Receive buffer, receive FIFO buffer, or transmit/receive FIFO buffer • Label addition function Ability to simultaneously store label information when storing a message in a receive buffer and FIFO buffer
Transmission	• Ability to transmit data frames and remote frames • Ability to select ID format used for transmission (standard ID only, extended ID only, or both standard and extended IDs) • Selectable one-shot transmission function • Ability to select ID priority transmission mode or mailbox number priority mode • Ability to abort transmission requests (and ability to confirm abort completion with a flag) • Ability to enable or disable transmit complete interrupt individually by mailbox	• Ability to transmit data frames and remote frames • Ability to select ID format used for transmission (standard ID only, extended ID only, or both) • One-shot transmission function • Ability to select ID priority transmission or transmit buffer number priority transmission • Transmit abort function (with ability to confirm abort completion with a flag) • Ability to enable or disable transmit complete interrupt individually by transmit buffer or transmit/receive FIFO buffer
Interval transmission function	—	Ability to set the message transmission interval time (transmit mode of transmit/receive FIFO buffers)
Transmit history function	—	Function for storing history information for transmitted messages

Item	RX63T	RX24T and RX24U
Error status monitoring	• Monitoring of CAN protocol errors (stuff errors, form errors, ACK errors, CRC errors, bit errors, and ACK delimiter errors) • Detection of error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Error counter reading —	• Monitoring of CAN protocol errors (stuff errors, form errors, ACK errors, CRC errors, bit errors, ACK delimiter errors, and bus dominant locking) • Detection of error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Error counter reading • Monitors DLC errors
Time stamp function	• Time stamp function using 16-bit counter • Ability to select reference clock among 1-, 2-, 4-, and 8-bit time periods	• Time stamp function using 16-bit counter • Time stamp clock source division function
Interrupt function	5 interrupt sources (receive end interrupt, transmit complete interrupt, receive FIFO interrupt, transmit FIFO interrupt, and error interrupt)	5 sources • Global (2 sources) Global receive FIFO interrupt Global error interrupt • Channels (3 sources per channel) • Channel transmit interrupts Transmit complete interrupt Transmit abort interrupt Transmit/receive FIFO transmit complete interrupt Transmit history interrupt • Transmit/receive FIFO receive interrupt • Channel error interrupt
CAN sleep mode	Ability to reduce current consumption by stopping the CAN clock	—
Software support units	3 software support units • Acceptance filtering support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	—
Test mode	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) —	Test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test)

Table 4.47 Points of Difference between I/O Registers Related to CAN Modules

Register Symbol	Bit Symbol	RX63T	RX24/24U
CTLR	—	Control register	Register not available
BCR	—	Bit configuration register	Register not available
MKRi (i = 0 to 7)	—	Mask register i (i = 0 to 7)	Register not available
FIDCR0	—	FIFO received ID compare register 0	Register not available
FIDCR1	—	FIFO received ID compare register 1	Register not available
MKIVLR	—	Mask invalid register	Register not available
MBj (j = 0 to 31)	—	Mailbox register j (j = 0 to 31)	Register not available
MIER	—	Mailbox interrupt enable register	Register not available
MCTLj (j = 0 to 31)	—	Message control register j (j = 0 to 31)	Register not available
RFCR	—	Receive FIFO control register	Register not available
RFPCR	—	Receive FIFO pointer control register	Register not available
TFCR	—	Transmit FIFO control register	Register not available
TFPCR	—	Transmit FIFO pointer control register	Register not available
STR	—	Status register	Register not available
MSMR	—	Mailbox search mode register	Register not available
MSSR	—	Mailbox search status register	Register not available
CSSR	—	Channel search support register	Register not available
AFSR	—	Acceptance filter support register	Register not available
EIER	—	Error interrupt enable register	Register not available
EIFR	—	Error interrupt source judge register	Register not available
RECR	—	Receive error count register	Register not available
TECR	—	Transmit error count register	Register not available
ECSR	—	Error code store register	Register not available
TSR	—	time stamp register	Register not available
TCR	—	Test control register	Register not available
CFGL	—	Register not available	Bit configuration register L
CFGH	—	Register not available	Bit configuration register H
CTRL	—	Register not available	Control register L
CTRH	—	Register not available	Control register H
STSL	—	Register not available	Status register L
STSH	—	Register not available	Status register H
ERFLL	—	Register not available	Error flag register L
ERFLH	—	Register not available	Error flag register H
GCFGL	—	Register not available	Global configuration register L
GCFGH	—	Register not available	Global configuration register H
GCTRL	—	Register not available	Global control register L
GCTRH	—	Register not available	Global control register H
GSTS	—	Register not available	Global status register
GERFLL	—	Register not available	Global error flag register

Register Symbol	Bit Symbol	RX63T	RX24/24U
GTINTSTS	—	Register not available	Global transmit interrupt status register
GTSC	—	Register not available	Timestamp register
GAFLCFG	—	Register not available	Receive rule number configuration register
GAFLIDLj (j = 0 to 15)	—	Register not available	Receive rule entry register jAL (j = 0 to 15)
GAFLIDHj (j = 0 to 15)	—	Register not available	Receive rule entry register jAH (j = 0 to 15)
GAFLMLj (j = 0 to 15)	—	Register not available	Receive rule entry register jBL (j = 0 to 15)
GAFLMHj (j = 0 to 15)	—	Register not available	Receive rule entry register jBH (j = 0 to 15)
GAFLPLj (j = 0 to 15)	—	Register not available	Receive rule entry register jCL (j = 0 to 15)
GAFLPHj (j = 0 to 15)	—	Register not available	Receive rule entry register jCH (j = 0 to 15)
RMNB	—	Register not available	Receive buffer number configuration register
RMND0	—	Register not available	Receive buffer receive complete flag register
RMIDLn (n = 0 to 15)	—	Register not available	Receive buffer register nAL (n = 0 to 15)
RMIDHn (n = 0 to 15)	—	Register not available	Receive buffer register nAH (n = 0 to 15)
RMTSn (n = 0 to 15)	—	Register not available	Receive buffer register nBL (n = 0 to 15)
RMPTRn (n = 0 to 15)	—	Register not available	Receive buffer register nBH (n = 0 to 15)
RMDF0n (n = 0 to 15)	—	Register not available	Receive buffer register nCL (n = 0 to 15)
RMDF1n (n = 0 to 15)	—	Register not available	Receive buffer register nCH (n = 0 to 15)
RMDF2n (n = 0 to 15)	—	Register not available	Receive buffer register nDL (n = 0 to 15)
RMDF3n (n = 0 to 15)	—	Register not available	Receive buffer register nDH (n = 0 to 15)
RFCCm (m = 0, 1)	—	Register not available	Receive FIFO control register m (m = 0 or 1)
RFSTSm (m = 0 or 1)	—	Register not available	Receive FIFO status register m (m = 0 or 1)
RFPCTRm (m = 0 or 1)	—	Register not available	Receive FIFO pointer control register m (m = 0 or 1)
RFIDLm (m = 0 or 1)	—	Register not available	Receive FIFO access register mAL (m = 0 or 1)
RFIDHm (m = 0 or 1)	—	Register not available	Receive FIFO access register mAH (m = 0 or 1)
RFTSm (m = 0 or 1)	—	Register not available	Receive FIFO access register mBL (m = 0 or 1)
RFPTRm (m = 0 or 1)	—	Register not available	Receive FIFO access register mBH (m = 0 or 1)

Register Symbol	Bit Symbol	RX63T	RX24/24U
RFDF0m (m = 0 or 1)	—	Register not available	Receive FIFO access register mCL (m = 0 or 1)
RFDF1m (m = 0 or 1)	—	Register not available	Receive FIFO access register mCH (m = 0 or 1)
RFDF2m (m = 0 or 1)	—	Register not available	Receive FIFO access register mDL (m = 0 or 1)
RFDF3m (m = 0 or 1)	—	Register not available	Receive FIFO access register mDH (m = 0 or 1)
CFCCL0	—	Register not available	Transmit/receive FIFO control register 0L
CFCCH0	—	Register not available	Transmit/receive FIFO control register 0H
CFSTS0	—	Register not available	Transmit/receive FIFO status register 0
CFPCTR0	—	Register not available	Transmit/receive FIFO pointer control register 0
CFIDL0	—	Register not available	Transmit/receive FIFO access register 0AL
CFIDH0	—	Register not available	Transmit/receive FIFO access register 0AH
CFTS0	—	Register not available	Transmit/receive FIFO access register 0BL
CFPTR0	—	Register not available	Transmit/receive FIFO access register 0BH
CFDF00	—	Register not available	Transmit/receive FIFO access register 0CL
CFDF10	—	Register not available	Transmit/receive FIFO access register 0CH
CFDF20	—	Register not available	Transmit/receive FIFO access register 0DL
CFDF30	—	Register not available	Transmit/receive FIFO access register 0DH
RFMSTS	—	Register not available	Receive FIFO message lost status register
CFMSTS	—	Register not available	Transmit/receive FIFO message lost status register
RFISTS	—	Register not available	Receive FIFO interrupt status register
CFISTS	—	Register not available	Transmit/receive FIFO receive interrupt status register
TMCp (p = 0 to 3)	—	Register not available	Transmit buffer control register p (p = 0 to 3)
TMSTSp (p = 0 to 3)	—	Register not available	Transmit buffer status register p (p = 0 to 3)
TMTRSTS	—	Register not available	Transmit buffer transmit request status register
TMTCSTS	—	Register not available	Transmit buffer transmit complete status register
TMTASTS	—	Register not available	Transmit buffer transmit abort status register
TMIEC	—	Register not available	Transmit buffer interrupt enable register

Register Symbol	Bit Symbol	RX63T	RX24/24U
TMIDLp (p = 0 to 3)	—	Register not available	Transmit buffer register pAL (p = 0 to 3)
TMIDHp (p = 0 to 3)	—	Register not available	Transmit buffer register pAH (p = 0 to 3)
TMPTRp (p = 0 to 3)	—	Register not available	Transmit buffer register pBH (p = 0 to 3)
TMDF0p (p = 0 to 3)	—	Register not available	Transmit buffer register pCL (p = 0 to 3)
TMDF1p (p = 0 to 3)	—	Register not available	Transmit buffer register pCH (p = 0 to 3)
TMDF2p (p = 0 to 3)	—	Register not available	Transmit buffer register pDL (p = 0 to 3)
TMDF3p (p = 0 to 3)	—	Register not available	Transmit buffer register pDH (p = 0 to 3)
THLCC0	—	Register not available	Transmit history buffer control register
THLSTS0	—	Register not available	Transmit history buffer status register
THLACC0	—	Register not available	Transmit history buffer access register
THLPCTR0	—	Register not available	Transmit history buffer pointer control register
GRWCR	—	Register not available	Global RAM window control register
GTSTCFG	—	Register not available	Global test configuration register
GTSTCTRL	—	Register not available	Global test control register
GLOCKK	—	Register not available	Global test protection unlock register
RPGACCr (r = 0 to 127)	—	Register not available	RAM test register r (r = 0 to 127)

4.4.21 Serial Peripheral Interface

Table 4.48 lists the points of difference between the serial peripheral interfaces, and Table 4.49 lists the points of difference between the I/O registers related to the serial peripheral interfaces.

Table 4.48 Points of Difference between Serial Peripheral Interfaces

Item	RX63T	RX24T and RX24U
Number of channels	2 channels	1 channel
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the externally input clock is used as the serial clock (the maximum frequency is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 6). Width at high level: 3 cycles of PCLK; width at low level: 3 cycles of PCLK
Buffer configuration	• The transmit and receive buffers have a double buffer configuration. —	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection —	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. —	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function
Interrupt sources	Interrupt sources: Receive buffer full interrupt Transmit buffer empty interrupt RSPI error interrupt (mode fault, overrun, parity error) RSPI idle interrupt (RSPI idle)	Interrupt sources: Receive buffer full interrupt Transmit buffer empty interrupt RSPI error interrupt (mode fault, overrun, underrun, parity error) RSPI idle interrupt (RSPI idle)
Other functions	— • Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function

Table 4.49 Points of Difference between I/O Registers Related to Serial Peripheral Interfaces

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
SPPCR	SPOM	RSPI output pin mode bit	Reserved
SPSR	UDRF	Reserved	Underrun error flag
SPCR2	SCKASE	Reserved	RSPCK auto-stop function enable bit

4.4.22 12-Bit A/D Converter

Table 4.50 lists the points of difference between the 12-bit A/D converters, and Table 4.51 lists the points of difference between the I/O registers related to the 12-bit A/D converters.

Table 4.50 Points of Difference between 12-Bit A/D Converters

Item	RX63T	RX24T and RX24U
Number of units	2 units	3 units
Input channels	8 channels (4 channels × 2 units)	22 channels (20 on 100-pin version of RX24U)
Extended analog function	—	Internal reference voltage (S12AD2 only)
Conversion time	1.0 μs per channel (when operating with A/D conversion clock ADCLK = 50 MHz)	1.0 μs per channel (when operating with A/D conversion clock ADCLK = 40 MHz)
A/D conversion clock	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency ratio is one of the following: PCLKB:ADCLK frequency ratio = 1:1, 1:2, 1:4, 1:8 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency ratio is one of the following: PCLK:ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.

Item	RX63T	RX24T and RX24U
Data register	• 8 registers for analog input, 1 for A/D converted data duplication in double trigger mode, and 2 for A/D-converted data duplication during extended operation in double trigger mode	• 22 registers for analog input, 1 for A/D converted data duplication in double trigger mode, and 2 for A/D-converted data duplication during extended operation in double trigger mode unit
	—	• 1 register for internal reference voltage
	—	• 1 register per unit for self-diagnostics
	• The results of A/D conversion are stored in 12-bit A/D data registers.	• The results of A/D conversion are stored in 12-bit A/D data registers.
	• Output with 8-, 10-, 12-bit accuracy supported for A/D conversion results. (ability to select between 2-bit and 4-bit right-shifted conversion result output)	• Output with 12-bit accuracy supported for A/D conversion results.
	• In A/D-converted value addition mode, the value obtained by adding up A/D-converted results is stored as a 14-bit value in the A/D data registers.	• The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode.
	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.
	• Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Item	RX63T	RX24T and RX24U
Operating mode	• Single-cycle scan mode: A/D conversion is performed only once on the analog inputs of up to 4 user-selected channels. —	• Single scan mode: A/D conversion is performed only once on the analog inputs of user-selected channels. A/D conversion is performed only once on the internal reference voltage (S12AD2).
	• Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 4 channels.	• Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of user-selected channels.
	• Group scan mode: Analog inputs on up to 4 channels are divided among group A and group B, and A/D conversion of the analog inputs on all channels of each group is performed once only. Separate A/D conversion start conditions can be selected for each group, making it possible to start A/D conversion at different times for group A and group B.	• Group scan mode: Either two (A and B) or three (A, B, and C) groups may be selected. (When the number of groups selected is two, only the combination of group A and group B is selectable.) The user-selected channels are divided among group A and group B or among group A, group B, and group C, and A/D conversion of the analog inputs selected on a group basis is performed only once. The scanning start conditions (synchronous triggers) can be selected independently for group A, group B, and group C, allowing conversion to start at a different time for each group.
	• Group scan mode (when group A is given priority): If a group A trigger is input during A/D conversion on group B, A/D conversion on group B stops and A/D conversion is performed on group A. After A/D conversion on group A completes, A/D conversion is restarted on group B (rescan).	• Group scan mode (with group priority control selected): If a trigger for a higher-priority group occurs when A/D conversion on a lower-priority group is in progress, scanning of the lower-priority group is stopped and scanning of the higher-priority group starts. Regarding the priority sequence, a setting is available to specify whether or not scanning of the lower-priority group restarts (rescan) after scanning finishes of group A (high priority), group B (middle priority), and group C (low priority). For rescanning, a setting is available to specify whether to start from the first of the selected channels or from the next unscanned channel after the last channel on which A/D conversion completed.

Item	RX63T	RX24T and RX24U
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by the multi-function timer pulse unit 3 (MTU3) or the general PWM timer (GPT) • Asynchronous trigger A/D conversion can be externally triggered by the ADTRGn# pin.	• Software trigger • Synchronous trigger Conversion start is triggered by the multi-function timer pulse unit 3 (MTU3d), the general PWM timer (GPT), or the 8-bit timer (TMR). • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (separately for each of three units).
Functions	• Sample-and-hold function • Channel-dedicated sample-and-hold function (3 channels per unit) • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • A/D-converted value adding mode • Discharge function • Double trigger mode (duplication of A/D conversion data) • Window comparator function (3 channels per unit) • Input signal amplification function using programmable gain amplifier (3 channels per unit) — —	— • Channel-dedicated sample-and-hold function (3 channels/S12AD1 only) • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode — • Double trigger mode (duplication of A/D conversion data) — • Input signal amplification function using programmable gain amplifier (1 channel/S12AD, 3 channels/S12AD1) • Analog input disconnection assist detection function (discharge function/precharge function) • Automatic clear function for A/D data registers

Item	RX63T	RX24T and RX24U
Interrupt sources	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a single scan.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a single scan (separately for each of three units).
	• In double trigger mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan.	• In double trigger mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a double scan (separately for each of three units).
	• In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI or GBADI1) can be generated.	• In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI, GBADI1, or GBADI2) can be generated, and on completion of a group C scan a dedicated group C scan end interrupt request (GCADI, GCADI1, or GCADI2) can be generated.
	• When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of two scans of group A. On completion of a group B scan a dedicated group B scan end interrupt request (S12GBADI or S12GBADI1) can be generated.	• When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of two scans of group A. On completion of two scans of group B or C a dedicated group B or group C scan end interrupt request (GBADI, GBADI1, GBADI2, GCADI, GCADI1, or GCADI2) can be generated.
	• An interrupt request (CMP0 to CMP2 or CMP4 to CMP6) is generated (and can be used as a POE source) in response to detection by the comparator.	—
	• The S12ADI, S12GBADI, S12ADI1, or S12GBADI1 interrupt or an interrupt among CMP0 to CMP2 or CMP4 to CMP6 interrupt can be used to activate the DMA controller (DMAC) or the data-transfer controller (DTC).	• The S12ADI/ S12ADI1/S12ADI2, GBADI GBADI/GBADI1/GBADI2, and GCADI/GCADI1/GCADI2 interrupts can activate the data transfer controller (DTC).

Table 4.51 Points of Difference between I/O Registers Related to 12-Bit A/D Converters

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
ADOCDR	—	Register not available	A/D internal reference voltage data register
ADANSA	—	A/D channel select register A	Register not available
ADANSB	—	A/D channel select register B	Register not available
ADANSA0	—	Register not available	A/D channel select register A0
ADANSA1	—	Register not available	A/D channel select register A1
ADANSB0	—	Register not available	A/D channel select register B0
ADANSB1	—	Register not available	A/D channel select register B1
ADANSC0	—	Register not available	A/D channel select register C0
ADANSC1	—	Register not available	A/D channel select register C1
ADADS	—	A/D-converted value addition mode select register	Register not available
ADADS0	—	Register not available	A/D-converted value addition/average function channel select register 0
ADADS1	—	Register not available	A/D-converted value addition/average function channel select register 1
ADADC A/D-converted value addition count select register (RX63T) A/D-converted value addition/average count select register (RX24T/RX24U)	ADC[1:0] (RX63T) ADC[2:0] (RX24T/24U)	Addition count select bits 0 0: 1-time conversion (no addition, same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times) Bit 2 is reserved.	Addition count select bits 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice) 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times)
	AVEE	Reserved	Average mode enable bit
ADCER	ADPRC[1:0]	A/D data register bit precision setting bits	Reserved
	DCE	Discharge enable bit	Reserved
	ACE	Automatic clearing enable bit	A/D data register automatic clearing enable bit
ADSSTRn (n = 0 to 3) (RX63T) (n = 0 to 11, L, O) (RX24T/RX24U)	—	Sampling time setting bits Initial value after a reset is different.	No bit name
ADDISCR	—	Register not available	A/D disconnection detection control register

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
ADGSPCR	LGRRS	Reserved	Restart channel select bit
	GBRP	Single-cycle scan continuous activation bit for group B (Enabled only when PGS = 1. Reserved bit when PGS = 0.) 0: Single-cycle scans through group B are not continuously activated. 1: Single-cycle scans through group B are continuously activated.	Single scan continuous start bit (Enabled only when PGS = 1. Reserved bit when PGS = 0.) 0: Single scan is not continuously activated. 1: Single scan is continuously activated for the lowest-priority group.
ADCMPMD0	—	Comparator operating-mode selection register 0	Register not available
ADCMPMD1	—	Comparator operating-mode selection register 1	Register not available
ADCMPNR0	—	Comparator filter-mode register 0	Register not available
ADCMPFR	—	Comparator detection flag register	Register not available
ADCMPSEL	—	Comparator interrupt selection register	Register not available
ADPG	—	A/D programmable gain amplifier register	Register not available
ADGSPMR	—	A/D group scan priority control register	Register not available
ADEXICR	—	Register not available	A/D conversion extended input control register
ADGCTRGR	—	Register not available	A/D group C trigger select register
ADSHCR	—	Register not available	A/D sample-and-hold circuit control register
ADGSPCR	—	Register not available	A/D group scan priority control register
ADPGACR	—	Register not available	A/D programmable gain amplifier control register
ADPGAGS0	—	Register not available	A/D programmable gain amplifier gain setting register 0

4.4.23 D/A Converter

Table 4.52 lists the points of difference between the D/A converters, and Table 4.53 lists the points of difference between the D/A converter registers.

Table 4.52 Points of Difference between D/A Converters

Item	RX63T	RX24T and RX24U
Resolution	10 bits	8 bits
Output channels	2 channels	2 channels
Countermeasure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 10-bit A/D converter synchronous D/A conversion enable input signal from the 10-bit A/D converter. (Degradation of A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.)	Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2). Therefore, degradation of A/D conversion accuracy caused by interference is reduced by controlling the 8-bit D/A converter inrush current generation timing with the enable signal.

Table 4.53 Points of Difference between D/A Converter Registers

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
DACR	DAE	D/A enable	Reserved

4.4.24 RAM

Table 4.54 lists the points of difference between the RAM modules.

Table 4.54 Points of Difference between the RAM Modules

Item	RX63T	RX24T and RX24U
RAM capacity	48 KB, 32 KB, or 24 KB	32 KB or 16 KB*[1]
RAM address	0000 0000h to 0000 BFFFh (48 KB) 0000 0000h to 0000 7FFFh (32 KB) 0000 0000h to 0000 5FFFh (24 KB) —	— 0000 0000h to 0000 7FFFh (32 KB) — 0000 0000h to 0000 3FFFh (16 KB)

Note 1. RX24T Group only

4.4.25 Flash Memory

Table 4.55 lists the points of difference between the flash memory modules, and Table 4.56 lists the points of difference between the I/O registers related to the flash memory modules.

Table 4.55 Points of Difference between Flash Memory Modules

	RX63T		RX24T and RX24U	
Item	**ROM**	**E2 DataFlash**	**ROM**	**E2 DataFlash**
Memory space	• User area: 512 KB 384 KB 256 KB • User boot area: 16 KB	• Data area: 32 KB	• User area: 512 KB 384 KB 256 KB (RX24T only) 128 KB —	• Data area: 8 KB
ROM cache	—		Capacity: 2 KB	
Read cycle	High-speed read operation using 1 cycle of ICLK is supported.	A read operation in word or byte units takes 6 cycles of PCLK.	No ROM wait cycles when ICLK ≤ 32 MHz, ROM wait cycle when ICLK > 32 MHz	—
Value after erase	FFh	Undetermined	FFh	FFh
Interrupt	A flash ready interrupt request (FRDYI) is generated upon completion of FCU command execution (program, P/E suspend, lock bit read 2, peripheral clock notify).	A flash ready interrupt request (FRDYI) is generated upon completion of FCU command execution (program, P/E suspend, blank check, peripheral clock notify).	A flash ready interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	
Programming/ erasing method	• On-chip dedicated sequencer (FCU) for programming of the ROM • Programming and erasing the ROM are handled by issuing commands to the FCU.		Software programming commands • The following software commands are implemented: Program, blank check, block erase, all-block erase • The following commands are implemented for programming the extra area: Start-up area information program, access window information program	
Suspension and resumption functions	• The CPU is able to execute program code from the ROM when programming or erasure of the ROM is suspended. • Programming and erasure of the ROM can be restarted (resumed) after suspension.		—	

Item	RX63T		RX24T and RX24U	
	ROM	E2 DataFlash	ROM	E2 DataFlash
Programming/ erasing unit	• Programming of user area and user boot area: 128 bytes • Erasing of user area: block; erasing of user boot area: 16 KB	• Programming of data area: 2 bytes • Erasing of data area: 32 bytes	• Unit of programming for the user area: 8 bytes • Unit of erasure for the user area: 2 KB	• Unit of programming for the data area: 1 byte • Unit of erasure for the data area: 1 KB
On-board programming	Programming in boot mode • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. • Ability to overwrite user boot area — Programming in user boot mode • Ability to create original boot programs of the user's making Programming by a routine for ROM/data flash programming within the user program • Ability to overwrite ROM/E2 DataFlash without resetting the system		Boot mode (SCI interface) • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. — Boot mode (FINE interface) • FINE is used • Ability to overwrite user area and data area — Self-programming • Ability to overwrite the user area and data area can be overwritten by means of a flash programming routine in a user program, without resetting the system	
Off-board programming	Ability to use a flash writer to program the user area and the user boot area.	—	The user area can be programmed using a flash programmer (serial programmer or parallel programmer) compatible with the RX24T Group.	
Software controlled protection function	The FENTRYR.FENTRY 0 bit, FWEPROR.FLWE [1:0] bits, and lock bits can be used to prevent unintentional programming.	The FENTRYR.FENTRY D bit, FWEPROR.FLWE [1:0] bits, and DFLREk and DFLWEk registers, can be used to prevent unintentional programming (k = 0 or 1).	The FENTRYR.FENTRY 0 bit can be used to prevent unintentional programming.	The FENTRYR.FENTRY D bit can be used to prevent unintentional programming.
ID code protection	• This function can be used to prevent reading, writing, or erasing by the host. • ID codes can be used for control when connected to an on-chip debugging emulator. —		• Connection with the serial programmer in boot mode can be enabled or disabled using ID codes in boot mode. • ID codes can be used for control when connected to an on-chip debugging emulator. • Control by ROM code is possible when connecting a parallel programmer.	

Item	RX63T		RX24T and RX24U	
	ROM	E2 DataFlash	ROM	E2 DataFlash
Start-up program protection function	—	—	This function is used to safely rewrite blocks 0 to 7.	
Area protection	—	—	This function enables rewriting only the selected blocks in the user area and disables writing to the other blocks during self-programming.	

Table 4.56 Points of Difference between I/O Registers Related to Flash Memory Modules

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
FWEPROR	—	Flash P/E protection register	Register not available
FMODR	—	Flash mode register	Register not available
FASTAT	—	Flash access status register	Register not available
FAEINT	—	Flash access error interrupt enable register	Register not available
FRDYIE	—	Flash ready interrupt enable register	Register not available
DFLRE0	—	E2 DataFlash read enable register 0	Register not available
DFLRE1	—	E2 DataFlash read enable register 1	Register not available
DFLWE0	—	E2 DataFlash P/E enable register 0	Register not available
DFLWE1	—	E2 DataFlash P/E enable register 1	Register not available
FSTATR0	PRGSPD	Programming suspend status flag (b0)	Not available
	ERERR	Not available	Erase error flag (b0)
	ERSSPD	Erasure suspend status flag (b1)	Not available
	PRGERR	Program error flag (b4)	Program error flag (b1)
	SUSRDY	Suspend ready flag (b3)	Not available
	BCERR	Not available	Blank check error flag (b3)
	ERSERR	Erasure error bit (b5)	Not available
	EILGLERR	Not available	Extra area illegal command error flag (b5)
	ILGLERR	Illegal command error flag (b6)	Reserved
	FRDY	Flash ready flag (b7)	Reserved
FSTATR1	FLOCKST	Lock bit status bit	Reserved
	FRDY	Reserved	Flash ready flag
	FCUERR	FCU error bit (b7)	Not available
	EXRDY	Not available	Extra area ready flag (b7)
FPROTR	—	Flash protection register	Register not available
FRESETR	FRKEY[7:0]	Key code	Reserved
FCMDR	—	FCU command register	Register not available
FCPSR	—	FCU processing switching register	Register not available
DFLBCCNT	—	E2 DataFlash blank check control register	Register not available
FPESTAT	—	Flash P/E status register	Register not available

Register Symbol	Bit Symbol	RX63T	RX24T and RX24U
DFLBCSTAT	—	E2 DataFlash blank check status register	Register not available
PCKAR	—	Peripheral clock notification register	Register not available
DFLCTL	—	Register not available	E2 DataFlash control register
FPR	—	Register not available	Protection unlock register
FPSR	—	Register not available	Protection unlock status register
FPMCR	—	Register not available	Flash P/E mode control register
FISR	—	Register not available	Flash initial setting register
FASR	—	Register not available	Flash area select register
FCR	—	Register not available	Flash control register
FEXCR	—	Register not available	Flash extra area control register
FSARH	—	Register not available	Flash processing start address register H
FSARL	—	Register not available	Flash processing start address register L
FEARH	—	Register not available	Flash processing end address register H
FEARL	—	Register not available	Flash processing end address register L
FWBn (n = 0 to 3)	—	Register not available	Flash write buffer n register
FEAMH	—	Register not available	Flash error address monitor register H
FEAML	—	Register not available	Flash error address monitor register L
FSCMR	—	Register not available	Flash start-up setting monitor register
FAWSMR	—	Register not available	Flash access window start address monitor register
FAWEMR	—	Register not available	Flash access window end address monitor register
UIDRn (n = 0 to 3)	—	Register not available	Unique ID register n
ROMCE	—	Register not available	ROM cache enable register
ROMCIV	—	Register not available	ROM cache disable register

5. Reference Documents

User's Manual: Hardware

RX63T Group User's Manual: Hardware Rev.2.00 (R01UH0238EJ0220)
(The latest version can be downloaded from the Renesas Electronics website.)

RX24T Group User's Manual: Hardware Rev.1.00 (R01UH0576EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

Compatibility with Technical Updates

This application note reflects the content of the following technical update.

TN-RX*-A173A/J

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Oct. 17, 2017	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.3.0-1 November 2016)

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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