RX63N Group, RX631 Group
Application Example of Exclusive Operation of Two Motors by One Set of Complementary PWM Outputs

Abstract
This application note describes an example of exclusive operation of two motors by one set of three-phase complementary pulse width modulation (PWM) outputs using multi-function timer pulse unit 2 (MTU).

Products
- RX63N Group, 177- and 176-pin versions, ROM capacity: 768 KB to 2 MB
- RX63N Group, 145- and 144-pin versions, ROM capacity: 768 KB to 2 MB
- RX63N Group, 100-pin version, ROM capacity: 768 KB to 2 MB
- RX631 Group, 177- and 176-pin versions, ROM capacity: 256 KB to 2 MB
- RX631 Group, 145- and 144-pin versions, ROM capacity: 256 KB to 2 MB
- RX631 Group, 100-pin version, ROM capacity: 256 KB to 2 MB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.
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1. Specifications

Using the MTU’s complementary PWM mode 3, three-phase complementary PWM waveforms and a toggle waveform synchronized with the PWM cycle are output. A dead time is specified for the complementary PWM outputs to ensure a non-overlapping relationship between the positive-phase and negative-phase pulses.

After a reset is canceled, complementary PWM waveforms are output on PWM output pin group 0 (PC5, PC4, PB3, PB1, PC2, and PC3). When a switch input is detected, the waveforms are output on PWM output pin group 1 (PB7, PB6, PE2, PE1, PE3, and PE4) takes place. Thereafter, the waveforms are output alternately from PWM output pin group 0 and group 1 each time a switch input is detected.

- PWM cycle: 200 μs
- PWM duty: Changes each PWM cycle (initial value: 50%)
- PWM active level: Low level
- Dead time: 4 μs

Table 1.1 lists the peripheral functions used and their applications, and figure 1.1 is a block diagram.

Table 1.1 Peripheral Functions and Their Applications

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>MTU2a channel 3 (MTU3)</td>
<td>Complementary PWM output and PWM cycle toggle output</td>
</tr>
<tr>
<td>MTU2a channel 4 (MTU4)</td>
<td>Complementary PWM output</td>
</tr>
<tr>
<td>MPC</td>
<td>Complementary PWM output pin switching</td>
</tr>
</tbody>
</table>

![Figure 1.1 Block Diagram](image-url)
2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller used</td>
<td>R5F563NBDDFC (RX63N Group)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>Main clock: 12 MHz&lt;br&gt;PLL: 192 MHz (main clock divided by 1 and multiplied by 16)&lt;br&gt;System clock (ICLK): 96 MHz (PLL divided by 2)&lt;br&gt;Peripheral module clock B (PCLKB): 48 MHz (PLL divided by 4)</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Integrated development environment</td>
<td>Renesas Electronics Corporation&lt;br&gt;High-performance Embedded Workshop Version 4.09.01</td>
</tr>
<tr>
<td>C compiler</td>
<td>Renesas Electronics Corporation&lt;br&gt;C/C++ Compiler Package for RX Family V.1.02 Release 01</td>
</tr>
<tr>
<td>C compiler Compiler options</td>
<td>-cpu=rx600 -output=obj=&quot;$(CONFIGDIR)$(FILELEAF).obj&quot; -debug -nologo&lt;br&gt;(The integrated development environment default settings are used.)</td>
</tr>
<tr>
<td>iodefine.h version</td>
<td>Version 1.80</td>
</tr>
<tr>
<td>Endian order</td>
<td>Little endian</td>
</tr>
<tr>
<td>Operating mode</td>
<td>Single-chip mode</td>
</tr>
<tr>
<td>Processor mode</td>
<td>Supervisor mode</td>
</tr>
<tr>
<td>Sample code version</td>
<td>Version 1.01</td>
</tr>
<tr>
<td>Board used</td>
<td>Renesas Starter Kit for RX63N (product No.: R0K50563NC010BR)</td>
</tr>
</tbody>
</table>

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

- RX63N Group, RX631 Group: Initial Setting, (R01AN1245EJ)

The initial setting function described in the above application note is used by the sample code in this application note. The latest version can be obtained from the Renesas Electronics Web site. If a newer version is available, replace the current version with the newest version.
4. Hardware

4.1 Hardware Configuration

Figure 4.1 shows a connection example.

![Connection Example Diagram]

4.2 Pins Used

Table 4.1 lists the pins used and their functions.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P32</td>
<td>Input</td>
<td>Switch input for changing PWM output pin group</td>
</tr>
<tr>
<td>P14/MTIOC3A</td>
<td>Output</td>
<td>PWM cycle toggle output</td>
</tr>
<tr>
<td>PC5/MTIOC3B</td>
<td>Output</td>
<td>PWM output 1 (positive-phase) PWM output pin group 0</td>
</tr>
<tr>
<td>PC4/MTIOC3D</td>
<td>Output</td>
<td>PWM output 1 (negative-phase) PWM output pin group 0</td>
</tr>
<tr>
<td>PB3/MTIOC4A</td>
<td>Output</td>
<td>PWM output 2 (positive-phase) PWM output pin group 0</td>
</tr>
<tr>
<td>PB1/MTIOC4C</td>
<td>Output</td>
<td>PWM output 2 (negative-phase) PWM output pin group 0</td>
</tr>
<tr>
<td>PC2/MTIOC4B</td>
<td>Output</td>
<td>PWM output 3 (positive-phase) PWM output pin group 0</td>
</tr>
<tr>
<td>PC3/MTIOC4D</td>
<td>Output</td>
<td>PWM output 3 (negative-phase) PWM output pin group 0</td>
</tr>
<tr>
<td>PB7/MTIOC3B</td>
<td>Output</td>
<td>PWM output 1 (positive-phase) PWM output pin group 1</td>
</tr>
<tr>
<td>PB6/MTIOC3D</td>
<td>Output</td>
<td>PWM output 1 (negative-phase) PWM output pin group 1</td>
</tr>
<tr>
<td>PE2/MTIOC4A</td>
<td>Output</td>
<td>PWM output 2 (positive-phase) PWM output pin group 1</td>
</tr>
<tr>
<td>PE1/MTIOC4C</td>
<td>Output</td>
<td>PWM output 2 (negative-phase) PWM output pin group 1</td>
</tr>
<tr>
<td>PE3/MTIOC4B</td>
<td>Output</td>
<td>PWM output 3 (positive-phase) PWM output pin group 1</td>
</tr>
<tr>
<td>PE4/MTIOC4D</td>
<td>Output</td>
<td>PWM output 3 (negative-phase) PWM output pin group 1</td>
</tr>
</tbody>
</table>
5. Software

After the initial settings, a toggle waveform synchronized with the PWM cycle, and three-phase complementary PWM waveforms on PWM output pin group 0, are output.

When a switch input is detected, the complementary PWM waveform output destination is switched between PWM output pin group 0 and group 1 alternately. The carrier cycle of the PWM output is 200 μs. This interrupt every 200 μs is used to generate 5 ms of switch input read cycle, and an input is determined when the switch input level matches three times in succession.

The peripheral function settings used are listed below.

**MTU (MTU3 and MTU4)**

- **Counter clock:** PCLKB/4 rising edge
- **Operation mode:** Complementary PWM mode 3 (transfer at crest and trough)
- **Dead time:** 4 μs
- **Carrier cycle (PWM cycle):** 200 μs (carrier frequency: 5 kHz)
- **TDTR register:** Sets offset value of MTU4.TCNT and MTU3.TCNT (dead time) (setting value: 48 = 4 μs / counter clock cycle)
- **TCDR register:** Sets MTU4.TCNT upper limit value (1/2 of carrier cycle) (setting value: 1200 = 100 μs / counter clock cycle)
- **TCBR register:** Operates as buffer register of TCDR register
- **MTU3.TGRA register:** Sets MTU3.TCNT upper limit value (1/2 of carrier cycle + dead time) (setting value: 1248 = 1200 + 48)
- **MTU3.TGRB register:** Sets duty of PWM output 1 (initial value: 50%) (setting value: 600 = 1200 / 2)
- **MTU3.TGRC register:** Operates as buffer register of MTU3.TGRA register
- **MTU3.TGRD register:** Operates as buffer register of MTU3.TGRB register
- **MTU4.TGRA register:** Sets duty of PWM output 2 (initial value: 50%) (setting value: 600 = 1200 / 2)
- **MTU4.TGRB register:** Sets duty of PWM output 3 (initial value: 50%) (setting value: 600 = 1200 / 2)
- **MTU4.TGRC register:** Operates as buffer register of MTU4.TGRA register
- **MTU4.TGRD register:** Operates as buffer register of MTU4.TGRB register
- **Positive-phase output levels:**
  - Initial output: High
  - Active level: Low
  - Compare match output (up counter): Low
  - Compare match output (down counter): High
- **Negative-phase output levels:**
  - Initial output: High
  - Active level: Low
  - Compare match output (up counter): High
  - Compare match output (down counter): Low
- **PWM sync output:** Toggle output enabled
- **PWM output pin 1:** MTIOC3B and MTIOC3D pin output enabled
- **PWM output pin 2:** MTIOC4A and MTIOC4C pin output enabled
- **PWM output pin 3:** MTIOC4B and MTIOC4D pin output enabled
- **Counter clearing:** Clearing TCNT disabled
- **Interrupt:** Use TGR interrupt request A (MTU3.TGIA3)
5.1 Operation

(1) Initial Settings
After the initial settings, a toggle waveform synchronized with the PWM cycle, and three-phase complementary PWM waveforms on PWM output pin group 0, are output.

(2) TGIA3 Interrupt Handler
The interrupt handler for TGIA3, which is generated every 200 µs, increments (+1) the switch read cycle counter for measuring 5 ms intervals, and changes the PWM output duty.

(3) Switch Input Determination
When the switch input level, which is read every 5 ms, matches three times consecutively, the switch input determination flag is set to 1.

(4) PWM Output Pin Group Switching
When the switch input determination flag is set to 1, PWM output pin group 0 is set as general input ports and group 1 is set as PWM output pins. The output of PWM output pin group 0 becomes high-impedance, and complementary PWM waveforms are output on group 1.

Figure 5.1 is a timing chart.
5.2 File Composition

Table 5.1 lists the files used in the sample code. Files generated by the integrated development environment are not included in this table.

Table 5.1 Files Used in the Sample Code

<table>
<thead>
<tr>
<th>File Name</th>
<th>Outline</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>main.c</td>
<td>Main processing</td>
<td></td>
</tr>
<tr>
<td>r_init_stop_module.c</td>
<td>Stop processing for peripheral functions that are active after a reset</td>
<td></td>
</tr>
<tr>
<td>r_init_stop_module.h</td>
<td>r_init_stop_module.c header file</td>
<td></td>
</tr>
<tr>
<td>r_init_non_existent_port.c</td>
<td>Nonexistent port initialization</td>
<td></td>
</tr>
<tr>
<td>r_init_non_existent_port.h</td>
<td>r_init_non_existent_port.c header file</td>
<td></td>
</tr>
<tr>
<td>r_init_clock.c</td>
<td>Clock initialization</td>
<td></td>
</tr>
<tr>
<td>r_init_clock.h</td>
<td>r_init_clock.c header file</td>
<td></td>
</tr>
</tbody>
</table>

5.3 Option-Setting Memory

Table 5.2 lists the option-setting memory configured in the sample code. When necessary, set a value suited to the user system.

Table 5.2 Option-Setting Memory Configured in the Sample Code

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFS0</td>
<td>FFFF FF8Fh to FFFF FF8Ch</td>
<td>FFFF FFFFh</td>
<td>IWDT is stopped after a reset. WDT is stopped after a reset.</td>
</tr>
<tr>
<td>OFS1</td>
<td>FFFF FF88h to FFFF FF88h</td>
<td>FFFF FFFFh</td>
<td>Voltage monitor 0 reset is disabled after a reset. HOCO oscillation is disabled after a reset.</td>
</tr>
<tr>
<td>MDES</td>
<td>FFFF FF83h to FFFF FF80h</td>
<td>FFFF FFFFh</td>
<td>Little endian</td>
</tr>
</tbody>
</table>
5.4 Constants
Table 5.3 lists the constants used in the sample code.

Table 5.3 Constants Used in the Sample Code

<table>
<thead>
<tr>
<th>Constant Name</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW_NUM</td>
<td>3</td>
<td>Switch match determination count</td>
</tr>
<tr>
<td>SW_CYCLE</td>
<td>25</td>
<td>Switch read cycle: 5 ms = PWM cycle (200 µs) × 25</td>
</tr>
<tr>
<td>LOW</td>
<td>0</td>
<td>Low level</td>
</tr>
<tr>
<td>HIGH</td>
<td>1</td>
<td>High level</td>
</tr>
<tr>
<td>PWM_GROUP_0</td>
<td>0</td>
<td>PWM output pin group 0</td>
</tr>
<tr>
<td>PWM_GROUP_1</td>
<td>1</td>
<td>PWM output pin group 1</td>
</tr>
<tr>
<td>PWM_DEAD_TIME</td>
<td>48</td>
<td>Dead time: 4 µs = MTU counter clock cycle (1/12 MHz) × 48</td>
</tr>
<tr>
<td>PWM_CYCLE</td>
<td>1200</td>
<td>1/2 of carrier cycle: 100 µs = MTU counter clock cycle (1/12 MHz) × 1200</td>
</tr>
<tr>
<td>PWM_MAX</td>
<td>(PWM_CYCLE + PWM_DEAD_TIME)</td>
<td>MTU3.TCNT upper limit value: 104 µs</td>
</tr>
<tr>
<td>PWM_DUTY_50</td>
<td>(PWM_CYCLE / 2)</td>
<td>PWM duty setting value: 50%</td>
</tr>
<tr>
<td>PWM_DUTY_ADD</td>
<td>0</td>
<td>PWM duty setting value state: Add</td>
</tr>
<tr>
<td>PWM_DUTY_SUB</td>
<td>1</td>
<td>PWM duty setting value state: Subtract</td>
</tr>
</tbody>
</table>

5.5 Variables
Table 5.4 lists the global variables.

Table 5.4 Global Variables

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>sw_cycle_cnt</td>
<td>Switch read cycle counter for measuring 5 ms intervals</td>
<td>main</td>
</tr>
<tr>
<td></td>
<td>sw_match_cnt</td>
<td>Switch match counter</td>
<td>sw_input_check</td>
</tr>
<tr>
<td></td>
<td>sw_level_last</td>
<td>Switch previous level</td>
<td>sw_input_check</td>
</tr>
<tr>
<td></td>
<td>sw_level_fix</td>
<td>Switch determination level</td>
<td>sw_input_check</td>
</tr>
<tr>
<td></td>
<td>sw_fix_flag</td>
<td>Switch input determination flag</td>
<td>main</td>
</tr>
<tr>
<td></td>
<td>pwm_pin</td>
<td>PWM output pin</td>
<td>pwm_pin_change</td>
</tr>
<tr>
<td></td>
<td>pwm_duty_state</td>
<td>PWM duty setting value state</td>
<td>Excep_MTU3_TGIA3</td>
</tr>
<tr>
<td>unsigned short</td>
<td>pwm_1_duty</td>
<td>PWM output 1 duty setting value</td>
<td>Excep_MTU3_TGIA3</td>
</tr>
<tr>
<td>unsigned short</td>
<td>pwm_2_duty</td>
<td>PWM output 2 duty setting value</td>
<td>Excep_MTU3_TGIA3</td>
</tr>
<tr>
<td>unsigned short</td>
<td>pwm_3_duty</td>
<td>PWM output 3 duty setting value</td>
<td>Excep_MTU3_TGIA3</td>
</tr>
</tbody>
</table>
5.6 Functions

Table 5.5 lists the functions used in the sample code.

Table 5.5 Functions Used in the Sample Code

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>main</td>
<td>Main processing</td>
</tr>
<tr>
<td>port_init</td>
<td>Port initialization</td>
</tr>
<tr>
<td>R_INIT_StopModule</td>
<td>Stop processing for active peripheral functions after a reset</td>
</tr>
<tr>
<td>R_INIT_NonExistentPort</td>
<td>Nonexistent port initialization</td>
</tr>
<tr>
<td>R_INIT_Clock</td>
<td>Clock initialization</td>
</tr>
<tr>
<td>peripheral_init</td>
<td>Peripheral function initialization</td>
</tr>
<tr>
<td>mtu_init</td>
<td>MTU initialization</td>
</tr>
<tr>
<td>pwm_pin_change</td>
<td>PWM output pin switching</td>
</tr>
<tr>
<td>pwm_pin_group_0</td>
<td>PWM output pin group 0 settings</td>
</tr>
<tr>
<td>pwm_pin_group_1</td>
<td>PWM output pin group 1 settings</td>
</tr>
<tr>
<td>sw_input_check</td>
<td>Switch input determination</td>
</tr>
<tr>
<td>Excep_MTU3_TGIA3</td>
<td>MTU3.TGIA3 interrupt handler</td>
</tr>
</tbody>
</table>
5.7 Function Specifications

The following tables list the sample code function specifications.

**main**

<table>
<thead>
<tr>
<th>Outline</th>
<th>Main processing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>None</td>
</tr>
<tr>
<td>Declaration</td>
<td>void main(void)</td>
</tr>
<tr>
<td>Description</td>
<td>After initialization, determine the input level of the switch input for changing PWM output pin group every 5 ms. When the switch input determination flag is set to 1, change the PWM output pins.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
</tbody>
</table>

**port_init**

<table>
<thead>
<tr>
<th>Outline</th>
<th>Port initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>None</td>
</tr>
<tr>
<td>Declaration</td>
<td>void port_init(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Initialize the ports.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
</tbody>
</table>

**R_INIT_StopModule**

<table>
<thead>
<tr>
<th>Outline</th>
<th>Stop processing for active peripheral functions after a reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>r_init_stop_module.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_INIT_StopModule(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Configure the setting to enter the module stop-state.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
<tr>
<td>Remarks</td>
<td>Transition to the module-stop state is not performed in the sample code. Refer to the application note RX63N Group, RX631 Group: Initial Setting, Rev. 1.00, for details of this function.</td>
</tr>
</tbody>
</table>

**R_INIT_NonExistentPort**

<table>
<thead>
<tr>
<th>Outline</th>
<th>Nonexistent port initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>r_init_non_existent_port.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_INIT_NonExistentPort(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Initialize port direction registers for ports that do not exist in products with less than 176 pins.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
<tr>
<td>Remarks</td>
<td>The number of pins in the sample code is set for the 176-pin package (PIN_SIZE=176). After this function is called, when writing in byte units to the PDR registers that have nonexistent ports, set the bits corresponding to nonexistent ports as follows: set the I/O select bits to 1 and set the output data store bits to 0. Refer to the application note RX63N Group, RX631 Group: Initial Setting, Rev. 1.00, for details of this function.</td>
</tr>
</tbody>
</table>
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by One Set of Complementary PWM Outputs

R_INIT_Clock

<table>
<thead>
<tr>
<th>Outline</th>
<th>Clock initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>r_init_clock.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_INIT_Clock(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Initialize the clock.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
<tr>
<td>Remarks</td>
<td>The sample code selects processing which uses PLL as the system clock without using the sub-clock. Refer to the application note RX63N Group, RX631 Group: Initial Setting, Rev. 1.00, for details of this function.</td>
</tr>
</tbody>
</table>

peripheral_init

<table>
<thead>
<tr>
<th>Outline</th>
<th>Peripheral function initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>None</td>
</tr>
<tr>
<td>Declaration</td>
<td>void peripheral_init(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Initialize the peripheral functions used by the sample code.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
</tbody>
</table>

mtu_init

<table>
<thead>
<tr>
<th>Outline</th>
<th>MTU initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>None</td>
</tr>
<tr>
<td>Declaration</td>
<td>void mtu_init(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Initialize the MTU (MTU3 and MTU4).</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
</tbody>
</table>

pwm_pin_change

<table>
<thead>
<tr>
<th>Outline</th>
<th>PWM output pin switching</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>None</td>
</tr>
<tr>
<td>Declaration</td>
<td>void pwm_pin_change(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Switch alternately between PWM output pin group 0 and group 1.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
</tbody>
</table>

pwm_pin_group_0

<table>
<thead>
<tr>
<th>Outline</th>
<th>PWM output pin group 0 settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>None</td>
</tr>
<tr>
<td>Declaration</td>
<td>void pwm_pin_group_0(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Change the PWM output pins from group 1 to group 0.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
</tbody>
</table>
pwm_pin_group_1

Outline
PWM output pin group 1 settings

Header
None

Declaration
void pwm_pin_group_1(void)

Description
Change the PWM output pins from group 0 to group 1.

Arguments
None

Return Value
None

sw_input_check

Outline
Switch input determination

Header
None

Declaration
void sw_input_check(void)

Description
Determine the switch input level. Compare the current level to the previous level, and determine the input level when the levels match three times consecutively. When the determination level is changed from high to low, set the switch input determination flag to 1.

Arguments
None

Return Value
None

Excep_MTU3_TGIA3

Outline
MTU3.TGIA3 interrupt handler

Header
None

Declaration
void Excep_MTU3_TGIA3(void)

Description
Change the duty of the PWM output, and update the switch read cycle counter for measuring 5 ms intervals.

Arguments
None

Return Value
None
5.8 Flowcharts

5.8.1 Main Processing

Figure 5.2 is a flowchart of the main processing routine.

![Flowchart](image-url)

**Figure 5.2 Main Processing**
5.8.2 Port Initialization

Figure 5.3 is a flowchart of the port initialization routine.

![Port Initialization Flowchart]

**Figure 5.3 Port Initialization**
5.8.3 Peripheral Function Initialization

Figure 5.4 is a flowchart of the peripheral function initialization routine.

```
<table>
<thead>
<tr>
<th>peripheral_init</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable writing to related registers</td>
</tr>
<tr>
<td>Cancel module stop state</td>
</tr>
<tr>
<td>Disable writing to related registers</td>
</tr>
<tr>
<td>MTU initialization mtu_init()</td>
</tr>
<tr>
<td>return</td>
</tr>
</tbody>
</table>
```

**Peripheral Function Initialization**

- PRCR register $\leftarrow$ A502h
- PRC1 bit = 1

- MSTPCRA register
- MTPA9 bit $\leftarrow$ 0

- PRCR register $\leftarrow$ A500h
- PRC1 bit = 0

: Cancels module stop state of MTU (MTU0 to MTU5).

Figure 5.4 Peripheral Function Initialization
5.8.4 MTU Initialization

Figures 5.5 and 5.6 are a flowchart of the MTU initialization routine.

Figure 5.5 MTU Initialization (1/2)
Application Example of Exclusive Operation of Two Motors
RX63N Group, RX631 Group
by One Set of Complementary PWM Outputs

Figure 5.6 MTU Initialization (2/2)
5.8.5 PWM Output Pin Switching

Figure 5.7 is a flowchart of the PWM output pin switching routine.

```
pwm_pin_change

PWM output pins are group 0?  
<table>
<thead>
<tr>
<th>Yes</th>
<th>No</th>
</tr>
</thead>
</table>
| PWM output pin group 1 settings  
pwm_pin_group_1() | PWM output pin group 0 settings  
pwm_pin_group_0() |
| Set PWM output pins to group 1 | Set PWM output pins to group 0 |

return
```

Figure 5.7 PWM Output Pin Switching
5.8.6 PWM Output Pin Group 0 Settings

Figure 5.8 is a flowchart of the PWM output pin group 0 settings routine.

```
Make group 1 port mode settings
PORTB.PMR register
B6 bit ← 0 : PB6/MTIOC3D: Use as general I/O port.
B7 bit ← 0 : PB7/MTIOC3B: Use as general I/O port.
PORTC.PMR register
B1 bit ← 0 : PE1/MTIOC4C: Use as general I/O port.
B2 bit ← 0 : PE2/MTIOC4A: Use as general I/O port.
B3 bit ← 0 : PE3/MTIOC4B: Use as general I/O port.
B4 bit ← 0 : PE4/MTIOC4D: Use as general I/O port.
Enable writing to PFS bit
PWPR register
B0WI bit ← 0
Enable writing to PFS register
PWPR register
PFSWE bit ← 1
Make group 1 pin function settings
PB6PFS register ← 00h
PSEL[4:0] bits = 00000b : Selects PB6 pin function: Hi-Z
PB7PFS register ← 00h
PSEL[4:0] bits = 00000b : Selects PB7 pin function: Hi-Z
PE1PFS register ← 00h
PSEL[4:0] bits = 00000b : Selects PE1 pin function: Hi-Z
PE2PFS register ← 00h
PSEL[4:0] bits = 00000b : Selects PE2 pin function: Hi-Z
PE3PFS register ← 00h
PSEL[4:0] bits = 00000b : Selects PE3 pin function: Hi-Z
PE4PFS register ← 00h
PSEL[4:0] bits = 00000b : Selects PE4 pin function: Hi-Z
Make group 0 pin function settings
PB1PFS register ← 02h
PSEL[4:0] bits = 00010b : Selects PB1 pin function: MTIOC4C
PB3PFS register ← 02h
PSEL[4:0] bits = 00010b : Selects PB3 pin function: MTIOC4A
PC2PFS register ← 01h
PSEL[4:0] bits = 00001b : Selects PC2 pin function: MTIOC4B
PC3PFS register ← 01h
PSEL[4:0] bits = 00001b : Selects PC3 pin function: MTIOC4D
PC4PFS register ← 01h
PSEL[4:0] bits = 00001b : Selects PC4 pin function: MTIOC3D
PC5PFS register ← 01h
PSEL[4:0] bits = 00001b : Selects PC5 pin function: MTIOC3B
Disable writing to PFS register
PWPR register
PFSWE bit ← 0
Disable writing to PFSWE bit
PWPR register
B0WI bit ← 1
Make group 0 port mode settings
PORTB.PMR register
B1 bit ← 1 : PB1/MTIOC4C: Used as peripheral function.
B3 bit ← 1 : PB3/MTIOC4A: Used as peripheral function.
PORTC.PMR register
B2 bit ← 1 : PC2/MTIOC4B: Used as peripheral function.
B3 bit ← 1 : PC3/MTIOC4D: Used as peripheral function.
B4 bit ← 1 : PC4/MTIOC3D: Used as peripheral function.
B5 bit ← 1 : PC5/MTIOC3B: Used as peripheral function.
return
```

Figure 5.8 PWM Output Pin Group 0 Settings
5.8.7 PWM Output Pin Group 1 Settings

Figure 5.9 is a flowchart of the PWM output pin group 1 settings routine.

```
pwm_pin_group_1

Make group 0 port mode settings
  PORTB.PMR register
  B1 bit ← 0
  B3 bit ← 0
  PORTC.PMR register
  B2 bit ← 0
  B3 bit ← 0
  B4 bit ← 0
  B5 bit ← 0
  PWPR register
  B0WI bit ← 0

Enable writing to PFS register
Make group 0 pin function settings
  PB1PFS register ← 00h
  PSEL[4:0] bits = 00000b
  PB3PFS register ← 00h
  PSEL[4:0] bits = 00000b
  PC2PFS register ← 00h
  PSEL[4:0] bits = 00000b
  PC3PFS register ← 00h
  PSEL[4:0] bits = 00000b
  PC4PFS register ← 00h
  PSEL[4:0] bits = 00000b
  PC5PFS register ← 00h
  PSEL[4:0] bits = 00000b

Make group 1 pin function settings
  PB6PFS register ← 01h
  PSEL[4:0] bits = 00001b
  PB7PFS register ← 01h
  PSEL[4:0] bits = 00001b
  PE1PFS register ← 01h
  PSEL[4:0] bits = 00001b
  PE2PFS register ← 01h
  PSEL[4:0] bits = 00001b
  PE3PFS register ← 01h
  PSEL[4:0] bits = 00001b
  PE4PFS register ← 01h
  PSEL[4:0] bits = 00001b

Disable writing to PFS register
PWPR register
PFSWE bit ← 0

Disable writing to PFSWE bit
PWPR register
B0WI bit ← 1

Make group 1 port mode settings
  PORTB.PMR register
  B6 bit ← 1
  B7 bit ← 1
  PORTE.PMR register
  B1 bit ← 1
  B2 bit ← 1
  B3 bit ← 1
  B4 bit ← 1

return
```

Figure 5.9 PWM Output Pin Group 1 Settings
5.8.8 Switch Input Determination

Figure 5.10 is a flowchart of the switch input determination routine.

```
sw_input_check

Read current port level

Current and previous port levels match?

Yes

Less than 3 consecutive matches?

Yes (level not determined)

Switch match counter + 1

No

Matched 3 times consecutively?

Yes

Matched level is low?

Yes

Switch determination level is high?

Yes

Set switch determination level to low

Set switch input determination flag

return

No

No

Set switch determination level to high

Clear switch match counter

Set previous level to current level

: 0: Low input
: 1: High input

Reads B2 bit in PORT3.PIDR register.

Figure 5.10 Switch Input Determination
```
5.8.9 MTU3.TGIA3 Interrupt Handler

Figure 5.11 is a flowchart of the MTU3.TGIA3 interrupt handler.

```
Excep_MTU3_TGIA3

Switch read cycle counter for measuring 5 ms intervals + 1

Duty setting value is 0?
  No
  Yes (duty 100%)

Set duty setting value state to "add"

Duty setting value is upper limit value?
  No
  Yes (duty 0%)

Set duty setting value state to "subtract"

Duty setting value state "add"?
  No
  Yes

Duty setting value + 1

Change PWM output duty MTU3.TGRD register ← pwm_1_duty
  MTU4.TGRC register ← pwm_2_duty
  MTU4.TGRD register ← pwm_3_duty

return
```

Figure 5.11 MTU3.TGIA3 Interrupt Handler
6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

User’s Manual: Hardware
RX63N Group, RX631 Group User’s Manual: Hardware Rev.1.80 (R01UH0041EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

User’s Manual: Development Tools
RX Family C/C++ Compiler Package V.1.01 User’s Manual Rev.1.00 (R20UT0570EJ)
The latest version can be downloaded from the Renesas Electronics website.

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http://www.renesas.com

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<th>Page</th>
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<td>Apr. 05, 2013</td>
<td>—</td>
<td>First edition issued</td>
<td></td>
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<td>1.01</td>
<td>Nov. 06, 2015</td>
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<td>18</td>
<td>Figure 5.6 is corrected.</td>
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<td>Program</td>
<td>A setting method of a TSTR register was corrected.</td>
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   When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal.
   Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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