RX62T

MTU3 Reset-Synchronized PWM Mode

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Introduction

The RX62T Group has on-chip Multi-Function Timer Pulse Unit 3 (MTU3), which comprises eight 16-bit timer channels.

Target Device

RX62T

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1. Specification

- Comprises eight 16-bit channels
- Operating frequency is 8 to100 MHz
- [Channels 0 to 4, 6, and 7]
- Waveform output on compare match
- Input capture function
- Counter-clearing operation
- Simultaneous writing to multiple timer counters (TCNT)
- Simultaneous clearing on compare match or input capture
- Simultaneous input and output to registers in synchronization with counter operations
- Up to 12-phase PWM output in combination with synchronous operation
- [Channels 0, 3, 4, 6, and 7]
- Buffer operation specifiable
- [Channels 3, 4, 6, and 7]
- Through interlocked operation of channels 3 and 4 or 6 and 7, output of positive and negative signals in six phases (for a total of 12 phases) in Complementary-PWM and Reset-PWM operation
- In complementary PWM mode, transfer of values from buffer registers to temporary registers on peaks and troughs of the timer-counter values or writing to the buffer registers (MTU3_4.TGRD and MTU3_7.TGRD)
- Double-buffering selectable in complementary PWM mode
- [Channels 3 and 4]
- Through interlocking with channel 0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and Reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)
- [Channels 1 and 2]
- Independently specifiable phase-counting mode
- Capable of cascade-connected operation
- [Channel 5]
- Capable of operation as a dead-time compensation counter

Fig. 1-1 is the block diagram of Multi-Function Timer Pulse Unit 3 (MTU3).

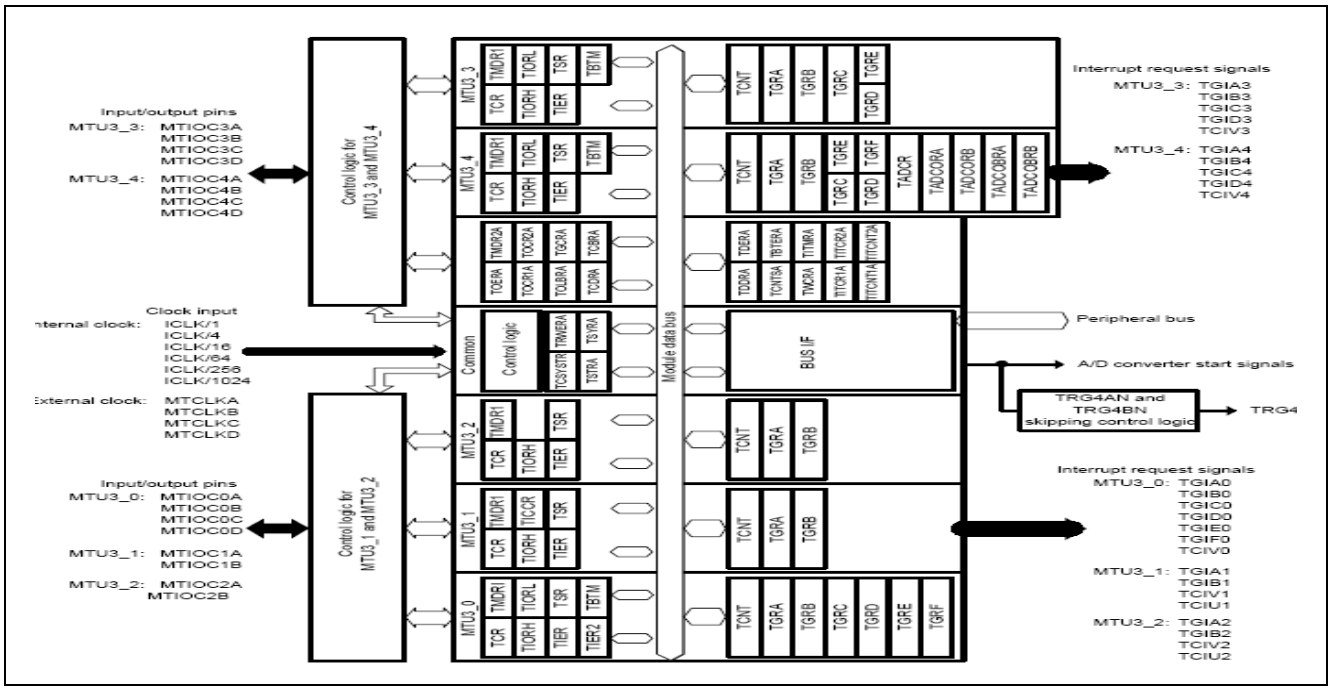


Figure 1-1 Block diagram for MTU3

Table 1-1 Specifications of Multi-Function Timer Pulse Unit 3 (MTU3) Register

TSTR	Timer start register
TOERA	Timer output master enable register A
TGCRA	Timer gate control register A
TOCR1A	Timer output control register 1A
TOCR2A	Timer output control register 2A
TCDRA	Timer cycle data register A
TDDRA	Timer dead time data register A
TCNTSA	Timer subcounter A
TCBRA	Timer cycle buffer register A
TITCR1A	Timer interrupt skipping set register 1A
TITCR2A	Timer interrupt skipping set register 2A
TITCNT1A	Timer interrupt skipping counter 1A
TITCNT2A	Timer interrupt skipping counter 2A
TBTERA	Timer buffer transfer set register A
TOLBRA	Timer output level buffer register A
TCR	Timer control register
TMDR1	Timer mode register 1
TMDR2A	Timer mode register 2A
TIORH	Timer I/O control register H
TIORL	Timer I/O control register L
TIER	Timer interrupt enable register
TCNT	Timer counter
TGRA	Timer general register A
TGRB	Timer general register B
TGRC	Timer general register C
TGRD	Timer general register D
TGRE	Timer general register E
TGRF	Timer general register F
TSR	Timer status register
TDERA	Timer dead time enable register A
TBTM	Timer buffer operation transfer mode register
TADCR	Timer A/D converter start request control register
TADCORA	Timer A/D converter start request cycle set register A
TADCORB	Timer A/D converter start request cycle set register B
TADCOBRA	Timer A/D converter start request cycle set buffer register A
TADCOBRB	Timer A/D converter start request cycle set buffer register B

2. Multi-Function Timer Pulse Unit 3 for Reset-Synchronized PWM Mode

2.1 Example of Reset-Synchronized PWM mode operation

In the Reset-synchronized PWM mode, three phases of positive and negative PWM waveforms (six phases in total) that share a common wave transition point can be output by combining channels 3 and 4 and channels 6 and 7.

When set for Reset-synchronized PWM mode, the MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, and MTIOC7D pins function as PWM output pins and timer counters 3 and 6 (MTU3_3.TCNT and MTU3_6.TCNT) functions as an up-counter.

Fig. 2-1 shows an example of Reset-Synchronized PWM mode operation.

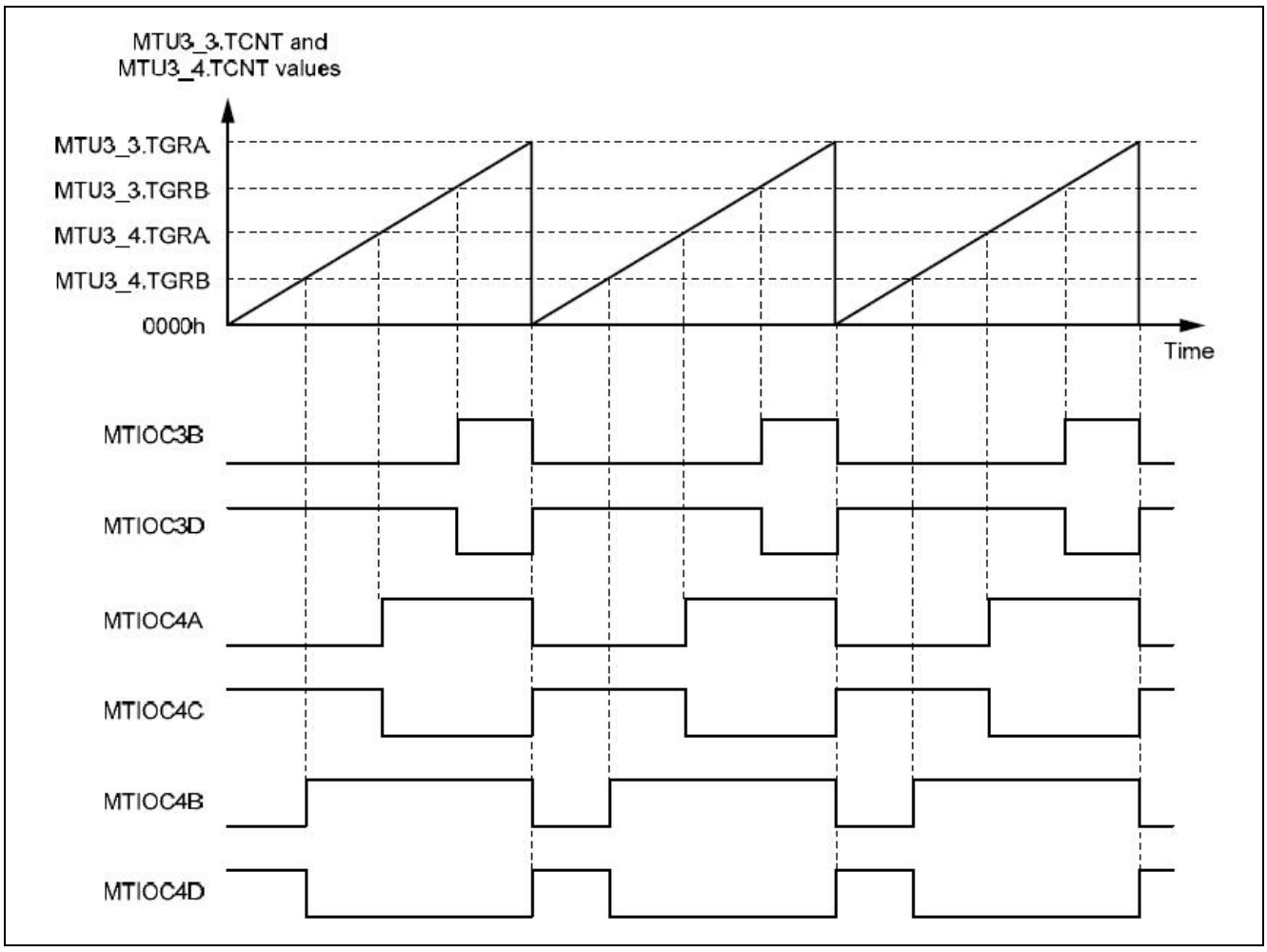


Figure 2-1 Example of Reset-Synchronized PWM mode operation

2.2 Example of Procedure for Setting Reset-Synchronized PWM Mode

Fig. 2-2 shows an example of the procedure for setting Reset-Synchronized PWM mode.

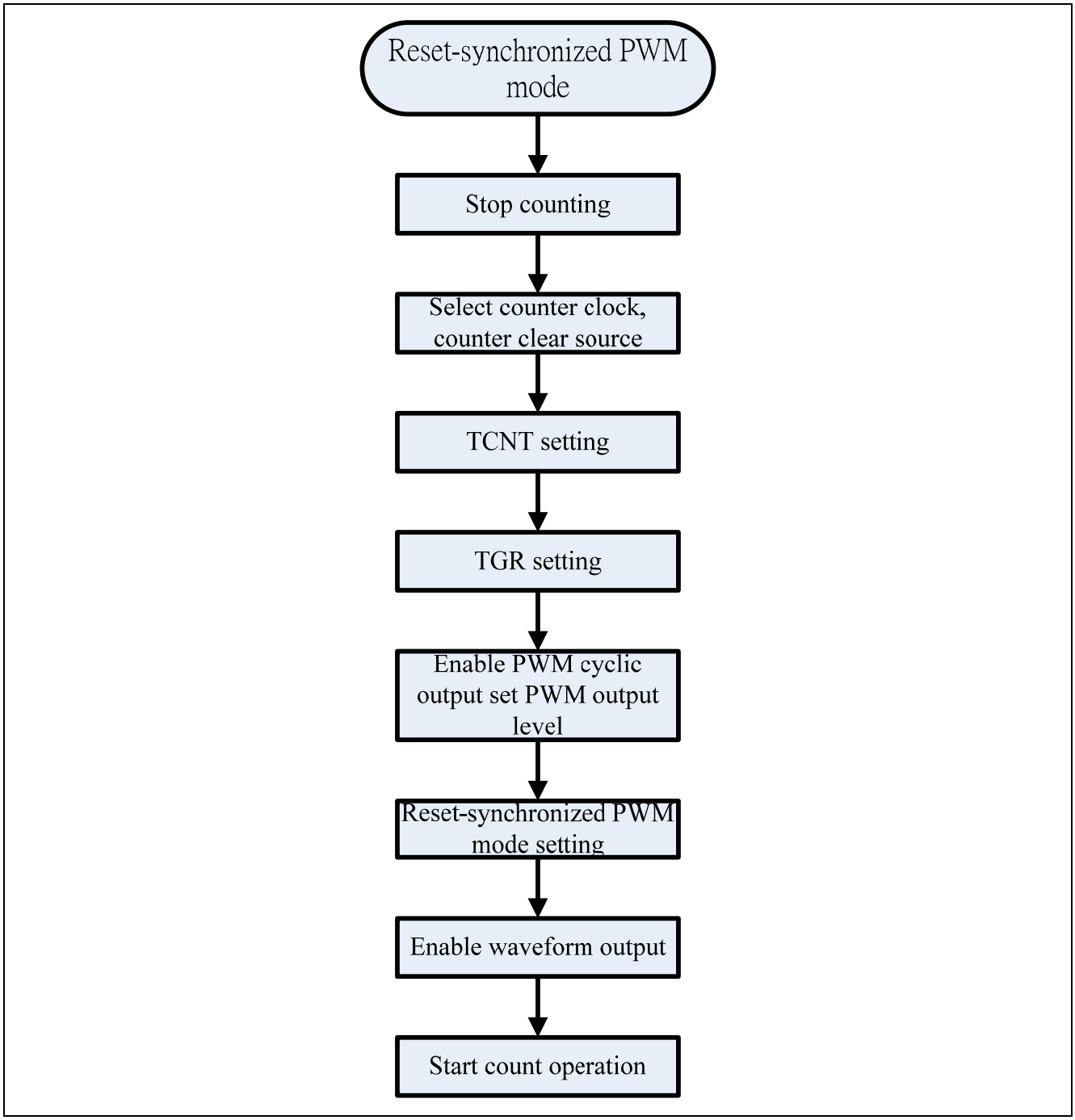
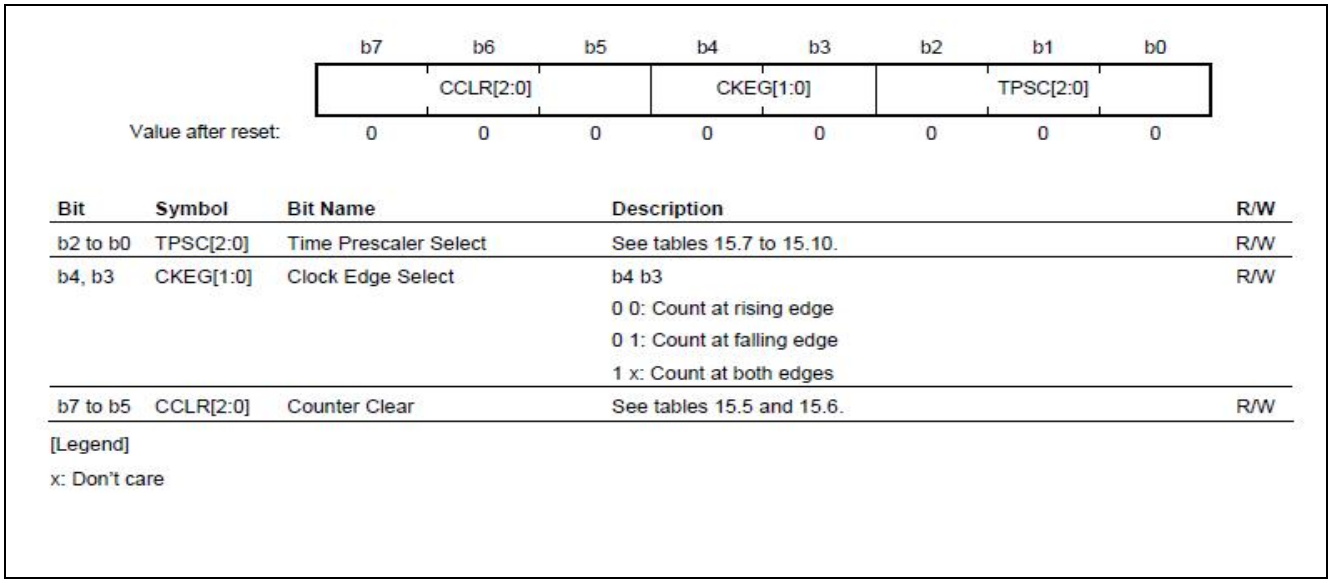


Figure 2-2 Example of Procedure for Setting Reset-Synchronized PWM Mode

3. Multi-Function Timer Pulse Unit (MTU3) 3 Software Register Setting

Timer Control Register (TCR):

TCR controls the TCNT operation for each channel. The MTU3 has a total of ten TCR registers, one each for channels 0 to 4, 6, and 7. TCR values should be specified only while TCNT operation is stopped.



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC[2:0]	Time Prescaler Select	See tables 15.7 to 15.10.	R/W
b4, b3	CKEG[1:0]	Clock Edge Select	b4 b3 0 0: Count at rising edge 0 1: Count at falling edge 1 x: Count at both edges	R/W
b7 to b5	CCLR[2:0]	Counter Clear	See tables 15.5 and 15.6.	R/W

[Legend]
x: Don't care

Figure 3-1 TCR Setting

Timer General Register (TGR):

TGR is a 16-bit readable/writable register.

TGRA, TGRB, TGRC, and TGRD function as either output compare or input capture registers. TGRC and TGRD for channels 0, 3, 4, 6, and 7 can also be designated for operation as buffer registers. TGR buffer register combinations are TGRA and TGRC, and TGRB and TGRD.

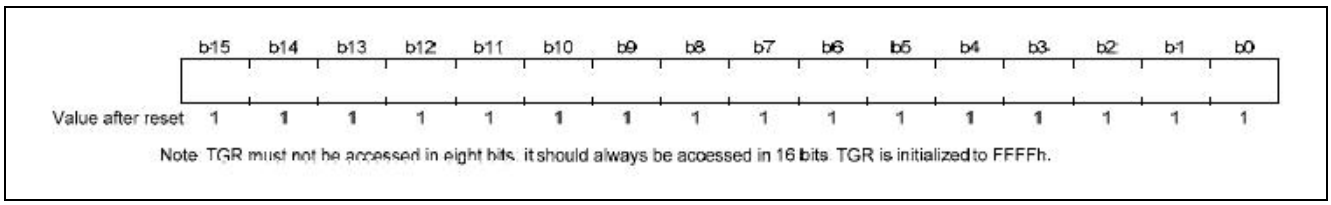
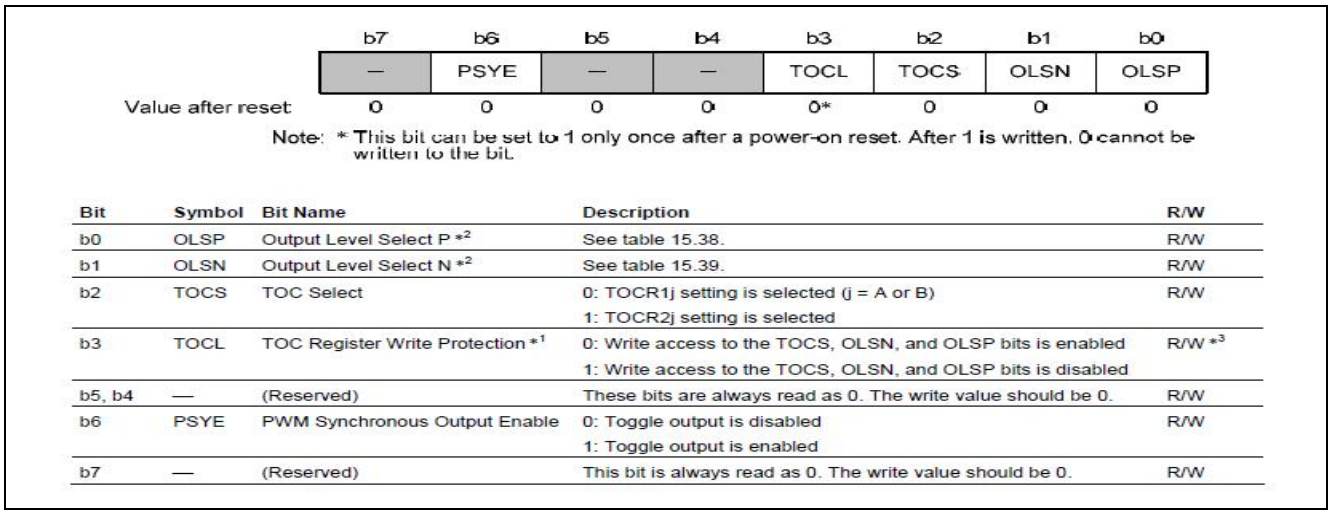


Figure 3-2 TGR Setting

Timer Output Control Registers (TOCRA):

TOCR1A and TOCR1B enable or disable PWM-synchronized toggle output in complementary PWM mode and Reset-synchronized PWM mode, and control inversion of PWM output level.



	b7	b6	b5	b4	b3	b2	b1	b0
	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
Value after reset:	0	0	0	0	0*	0	0	0

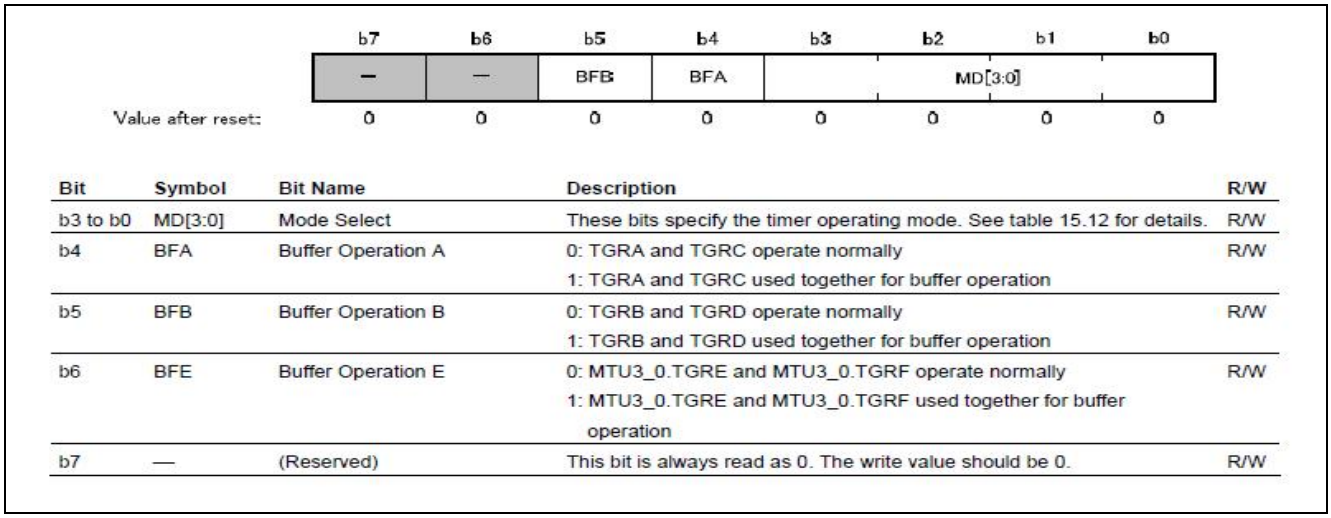
Note: * This bit can be set to 1 only once after a power-on reset. After 1 is written, 0 cannot be written to the bit.

Bit	Symbol	Bit Name	Description	R/W
b0	OLSP	Output Level Select P *2	See table 15.38.	R/W
b1	OLSN	Output Level Select N *2	See table 15.39.	R/W
b2	TOCS	TOC Select	0: TOCR1j setting is selected (j = A or B) 1: TOCR2j setting is selected	R/W
b3	TOCL	TOC Register Write Protection *1	0: Write access to the TOCS, OLSN, and OLSP bits is enabled 1: Write access to the TOCS, OLSN, and OLSP bits is disabled	R/W *3
b5, b4	—	(Reserved)	These bits are always read as 0. The write value should be 0.	R/W
b6	PSYE	PWM Synchronous Output Enable	0: Toggle output is disabled 1: Toggle output is enabled	R/W
b7	—	(Reserved)	This bit is always read as 0. The write value should be 0.	R/W

Figure 3-3 TOCRA Setting

Timer Mode Register (TMDR):

TMDR1 specifies the operating mode of each channel. The MTU3 has a total of seven TMDR1 registers, one each for channels 0 to 4, 6, and 7. TMDR1 values should be specified only while TCNT operation is stopped.



	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	BFB	BFA	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	MD[3:0]	Mode Select	These bits specify the timer operating mode. See table 15.12 for details.	R/W
b4	BFA	Buffer Operation A	0: TGRA and TGRC operate normally 1: TGRA and TGRC used together for buffer operation	R/W
b5	BFB	Buffer Operation B	0: TGRB and TGRD operate normally 1: TGRB and TGRD used together for buffer operation	R/W
b6	BFE	Buffer Operation E	0: MTU3_0.TGRE and MTU3_0.TGRF operate normally 1: MTU3_0.TGRE and MTU3_0.TGRF used together for buffer operation	R/W
b7	—	(Reserved)	This bit is always read as 0. The write value should be 0.	R/W

Figure 3-4 TMDR Setting

Timer Output Master Enable Register (TOER):

TOERA enables or disables output settings for output pins MTIOC4D, MTIOC4C, MTIOC3D, MTIOC4B, MTIOC4A, and MTIOC3B.

TOERB enables or disables output settings for output pins MTIOC7D, MTIOC7C, MTIOC6D, MTIOC7B, MTIOC7A, and MTIOC6B.

These pins do not output correctly if the TOER bits have not been set. In channels 3, 4, 6, and 7, set TOER prior to setting TIOR.

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OE3B	Master Enable MTIOC3B	0: MTU3 output is disabled * 1: MTU3 output is enabled	R/W
b1	OE4A	Master Enable MTIOC4A	0: MTU3 output is disabled * 1: MTU3 output is enabled	R/W
b2	OE4B	Master Enable MTIOC4B	0: MTU3 output is disabled * 1: MTU3 output is enabled	R/W
b3	OE3D	Master Enable MTIOC3D	0: MTU3 output is disabled * 1: MTU3 output is enabled	R/W
b4	OE4C	Master Enable MTIOC4C	0: MTU3 output is disabled * 1: MTU3 output is enabled	R/W
b5	OE4D	Master Enable MTIOC4D	0: MTU3 output is disabled * 1: MTU3 output is enabled	R/W
b7, b6	—	(Reserved)	These bits are always read as 1. The write value should be 1.	R/W

Figure 3-5 TOER Setting

4. Experiment Result

Fig. 4-1 to Fig. 4-3 the f_{sw} is 20 kHz. Fig. 4-1 is MTU3 for 25% duty; Fig. 4-2 is MTU3 for 50% duty; and Fig. 4-3 is MTU3 for 75% duty.

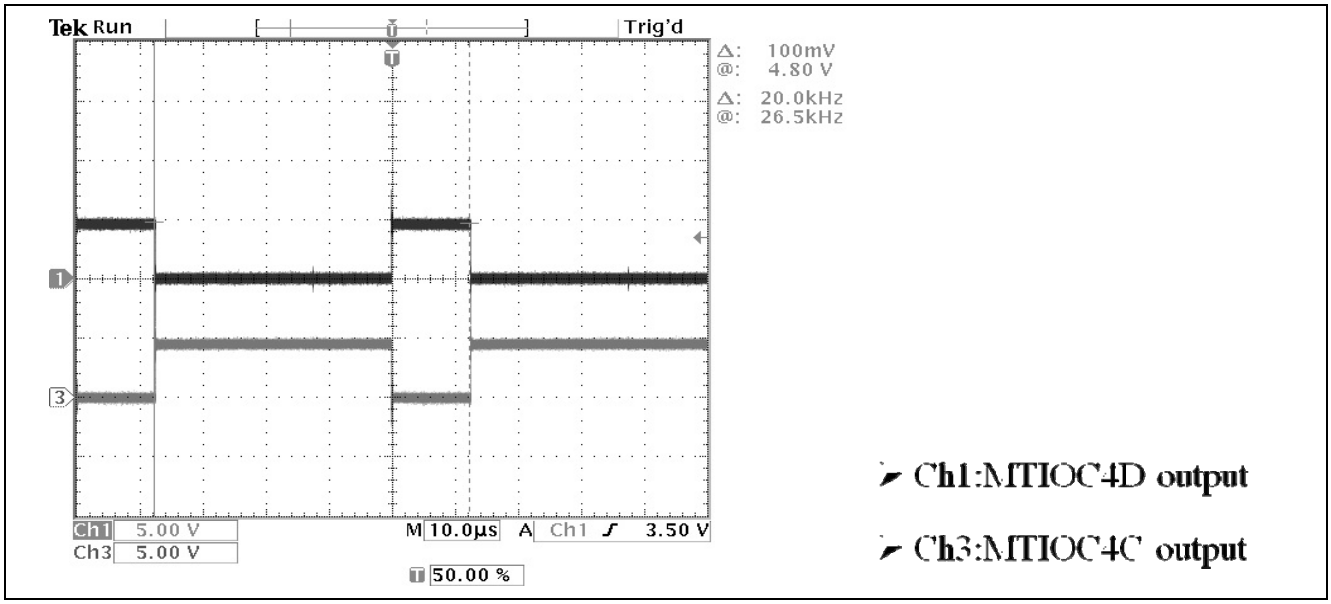


Figure 4-1 MTU3 output for 25% duty

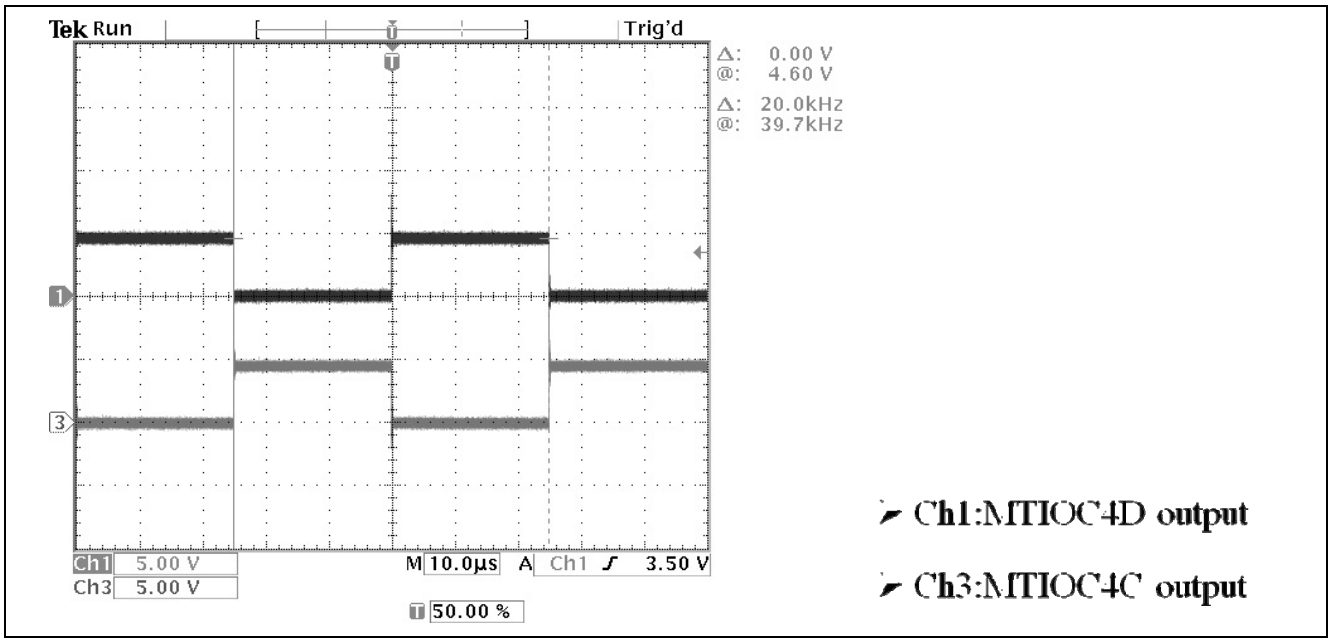


Figure 4-2 MTU3 output for 50% duty

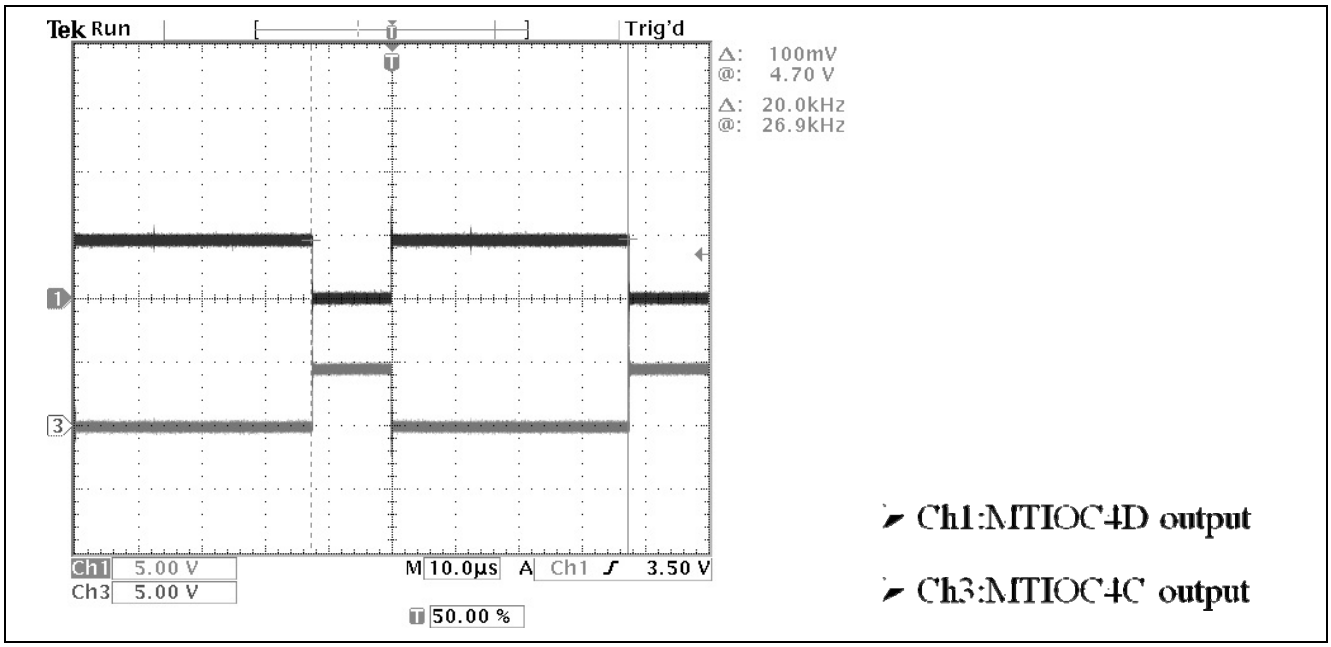


Figure 4-3 MTU3 output for 75% duty

5. Conclusion

From experimental result, we can use Multi-Function Timer Pulse Unit 3 for Reset-Synchronized PWM control.

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Revision Record

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		Page	Summary
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   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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