

# RX62T Group

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Usage Example of 12-Bit AD Converter in One Shunt Current Detection Method

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#### 1 Overview

#### 1.1 Configuration

This application note describes a setting example of AD detection timing synchronized with PWM output and examples of using built-in programmable gain amplifiers (hereinafter referred to as PGA) and built-in comparators on the basis of a motor control board using one shunt current detection method (Figure 1).

Settings for S/W registers in this application note are generated by using Renesas Electronics' free tool, 'Peripheral I/O driver generator tool: Peripheral Driver Generator V.2 (hereinafter called PDG2) Ver2.02'. For details of register setting values, refer to PDG2 User's Manual.

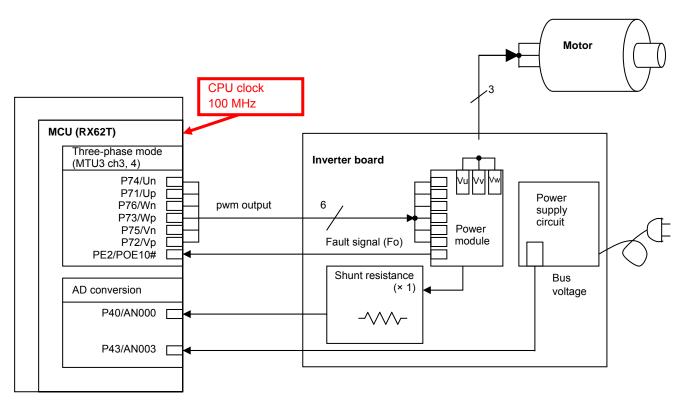


Figure 1. System Configuration Diagram



# 1.2 List of Used Functions

Table 1 shows a list of RX62T functions used in this application note.

Function	Name	Content
Three-phase output	MTU3 (ch3,4)	<ul> <li>Sine wave output using the complementally PWM mode by MTU3 (ch3, 4)</li> <li>Input two times at any given timing of three-phase PWM using AD delayed trigger generator function</li> </ul>
Current input for shunt	12-bit ADA (AN000)	<ul> <li>Support one shunt current detection method with AD 1 ch (double data registers)</li> </ul>
Shunt current amplification	PGA	· The shunt current is amplified twice by using a built-in PGA.
Bus voltage input	12-bit ADA (AN003)	· AD input by trigger from MTU3 synchronization
Fault signal input	POE (POE10)	<ul> <li>Shutdown of three-phase outputs upon detecting the "falling" edge of overcurrent signal when a fault occurs from IPM. (High impedance)</li> </ul>
Overcurrent detection	Comparator in 12-bit ADA	<ul> <li>Shutdown of three-phase outputs upon detecting positive and negative overcurrents by using the window comparator function.</li> </ul>

#### Table 1. List of Functions Used by S/W



## 2 Contents of Control

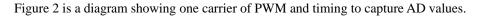
## 2.1 Port Assignment

#### Table 2. Port Assignment

		RX62T		RX62T-RSK	
Purpose of Use	I/O	Use function	Pin No	JA	J
Vcc	HW	Vcc	14,42,60	JA1-1,JA6-23	J1-1,J2-17,J3-10
Vss	HW	Vss	3,12,44,62	JA1-2,4,JA2-4,JA6-24	J1-3,12,J2-19,J3-12
VCL	HW	VCL	5	-	-
AVcc	HW	AVCC0	92	JA1-5	J4-17
AVss	HW	AVSS0	95	JA1-6	J4-20
PLLVss	HW	PLLVss	31	-	-
EXTAL	HW	EXTAL	13	-	J1-13
XTAL	HW	XTAL	11	-	J1-11
MD1	HW	MD1	6	-	J1-6
RESET	HW	RES#	10	JA2-1	J1-10
ASEMD0	HW	MD0	7	-	J1-7
Fault signal input	IN	POE10#-A	15	JA2-3	J1-15
Motor UP-phase output	OUT	MTIOC3B	56	JA2-13	J3-6
Motor UN-phase output	OUT	MTIOC3D	53	JA2-14	J3-3
Motor VP-phase output	OUT	MTIOC4A	55	JA2-15	J3-5
Motor WP-phase output	OUT	MTIOC4B	54	JA2-17	J3-4
Motor VN-phase output	OUT	MTIOC4C	52	JA2-16	J3-2
Motor WN-phase output	OUT	MTIOC4D	51	JA2-18	J3-1
AD input for bus voltage	IN	AN003	88	JA1-12	J4-13
AD input for 1-shunt current	IN	AN000	91	JA1-9	J4-16



# 2.2 Timing Diagram



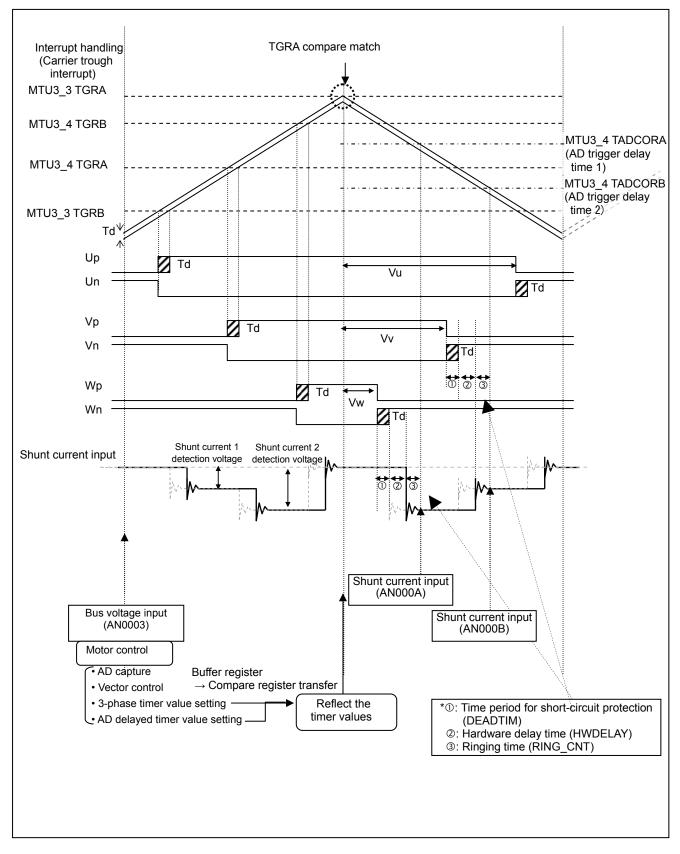


Figure 2. AD Conversion Timing Diagram



#### RX62T Group Usage Example of 12-Bit AD Converter in One Shunt Current Detection Method

#### 2.3 12-bit AD Converter (S12ADA)

#### (1) AD Detection Items

Table 3 lists items detected by the AD conveters.

Table 3. AD Detection Items			
Item	A/D input port		
Shunt current 1	AN000A		
Shunt current 2	AN000B		
Bus voltage	AN003		

#### Table 4 shows settings for the 12-bit AD converters.

(2) AD Converter Settings

Item	Content	
Conversion mode	2-channel scan mode	
Conversion pin	Group 0: AN000A, AN000B	
	Group 1: AN001 to AN003	
Trigger select	Group 0: MTU3 TRG4AN or TRG4BN	
	Group 1: MTU3 TRGA4N (carrier trough)	
Bit select	12 bits (right aligned)	
Sampling method	Sample-and-hold function + dedicated sample-and-hold for e	
	channel	
Frequency select	PCLK = 50MHz, ADCLK = 50MHz	
A/D conversion time	1.82µs (4 cycles ÷ PCLK + 88 cycles ÷ ADCLK)	
A/D conversion interrupt	Unused	
PGA	Amplification rate: 2 times (AN000A, AN000B)	
Comparator function select	Window comparator (High: 6/8AVCC, Low: 1/8AVCC)	
Noise cancellation filter	Comparator detection results are sampled 16 times with PCLK/8	
Comparator interrupt	Used as a POE interrupt request	

#### Table 4. AD Conversion Mode Setting

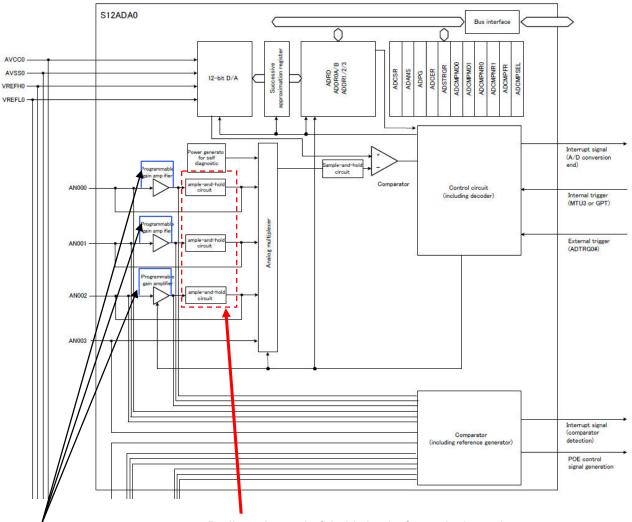
#### (3) How to Calculate the AD Conversion Time

To use PGA, it is necessary to use a dedicated sample-and-hold circuit set for each channel of 12-bit AD converters (excluding AN003 and AN103).

The AD conversion time can be calculated by a below formula which is described in Section 27.3.3, p.1225 i n RX62T Group Hardwar Manual Rev1.10 .

• When a dedicated sample-and-hold circuit for the channel is used and self diagnosis function is not used:  $tSCAN = tD + tSPLSH + (tCONV \times n) + tED$ 





Dedicated sample & hold circuits for each channel

Bypass lines which can be selected by the programmable gain amplifier select bit

Figure 3. Excerpt from AD Converter Block Diagram



#### 2.4 Port Output Enable 3 (POE3)

#### (1) Item Detected by Port Output Enable 3

Table 5 shows an item detected by Port Output Enable 3.

#### Table 5. Item Detected by Port Output Enable 3

Item	Port	Content
Fault signal input	POE10	Detect a fault signal from IPM

#### (2) Settings for Port Output Enable 3

Table 6 shows settings for POE3.

#### Table 6. Settings for POE3

Item	Content			
Target	Three-phase output ports (6 pins)			
	Comparator detection (AN000)			
High-impedance	POE10 input level detection			
conditions	<ul> <li>When upper and lower arms in any phase of the three-phase</li> </ul>			
	PWM outputs have simultaneously reached an active level			
Interrupt	POE10: priority level 15			
Interrupt source	A request is accepted at the falling edge of POE10 pin.			

#### 2.5 Multi-Function Timer Unit 3 (MTU3)

(1) Settings for the multi-function timer unit 3

Table 7 shows settings for the multi-function timer unit 3.

#### Table 7. Setting Items in Multi-Function Timer Unit 3

Item	Content
Used channel	MTU3 ch3, 4
Operating mode	Complementary PWM mode
Frequency select	ICLK = 100MHz
Dead time	2µs
Buffer transfer timing	Buffer transfer at counter trough
Interrupt skipping	None
Interrupt	Interrupts at MTU3_4 underflow (priority level 10)



# 3 PDG2 Setting

Sample S/W registers for this application note are generated and set by using PDG2. This chapter illustrates settings to configure an operation environment in user system by using PDG2.

\*Note

The sample S/W is adjusted to operate on a PC in which PDG2 has not been installed. Therefore, settings according to displays shown below do not mean that a project built on the High-performance Embedded Workshop (HEW) has the same configuration as the sample S/W.

There is no difference in operations.

#### 3.1 System Setting

<ul> <li>System</li> <li>Clock Generation Circuit</li> <li>Pin</li> </ul>	Main clock (EXTAL input) frequency:	12.5	MHz 😯	
	Frequency setting	Clock source	Frequency	
	System clock (ICLK):	EXTAL * 8	100.000000	MHz
	Peripheral module clock (PCLK):	EXTAL * 4	50.000000	MHz
	On-chip oscillator clock (OCOCLK):	On-chip oscillator	0.125	MHz
	Oscillation stop detection	n stop detection function	•	

Figure 4. System Setting Display



### 3.2 MTU3ch3 Setting

When the complementary PWM mode is selected as operation mode for MTU3ch3, ch4 is automatically set in accordance with ch3 setting.

<ul> <li>Multi-Function Timer Pulse Unit 3 (MTU3)</li> <li>MTU3_0</li> <li>MTU3_1</li> <li>MTU3_2</li> <li>MTU3_3</li> <li>MTU3_4</li> <li>MTU3_5</li> <li>MTU3_6</li> <li>MTU3_7</li> </ul>	Complementary PWM modes (1 to 3) and reset-synchronized PWM mode: MTU3_3 (paired with MTU3_4) and MTU3_6 (paired with MTU3_7)     MTU3_1 and MTU3_2 can act as a 32-bit timer when MTU3_1 is used for counting overflows of MTU3_2.     MTU3_5 has dedicated U, V, and W counters for dead-time compensation.     MTU3_0   MTU3_1   MTU3_2   MTU3_3   MTU3_4   MTU3_5   MTU3_6   MTU3_7        Wise this channel      Timer synchronous operation     Include this channel in the synchronous operation     Operation mode     Mode selection: Complementary PWM mode     Description:     Three phases of non-overlapping positive and negative PWM waveforms (six phases in total) can be output. PWM waveforms without non-overlapping interval are also available.     MTU3_3_TENT MTU3_3_TENT MTU3_7_TENT function as up/down-counters.
	Count settings Counter clearing source: Disable counter clear
	Count source: ICLK (system clock)
	Count source frequency: 100.000000 MHz Timer operating period: 100.000000 usec Actual value: 100.000000usec Error: 0.000000%
	Cycle register value: 5000 Complementary PW/M mode settings
	Dead time (non-overlapping interval): Generated  Dead time: 2.000000 usec  Actual value: 2.000000usec Error: 0.000000%
	Value of dead time data register (TDDR): 200

Figure 5. MTU3 Setting Display 1



### RX62T Group

# Usage Example of 12-Bit AD Converter in One Shunt Current Detection Method

Multi-Function Timer Pulse Unit 3 (MTU3) MTU3_0	Brushless DC motor control settings	
- MTU3_1 - MTU3_2 - MTU3_2 - MTU3_3 - MTU3_4	Enable U, V and W phase output control by software or external input signal	2
	Method to control output.	l
	Positive-phase output control (Initial value).	1
<ul> <li>MTU3_5</li> <li>MTU3_6</li> </ul>	Negative phase output control (Initial value)	]
MTU3_7	Cutput settings	
	The pulse outputs of MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D are disabled in the initial st Call R_PG_Timer_ControlOutputPin_MTU_U0_C3_C4 before starting the count to enable the pulse output to be used.	ate.
	Buffer transfer timing of PWM output level setting: Transfers data at the trough of the count	I
	U phase: MTIOC38 pin (positive-phase) / MTIOC3D pin (negative-phase)	
	MTU3_3/Initial value of general register B (TGRB) 2600	
	Initial value of buffer register A (MTU3_3/TGRD): 2600	
	Initial value of buffer register B (MTU3_3/TGRE) 0	
	Initial output level of MTIOC3B pin (positive-phase):	
	Active level:H (Initial output:L, output at compare match on up-count:H, output at compare match on down-count:L)	٠
	Initial output level of MTIOC3D pin (negative-phase):	
	V phase: MTI0C4A pin (positive-phase) / MTI0C4C pin (negative-phase) MTU3_4/Initial value of general register A (TGRA): 2600 Initial value of buffer register A (MTU3_4/TGRC): 2600 Initial value of buffer register B (MTU3_4/TGRE) 0 Initial output level of MTI0C4A pin (positive-phase):	
	Active level H (Initial output L, output at compare match on up-count:H, output at compare match on down-count:L)	-
	Initial output level of MTIOC4C pin (negative-phase):	
	Active level H (Initial output L, output at compare match on up-count L, output at compare match on down-count H)	-
	W phase: MTIOC48 pin (positive-phase) / MTIOC4D pin (negative-phase)	
	MTU3_4/Initial value of general register B (TGRB): 2600	
	Initial value of buffer register A (MTU3_4/TGRD): 2600	
	Initial value of buffer register B (MTU3_4/TGRF) 0	
	Initial output level of MTIOC4B pin (positive-phase):	
	Active level H (Initial output L, output at compare match on up-count H, output at compare match on down-count L)	•
	Initial output level of MTIOC4D pin (negative-phase):	
	Initial output level of MTIOC4D pin (negative-phase): Active levet.H (Initial output.L, output at compare match on up-count.L, output at compare match on down-count.H)	•

Figure 6. MTU3 Setting Display 2



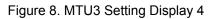
	-		
Multi-Function Timer Pulse Unit 3 (MTU3)     MTU3_0	Buffer register and synchronous clearin	g operation settings	
- MTU3_1	Buffer transfer timing of general register Transfer at the trough of the count (Co		-
- MTU3_2 - MTU3_3			
- MTU3_4	<ol> <li>Eneble synchronous counter cles</li> </ol>	ring on MTU3_3/TGRA compare match	
- MTU3_5 - MTU3_6	Waveform output immediately be	fore synchronous clearing is retained 🛛 😯	
	Enable double buffer function		
	Data transfer timing from buffer register	to temporary register. Do not link with interrupt skipping function	on 1 💌
	General register buffer operation		
	Use TGRC as a buffer register of	TGRA	
	Use TGRD as a buffer register of	TGRB	
	Interrupt skipping mode setting		
	Interrupt skipping mode: Disab	le interrupt skipping function	<u> </u>
	Interrupt settings		
		ch (the crest of the count) interrupt (TGIAn)	
	Interrupt request destination:	CPU Y	]
	Interrupt notification function name:	Mbu3htFunc_A	1
	Interrupt skipping count.	Skipping count of 1 (counted once every 2 times)	]
	Use MTU3_3/TGRB compare mat	ch interrupt (TGIBn)	
	Interrupt request destination	CPU	]
	Interrupt notification function name:	Mtu3In/Func_B	5
	CPU interrupt priority level (Shared with	MTU3_3/TGIAn and MTU3_3/TGIBn) 15	
	Use MTU3_4/TGRA compare mab	ch interrupt (TGIAn)	
	Interrupt request destination:	CPU	]
	Interrupt notification function name:	Mtu4IntFunc_A	1
	Use MTU3_4/TGRB compare mat	ch interrupt (TGIBn)	
	Interrupt request destination:	CPU Y	]
	Interrupt notification function name:	Mtu4IntFunc_B	-
	CPU interrupt priority level (Shared with	MTU3_4/TGIAn and MTU3_4/TGIBn): 15	
	Use MTU3_4/underflow (the troug	h of the count) interrupt (TCIVn)	
	Interrupt request destination:	CPU 👱	
	Interrupt notification function name:	[Mtu4IntFunc_V	
	Interrupt skipping count.	Skipping count of 1 (counted once every 2 times)	]
	CPU interrupt priority level:	12 *	

Figure 7. MTU3 Setting Display 3



### RX62T Group Usage Example of 12-Bit AD Converter in One Shunt Current Detection Method

Multi-Function Timer Pulse Unit 3 (MTU3)     MTU3_0     MTU3_1     MTU3_2     MTU3_3     MTU3_4     MTU3_5     MTU3_6	A/D conversion start triggers Enable A/D conversion start requ Enable A/D conversion start requ Enable A/D conversion start requ	est on TGRA compare match (trigge	signal of MTU3_4 TRGA			
- MTU3_7	Interrupt skipping count:	Skipping count of 1 (counted o	nce every 2 firses)	2		
	A/D conversion start request condition	n on matching of the counter and the Disable output	e cycle set register A valu	r.		
	Initial value of A/D conversion start		65535			
	Initial value of cycle set buffer regist		65535			
	Link with TGIA3 interrupt skipping	the second s				
	Link with TCIV4 interrupt skipping	a				
	A/D conversion start request condition	n on matching of the counter and the Disable output	e cycle set register B valu	<u>.</u>		
	Initial value of A/D conversion start	request cycle set register 8	65535			
	Initial value of cycle set butler regist	er 8	65535			
	Link with TGIA3 interrupt ekipping					
	Link with TCIV4 interrupt skippin	a .				
	Transfer, data from the cycle set b Transfer trans	offer register		<u>.</u>		
	MTU3_6, MTU3_7 timer synchronous of					
	Enable counter synchronous clearin	-				
	and the second se	Enable counter synchronous clearing at MTU3_0/TGRB input capture/compare match				
	Enable counter synchronous clearing at MTU3_0/TGRC input capture/compare match					
	Enable counter synchronous clearing at MTU3_0/TGRD input capture/compare match					
	Enable counter synchronous clearing at MTU3_1/TGRA input capture/compare match     Enable counter synchronous clearing at MTU3_1/TGRP input capture/compare match					
		Enable counter synchronous clearing at MTU3_1/TGRB input capture/compare match     Enable counter synchronous clearing at MTU3_2/TGRA input capture/compare match				
	Enable counter synchronous clearin					
	Enable counter synchronous clearin	g at MTU3_2/TGRB input capture/	compare match			





# 3.3 POE3 Setting

- Port Output Enable 3 (POE3)				
	MTU3_3,3_4 and GPT0,1,2 output pin control			_
	Target pins for high-impedance control			
	P71/MTIOC38/GTIOC0A.A. P74/MTIO			
	P72/MTIOC4A/GTIOC1A-A, P75/MTIC P73/MTIOC4B/GTIOC2A-A, P76/MTIC			
	Target pins for high-impedance condition A/D comparator detection	addition		
	POE4# input level detection			
	POE8# input level detection			
	POE10# input level detection			
	POE11# input level detection			
	Output enable interrupt 1 (OEI1 : Interrupt by	POE0F and OSF1)	<u></u>	
	Use output enable interrupt 1 (0EI1)	Interrupt notification function name:	PoeOei1IntFunc	
		Interrupt generation condition:	POEOF	
	High-impedance request conditions			
	POEOF (POEO# pin input)			
	OSF1 (Any one of the three pairs of two or GPT0 to GPT2 pins for the GPT large			
	Specify an active level for the short-o	ircuit detection of MTU3 and GPT 🛛 🍳		
	P71 MTI0C38/GTI0C0A-A: Active h	igh 💌		
	P74 MTIOC3D/GTIOC0B-A: Active h	igh 💌		
	P72 MTIOC4A/GTIOC1A-A: Active h	igh 💌		
	P73 MTIOC48/GTIOC2A-A: Active h	igh 💌		
	P75 MTIOC4C/GTIOC18-A: Active h	igh 💌		
	P76 MTIOC4D/GTIOC2B-A: Active P	6) <b>-</b>		
	MTU3_6.3_7 output pin control			
	Target pins for high-impedance control			
	P95/MTIOC68, P92/MTIOC60			
	F P94/MTIOC7A, P91/MTIOC7C			
	P93/MTIOC78, P90/MTIOC7D			
	Target pins for high-impedance condition	addition		
	A/D comparator detection			
I	POED# input level detection			
I	POE8# input level detection     POE10# input level detection			
I	POE11# nov/ level detection			
I	Output enable interrupt 2 (OEI2 : Interrupt by	POEAE and OSEAL		
	Use output enable interrupt 2 (DEI2)	Interrupt notification function nam	e PoeOei2IntFunc	
I	and a substantial and a factory			
I		Interrupt generation condition	POE4F	

Figure 9. POE3 Setting Display 1



- Port Output Enable 3 (POE3)					
	MTU3_6,3_7 output pin control				
	Target pins for high-impedance control				
	P95/MTIOC68, P92/MTIOC6D				
	P94/MTI0C7A, P91/MTI0C7C				
	P93/MTIOC7B, P90/MTIOC7D				
	Target pins for high-impedance condition	addition			
	A/D comparator detection				
	POE0# input level detection				
	POE8# input level detection				
	P0E10# input level detection				
	POE11# input level detection				
	Output enable interrupt 2 (OEI2 : Interrupt by P	OE4F and OSF4)			
	Use output enable interrupt 2 (OEI2)	Interrupt notification function name:	Poe0ei2IntFunc		
		Interrupt generation condition	POE4F 💌		
	High-impedance request conditions				
	POE4F (POE4# pin input				
	OSF2 (Any one of the three pairs of two-	phase MTU3_6 and MTU3_7 pins			
	for MTU complementary PWM output to I		an active level)		
	MTU3_0 output pin control				
	Target pins for high-impedance control				
	PB3/MTIOC0A-A, P31/MTIOC0A-B				
	PB2/MTIOCOB-A, P30/MTIOCOB-B				
	PB1/MTIOCOC				
	F PB0/MTIOCOD				
	Target pins for high-impedance condition	addition			
	A/D comparator detection				
	POE0# input level detection				
	P0E4# input level detection				
	PGE10# input level detection				
	PDE11# input level detection				
	Output enable interrupt 3 (OEI3 : Interrupt by POE8F)				
	Use output enable interrupt 3 (OEI3)	Interrupt notification function name:	PoeOei3IntFunc		
	High-impedance request conditions				
	POESF (POES# pin input)				
	GPT0,1 output pin control				
	Target pins for high-impedance control				
	PD7/GTIOC0A-8, PD6/GTIOC08-8				
	PD5/GTIOC1A-8, PD4/GTIOC18-8				
	Target pins for high-impedance condition	addition			
	A/D comparator detection				
	POE0# input level detection				

Figure 10. POE3 Setting Display 2



— 🔲 Port Output Enable 3 (POE3)	Target pins for high-impedance control	
	Target pins for high-impedance condition addition  AVD compositor detection  PDEDIB input level detection  PDEBIB input level detection  PDEBIB input level detection  PDEBIB input level detection	
	High-impedance request conditions	
	GPT2.3 output pin control	
	Target pins for high-impedance control P03/GTI0C2A-8, P02/GTI0C28-8 P01/GTI0C3A, P00/GTI0C38	
	Target pins for high-impedance condition addition  A/D comparator detection  POEDII input level detection	
	High-impedance request conditions	
	GPT3 to 0 interrupt Output enable interrupt 4 (DEI4 : Interrupt by POE10F, POE11F) Use output enable interrupt 4 (DEI4) Interrupt root/cation function name PoeDer#intFunc	
	Interrupt generation condition POETOF and POETIF	
	CPU interrupt priority level (Shared with OEI1,0EI2,0EI3 and 0EI4): 15 at	
	Request acceptance conditions	
	Request acceptance conditions is POEOF (POEO# prininput) Accepts a request on the falling edge of POEO# input	*
	Request acceptance conditions is PDE4F (PDE4# pin input) Accepts a request on the falling edge of PDE4# input	<u>*</u>
	Request acceptance conditions is POEBF (POEB# primox) Accepts a request on the falling edge of POEB# input	Ŧ
	Request acceptance conditions is POE10F (POE10# pin input) Accepts a request on the falling edge of POE10# input	-
	Request acceptance conditions is POE11F (POE11# pin input) Accepts a request on the falling edge of POE11# input	

Figure 11. POE3 Setting Display 3



# 3.4 12-Bit ADA Setting

12-Bit A/D Converter (S12ADA)     S12ADA0     S12ADA1	Unit: S12ADA0	
	C Operation settings	
	Mode: 2-channel scan mode	
	Conversion start trigger (Group 0):	
	Compare-match of A/D conversion start request cycle set register A or B in MTU3_4 (TRG4AN/TRG4BN)	<u>_</u>
	Conversion start trigger (Group 1):	
	Compare-match/Input-capture A signal from MTU3_4, or underflow signal in complementary PWM mode (TRGA4N)	<u> </u>
	Analog input channel:	
	Group 0: AN000 / Group 1: AN001 - AN003	*
	Data placement  Right-alignment	
	Data accuracy. 12-bit accuracy	
	Enables automatic clearing of data registers after being read     Use dedicated sample-and-hold circuit	
	Setting of programmable gain amplifier         AN000       Image: Enable programmable gain amplifier         AN001       Image: Enable programmable gain amplifier         AN002       Image: Enable programmable gain amplifier         Gain:       12.0         AN002       Image: Enable programmable gain amplifier         Gain:       12.0	
	Conversion time	
	Conversion clock (ADCLK) Internal clock (PCLK)	
	Conversion clock (ADCLK) frequency: 50.000000 MHz 😵	
	Input sampling time: 0.400000 usec Actual value:	
	Error:	
	Sampling state register value: 20	
	Interrupt settings	
	Use A/D conversion end interrupt (S12ADIn)	
	Interrupt request destination	
	CPU interrupt priority level.	
	Interrupt notification function name. \$12ad0IntFunc	

Figure 12. 12-Bit AD Setting Display



# 4 S/W Descriptions

This chapter describes settings of modules which are not supported by PDG2 and control flows.

### 4.1 Register Settings

Register	Initial	Content
	value	
MTU4.TIER.BIT.TTGE	1	Enable to generate an AD conversion start request
MTU4.TIER.BIT.TTGE2	1	Enable an AD conversion request at trough
MTU4.TADCOBRA	5200	Set a cycle for AD conversion start request (buffer)
MTU4.TADCOBRB	5200	Set a cycle for AD conversion start request (buffer)
MTU4.TADCORA	5200	Set a cycle for AD conversion start request
MTU4.TADCORB	5200	Set a cycle for AD conversion start request
MTU4.TADCR.WORD	0x4050	Buffer transfer at TCNT4 peak
		As for TRG4AN and TRG4BN, AD converter start requests are enabled when TCNT4
		decrements.
		Not link the transfer with interrupt skipping function
S12AD.ADCMPFR.BIT.C000FLAG	0	Clear the comparator detection flag for AN000
S12AD.ADCMPMD0.BIT.CEN000	3	Use AN000 as the window comparator (Low/High)
S12AD.ADCMPMD1.WORD	0x0661	REFL: AVCC0 × 1/8, REFH: AVCC0 × 6/8
		Use a signal before amplified by the PGA as a comparator input with reference to
		REFH/REFL
S12AD.ADCMPNR0.BIT.C000NR	10	Sample the comparator result 16 times at PCLK/2
S12AD.ADCMPSEL.WORD	0x0301	Use the detection in the comparator as an interrupt or POE request
POE.POECR4.BIT.CMADDMT34ZE	1	Add the S12ADA.ADCMPFR.CjFLAG (j = 0 to 2 and 4 to 6) flag to high-impedance
		conditions of MTU3_3 and MTU3_4
IR (S12AD,CMPI)	0	Clear the interrupt request flag (comparator IR)
IPR (S12AD,CMPI)	0x0c	Comparator interrupt priority level = 12
IEN (S12AD,CMPI)	1	Enable comparator interrupts
POE.ICSR4.BIT.POE10F	0	Clear the POE10 interrupt request flag
POE.OCSR1.BIT.OSF1	0	Clear the output short flag

## 4.2 Settings of Variables

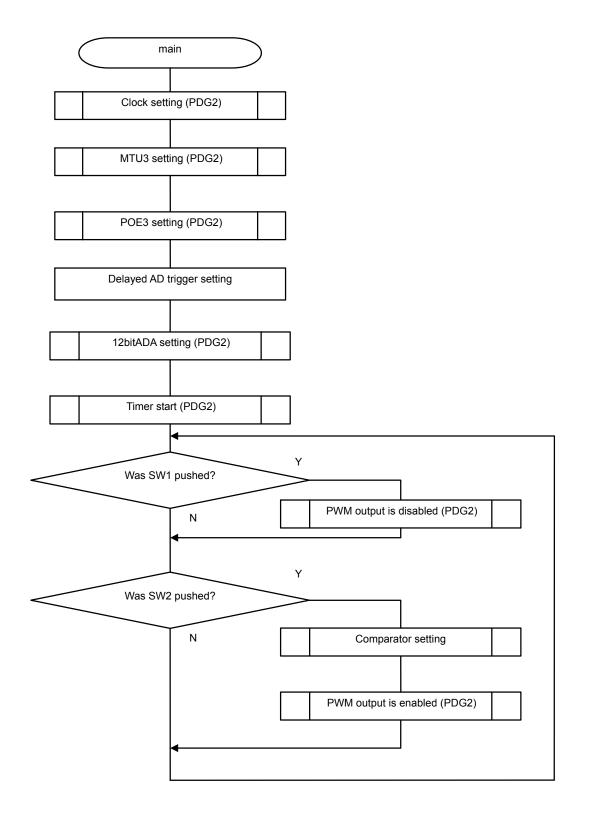
Defined name	(Type) Initial value	Content
du	(float) 0	Variable to store the U-phase output value
dv	(float) 5200 / 3	Variable to store the V-phase output value
dw	(float) 5200 / 3 × 2	Variable to store the W-phase output value
AD_data [5]	(short) 0	Variable to store the AD conversion result (For details, refer to the section about 12-
		bit A/D converter in PDG2 reference manual.)
t_c1	(int) 0	Counter to prevent chattering (for SW1)
t_c2	(int) 0	Counter to prevent chattering (for SW2)

# 4.3 Settings of Constants

Defined name	Value	Content	
CARR_CNT	10000	Carrier cycle	
DTT_CNT	200	Dead time	
CMP_TIMING_1	5	Constant to generate a timing for AD conversion start trigger	
CMP_TIMING_2	15	Constant to generate a timing for AD conversion start trigger	
PWM_CHANGE_VAL	0.1	Constant to control changes in PWM output	

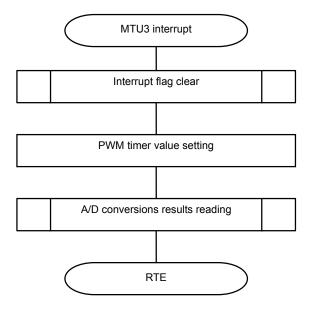


### 4.4 Main Function Flow

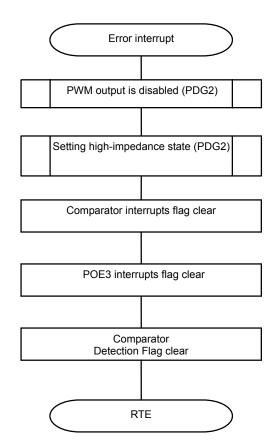




#### 4.5 MTU3 Interrupt Flow



### 4.6 Error Interrupt Flow





#### Website and Support

- Renesas Electronics Website http://www.renesas.com/
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# **Revision Record**

		Description	
Rev.	Date	Page	Summary
1.00	2012.02.17	—	First edition issued

# General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at
- which resetting has been specified.
- 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access
  these addresses; the correct operation of LSI is not guaranteed if they are accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal.
   Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

— The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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