RX62T Group, RX63T Group

Differences between RX62T Group and RX63T Group (144, 120, 112, and 100-Pin Versions)

R01AN1530EJ0101
Rev.1.01
Jan. 08, 2018

Abstract

This application note provides reference information on the differences between RX62T Group and RX63T Group microcontrollers.

Products

RX62T Group, RX63T Group

Contents

1. Switching from the RX62T Group to the RX63T Group

The RX62T Group and RX63T Group are not interchangeable devices. Therefore, care must be exercised when switching to the RX63T Group. For details, see section 2., Description of Differences, as well as RX62T Group—User's Manual: Hardware and RX63T Group—User's Manual: Hardware.

1.1 Newly Added Functions

(1) Software reset
(2) Cold start/warm start determination function
(3) Option-setting memory
(4) Low-speed clock oscillator (LOCO)
(5) Clock frequency accuracy checker (CAC)
(6) Register write protection function
(7) DMA controller (DMACA)
(8) Multi-function pin controller (MPC)
(9) USB 2.0 host/function module (USBa)
(10) D/A converter (DAa)
(11) Data operation circuit (DOC)

1.2 Eliminated Functions

(1) MD1 pin (mode 1 pin), MDE pin (endian selection pin)
(2) MD1 pin and MDE pin status flags (MD1 and MDE in MDMONR)
(3) Mode status register (MDSR)
(4) Standby timer select bits (STS4 to STS0 in SBYCR)
(5) Deep standby wait control register (DPSWCR)
(6) LIN module (LIN)

1.3 Modified Functions

1.3.1 Modification Type 1: Items Requiring Reconsideration Due to Specification Changes or Elimination of Functions

(1) MCU operation mode entry methods: MD pin eliminated and added.
(2) Endian determination method: Bits MDE2 to MDE0 in MDES
(3) Clock oscillator circuit: Low-speed clock oscillator (LOCO) startup, PLL frequency division, and oscillation stop detection added, etc.
(4) Voltage detection circuit: Key code register eliminated, voltage detection conditions added, etc.
(5) Low power consumption functions: Oscillation settling time modified, etc.
(6) Interrupt controller (ICUb): Group interrupts, etc.
(7) Buses: Peripheral bus update, bus priority added, etc.
(8) Data transfer controller (DTCa): Maximum transfer count changed, etc.
(9) I/O ports: Modifications to multi-function pin controller, etc.
(10) Multi-function timer pulse unit 3 (MTU3): Base clock changed from ICLK to PCLKA.
(11) Port output enable 3 (POE3): Register added.
(12) General PWM timer (GPT): Base clock changed from ICLK to PCLKA, register added.
(13) Watchdog timer (WDT): 8-bit → 14-bit, Operation mode eliminated, etc.
(14) Independent watchdog timer (IWDT): Window function added.
(15) I^2C bus interface (RIIC): ICR eliminated, usage notes.
(16) CAN module: CCLKS bit added in BCR, etc.
(17) Serial peripheral interface (RSPI): Number of channels increased from 1 to 2, register eliminated (SPDCR.SLSEL), etc.
(18) 12-bit A/D converter (S12ADB): Registers changed, etc.
(19) 10-bit A/D converter (ADA): Changed from 12 channels to 20 channels, registers changed, etc.
(20) ROM (flash memory for code storage): Block and write units modified, etc.
(21) E2 Data flash: Block and write units modified, etc.

1.3.2 Modification Type 2: Items Requiring Reconsideration of Error Handling Due to Changes to the Interrupt Controller

(1) Serial communications interfaces (SCIc and SCId): ERIx are group interrupts.

1.4 Compatible Functions

(1) Compare match timer (CMT)
(2) CRC calculator (CRC)

2. Description of Differences

2.1 Differences in Functions and Specifications

Tables 2.1 to 2.31 list the differences in functions and specifications.

Table 2.1 Differences in Functions and Specifications (1)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>Memory</td><td>ROM/RAM</td><td>• Memory configurations
<table><tr><td>ROM/RAM capacity</td><td>64 KB / 8 KB</td></tr><tr><td></td><td>128 KB / 8 KB</td></tr><tr><td></td><td>256 KB / 16 KB</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr></table></td><td>• Memory configurations
<table><tr><td>ROM/RAM capacity</td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>256 KB / 24 KB</td></tr><tr><td></td><td>384 KB / 32 KB</td></tr><tr><td></td><td>512 KB / 48 KB</td></tr></table></td></tr>
<tr><td>MCU operating modes</td><td>Operating modes</td><td>• Mode entry
<table><tr><th>MD1</th><th>MD0</th><th>Operating mode</th></tr><tr><td>0</td><td>1</td><td>SCI boot mode</td></tr><tr><td>1</td><td>1</td><td>Single-chip mode</td></tr></table>• Operating mode selection
<table><tr><th>SYSCR0 register
ROME</th><th>Operating mode</th></tr><tr><td>0</td><td rowspan="2">Single-chip mode</td></tr><tr><td>1</td></tr></table>• Endian selection
• MDE pins
MDE pin = 0: Little-endian
MDE pin = 1: Big-endian</td><td>• Mode entry
<table><tr><th>MD</th><th>P00</th><th>Operating mode</th></tr><tr><td>High</td><td>—</td><td>Single-chip mode</td></tr><tr><td rowspan="3">Low</td><td>Low</td><td>Boot mode</td></tr><tr><td rowspan="2">High</td><td>USB boot mode</td></tr><tr><td>User boot mode</td></tr></table>• Operating mode selection
<table><tr><th colspan="2">SYSCR0 register</th><th rowspan="2">Operating mode</th></tr><tr><th>ROME</th><th>EXBE</th></tr><tr><td>0</td><td>0</td><td rowspan="2">Single-chip mode, User boot mode</td></tr><tr><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>On-chip ROM disabled extended mode</td></tr><tr><td>1</td><td>1</td><td>On-chip ROM enabled extended mode</td></tr></table>• Endian selection
• MDEB.MDE[2:0] or MDES.MDE[2:0]
MDE[2:0] = 111b: Little-endian
MDE[2:0] = 000b: Big-endian</td></tr>
<tr><td></td><td>Registers/ bits</td><td>• Mode monitor register (MDMONR)
<table><tr><td>b0</td><td>MD0</td><td>MD0 pin status flag</td></tr><tr><td>b1</td><td>MD1</td><td>MD1 pin status flag</td></tr><tr><td>b7</td><td>MDE</td><td>MDE pin status flag</td></tr><tr><td>b15</td><td>—</td><td>(Reserved bit) Note: Value is 1 when read.</td></tr></table>• Mode status register (MDSR)
<table><tr><td>b0</td><td>IROM</td><td>On-chip ROM startup status flag</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit) Note: Value is 1 when read.</td></tr><tr><td>b4</td><td>BOTS</td><td>Boot mode startup flag</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr></table>• System control register0 (SYSCR0)
<table><tr><td>b0</td><td>ROME</td><td>On-chip ROM enable bit</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b8 b15</td><td>KEY[7:0]</td><td>SYSCR0 Key code</td></tr></table></td><td>• Mode monitor register (MDMONR)
<table><tr><td>b0</td><td>MD</td><td>MD pin status flag</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b15</td><td>—</td><td>(Reserved bit) Note: Value is 0 when read.</td></tr></table>• Mode status register (MDSR)
<table><tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit) Note: Value is 0 when read.</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>UBTS</td><td>User boot mode startup flag</td></tr></table>• System control register0 (SYSCR0)
<table><tr><td>b0</td><td>ROME</td><td>On-chip ROM enable bit</td></tr><tr><td>b1</td><td>EXBE</td><td>External bus enable bit</td></tr><tr><td>b8 b15</td><td>KEY[7:0]</td><td>SYSCR0 Key code</td></tr></table></td></tr>
<tr><td>Resets</td><td>Functions</td><td>• Specification overview
<table><tr><td>Reset types</td><td>Pin reset</td></tr><tr><td></td><td>Power-on reset</td></tr><tr><td></td><td>Voltage monitoring reset</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>Deep software standby reset</td></tr><tr><td></td><td>Independent watchdog timer reset</td></tr><tr><td></td><td>Watchdog timer reset</td></tr><tr><td></td><td>—</td></tr><tr><td>—</td><td>—</td></tr></table></td><td>• Specification overview
<table><tr><td>Reset types</td><td>Pin reset</td></tr><tr><td></td><td>Power-on reset</td></tr><tr><td></td><td>Voltage monitoring 0 reset</td></tr><tr><td></td><td>Voltage monitoring 1 reset</td></tr><tr><td></td><td>Voltage monitoring 2 reset</td></tr><tr><td></td><td>Deep software standby reset</td></tr><tr><td></td><td>Independent watchdog timer reset</td></tr><tr><td></td><td>Watchdog timer reset</td></tr><tr><td></td><td>Software reset</td></tr><tr><td>Extended function</td><td>Cold start/warm start determination function</td></tr></table></td></tr>
<tr><td></td><td>Registers/ bits</td><td>• Reset status register (RSTSR)
<table><tr><td>b0</td><td>PORF</td><td>Power-on reset flag</td></tr><tr><td>b1</td><td>LVD1F</td><td>LVD1 detect flag</td></tr><tr><td>b2</td><td>LVD2F</td><td>LVD2 detect flag</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>DPSRSTF</td><td>Deep software standby reset flag</td></tr></table></td><td>• Reset status register 0 (RSTSR0)
<table><tr><td>b0</td><td>PORF</td><td>Power-on reset detect flag</td></tr><tr><td>b1</td><td>LVD0RF</td><td>Voltage monitoring 0 reset detect flag</td></tr><tr><td>b2</td><td>LVD1RF</td><td>Voltage monitoring 1 reset detect flag</td></tr><tr><td>b3</td><td>LVD2RF</td><td>Voltage monitoring 2 reset detect flag</td></tr><tr><td>b7</td><td>DPSRSTF</td><td>Deep software standby reset flag</td></tr></table></td></tr>
</table>

Table 2.2 Differences in Functions and Specifications (2)

Item		RX62T Group	RX63T Group
Resets	Registers/ bits	—	• Reset status register 1 (RSTSR1) • Reset status register 2 (RSTSR2)
		• Reset control/status register (RSTCSR)	—
		—	• Software reset register (SWRR)
Option-setting memory	Registers/ bits	—	• Option function select register 0 (OFS0) • Option function select register 1 (OFS1) • Endian select register S (MDES) • Endian select register B (MDEB)
Voltage detection circuit	Functions	• Specification overview Voltage detection types: — Voltage detection conditions: — Processing at voltage detection: Reset or interrupt	• Specification overview Voltage detection types: Voltage monitor 0: Vdet0; Voltage monitor 1: Vdet1; Voltage monitor 2: Vdet2 Voltage detection conditions*1: Voltage rises past Vdetx.; Voltage drops past Vdetx. Processing at voltage detection*2: Reset or interrupt (voltage monitors 1 and 2) Notes: 1. Voltage drops past Vdetx. only for voltage monitor 0. 2. Reset only for voltage monitor 0.
	Registers/ bits	—	• Voltage monitoring 1 circuit control register 1 (LVD1CR1) • Voltage monitoring 1 circuit status register (LVD1SR) • Voltage monitoring 2 circuit control register 1 (LVD2CR1) • Voltage monitoring 2 circuit status register (LVD2SR) • Voltage monitoring circuit control register (LVCMPCR) • Voltage detection level select register (LVDLVLR) • Voltage monitoring 1 circuit control register 0 (LVD1CR0) • Voltage monitoring 2 circuit control register 0 (LVD2CR0)
		• Key code register for low-voltage detection control register (LVDKEYR)	—
		• Low-voltage detection control register (LVDCR)	—
Clock oscillator	Functions	• Specification overview Clock types: ICLK: 100.0 MHz (max); PCLK: 50.0 MHz (max); —; —; —; —; —; —; —; —; IWDTCLK: 125.000 KHz (typ); —	• Specification overview Clock types: ICLK: 100.0 MHz (max); PCLKA: 100.0 MHz (max); PCL KB : 50.0 MHz (max); PCLKC: 100.0 MHz (max); PCLKD: 50.0 MHz (max); FCLK: 50.0 MHz (max); BCLK: 50.0 MHz (max) BCLK output pin: 50.0 MHz (max); UCLK: 48.0 MHz (max); CANMCLK: 14.0 MHz (max); CACCLK: Same as clock of each oscillator (main clock oscillator, PLL circuit, IWDT dedicated low-speed clock oscillator); IWDTCLK: 125.000KHz (typ); JTAGTCK [generated]:10.0 MHz (max) JTAGTCK [input]: 10.0 MHz (max)
	Main clock oscillator	• Specification overview Resonator: Crystal oscillator; — Frequency: 8.0 MHz to 12.5 MHz External clock: 12.5 MHz (max)	• Specification overview Resonator: Crystal oscillator; Ceramic oscillator Frequency: 8.0 MHz to 12.5 MHz External clock: 14.0 MHz (max)
	Low-speed on-chip oscillator	—	• Oscillation frequency: 125.0 KHz
	IWDT-dedicated on-chip oscillator	• IWDT dedicated low-speed on-chip oscillator: 125.0 kHz Supplies IWDTOCLK to IWDT.	• IWDT dedicated low-speed clock oscillator: 125.0 kHz Supplies IWDTOCLK to IWDT and CAC.

Table 2.3 Differences in Functions and Specifications (3)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="5">Clock oscillator</td><td rowspan="5">Registers/ bits</td><td>• System clock control register (SCKCR)
<table><tr><td>b0
b3</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b4
b7</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b8
b11</td><td>PCK [3:0]</td><td>Peripheral module clock select bits</td></tr><tr><td>b12
b15</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b16
b19</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b20
b23</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b24
b27</td><td>ICK [3:0]</td><td>System clock select bits</td></tr><tr><td>b28
b31</td><td>—</td><td>(Reserved bits)</td></tr></table>• PCK[3:0]
0001b: ×4
0010b: ×2
0011b: ×1
• ICK[3:0]
0000b: ×8
0001b: ×4
0010b: ×2
0011b: ×1</td><td>• System clock control register (SCKCR)
<table><tr><td>b0
b3</td><td>PCKD[3:0]</td><td>S12AD clock (PCLKD) select bits</td></tr><tr><td>b4
b7</td><td>PCKC[3:0]</td><td>AD clock (PCLKC) select bits</td></tr><tr><td>b8
b11</td><td>PC KB[3:0]</td><td>Peripheral module clock B (PCLKB) select bits</td></tr><tr><td>b12
b15</td><td>PCKA[3:0]</td><td>Timer module clock (PCLKA) select bits</td></tr><tr><td>b16
b19</td><td>BCK[3:0]</td><td>External bus clock (BCLK) select bits</td></tr><tr><td>b23</td><td>PSTOP1</td><td>BCLK pin output control bit</td></tr><tr><td>b24
b27</td><td>ICK [3:0]</td><td>System clock (ICLK) select bits</td></tr><tr><td>b28
b31</td><td>FCK [3:0]</td><td>FlashIF clock (FCLK) select bits</td></tr></table>• PCKD[3:0], PC KB[3:0], PCKA[3:0], ICK[3:0], FCK[3:0]
0000b: ×1/1
0001b: ×1/2
0010b: ×1/4
0011b: ×1/8
0100b: ×1/16
0101b: ×1/32
0110b: ×1/64</td></tr>
<tr><td>—</td><td>• System clock control register 2 (SCKCR2)
• System clock control register 3 (SCKCR3)
• PLL control register (PLLCR)
• PLL control register 2 (PLLCR2)
• External bus clock control register (BCKCR)
• Main clock oscillator control register (MOSCCR)
• Low-speed on-chip oscillator control register (LOCOCR)
• IWDT-dedicated on-chip oscillator control register (ILOCOCR)</td></tr>
<tr><td>• Oscillation stop detection control register (OSTDCR)
<table><tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b1
b5</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b6</td><td>OSTDF</td><td>Oscillation stop detection flag</td></tr><tr><td>b7</td><td>OSTDE</td><td>Oscillation stop detection function enable bit</td></tr><tr><td>b8
b15</td><td>KEY[7:0]</td><td>OSTDCR Key code</td></tr></table></td><td>• Oscillation stop detection control register (OSTDCR)
<table><tr><td>b0</td><td>OSTDIE</td><td>Oscillation stop detection interrupt enable bit</td></tr><tr><td>b1
b6</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b7</td><td>OSTDE</td><td>Oscillation stop detection function enable bit</td></tr></table>• Oscillation stop detection status register (OSTDSR)
<table><tr><td>b0</td><td>OSTDF</td><td>Oscillation stop detection flag</td></tr></table></td></tr>
<tr><td>—</td><td>• Main clock oscillator forced oscillation control register (MOFCR)</td></tr>
<tr><td>Frequency accuracy checker function</td><td>Registers/ bits</td><td>—</td><td>• CAC control register 0 (CACR0)
• CAC control register 1 (CACR1)
• CAC control register 2 (CACR2)
• CAC interrupt control register (CAICR)
• CAC status register (CASTR)
• CAC upper-limit value setting register (CAULVR)
• CAC lower-limit value setting register (CALLVR)
• CAC counter buffer register (CACNTBR)</td></tr>
</table>

Table 2.4 Differences in Functions and Specifications (4)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="3">Low power consumption functions</td><td rowspan="3">Registers/ bits</td><td>
• Standby control register (SBYCR)
<table>
<tr><td>b8
b12</td><td>STS[4:0]</td><td>Standby timer select bits</td></tr>
<tr><td>b14</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b15</td><td>SSBY</td><td>Software standby bit</td></tr>
</table>
• SBYCR.STS[4:0]
00000b: (Setting prohibited)
00001b: (Setting prohibited)
00010b: (Setting prohibited)
00011b: (Setting prohibited)
00100b: (Setting prohibited)
00101b: Waiting time = 64 cycles
00110b: Waiting time = 512 cycles
00111b: Waiting time = 1024 cycles
01000b: Waiting time = 2048 cycles
01001b: Waiting time = 4096 cycles
01010b: Waiting time = 16384 cycles
01011b: Waiting time = 32768 cycles
01100b: Waiting time = 65536 cycles
01101b: Waiting time = 131072 cycles
01110b: Waiting time = 262144 cycles
01111b: Waiting time = 524288 cycles
</td><td>
• Standby control register (SBYCR)
<table>
<tr><td>b8
b12</td><td>—</td><td>(Reserved bits)</td></tr>
<tr><td>b14</td><td>OPE</td><td>Output port enable bit</td></tr>
<tr><td>b15</td><td>SSBY</td><td>Software standby bit</td></tr>
</table>
• Main clock oscillator wait control register (MOSCWTCR)
<table>
<tr><td>b0
b4</td><td>MSTS[4:0]</td><td>Main clock oscillator waiting time setting bits</td></tr>
</table>
• MOSCWTCR. MSTS[4:0]
00000b: Waiting time = 2 cycles
00001b: Waiting time = 4 cycles
00010b: Waiting time = 8 cycles
00011b: Waiting time = 16 cycles
00100b: Waiting time = 32 cycles
00101b: Waiting time = 64 cycles
00110b: Waiting time = 512 cycles
00111b: Waiting time = 1024 cycles
01000b: Waiting time = 2048 cycles
01001b: Waiting time = 4096 cycles
01010b: Waiting time = 16384 cycles
01011b: Waiting time = 32768 cycles
01100b: Waiting time = 65536 cycles
01101b: Waiting time = 131072 cycles
01110b: Waiting time = 262144 cycles
01111b: Waiting time = 524288 cycles
• PLL wait control register (PLLWTCR)
<table>
<tr><td>b0
b4</td><td>PSTS[4:0]</td><td>PLL waiting time setting bits</td></tr>
</table>
• PLLWTCR.PSTS[4:0]
00000b: Waiting time = 16 cycles
... ...
01111b: Waiting time = 4194304 cycles
</td></tr>
<tr><td>
• Module stop control register A (MSTPCRA)
<table>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>MSTPA 7</td><td>General PWM timer module stop bit</td></tr>
<tr><td>b9</td><td>MSTPA 9</td><td>Multifunction timer pulse unit 3 module stop bit</td></tr>
<tr><td>b14</td><td>MSTPA14</td><td>Compare match timer (unit 1) module stop bit</td></tr>
<tr><td>b15</td><td>MSTPA15</td><td>Compare match timer (unit 0) module stop bit</td></tr>
<tr><td>b16</td><td>MSTPA16</td><td>12-bit A/D converter (unit 1) module stop bit</td></tr>
<tr><td>b17</td><td>MSTPA17</td><td>12-bit A/D converter (unit 0) module stop bit</td></tr>
<tr><td>b19</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b23</td><td>MSTPA23</td><td>10-Bit A/D converter module stop bit</td></tr>
<tr><td>b24</td><td>MSTPA24</td><td>12-Bit A/D converter control section module stop bit</td></tr>
<tr><td>b27</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b28</td><td>MSTPA28</td><td>Data transfer controller module stop bit</td></tr>
<tr><td>b29</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b31</td><td>ACSE</td><td>All-module clock stop mode enable bit</td></tr>
</table>
</td><td>
• Module stop control register A (MSTPCRA)
<table>
<tr><td>b6</td><td>MSTPA 6</td><td>General PWM Timer (unit 1) module stop bit</td></tr>
<tr><td>b7</td><td>MSTPA 7</td><td>General PWM Timer (unit 0) module stop bit</td></tr>
<tr><td>b9</td><td>MSTPA 9</td><td>Multifunction timer pulse unit 3 module stop bit</td></tr>
<tr><td>b14</td><td>MSTPA14</td><td>Compare match timer (unit 1) module stop bit</td></tr>
<tr><td>b15</td><td>MSTPA15</td><td>Compare match timer (unit 0) module stop bit</td></tr>
<tr><td>b16</td><td>MSTPA16</td><td>12-bit A/D converter (unit 1) module stop bit</td></tr>
<tr><td>b17</td><td>MSTPA17</td><td>12-bit A/D converter (unit 0) module stop bit</td></tr>
<tr><td>b19</td><td>MSTPA19</td><td>D/A converter module stop bit</td></tr>
<tr><td>b23</td><td>MSTPA23</td><td>10-bit A/D converter module stop bit</td></tr>
<tr><td>b24</td><td>MSTPA24</td><td>12-bit A/D converter control section module stop bit</td></tr>
<tr><td>b27</td><td>MSTPA27</td><td>Module stop A27 bit</td></tr>
<tr><td>b28</td><td>MSTPA28</td><td>DMA controller/data transfer controller module stop bit</td></tr>
<tr><td>b29</td><td>MSTPA29</td><td>Module stop A29 bit</td></tr>
<tr><td>b31</td><td>ACSE</td><td>All-module clock stop mode enable bit</td></tr>
</table>
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</table>

Table 2.5 Differences in Functions and Specifications (5)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="4">Low power consumption functions</td><td rowspan="4">Registers/ bits</td><td>• Module stop control register B (MSTPCRB)
<table>
<tr><td>b0</td><td>MSTPB0</td><td>CAN module stop bit</td></tr>
<tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>MSTPB7</td><td>LIN module stop bit</td></tr>
<tr><td>b16</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b17</td><td>MSTPB17</td><td>Serial peripheral interface module stop bit</td></tr>
<tr><td>b19</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b20</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b21</td><td>MSTPB21</td><td>I²C bus interface module stop bit</td></tr>
<tr><td>b23</td><td>MSTPB23</td><td>CRC calculator module stop bit</td></tr>
<tr><td>b28</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b29</td><td>MSTPB29</td><td>Serial communications interface 2 module stop bit</td></tr>
<tr><td>b30</td><td>MSTPB30</td><td>Serial communications interface 1 module stop bit</td></tr>
<tr><td>b31</td><td>MSTPB31</td><td>Serial communications interface 0 module stop bit</td></tr>
</table></td><td>• Module stop control register B (MSTPCRB)
<table>
<tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b1</td><td>MSTPB1</td><td>CAN module 1 module stop bit</td></tr>
<tr><td>b4</td><td>MSTPB4</td><td>Serial communications interface SCId module stop bit</td></tr>
<tr><td>b6</td><td>MSTPB6</td><td>Data operation circuit module stop bit</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b16</td><td>MSTPB16</td><td>Serial peripheral interface 1 module stop bit</td></tr>
<tr><td>b17</td><td>MSTPB17</td><td>Serial peripheral interface 0 module stop bit</td></tr>
<tr><td>b19</td><td>MSTPB19</td><td>Universal serial bus interface (port 0) module stop bit</td></tr>
<tr><td>b20</td><td>MSTPB20</td><td>I²C bus interface 1 module stop bit</td></tr>
<tr><td>b21</td><td>MSTPB21</td><td>I²C bus interface 0 module stop bit</td></tr>
<tr><td>b23</td><td>MSTPB23</td><td>CRC calculator module stop bit</td></tr>
<tr><td>b28</td><td>MSTPB28</td><td>Serial communications interface 3 module stop bit</td></tr>
<tr><td>b29</td><td>MSTPB29</td><td>Serial communications interface 2 module stop bit</td></tr>
<tr><td>b30</td><td>MSTPB30</td><td>Serial communications interface 1 module stop bit</td></tr>
<tr><td>b31</td><td>MSTPB31</td><td>Serial communications interface 0 module stop bit</td></tr>
</table></td></tr>
<tr><td>• Module stop control register C (MSTPCRC)
<table>
<tr><td>b0</td><td>MSTPC0</td><td>RAM module stop bit</td></tr>
<tr><td>b19</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Module stop control register C (MSTPCRC)
<table>
<tr><td>b0</td><td>MSTPC0</td><td>RAM0 module stop bit</td></tr>
<tr><td>b19</td><td>MSTPC19</td><td>Clock frequency accuracy measurement circuit module stop bit</td></tr>
</table></td></tr>
<tr><td>• Deep standby control register (DPSBYCR)
<table>
<tr><td>b4
b5</td><td>—</td><td>(Reserved bits)
Note: Value is 1 when read.</td></tr>
<tr><td>b6</td><td>IOKEEP</td><td>I/O port retention bit</td></tr>
<tr><td>b7</td><td>DPSBY</td><td>Deep software standby bit</td></tr>
</table></td><td>• Deep standby control register (DPSBYCR)
<table>
<tr><td>b4
b5</td><td>—</td><td>(Reserved bits)
Note: Value is 0 when read.</td></tr>
<tr><td>b6</td><td>IOKEEP</td><td>I/O port retention bit</td></tr>
<tr><td>b7</td><td>DPSBY</td><td>Deep software standby bit</td></tr>
</table></td></tr>
</table>

Table 2.6 Differences in Functions and Specifications (6)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="4">Low power consumption functions</td><td rowspan="4">Registers/ bits</td><td>• Deep standby wait control register (DPSWCR)
• DPSWCR.WTSTS[5:0]
000101b: Waiting time = 64 cycles
000110b: Waiting time = 512 cycles
000111b: Waiting time = 1024 cycles
001000b: Waiting time = 2048 cycles
001001b: Waiting time = 4096 cycles
001010b: Waiting time = 16384 cycles
001011b: Waiting time = 32768 cycles
001100b: Waiting time = 65536 cycles
001101b: Waiting time = 131072 cycles
001110b: Waiting time = 262144 cycles
001111b: Waiting time = 524288 cycles</td><td>—</td></tr>
<tr><td>• Deep standby interrupt enable register (DPSIER)
<table><tr><td>b0</td><td>DIRQ0E</td><td>IRQ0 pin enable bit</td></tr><tr><td>b1</td><td>DIRQ1E</td><td>IRQ1 pin enable bit</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>DLVDE</td><td>LVD deep standby cancel signal enable bit</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>DNMIE</td><td>NMI pin enable bit</td></tr></table></td><td>• Deep standby interrupt enable register 0 (DPSIER0)
<table><tr><td>b0</td><td>DIRQ0E</td><td>IRQ0-DS pin enable bit</td></tr><tr><td>b1</td><td>DIRQ1E</td><td>IRQ1-DS pin enable bit</td></tr><tr><td>b2</td><td>DIRQ2E</td><td>IRQ2-DS pin enable bit</td></tr><tr><td>b3</td><td>DIRQ3E</td><td>IRQ3-DS pin enable bit</td></tr><tr><td>b4</td><td>DIRQ4E</td><td>IRQ4-DS pin enable bit</td></tr><tr><td>b5</td><td>DIRQ5E</td><td>IRQ5-DS pin enable bit</td></tr><tr><td>b6</td><td>DIRQ6E</td><td>IRQ6-DS pin enable bit</td></tr><tr><td>b7</td><td>DIRQ7E</td><td>IRQ7-DS pin enable bit</td></tr></table>• Deep standby interrupt enable register 2 (DPSIER2)
<table><tr><td>b0</td><td>DLVD1IE</td><td>LVD1 deep standby cancel signal enable bit</td></tr><tr><td>b1</td><td>DLVD2IE</td><td>LVD2 deep standby cancel signal enable bit</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>DNMIE</td><td>NMI pin enable bit</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
<tr><td>• Deep standby interrupt flag register (DPSIFR)
<table><tr><td>b0</td><td>DIRQ0F</td><td>IRQ0 deep standby cancel flag</td></tr><tr><td>b1</td><td>DIRQ1F</td><td>IRQ1 deep standby cancel flag</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>DLVDF</td><td>LVD deep standby cancel flag</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>DNMIF</td><td>NMI deep standby cancel flag</td></tr></table></td><td>• Deep standby interrupt flag register 0 (DPSIFR0)
<table><tr><td>b0</td><td>DIRQ0F</td><td>IRQ0-DS pin deep standby cancel flag</td></tr><tr><td>b1</td><td>DIRQ1F</td><td>IRQ1-DS pin deep standby cancel flag</td></tr><tr><td>b2</td><td>DIRQ2F</td><td>IRQ2-DS pin deep standby cancel flag</td></tr><tr><td>b3</td><td>DIRQ3F</td><td>IRQ3-DS pin deep standby cancel flag</td></tr><tr><td>b4</td><td>DIRQ4F</td><td>IRQ4-DS pin deep standby cancel flag</td></tr><tr><td>b5</td><td>DIRQ5F</td><td>IRQ5-DS pin deep standby cancel flag</td></tr><tr><td>b6</td><td>DIRQ6F</td><td>IRQ6-DS pin deep standby cancel flag</td></tr><tr><td>b7</td><td>DIRQ7F</td><td>IRQ7-DS pin deep standby cancel flag</td></tr></table>• Deep standby interrupt flag register 2 (DPSIFR2)
<table><tr><td>b0</td><td>DLVD1IF</td><td>LVD1 deep standby cancel flag</td></tr><tr><td>b1</td><td>DLVD2IF</td><td>LVD2 deep standby cancel flag</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>DNMIF</td><td>NMI deep standby cancel flag</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
</table>

Table 2.7 Differences in Functions and Specifications (7)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>Low power consumption functions</td><td>Registers/ bits</td><td>• Deep standby interrupt edge register (DPSIEGR)<table><tr><td>b0</td><td>DIRQ0EG</td><td>IRQ0 edge select bit</td></tr><tr><td>b1</td><td>DIRQ1EG</td><td>IRQ1 edge select bit</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>DNMIEG</td><td>NMI edge select bit</td></tr></table></td><td>• Deep standby interrupt edge register 0 (DPSIEGR0)<table><tr><td>b0</td><td>DIRQ0EG</td><td>IRQ0-DS edge select bit</td></tr><tr><td>b1</td><td>DIRQ1EG</td><td>IRQ1-DS edge select bit</td></tr><tr><td>b2</td><td>DIRQ2EG</td><td>IRQ2-DS edge select bit</td></tr><tr><td>b3</td><td>DIRQ3EG</td><td>IRQ3-DS edge select bit</td></tr><tr><td>b4</td><td>DIRQ4EG</td><td>IRQ4-DS edge select bit</td></tr><tr><td>b5</td><td>DIRQ5EG</td><td>IRQ5-DS edge select bit</td></tr><tr><td>b6</td><td>DIRQ6EG</td><td>IRQ6-DS pin edge select bit</td></tr><tr><td>b7</td><td>DIRQ7EG</td><td>IRQ7-DS pin edge select bit</td></tr></table>• Deep standby interrupt edge register 2 (DPSIEGR2)<table><tr><td>b0</td><td>DLVD1EG</td><td>LVD1 edge select bit</td></tr><tr><td>b1</td><td>DLVD2EG</td><td>LVD2 edge select bit</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>DNMIEG</td><td>NMI edge select bit</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
<tr><td>Register write protection function</td><td>Registers/ bits</td><td>—</td><td>• Protect register (PRCR)</td></tr>
<tr><td>Interrupt controller</td><td>Functions</td><td>• Peripheral function interrupts<table><tr><td>Interrupts</td><td>Interrupts from peripheral modules</td></tr><tr><td>Sources</td><td>101</td></tr><tr><td>Interrupt detection</td><td>Edge detection/level detection</td></tr></table>—• External pin interrupts<table><tr><td>Interrupts</td><td>Interrupts from IRQ0-IRQ7 pins</td></tr><tr><td>Sources</td><td>8</td></tr><tr><td>—</td><td>—</td></tr></table>• Non-maskable interrupts<table><tr><td>Interrupt types</td><td>NMI pin interrupt</td></tr><tr><td></td><td>Oscillation stop detection</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>Voltage monitoring interrupt</td></tr><tr><td></td><td>—</td></tr></table></td><td>• Peripheral function interrupts<table><tr><td>Interrupts</td><td>Interrupts from peripheral modules</td></tr><tr><td>Sources</td><td>163</td></tr><tr><td>Interrupt detection</td><td>Edge detection/level detection</td></tr></table>• Group function interrupts<table><tr><td>Edge detection</td><td>1 (group 0)</td></tr><tr><td>Level detection</td><td>1 (group 12)</td></tr></table>• External pin interrupts<table><tr><td>Interrupts</td><td>Interrupts from IRQ0-IRQ7 pins</td></tr><tr><td>Sources</td><td>8</td></tr><tr><td>Digital filter function</td><td>Supported</td></tr></table>• Non-maskable interrupts<table><tr><td>Interrupt types</td><td>NMI pin interrupt</td></tr><tr><td></td><td>Oscillation stop detection interrupt</td></tr><tr><td></td><td>WDT underflow/ refresh error</td></tr><tr><td></td><td>IWDT underflow/ refresh error</td></tr><tr><td></td><td>Voltage monitoring 1 interrupt</td></tr><tr><td></td><td>Voltage monitoring 2 interrupt</td></tr></table></td></tr>
</table>

Table 2.8 Differences in Functions and Specifications (8)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="2">Interrupt controller</td><td>Functions</td><td>
• Return from power-down modes
<table>
<tr><td>Sleep mode</td><td>All interrupt sources
Reset by RES# pin
Power-on reset
Voltage monitoring reset
Reset at WDT overflow
Reset at IWDT underflow</td></tr>
<tr><td>All-module clock stop mode</td><td>NMI pin interrupt
Voltage monitoring interrupt
—
Oscillation stop detection interrupt
—
WDT overflow interrupt
—
Interrupts from IRQ0-IRQ7 pins
Reset by RES# pin
Power-on reset
Voltage monitoring reset
WDT reset
—</td></tr>
<tr><td>Software standby mode</td><td>NMI pin interrupt
Voltage monitoring interrupt
—
—
—
Interrupts from IRQ0-IRQ7 pins
Reset by RES# pin
Power-on reset
Voltage monitoring reset
—</td></tr>
<tr><td>Deep software standby mode</td><td>NMI pin interrupt
Voltage monitoring interrupt
—
IRQ0-A and IRQ1-A pin interrupts
Reset by RES# pin
Power-on reset
Voltage monitoring reset</td></tr>
</table>
</td><td>
• Return from power-down modes
<table>
<tr><td>Sleep mode</td><td>All interrupt sources
Reset by RES# pin
Power-on reset
Voltage monitoring reset
—
Reset at IWDT underflow</td></tr>
<tr><td>All-module clock stop mode</td><td>NMI pin interrupt
Voltage monitoring 1 interrupt
Voltage monitoring 2 interrupt
Oscillation stop detection interrupt
IWDT underflow/ refresh error
—
USB suspend/resume
Interrupts from IRQ0-IRQ7 pins
Reset by RES# pin
Power-on reset
Voltage monitoring reset
—
IWDT reset</td></tr>
<tr><td>Software standby mode</td><td>NMI pin interrupt
Voltage monitoring 1 interrupt
Voltage monitoring 2 interrupt
IWDT underflow/refresh error
USB suspend/resume
IRQ0 to IRQ7 interrupt
Reset by RES# pin
Power-on reset
Voltage monitoring reset
IWDT reset</td></tr>
<tr><td>Deep software standby mode</td><td>NMI pin interrupt
Voltage monitoring 1 interrupt
Voltage monitoring 2 interrupt
IRQ0-DS to IRQ7-DS interrupts
Reset by RES# pin
Power-on reset
Voltage monitoring 0 reset</td></tr>
</table>
</td></tr>
<tr><td>Vector table</td><td>
• Vector table (1/4)
<table>
<tr><th>No</th><th>Interrupt</th><th>Name</th><th>DTCER</th><th>IPR</th></tr>
<tr><td>0</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>1</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>2</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>3</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>4</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>5</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>6</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>7</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>8</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>9</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>10</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>11</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>12</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>13</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>14</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>15</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>16</td><td>Bus error</td><td>BUSERR</td><td>—</td><td>00</td></tr>
<tr><td>21</td><td rowspan="2">FCUIF</td><td>FIFERR</td><td rowspan="2">—</td><td>01</td></tr>
<tr><td>23</td><td>FRDYI</td><td>02</td></tr>
<tr><td>27</td><td>ICU</td><td>SWINT</td><td>027</td><td>03</td></tr>
<tr><td>28</td><td>CMT0</td><td>CMI0</td><td>028</td><td>04</td></tr>
<tr><td>29</td><td>CMT1</td><td>CMI1</td><td>029</td><td>05</td></tr>
<tr><td>30</td><td>CMT2</td><td>CMI2</td><td>030</td><td>06</td></tr>
<tr><td>31</td><td>CMT3</td><td>CMI3</td><td>031</td><td>07</td></tr>
<tr><td>33</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>34</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>35</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
</table>
</td><td>
• Vector table (1/4)
<table>
<tr><th>No</th><th>Interrupt</th><th>Name</th><th>DTCER</th><th>IPR</th></tr>
<tr><td>0</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>1</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>2</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>3</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>4</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>5</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>6</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>7</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>8</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>9</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>10</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>11</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>12</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>13</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>14</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>15</td><td>—</td><td>Unconditional trap (dedicated)</td><td>—</td><td>—</td></tr>
<tr><td>16</td><td>BSC</td><td>BUSERR</td><td>—</td><td>000</td></tr>
<tr><td>21</td><td rowspan="2">FCU</td><td>FIFERR</td><td rowspan="2">—</td><td>001</td></tr>
<tr><td>23</td><td>FRDYI</td><td>002</td></tr>
<tr><td>27</td><td>ICU</td><td>SWINT</td><td>027</td><td>003</td></tr>
<tr><td>28</td><td>CMT0</td><td>CMI0</td><td>028</td><td>004</td></tr>
<tr><td>29</td><td>CMT1</td><td>CMI1</td><td>029</td><td>005</td></tr>
<tr><td>30</td><td>CMT2</td><td>CMI2</td><td>030</td><td>006</td></tr>
<tr><td>31</td><td>CMT3</td><td>CMI3</td><td>031</td><td>007</td></tr>
<tr><td>33</td><td>USB0</td><td>D0FIFO0</td><td>033</td><td>033</td></tr>
<tr><td>34</td><td>*1 *2</td><td>D1FIFO0</td><td>034</td><td>034</td></tr>
<tr><td>35</td><td></td><td>USBI0</td><td>—</td><td>035</td></tr>
</table>
</td></tr>
</table>

Table 2.9 Differences in Functions and Specifications (9)

Item		RX62T Group	RX63T Group
Interrupt controller	Vector table	• Vector table (2/4)	• Vector table(2/4)

No	Interrupt	Name	DTCER	IPR
36	—	(Reserved)	—	—
37	—	(Reserved)	—	—
38	—	(Reserved)	—	—
39	—	(Reserved)	—	—
40	—	(Reserved)	—	—
41	—	(Reserved)	—	—
42	—	(Reserved)	—	—
43	—	(Reserved)	—	—
44	RSPI0	SPEI0	—	14
45		SPRI0	045	
46		SPTI0	046	
47		SPII0	—	
48	—	(Reserved)	—	—
49	—	(Reserved)	—	—
50	—	(Reserved)	—	—
51	—	(Reserved)	—	—
52	—	(Reserved)	—	—
53	—	(Reserved)	—	—
54	—	(Reserved)	—	—
55	—	(Reserved)	—	—
56	CAN0	ERS0	—	18
57		RXF0		
58		TXF0		
59		RXM0		
60		TXM0		
64	External pin	IRQ0	064	20
65		IRQ1	065	21
66		IRQ2	066	22
67		IRQ3	067	23
68		IRQ4	068	24
69		IRQ5	069	25
70		IRQ6	070	26
71		IRQ7	071	27
90	—	(Reserved)	—	—
96	WDT	WOVI	—	40
98	AD0	ADI0	098	44
102	S12AD0	S12ADI0	102	48
103	S12AD1	S12ADI1	103	
104	—	(Reserved)	—	—
105	—	(Reserved)	—	—
106	Comparators	CMPI	106	49
114	MTU0	TGIA0	114	51
115		TGIB0	115	
116		TGIC0	116	
117		TGID0	117	
118		TCIV0	—	52
119		TGIE0		
120		TGIF0		

No	Interrupt	Name	DTCER	IPR
36	CAC	FERRF	—	036
37		MENDF		
38		OVFF		
39	RSPI0	SPRI0	039	039
40		SPTI0	040	
41		SPII0	—	
42	RSPI1	SPRI1	042	042
43		SPTI1	043	
44		SPII1	—	
45	CAN1	RXF1	—	045
46		TXF1		
47		RXM1		
48		TXM1		
49	GPT7	GTCIA7	049	049
50		GTCIB7	050	
51		GTCIC7	051	
52		GTCIE7	052	052
53		GTCIV7	053	
54	Comparators	CMP4	054	054
55		CMP5	055	055
56		CMP6	056	056
57	DOC	DOPCF	—	057
58	—	(Reserved)	—	—
59	—	(Reserved)	—	—
60	—	(Reserved)	—	—
64	ICU	IRQ0	064	064
65		IRQ1	065	065
66		IRQ2	066	066
67		IRQ3	067	067
68		IRQ4	068	068
69		IRQ5	069	069
70		IRQ6	070	070
71		IRQ7	071	071
90	USB *1 *2	USBR0	—	090
96	—	(Reserved)	—	—
98	AD	ADI0	098	098
102	S12AD	S12ADI	102	102
103		S12GBADI	103	103
104	S12AD1	S12ADI1	104	104
105		S12GBADI1	105	105
106	ICU	GROUP0	—	106
114	ICU	GROUP12	—	114
115	—	(Reserved)	—	—
116	—	(Reserved)	—	—
117	—	(Reserved)	—	—
118	—	(Reserved)	—	—
119	—	(Reserved)	—	—
120	—	(Reserved)	—	—

Table 2.10 Differences in Functions and Specifications (10)

Item		RX62T Group	RX63T Group
Interrupt controller	Vector table	• Vector table (3/4)	• Vector table (3/4)

No	Interrupt	Name	DTCER	IPR
121	MTU1	TGIA1	122	53
122		TGIB1	123	
123		TCIV1	—	54
124		TCIU1		
125	MTU2	TGIA2	125	55
126		TGIB2	126	
127		TCIV2	—	56
128		TCIU2		
129	MTU3	TGIA3	129	57
130		TGIB3	130	
131		TGIC3	131	
132		TGID3	132	
133		TCIV3	—	58
134	MTU4	TGIA4	134	59
135		TGIB4	135	
136		TGIC4	136	
137		TGID4	137	
138		TCIV4	138	5A
139	MTU5	TGIU5	139	5B
140		TGIV5	140	
141		TGIW5	141	
142	MTU6	TGIA6	142	5C
143		TGIB6	143	
144		TGIC6	144	
145		TGID6	145	
146		TCIV6	—	5D
147	—	(Reserved)	—	—
148	—	(Reserved)	—	—
149	MTU7	TGIA7	149	5E
150		TGIB7	150	
151		TGIC7	151	5F
152		TGID7	152	
153		TCIV7	153	60
154	—	(Reserved)	—	—
155	—	(Reserved)	—	—
156	—	(Reserved)	—	—
157	—	(Reserved)	—	—
158	—	(Reserved)	—	—
161	—	(Reserved)	—	—
162	—	(Reserved)	—	—
163	—	(Reserved)	—	—
164	—	(Reserved)	—	—
165	—	(Reserved)	—	—
166	—	(Reserved)	—	—
167	—	(Reserved)	—	—
168	—	(Reserved)	—	—
169	—	(Reserved)	—	—
170	POE	OEI1	—	67
171		OEI2		
172		OEI3		
173		OEI4		
174	GPT0	GTCIA0	174	68
175		GTCIB0	175	
176		GTCIC0	176	
177		GTCIE0	177	69
178		GTCIV0	178	
179		LOCO1	179	

No	Interrupt	Name	DTCER	IPR
121	—	(Reserved)	—	—
122	SCI12	SCIX0	—	122
123		SCIX1		
124		SCIX2		
125		SCIX3		
126	MTU0	TGIA0	126	126
127		TGIB0	127	
128		TGIC0	128	
129		TGID0	129	
130		TCIV0	—	130
131		TGIE0		
132		TGIF0		
133	MTU1	TGIA1	133	133
134		TGIB1	134	
135		TCIV1	—	135
136		TCIU1		
137	MTU2	TGIA2	137	137
138		TGIB2	138	
139		TCIV2	—	139
140		TCIU2		
141	MTU3	TGIA3	141	141
142		TGIB3	142	
143		TGIC3	143	
144		TGID3	144	
145		TCIV3	—	145
146	MTU4	TGIA4	146	146
147		TGIB4	147	
148		TGIC4	148	
149		TGID4	149	
150		TCIV4	150	150
151	MTU5	TGIU5	151	151
152		TGIV5	152	
153		TGIW5	153	
154	MTU6	TGIA6	154	154
155		TGIB6	155	
156		TGIC6	156	
157		TGID6	157	
158		TCIV6	—	158
161	MTU7	TGIA7	161	161
162		TGIB7	162	
163		TGIC7	163	163
164		TGID7	164	
165		TCIV7	165	165
166	POE	OEI1	—	166
167		OEI2		
168		OEI3		
169		OEI4		
170		OEI5		
171	Comparators	CMP0	171	171
172		CMP1	172	172
173		CMP2	173	173
174	GPT4	GTCIA4	174	174
175		GTCIB4	175	
176		GTCIC4	176	
177		GTCIE4	177	177
178		GTCIV4	178	
179		LOCOI4	179	

Table 2.11 Differences in Functions and Specifications (11)

Item		RX62T Group	RX63T Group
Interrupt controller	Vector table	• Vector table (4/4)	• Vector table (4/4)

No	Interrupt	Name	DTCER	IPR
180	GPT1	GTCIA1	180	6A
181		GTCIB1	181	
182		GTCIC1	182	
183		GTCIE1	183	6B
184		GTCIV1	184	
185		(Reserved)	—	—
186	GPT2	GTCIA2	186	6C
187		GTCIB2	187	
188		GTCIC2	188	
189		GTCIE2	189	6D
190		GTCIV2	190	
191		(Reserved)	—	—
192	GPT3	GTCIA3	192	6E
193		GTCIB3	193	
194		GTCIC3	194	
195		GTCIE3	195	6F
196		GTCIV3	196	
197		(Reserved)	—	—
198	—	(Reserved)	—	—
199	—	(Reserved)	—	—
200	—	(Reserved)	—	—
201	—	(Reserved)	—	—
214	SCI0	ERI0	—	80
215		RXI0	215	
216		TXI0	216	
217		TEI0	—	
218	SCI1	ERI1	—	81
219		RXI1	219	
220		TXI1	220	
221		TEI1	—	
222	SCI2	ERI2	—	82
223		RXI2	223	
224		TXI2	224	
225		TEI2	—	
226	—	(Reserved)	—	—
227	—	(Reserved)	—	—
228	—	(Reserved)	—	—
229	—	(Reserved)	—	—
230	—	(Reserved)	—	—
231	—	(Reserved)	—	—
232	—	(Reserved)	—	—
233	—	(Reserved)	—	—
234	—	(Reserved)	—	—
235	—	(Reserved)	—	—
236	—	(Reserved)	—	—
238	—	(Reserved)	—	—
239	—	(Reserved)	—	—
240	—	(Reserved)	—	—
241	—	(Reserved)	—	—
242	—	(Reserved)	—	—
244	—	(Reserved)	—	—
245	—	(Reserved)	—	—
246	RIIC0	ICEEI0	—	88
247		ICRXI0	247	89
248		ICTXI0	248	8A
249		ICTEI0	—	8B
250	—	(Reserved)	—	—
251	—	(Reserved)	—	—
252	—	(Reserved)	—	—
254	LIN0	LIN0	—	90

No	Interrupt	Name	DTCER	IPR
180	GPT5	GTCIA5	180	180
181		GTCIB5	181	
182		GTCIC5	182	
183		GTCIE5	183	183
184		GTCIV5	184	
185	GPT6	GTCIA6	185	185
186		GTCIB6	186	
187		GTCIC6	187	
188		GTCIE6	188	188
189		GTCIV6	189	
190	RIIC1 *1 *2	EEI1	—	190
191		RXI1	191	
192		TXI1	192	
193		TEI1	—	
194	RIIC0	EEI0	—	194
195		RXI0	195	
196		TXI0	196	
197		TEI0	—	
198	DMAC	DMAC0I	198	198
199		DMAC1I	199	199
200		DMAC2I	200	200
201		DMAC3I	201	201
214	SCI0	RXI0	214	214
215		TXI0	215	
216		TEI0	—	
217	SCI1	RXI1	217	217
218		TXI1	218	
219		TEI1	—	
220	SCI2	RXI2	220	220
221		TXI2	221	
222		TEI2	—	
223	SCI3 *2	RXI3	223	223
224		TXI3	224	
225		TEI3	—	
226	GPT0	GTCIA0	226	226
227		GTCIB0	227	
228		GTCIC0	228	
229		GTCIE0	229	229
230		GTCIV0	230	
231		LOCOI0	231	
232	GPT1	GTCIA1	232	232
233		GTCIB1	233	
234		GTCIC1	234	
235		GTCIE1	235	235
236		GTCIV1	236	
238	GPT2	GTCIA2	238	238
239		GTCIB2	239	
240		GTCIC2	240	
241		GTCIE2	241	241
242		GTCIV2	242	
244	GPT3	GTCIA3	244	244
245		GTCIB3	245	
246		GTCIC3	246	
247		GTCIE3	247	247
248		GTCIV3	248	
249	—	(Reserved)	—	—
250	SCI12	RXI12	250	250
251		TXI12	251	
252		TEI12	—	
254	—	(Reserved)	—	—

Notes: 1. USB0 and RIIC1 are not implemented on the 112-pin version.
2. USB0, RIIC1, and SCI3 are not implemented on the 100-pin version.

Table 2.12 Differences in Functions and Specifications (12)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="11">Interrupt controller</td><td rowspan="11">Registers/ bits</td><td>• Interrupt request register i (IRi)</td><td>• Interrupt request register n (IRn)</td></tr>
<tr><td>• Interrupt source priority register m (IPRm)
(m = 00h to 90h)</td><td>• Interrupt source priority register n (IPRn)
(n = 000 to 250)</td></tr>
<tr><td>• DTC activation enable register n (DTCERn)
(n = interrupt vector number)</td><td>• DTC activation enable register n (DTCERn)
(n = interrupt vector number)</td></tr>
<tr><td rowspan="3">—</td><td>• DMAC activation request select register m (DMRSRm)</td></tr>
<tr><td>• IRQ pin digital filter enable register 0 (IRQFLTE0)</td></tr>
<tr><td>• IRQ pin digital filter setting register 0 (IRQFLTC0)</td></tr>
<tr><td>• Non-maskable interrupt status register (NMISR)
<table>
<tr><td>b0</td><td>NMIST</td><td>NMI status flag</td></tr>
<tr><td>b1</td><td>LVDST</td><td>Voltage monitoring interrupt status flag</td></tr>
<tr><td>b2</td><td>OSTST</td><td>Oscillation stop detection interrupt status flag</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Non-maskable interrupt status register (NMISR)
<table>
<tr><td>b0</td><td>NMIST</td><td>NMI status flag</td></tr>
<tr><td>b1</td><td>OSTST</td><td>Oscillation stop detection interrupt status flag</td></tr>
<tr><td>b2</td><td>WDTST</td><td>WDT underflow/refresh error status flag</td></tr>
<tr><td>b3</td><td>IWDTST</td><td>IWDT underflow/refresh error status flag</td></tr>
<tr><td>b4</td><td>LVD1ST</td><td>Voltage monitoring 1 interrupt status flag</td></tr>
<tr><td>b5</td><td>LVD2ST</td><td>Voltage monitoring 2 interrupt status flag</td></tr>
</table></td></tr>
<tr><td>• Non-maskable interrupt enable register (NMIER)
<table>
<tr><td>b0</td><td>NMIEN</td><td>NMI pin interrupt enable bit</td></tr>
<tr><td>b1</td><td>LVDEN</td><td>Voltage monitoring interrupt enable bit</td></tr>
<tr><td>b2</td><td>OSTEN</td><td>Oscillation stop detection interrupt enable bit</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Non-maskable interrupt enable register (NMIER)
<table>
<tr><td>b0</td><td>NMIEN</td><td>NMI pin interrupt enable bit</td></tr>
<tr><td>b1</td><td>OSTEN</td><td>Oscillation stop detection interrupt enable bit</td></tr>
<tr><td>b2</td><td>WDTEN</td><td>WDT underflow/refresh error enable bit</td></tr>
<tr><td>b3</td><td>IWDTEN</td><td>IWDT underflow/refresh error enable bit</td></tr>
<tr><td>b4</td><td>LVD1EN</td><td>Voltage monitoring 1 interrupt enable bit</td></tr>
<tr><td>b5</td><td>LVD2EN</td><td>Voltage monitoring 2 interrupt enable bit</td></tr>
</table></td></tr>
<tr><td>• Non-maskable interrupt clear register (NMICLR)
<table>
<tr><td>b0</td><td>NMICLR</td><td>NMI clear bit</td></tr>
<tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b2</td><td>OSTCLR</td><td>OST clear bit</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Non-maskable interrupt status clear register (NMICLR)
<table>
<tr><td>b0</td><td>NMICLR</td><td>NMI clear bit</td></tr>
<tr><td>b1</td><td>OSTCLR</td><td>OST clear bit</td></tr>
<tr><td>b2</td><td>WDTCLR</td><td>WDT clear bit</td></tr>
<tr><td>b3</td><td>IWDTCLR</td><td>IWDT clear bit</td></tr>
<tr><td>b4</td><td>LVD1CLR</td><td>LVD1 clear bit</td></tr>
<tr><td>b5</td><td>LVD2CLR</td><td>LVD2 clear bit</td></tr>
</table></td></tr>
<tr><td rowspan="5">—</td><td>• NMI pin digital filter enable register (NMIFLTE)</td></tr>
<tr><td>• NMI pin digital filter setting register (NMIFLTC)</td></tr>
<tr><td>• Group m interrupt source register (GRPm)</td></tr>
<tr><td>• Group m interrupt enable register (GENm)</td></tr>
<tr><td>• Group m interrupt clear register (GCRm)</td></tr>
</table>

Table 2.13 Differences in Functions and Specifications (13)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="3">Bus</td><td>Function</td><td>
• Bus configuration
<table>
<tr><td>Internal main bus 2</td><td>DTC
On-chip RAM, On-chip ROM</td><td>ICLK</td></tr>
<tr><td>Internal peripheral bus 1</td><td>Interrupt controller, bus error monitoring section</td><td>ICLK</td></tr>
<tr><td>Internal peripheral bus 2</td><td>Peripheral functions (WDT, CMT, CRC, SCI, etc)</td><td>PCLK</td></tr>
<tr><td>—</td><td>—</td><td>—</td></tr>
<tr><td>Internal peripheral bus 4</td><td>Peripheral functions (MTU3, GPT)</td><td>ICLK</td></tr>
<tr><td>—</td><td>—</td><td>—</td></tr>
<tr><td>Internal peripheral bus 6</td><td>On-chip ROM (P/E), data flash</td><td>PCLK</td></tr>
<tr><td>—</td><td>—</td><td>—</td></tr>
</table>
• Bus error (illegal address access)
<table>
<tr><th>Address</th><th>Illegal address access</th></tr>
<tr><td>0000 0000h to 0000 3FFFh</td><td>—</td></tr>
<tr><td>0000 4000h to 0007 FFFFh</td><td>—</td></tr>
<tr><td>0008 0000h to 0009 0FFFh</td><td>—</td></tr>
<tr><td>0009 1000h to 0009 3FFFh</td><td>○</td></tr>
<tr><td>0009 4000h to 0009 41FFh</td><td>—</td></tr>
<tr><td>0009 4200h to 0009 FFFFh</td><td>○</td></tr>
<tr><td>000A 0000h to 000B FFFFh</td><td>○</td></tr>
<tr><td>000C 0000h to 000C 0FFFh</td><td>○</td></tr>
<tr><td>000C 1000h to 000C 27FFh</td><td>—</td></tr>
<tr><td>000C 2800h to 000D FFFFh</td><td>○</td></tr>
<tr><td>000E 0000h to 000F FFFFh</td><td>○</td></tr>
<tr><td>0010 0000h to 0011 FFFFh</td><td>—</td></tr>
<tr><td>0012 0000h to 007F 7FFFh</td><td>○</td></tr>
<tr><td>007F 8000h to 007F 9FFFh</td><td>—</td></tr>
<tr><td>007F A000h to 007F BFFFh</td><td>○</td></tr>
<tr><td>007F C000h to 007F C4FFh</td><td>—</td></tr>
<tr><td>007F C500h to 007F FBFFh</td><td>○</td></tr>
<tr><td>007F FC00h to 007F FFFFh</td><td>—</td></tr>
<tr><td>0080 0000h to 00DF FFFFh</td><td>—</td></tr>
<tr><td>00E0 0000h to 00FF FFFFh</td><td>—</td></tr>
<tr><td>0100 0000h to 7FFF FFFFh</td><td>○</td></tr>
<tr><td>8000 0000h to FFFF FFFFh</td><td>—</td></tr>
</table>
—
</td><td>
• Bus configuration
<table>
<tr><td>Internal main bus 2</td><td>DTC, DMAC
RAM, ROM</td><td>ICLK</td></tr>
<tr><td>Internal peripheral bus 1</td><td>DTC, DMAC interrupt controller, bus error monitoring section</td><td>ICLK</td></tr>
<tr><td>Internal peripheral bus 2</td><td>Peripheral functions (modules other than those connected to internal peripheral buses 1, 3, 4, and 5)</td><td>PCLKB</td></tr>
<tr><td>Internal peripheral bus 3</td><td>Peripheral functions (USB)</td><td>PCLKB</td></tr>
<tr><td>Internal peripheral bus 4</td><td>Peripheral functions (MTU3, GPT)</td><td>PCLKA</td></tr>
<tr><td>Internal peripheral bus 5</td><td>—</td><td>—</td></tr>
<tr><td>Internal peripheral bus 6</td><td>ROM (P/E), E2 data flash</td><td>FCLK</td></tr>
<tr><td>CS area</td><td>External device</td><td>BCLK</td></tr>
</table>
• Bus error (illegal address access)
<table>
<tr><th rowspan="2">Address</th><th colspan="2">Illegal address access</th></tr>
<tr><th colspan="2">On-chip ROM mode</th></tr>
<tr><th>Enabled</th><th>Disabled</th></tr>
<tr><td>0000 0000h to 0007 FFFFh</td><td colspan="2">—</td></tr>
<tr><td>0008 0000h to 0008 7FFFh</td><td colspan="2">—</td></tr>
<tr><td>0008 8000h to 0009 FFFFh</td><td colspan="2">Δ</td></tr>
<tr><td>000A 0000h to 000B FFFFh</td><td colspan="2">Δ</td></tr>
<tr><td>000C 0000h to 000D FFFFh</td><td colspan="2">Δ</td></tr>
<tr><td>000E 0000h to 000F FFFFh</td><td colspan="2">—</td></tr>
<tr><td>0010 0000h to 00FF FFFFh</td><td>Δ</td><td>○</td></tr>
<tr><td>0100 0000h to 04FF FFFFh</td><td colspan="2">○</td></tr>
<tr><td>0500 0000h to 07FF FFFFh</td><td colspan="2">[IA]</td></tr>
<tr><td>0800 0000h to 0FFF FFFFh</td><td colspan="2">—</td></tr>
<tr><td>1000 0000h to 7FFF FFFFh</td><td colspan="2">○</td></tr>
<tr><td>8000 0000h to FEFF FFFFh</td><td>—</td><td>○</td></tr>
<tr><td>FF00 0000h to FFFF FFFFh</td><td>—</td><td>[IA]</td></tr>
</table>
• Time out
</td></tr>
<tr><td>Registers/ bits</td><td>—</td><td>
• CSn control register (CSnCR)
• CSn recovery cycle setting register (CSnREC)
• CS recovery cycle insertion enable register (CSRECEN)
• CSn mode register (CSnMOD)
• CSn wait control register 1 (CSnWCR1)
• CSn wait control register 2 (CSnWCR2)
</td></tr>
<tr><td></td><td>
• Bus error monitoring enable register (BEREN)
<table>
<tr><td>b0</td><td>IGAEN</td><td>Illegal address access detection enable bit</td></tr>
<tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr>
</table>
</td><td>
• Bus error monitoring enable register (BEREN)
<table>
<tr><td>b0</td><td>IGAEN</td><td>Illegal address access detection enable bit</td></tr>
<tr><td>b1</td><td>TOEN</td><td>Timeout detection enable bit</td></tr>
</table>
</td></tr>
</table>

Table 2.14 Differences in Functions and Specifications (14)

Item		RX62T Group	RX63T Group
Bus	Registers/ bits	• Bus error status register 1 (BERSR1) b0 IA Illegal address access bit b1 — (Reserved bit) b4 b6 MST[2:0] Bus master code bits • BERSR1.MST[2:0] 000b: CPU 001b: Setting prohibited 010b: Setting prohibited 011b: DTC 100b: Setting prohibited 101b: Setting prohibited 110b: Setting prohibited 111b: Setting prohibited	• Bus error status register 1 (BERSR1) b0 IA Illegal address access bit b1 TO Time out bit b4 b6 MST[2:0] Bus master code bits • BERSR1.MST[2:0] 000b: CPU 001b: Reserved 010b: Reserved 011b: DTC/DMAC 100b: Reserved 101b: Reserved 110b: Reserved 111b: Reserved
		—	• Bus priority control register (BUSPRI)
DMA controller	Registers/ bits	—	• DMA transfer source address register (DMSAR) • DMA transfer destination address register (DMDAR) • DMA transfer count register (DMCRA) • DMA block transfer count register (DMCRB) • DMA transfer mode register (DMTMD) • DMA interrupt setting register (DMINT) • DMA address mode register (DMAMD) • DMA offset register (DMOFR) • DMA transfer enable register (DMCNT) • DMA software start register (DMREQ) • DMA status register (DMSTS) • DMA activation source flag control register (DMCSL) • DMA module activation register (DMAST)
DTC controller	Registers/ bits	• DTC transfer count register A(CRA) Block transfer mode: Transfer count: 1 to 255 • 00h setting prohibited • DTC transfer count register B (CRB) • Set to FFFFh for normal transfer mode. • DTC vector base register (DTCVBR) b11 to b0: Value is 0 when read. b31 to b12: Writing to b31 to b28 has no effect. • 14.3 Sources of Activation • None listed.	• DT transfer count register A(CRA) Block transfer mode: Transfer count: 1 to 256 • No limitations. • DTC transfer count register B (CRB) • The CRB register is not used in normal transfer mode. • DTC vector base register (DTCVBR) b9 to b0: Value is 0 when read. b31 to b10: Writing to b31 to b28 has no effect. • 19.3 Sources of Activation • Once the DTC acknowledges a startup request, (omitted) the highest priority request is acknowledged.
I/O port	Registers/ bits	• Data direction register (DDR) • Data register (DR) • Port register (PORT) • Input buffer control register (ICR)	• Port direction register (PDR) • Port output data register (PODR) • Port input data register (PIDR) • Port mode register (PMR)
		—	• Open drain control register 0 (ODR0) • Open drain control register 1 (ODR1) • Driving ability control register 1 (DSCR1) • Driving ability control register 2 (DSCR2)
		• Port function register 8 (PF8IRQ) • Port function register 9 (PF9IRQ) • Port function register A (PFAADC) • Port function register C (PFCMTU) • Port function register D (PFDGPT) • Port function register F (PFFSCI) • Port function register G (PFGSPI) • Port function register H (PFHSPI) • Port function register J (PFJCAN) • Port function register K (PFKLIN)	—

Table 2.15 Differences in Functions and Specifications (15)

Item		RX62T Group	RX63T Group
I/O port	Registers/ bits	• Port function register M (PFMPOE) • Port function register N (PFNPOE)	—
Multi-function pin controller	Registers/ bits	—	• Write-protect register (PWPR) • P0n pin function control register (P0nPFS) • P1n pin function control register (P1nPFS) • P2n pin function control register (P2nPFS) • P3n pin function control register (P3nPFS) • P4n pin function control register (P4nPFS) • P5n pin function control register (P5nPFS) • P6n pin function control register (P6nPFS) • P7n pin function control register (P7nPFS) • P8n pin function control register (P8nPFS) • P9n pin function control register (P9nPFS) • PAn pin function control register (PAnPFS) • PBn pin function control register (PBnPFS) • PCn pin function control register (PCnPFS) • PDn pin function control register (PDnPFS) • PEn pin function control register (PEnPFS) • PFn pin function control register (PFnPFS) • PGn pin function control register (PGnPFS) • USB0_DPUPE pin function control register (UDPUPEPFS) • CS output enable register (PFCSE) • CS output pin select register 0 (PFCSS0) • Address output enable register 0 (PFAOE0) • Address output enable register 1 (PFAOE1) • External bus control register 0 (PFBCR0) • External bus control register 1 (PFBCR1) • USB0 control register (PFUSB0)
Multi-function timer pulse unit 3	Registers/ bits	• Timer control register (TCR) MTU0, MTU1, MTU2, MTU3, MTU4, MTU6, MTU7 b0 b2 | TPSC[2:0] | Time prescaler select bits • TPSC[2:0] (MTU0) 000b: Internal clock: counts on ICLK/1 001b: Internal clock: counts on ICLK/4 010b: Internal clock: counts on ICLK/16 011b: Internal clock: counts on ICLK/64 100b: External clock: counts on MTCLKA pin input 101b: External clock: counts on MTCLKB pin input 110b: External clock: counts on MTCLKC pin input 111b: External clock: counts on MTCLKD pin input • TPSC[2:0] (MTU1) 000b: Internal clock: counts on ICLK/1 001b: Internal clock: counts on ICLK/4 010b: Internal clock: counts on ICLK/16 011b: Internal clock: counts on ICLK/64 100b: External clock: counts on MTCLKA pin input 101b: External clock: counts on MTCLKB pin input 110b: Internal clock: counts on ICLK/256 111b: Counts on MTU2.TCNT overflow/underflow	• Timer control register (TCR) MTU0, MTU1, MTU2, MTU3, MTU4, MTU6, MTU7 b0 b2 | TPSC[2:0] | Time prescaler select bits • TPSC[2:0] (MTU0) 000b: Internal clock: counts on PCLKA/1 001b: Internal clock: counts on PCLKA/4 010b: Internal clock: counts on PCLKA/16 011b: Internal clock: counts on PCLKA/64 100b: External clock: counts on MTCLKA pin input 101b: External clock: counts on MTCLKB pin input 110b: External clock: counts on MTCLKC pin input 111b: External clock: counts on MTCLKD pin input • TPSC[2:0] (MTU1) 000b: Internal clock: counts on PCLKA/1 001b: Internal clock: counts on PCLKA/4 010b: Internal clock: counts on PCLKA/16 011b: Internal clock: counts on PCLKA/64 100b: External clock: counts on MTCLKA pin input 101b: External clock: counts on MTCLKB pin input 110b: Internal clock: counts on PCLKA/256 111b: Counts on MTU2.TCNT overflow/underflow

Table 2.16 Differences in Functions and Specifications (16)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>Multi-function timer pulse unit 3</td><td>Registers/ bits</td><td>• TPSC[2:0] (MTU2)
000b: Internal clock: counts on ICLK/1
001b: Internal clock: counts on ICLK/4
010b: Internal clock: counts on ICLK/16
011b: Internal clock: counts on ICLK/64
100b: External clock: counts on MTCLKA pin input
101b: External clock: counts on MTCLKB pin input
110b: External clock: counts on MTCLKC pin input
111b: Internal clock: counts on ICLK/1024
• TPSC[2:0] (MTU3,4,6,7)
000b: Internal clock: counts on ICLK/1
001b: Internal clock: counts on ICLK/4
010b: Internal clock: counts on ICLK/16
011b: Internal clock: counts on ICLK/64
100b: Internal clock: counts on ICLK/256
101b: Internal clock: counts on ICLK/1024
110b: External clock: counts on MTCLKA pin input *1
111b: External clock: counts on MTCLKB pin input *1
Note 1. This setting is not allowed in MTU6 and MTU7
MTU5
<table><tr><td>b0
b2</td><td>TPSC[1:0]</td><td>Time prescaler select bit</td></tr></table>• TPSC[1:0] (MTU5)
00b: Internal clock: counts on ICLK/1
01b: Internal clock: counts on ICLK/4
10b: Internal clock: counts on ICLK/16
11b: Internal clock: counts on ICLK/64</td><td>• TPSC[2:0] (MTU2)
000b: Internal clock: counts on PCLKA/1
001b: Internal clock: counts on PCLKA/4
010b: Internal clock: counts on PCLKA/16
011b: Internal clock: counts on PCLKA/64
100b: External clock: counts on MTCLKA pin input
101b: External clock: counts on MTCLKB pin input
110b: External clock: counts on MTCLKC pin input
111b: Internal clock: counts on PCLKA/1024
• TPSC[2:0] (MTU3,4,6,7)
000b: Internal clock: counts on PCLKA/1
001b: Internal clock: counts on PCLKA/4
010b: Internal clock: counts on PCLKA/16
011b: Internal clock: counts on PCLKA/64
100b: Internal clock: counts on PCLKA/256
101b: Internal clock: counts on PCLKA/1024
110b: External clock: counts on MTCLKA pin input *1
111b: External clock: counts on MTCLKB pin input *1
Note 1. This setting is not allowed in MTU6 and MTU7
MTU5
<table><tr><td>b0
b2</td><td>TPSC[1:0]</td><td>Time prescaler select bit</td></tr></table>• TPSC[1:0] (MTU5)
00b: Internal clock: counts on PCLKA/1
01b: Internal clock: counts on PCLKA/4
10b: Internal clock: counts on PCLKA/16
11b: Internal clock: counts on PCLKA/64</td></tr>
<tr><td rowspan="2">Port output enable 3</td><td>Specification</td><td>• Specification overview
<table><tr><td>Input pins</td><td>POE0#, POE4#, POE8#, POE10#, POE11#</td></tr></table></td><td>• Specification overview
<table><tr><td>Input pins</td><td>POE0#, POE4#, POE8#, POE10#, POE11#, POE12#</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>—</td><td>• Active level register 2 (ALR2)
• Input level control/status register 7 (ICSR7)</td></tr>
</table>

Table 2.17 Differences in Functions and Specifications (17)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="2">Port output enable 3</td><td rowspan="2">Registers/ bits</td><td>• Software port output enable register (SPOER)
<table>
<tr><td>b0</td><td>MTUCH34HIZ</td><td>MTU3 and MTU4 output impedance enable bit</td></tr>
<tr><td>b1</td><td>MTUCH67HIZ</td><td>MTU6 amd MTU7 output impedance enable bit</td></tr>
<tr><td>b2</td><td>MTUCH0HIZ</td><td>MTU0 output high-impedance enable bit</td></tr>
<tr><td>b3</td><td>GPT01HIZ</td><td>GPT0 and GPT1 output high-impedance enable bit</td></tr>
<tr><td>b4</td><td>GPT23HIZ</td><td>GPT2 and GPT3 output high-impedance enable bit</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
</table>
• Port output enable control register 4 (POECR4)
<table>
<tr><td>b0</td><td>CMADDMT34ZE</td><td>MTU CH34high-impedance CFLAG add bit</td></tr>
<tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b2</td><td>IC2ADDMT34ZE</td><td>MTU CH34 high-impedance POE4F add bit</td></tr>
<tr><td>b3</td><td>IC3ADDMT34ZE</td><td>MTU CH34 high-impedance POE8F add bit</td></tr>
<tr><td>b4</td><td>IC4ADDMT34ZE</td><td>MTU CH34 high-impedance POE10F add bit</td></tr>
<tr><td>b5</td><td>IC5ADDMT34ZE</td><td>MTU CH34 high-impedance POE11F add bit</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b8</td><td>CMADDMT67ZE</td><td>MTU CH67 high-impedance CFLAG add bit</td></tr>
<tr><td>b9</td><td>IC1ADDMT67ZE</td><td>MTU CH67 high-impedance POE0F add bit</td></tr>
<tr><td>b10</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b11</td><td>IC3ADDMT67ZE</td><td>MTU CH67 high-impedance POE8F add bit</td></tr>
<tr><td>b12</td><td>IC4ADDMT67ZE</td><td>MTU CH67 high-impedance POE10F add bit</td></tr>
<tr><td>b13</td><td>IC5ADDMT67ZE</td><td>MTU CH67 high-impedance POE11F add bit</td></tr>
<tr><td>b14</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b15</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Software port output enable register (SPOER)
<table>
<tr><td>b0</td><td>MTUCH34HIZ</td><td>MTU3 and MTU4 or MTU6 and MTU7 output impedance enable bit</td></tr>
<tr><td>b1</td><td>MTUCH67HIZ</td><td>MTU6 and MTU7 output high-impedance enable bit</td></tr>
<tr><td>b2</td><td>MTUCH0HIZ</td><td>MTU0 output high-impedance enable bit</td></tr>
<tr><td>b3</td><td>GPT01HIZ</td><td>GPT0 and GPT1 output high-impedance enable bit</td></tr>
<tr><td>b4</td><td>GPT23HIZ</td><td>GPT2 and GPT3 output high-impedance enable bit</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>GPT67HIZ</td><td>GPT6 and GPT7 output high-impedance enable bit</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
</table>
• Port output enable control register 4 (POECR4)
<table>
<tr><td>b0</td><td>CMADDMT34ZE</td><td>MTU CH34 high-impedance CFLAG add bit</td></tr>
<tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b2</td><td>IC2ADDMT34ZE</td><td>MTU CH34 high-impedance POE4F add bit</td></tr>
<tr><td>b3</td><td>IC3ADDMT34ZE</td><td>MTU CH34 high-impedance POE8F add bit</td></tr>
<tr><td>b4</td><td>IC4ADDMT34ZE</td><td>MTU CH34 high-impedance POE10F add bit</td></tr>
<tr><td>b5</td><td>IC5ADDMT34ZE</td><td>MTU CH34 high-impedance POE11F add bit</td></tr>
<tr><td>b6</td><td>IC6ADDMT34ZE</td><td>MTU CH34 high-impedance POE12F add bit</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b8</td><td>CMADDMT67ZE</td><td>MTU CH67 high-impedance CFLAG add bit</td></tr>
<tr><td>b9</td><td>IC1ADDMT67ZE</td><td>MTU CH67 high-impedance POE0F add bit</td></tr>
<tr><td>b10</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b11</td><td>IC3ADDMT67ZE</td><td>MTU CH67 high-impedance POE8F add bit</td></tr>
<tr><td>b12</td><td>IC4ADDMT67ZE</td><td>MTU CH67 high-impedance POE10F add bit</td></tr>
<tr><td>b13</td><td>IC5ADDMT67ZE</td><td>MTU CH67 high-impedance POE11F add bit</td></tr>
<tr><td>b14</td><td>IC6ADDMT67ZE</td><td>MTU CH67 high-impedance POE12F add bit</td></tr>
<tr><td>b15</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td></tr>
</table>

Table 2.18 Differences in Functions and Specifications (18)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="4">Port output enable 3</td><td rowspan="4">Registers/ bits</td><td>• Port output enable control register 5 (POECR5)
<table>
<tr><td>b0</td><td>CMADDMT0ZE</td><td>MTU CH0 high-impedance CFLAG add bit</td></tr>
<tr><td>b1</td><td>IC1ADDMT0ZE</td><td>MTU CH0 high-impedance POE0F add bit</td></tr>
<tr><td>b2</td><td>IC2ADDMT0ZE</td><td>MTU CH0 high-impedance POE4F add bit</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>IC4ADDMT0ZE</td><td>MTU CH0 high-impedance POE10F add bit</td></tr>
<tr><td>b5</td><td>IC5ADDMT0ZE</td><td>MTU CH0 high-impedance POE11F add bit</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7
b15</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Port output enable control register 5 (POECR5)
<table>
<tr><td>b0</td><td>CMADDMT0ZE</td><td>MTU CH0 high-impedance CFLAG add bit</td></tr>
<tr><td>b1</td><td>IC1ADDMT0ZE</td><td>MTU CH0 high-impedance POE0F add bit</td></tr>
<tr><td>b2</td><td>IC2ADDMT0ZE</td><td>MTU CH0 high-impedance POE4F add bit (Reserved bit)</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>IC4ADDMT0ZE</td><td>MTU CH0 high-impedance POE10F add bit</td></tr>
<tr><td>b5</td><td>IC5ADDMT0ZE</td><td>MTU CH0 high-impedance POE11F add bit</td></tr>
<tr><td>b6</td><td>IC6ADDMT0ZE</td><td>MTU CH0 high-impedance POE12F add bit</td></tr>
<tr><td>b7
b15</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td></tr>
<tr><td>• Port output enable control register 6 (POECR6)
<table>
<tr><td>b0</td><td>CMADDGPT01ZE</td><td>GPT CH01 high-impedance CFLAG add bit</td></tr>
<tr><td>b1</td><td>IC1ADDGPT01ZE</td><td>GPT CH01 high-impedance POE0F add bit</td></tr>
<tr><td>b2</td><td>IC2ADDGPT01ZE</td><td>GPT CH01 high-impedance POE4F add bit</td></tr>
<tr><td>b3</td><td>IC3ADDGPT01ZE</td><td>GPT CH01 high-impedance POE8F add bit</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>IC5ADDGPT01ZE</td><td>GPT CH01 high-impedance POE11F add bit</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b8</td><td>CMADDGPT23ZE</td><td>GPT CH23 high-impedance CFLAG add bit</td></tr>
<tr><td>b9</td><td>IC1ADDGPT23ZE</td><td>GPT CH23 high-impedance POE0F add bit</td></tr>
<tr><td>b10</td><td>IC2ADDGPT23ZE</td><td>GPT CH23 high-impedance POE4F add bit</td></tr>
<tr><td>b11</td><td>IC3ADDGPT23ZE</td><td>GPT CH23 high-impedance POE8F add bit</td></tr>
<tr><td>b12</td><td>IC4ADDGPT23ZE</td><td>GPT CH23 high-impedance POE10F add bit</td></tr>
<tr><td>b13</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b14</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b15</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Port output enable control register 6 (POECR6)
<table>
<tr><td>b0</td><td>CMADDGPT01ZE</td><td>GPT CH01 high-impedance CFLAG add bit</td></tr>
<tr><td>b1</td><td>IC1ADDGPT01ZE</td><td>GPT CH01 high-impedance POE0F add bit</td></tr>
<tr><td>b2</td><td>IC2ADDGPT01ZE</td><td>GPT CH01 high-impedance POE4F add bit</td></tr>
<tr><td>b3</td><td>IC3ADDGPT01ZE</td><td>GPT CH01 high-impedance POE8F add bit</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>IC5ADDGPT01ZE</td><td>GPT CH01 high-impedance POE11F add bit</td></tr>
<tr><td>b6</td><td>IC6ADDGPT01ZE</td><td>GPT CH01 high-impedance POE12F add bit</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b8</td><td>CMADDGPT23ZE</td><td>GPT CH23 high-impedance CFLAG add bit</td></tr>
<tr><td>b9</td><td>IC1ADDGPT23ZE</td><td>GPT CH23 high-impedance POE0F add bit</td></tr>
<tr><td>b10</td><td>IC2ADDGPT23ZE</td><td>GPT CH23 high-impedance POE4F add bit</td></tr>
<tr><td>b11</td><td>IC3ADDGPT23ZE</td><td>GPT CH23 high-impedance POE8F add bit</td></tr>
<tr><td>b12</td><td>IC4ADDGPT23ZE</td><td>GPT CH23 high-impedance POE10F add bit</td></tr>
<tr><td>b13</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b14</td><td>IC6ADDGPT23ZE</td><td>GPT CH23 high-impedance POE12F add bit</td></tr>
<tr><td>b15</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td></tr>
<tr><td>—</td><td>• Port output enable control register 7 (POECR7)
• Port output enable control register 8 (POECR8)
• Input level control/status register 6 (ICSR6)</td></tr>
</table>

Table 2.19 Differences in Functions and Specifications (19)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="2">General PWM timer</td><td>Functions</td><td>• Specification overview<table><tr><td>Oscillation anomaly detection function</td><td>It is possible to use the count clock obtained by frequency dividing the system clock (ICLK) to measure the frequency-divided IWDT dedicated low-speed on-chip oscillator clock edges.</td></tr></table></td><td>• Specification overview<table><tr><td>Oscillation anomaly detection function</td><td>It is possible to use the count clock obtained by frequency dividing the timer module clock (PCLKA) to measure the frequency-divided IWDT dedicated low-speed clock (IWDTCLK) edges.</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>• General PWM timer hardware start source select register (GTHSSR)<table><tr><td>b0
b3</td><td>CSHSL0[3:0]</td><td>GPT0.GTCNT hardware counter start source select bits</td></tr><tr><td>b4
b7</td><td>CSHSL1[3:0]</td><td>GPT1.GTCNT hardware counter start source select bits</td></tr><tr><td>b8
b11</td><td>CSHSL2[3:0]</td><td>GPT2.GTCNT hardware counter start source select bits</td></tr><tr><td>b12
b15</td><td>CSHSL3[3:0]</td><td>GPT3.GTCNT hardware counter start source select bits</td></tr></table>• GTHSSR.CSHSL0[3:0], CSHSL1[3:0], CSHSL2[3:0], CSHSL3[3:0]
0000b: AN000 comparator detection
0001b: AN001 comparator detection
0010b: AN002 comparator detection
0011b: Do not use this setting
0100b: AN100 comparator detection
0101b: AN101 comparator detection
0110b: AN102 comparator detection
0111b: Do not use this setting
1000b: GTIOC3A pin input
1001b: GTIOC3B pin input
1010b: GTIOC3A internal output (output compare)
1011b: GTIOC3B internal output (output compare)
1100b: GTETRG pin input</td><td>• General PWM timer hardware start source select register (GTHSSR)<table><tr><td>b0
b3</td><td>CSHSL0[3:0]</td><td>GPT0.GTCNT hardware counter start source select bits</td></tr><tr><td>b4
b7</td><td>CSHSL1[3:0]</td><td>GPT1.GTCNT hardware counter start source select bits</td></tr><tr><td>b8
b11</td><td>CSHSL2[3:0]</td><td>GPT2.GTCNT hardware counter start source select bits</td></tr><tr><td>b12
b15</td><td>CSHSL3[3:0]</td><td>GPT3.GTCNT hardware counter start source select bits</td></tr></table>• GPT.GTHSSR.CSHSL0[3:0], CSHSL1[3:0], CSHSL2[3:0], CSHSL3[3:0]
0000b: AN000 comparator detection
0001b: AN001 comparator detection
0010b: AN002 comparator detection
0011b: Do not use this setting
0100b: AN100 comparator detection
0101b: AN101 comparator detection
0110b: AN102 comparator detection
0111b: Do not use this setting
1000b: GTIOC3A pin input
1001b: GTIOC3B pin input
1010b: GTIOC3A internal output (output compare)*
1011b: GTIOC3B internal output (output compare)*
1100b: GTETRG0 pin input

<table><tr><td>b0
b3</td><td>CSHSL4[3:0]</td><td>GPT4.GTCNT hardware counter start source select bit</td></tr><tr><td>b4
b7</td><td>CSHSL5[3:0]</td><td>GPT5.GTCNT hardware counter start source select bit</td></tr><tr><td>b8
b11</td><td>CSHSL6[3:0]</td><td>GPT6.GTCNT hardware counter start source select bit</td></tr><tr><td>b12
b15</td><td>CSHSL7[3:0]</td><td>GPT7.GTCNT hardware counter start source select bit</td></tr></table>• GPTB.GTHSSR.CSHSL4[3:0], CSHSL5[3:0], CSHSL6[3:0], CSHSL7[3:0]
0000b: AN000 comparator detection
0001b: AN001 comparator detection
0010b: AN002 comparator detection
0011b: Do not use this setting
0100b: AN100 comparator detection
0101b: AN101 comparator detection
0110b: AN102 comparator detection
0111b: Do not use this setting
1000b: GTIOC7A pin input
1001b: GTIOC7B pin input
1010b: GTIOC7A internal output (output compare)*
1011b: GTIOC7B internal output (output compare)*
1100b: GTETRG1 pin input

Note: * “Do not use this setting” is indicated for CSHSL3[3:0] and CSHSL7[3:0].</td></tr>
</table>

Table 2.20 Differences in Functions and Specifications (20)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>General PWM timer</td><td>Registers/ bits</td><td>
• General PWM timer hardware stop/clear source select register (GTHPSR)
<table>
<tr><td>b0
b3</td><td>CSHPL0[3:0]</td><td>GPT0.GTCNT hardware counter stop/clear source select bits</td></tr>
<tr><td>b4
b7</td><td>CSHPL1[3:0]</td><td>GPT1.GTCNT hardware counter stop/clear source select bits</td></tr>
<tr><td>b8
b11</td><td>CSHPL2[3:0]</td><td>GPT2.GTCNT hardware counter stop/clear source select bits</td></tr>
<tr><td>b12
b15</td><td>CSHPL3[3:0]</td><td>GPT3.GTCNT hardware counter stop/clear source select bits</td></tr>
</table>
• GTHPSR.CSHPL0[3:0], CSHPL1[3:0], CSHPL2[3:0], CSHPL3[3:0]
0000b: AN000 comparator detection
0001b: AN001 comparator detection
0010b: AN002 comparator detection
0011b: Do not use this setting
0100b: AN100 comparator detection
0101b: AN101 comparator detection
0110b: AN102 comparator detection
0111b: Do not use this setting
1000b: GTIOC3A pin input
1001b: GTIOC3B pin input
1010b: GTIOC3A internal output (output compare)
1011b: GTIOC3B internal output (output compare)
1100b: GTETRG pin input
</td><td>
• General PWM timer hardware stop/clear source select register (GTHPSR)
<table>
<tr><td>b0
b3</td><td>CSHPL0[3:0]</td><td>GPT0.GTCNT hardware counter stop/clear source select bits</td></tr>
<tr><td>b4
b7</td><td>CSHPL1[3:0]</td><td>GPT1.GTCNT hardware counter stop/clear source select bits</td></tr>
<tr><td>b8
b11</td><td>CSHPL2[3:0]</td><td>GPT2.GTCNT hardware counter stop/clear source select bits</td></tr>
<tr><td>b12
b15</td><td>CSHPL3[3:0]</td><td>GPT3.GTCNT hardware counter stop/clear source select bits</td></tr>
</table>
• GPT.GTHPSR.CSHPL0[3:0], CSHPL1[3:0], CSHPL2[3:0], CSHPL3[3:0]
0000b: AN000 comparator detection
0001b: AN001 comparator detection
0010b: AN002 comparator detection
0011b: Do not use this setting
0100b: AN100 comparator detection
0101b: AN101 comparator detection
0110b: AN102 comparator detection
0111b: Do not use this setting
1000b: GTIOC3A pin input
1001b: GTIOC3B pin input
1010b: GTIOC3A internal output (output compare)*
1011b: GTIOC3B internal output (output compare)*
1100b: GTETRG0 pin input
<table>
<tr><td>b0
b3</td><td>CSHPL4[3:0]</td><td>GPT4.GTCNT hardware counter stop/clear source select bits</td></tr>
<tr><td>b4
b7</td><td>CSHPL5[3:0]</td><td>GPT5.GTCNT hardware counter stop/clear source select bits</td></tr>
<tr><td>b8
b11</td><td>CSHPL6[3:0]</td><td>GPT6.GTCNT hardware counter stop/clear source select bits</td></tr>
<tr><td>b12
b15</td><td>CSHPL7[3:0]</td><td>GPT7.GTCNT hardware counter stop/clear source select bits</td></tr>
</table>
• GPTB.GTHPSR.CSHPL4[3:0], CSHPL5[3:0], CSHPL6[3:0], CSHPL7[3:0]
0000b: AN000 comparator detection
0001b: AN001 comparator detection
0010b: AN002 comparator detection
0011b: Do not use this setting
0100b: AN100 comparator detection
0101b: AN101 comparator detection
0110b: AN102 comparator detection
0111b: Do not use this setting
1000b: GTIOC7A pin input
1001b: GTIOC7B pin input
1010b: GTIOC7A internal output (output compare)*
1011b: GTIOC7B internal output (output compare)*
1100b: GTETRG1 pin input

Note: * “Do not use this setting” is indicated for CSHSL3[3:0] and CSHSL7[3:0].
</td></tr>
</table>

Table 2.21 Differences in Functions and Specifications (21)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>General PWM timer</td><td>Registers/ bits</td><td>

• General PWM timer write-protection register (GTWP)

b0	WP0	GPT0 register write enable bit
b1	WP1	GPT1 register write enable bit
b2	WP2	GPT2 register write enable bit
b3	WP3	GPT3 register write enable bit
b4 b15	—	(Reserved bits)

• General PWM timer sync register (GTSYNC)

b0 b1	SYNC0[1:0]	GPT0.GTCNT counter synchronized-clear source select bits
b2 b3	—	(Reserved bits)
b4 b5	SYNC1[1:0]	GPT1.GTCNT counter synchronized-clear source select bits
b6 b7	—	(Reserved bits)
b8 b9	SYNC2[1:0]	GPT2.GTCNT counter synchronized-clear source select bits
b10 b11	—	(Reserved bits)
b12 b13	SYNC3[1:0]	GPT3.GTCNT counter synchronized-clear source select bits
b14 b15	—	(Reserved bits)

</td><td>

• General PWM timer write-protection register (GTWP)

• GPT.GTWP

b0	WP0	GPT0 register write enable bit
b1	WP1	GPT1 register write enable bit
b2	WP2	GPT2 register write enable bit
b3	WP3	GPT3 register write enable bit
b4 b15	—	(Reserved bits)

• GPTB.GTWP

b0	WP4	GPT4 register write enable bit
b1	WP5	GPT5 register write enable bit
b2	WP6	GPT6 register write enable bit
b3	WP7	GPT7 register write enable bit
b4 b15	—	(Reserved bits)

• General PWM timer sync register (GTSYNC)

• GPT.GTSYNC

b0 b1	SYNC0[1:0]	GPT0.GTCNT counter synchronized-clear source select bits
b2 b3	—	(Reserved bits)
b4 b5	SYNC1[1:0]	GPT1.GTCNT counter synchronized-clear source select bits
b6 b7	—	(Reserved bits)
b8 b9	SYNC2[1:0]	GPT2.GTCNT counter synchronized-clear source select bits
b10 b11	—	(Reserved bits)
b12 b13	SYNC3[1:0]	GPT3.GTCNT counter synchronized-clear source select bits
b14 b15	—	(Reserved bits)

• GPTB.GTSYNC

b0 b1	SYNC4[1:0]	GPT4.GTCNT counter synchronized-clear source select bits
b2 b3	—	(Reserved bits)
b4 b5	SYNC5[1:0]	GPT5.GTCNT counter synchronized-clear source select bits
b6 b7	—	(Reserved bits)
b8 b9	SYNC6[1:0]	GPT6.GTCNT counter synchronized-clear source select bits
b10 b11	—	(Reserved bits)
b12 b13	SYNC7[1:0]	GPT7.GTCNT counter synchronized-clear source select bits
b14 b15	—	(Reserved bits)

</td></tr>
</table>

Table 2.22 Differences in Functions and Specifications (22)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>General PWM timer</td><td>Registers/ bits</td><td>

• General PWM timer start write-protection register (GTSWP)

b0	SWP0	GTSTR.CST0 bit write disable bit
b1	SWP1	GTSTR.CST1 bit write disable bit
b2	SWP2	GTSTR.CST2 bit write disable bit
b3	SWP3	GTSTR.CST3 bit write disable bit
b4 b15	—	(Reserved bits)

• LOCO count control register (LCCR)

b0	LCNTE	LOCO count function enable bit
b1	LCNTCR	LOCO count value clear bit
b2	LCNTS	LOCO count value setting bit
b3	—	(Reserved bit)
b4	LCINTC	Frequency-divided LOCO clock rise interrupt enable bit
b5	LCINTD	LOCO count value deviation exceedance interrupt enable bit
b6	LCINTO	LCNT overflow interrupt enable bit
b7	—	(Reserved bit)
b8 b10	LCTO[2:0]	Frequency-divided LOCO clock rise interrupt skipping count setting bits
b11	LCNTAT	LOCO count result skipping setting bit
b12 b13	TPSC[1:0]	LOCO count clock select bits
b14 b15	LPSC[1:0]	Frequency-divided LOCO clock select bits

LCCR.TPSC[1:0]
00b: ICLK (system clock)
01b: ICLK/2 (system clock/2)
10b: ICLK/4 (system clock/4)
11b: ICLK/8 (system clock/8)

</td><td>

• General PWM timer start write-protection register (GTSWP)

• GPT.GTSWP

b0	SWP0	GTSTR.CST0 bit write disable bit
b1	SWP1	GTSTR.CST1 bit write disable bit
b2	SWP2	GTSTR.CST2 bit write disable bit
b3	SWP3	GTSTR.CST3 bit write disable bit
b4 b15	—	(Reserved bits)

• GPTB.GTSWP

b0	SWP4	GTSTR.CST4 bit write disable bit
b1	SWP5	GTSTR.CST5 bit write disable bit
b2	SWP6	GTSTR.CST6 bit write disable bit
b3	SWP7	GTSTR.CST7 bit write disable bit
b4 b15	—	(Reserved bits)

• LOCO count control register (LCCR)

b0	LCNTE	Count function enable bit
b1	LCNTCR	Count value clear bit
b2	LCNTS	Count value setting bit
b3	—	(Reserved bit)
b4	LCINTC	Frequency-divided IWDTCLK clock rise interrupt enable bit
b5	LCINTD	Count Value deviation exceedance interrupt enable bit
b6	LCINTO	LCNT overflow interrupt enable bit
b7	—	(Reserved bit)
b8 b10	LCTO[2:0]	Frequency-divided IWDTCLK clock rise interrupt skipping count setting bits
b11	LCNTAT	Count result skipping setting bit
b12 b13	TPSC[1:0]	Count clock select bit
b14 b15	LPSC[1:0]	Frequency-divided IWDTCLK clock select bits

LCCR.TPSC[1:0]
00b: PCLKA (timer module clock)
01b: PCLKA/2 (timer module clock/2)
10b: PCLKA/4 (timer module clock/4)
11b: PCLKA/8 (timer module clock/8)

</td></tr>
</table>

Table 2.23 Differences in Functions and Specifications (23)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>General PWM timer</td><td>Registers/ bits</td><td>

• LOCO count status register (LCST)

b0	LISC	Frequency-divided LOCO clock rise interrupt request flag
b1	LISD	LOCO count value deviation exceedance interrupt request flag
b2	LISO	LCNT overflow interrupt request flag

• General PWM timer control register (GTCR)

b0 b2	MD[2:0]	Mode select bits
b3 b7	—	(Reserved bits)
b8 b9	TPCS[1:0]	Timer prescaler select bits
b10 b11	—	(Reserved bits)
b12 b13	CCLR[1:0]	Counter clear source select bits
b14 b15	—	(Reserved bits)

GTCR.CCLR[1:0]
00b: ICLK (system clock)
01b: ICLK/2 (system clock/2)
10b: ICLK/4 (system clock/4)
11b: ICLK/8 (system clock/8)

• General PWM timer interrupt and A/D converter start request skipping setting register (GTITC)

b0	ITLA	GTCCRA compare match/input capture interrupt link bit
b1	ITLB	GTCCRB compare match/input capture interrupt link bit
b2	ITLC	GTCCRC compare match interrupt link bit
b3	ITLD	GTCCRD compare match interrupt link bit
b4	ITLE	GTCCRE compare match interrupt link bit
b5	ITLF	GTCCRF compare match interrupt link bit
b6 b7	IVTC[1:0]	GTCIV interrupt skipping function select bits
b8 b10	IVTT[2:0]	GTCIV interrupt skipping count select bits
b11	—	(Reserved bit)
b12	ADTAL	GTADTRA A/D converter start request link bit
b13	—	(Reserved bit)
b14	ADTBL	GTADTRB A/D converter start request link bit
b15	—	(Reserved bit)

GTITC.IVTC[1:0]
00b: No skipping
01b: Skipping is performed by counting overflows in the case of sawtooth waves and (peaks) in the case of triangle waves.
10b: Skipping is performed by counting underflows in the case of sawtooth waves and (troughs) in the case of triangle waves.
11b: Skipping is performed by counting both overflows and underflows in the case of sawtooth waves and both (troughs and peaks) in the case of triangle waves.

• Dead time control register (GTDTCR)

</td><td>

• LOCO count status register (LCST)

b0	LISC	Frequency-divided IWDTCLK clock rise interrupt request flag
b1	LISD	IWDTCLK count value deviation exceedance interrupt request flag
b2	LISO	LCNT overflow interrupt request flag

• General PWM timer control register (GTCR)

b0 b2	MD[2:0]	Mode select bits
b3 b7	—	(Reserved bits)
b8 b9	TPCS[1:0]	Timer prescaler select bits
b10 b11	—	(Reserved bits)
b12 b13	CCLR[1:0]	Counter clear source select bits
b14 b15	—	(Reserved bits)

GTCR.CCLR[1:0]
00b: PCLKA (timer module clock)
01b: PCLKA/2 (timer module clock/2)
10b: PCLKA/4 (timer module clock/4)
11b: PCLKA/8 (timer module clock/8)

• General PWM timer interrupt and A/D converter start request skipping setting register (GTITC)

b0	ITLA	GTCCRA compare match/input capture interrupt link bit
b1	ITLB	GTCCRB compare match/input capture interrupt link bit
b2	ITLC	GTCCRC compare match interrupt link bit
b3	ITLD	GTCCRD compare match interrupt link bit
b4	ITLE	GTCCRE compare match interrupt link bit
b5	ITLF	GTCCRF compare match interrupt link bit
b6 b7	IVTC[1:0]	GTCIV interrupt skipping function select bits
b8 b10	IVTT[2:0]	GTCIV interrupt skipping count select bits
b11	—	(Reserved bit)
b12	ADTAL	GTADTRA A/D converter start request link bit
b13	—	(Reserved bit)
b14	ADTBL	GTADTRB A/D converter start request link bit
b15	—	(Reserved bit)

GTITC.IVTC[1:0]
00b: No skipping
01b: Skipping is performed by counting both overflows and underflows in the case of sawtooth waves and (peaks) in the case of triangle waves.
10b: Skipping is performed by counting both overflows and underflows in the case of sawtooth waves and (troughs) in the case of triangle waves.
11b: Skipping is performed by counting both overflows and underflows in the case of sawtooth waves and both (troughs and peaks) in the case of triangle waves.

• General PWM timer dead time control register (GTDTCR)

</td></tr>
</table>

Table 2.24 Differences in Functions and Specifications (24)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="2">Watchdog timer</td><td>Functions</td><td>• Specification overview<table><tr><td>Clock division ratio</td><td>Divide by 4, 64, 128, 512, 2048, 8192, 32768, or 131072</td></tr><tr><td>Number of bits</td><td>8</td></tr><tr><td>Operating mode</td><td>Watchdog timer mode</td></tr><tr><td></td><td>Interval timer mode</td></tr><tr><td>Operation start mode</td><td>—</td></tr><tr><td></td><td>Register start mode</td></tr><tr><td>—</td><td>—</td></tr><tr><td>Output signals</td><td>WDTOVF# signal output (external)</td></tr><tr><td></td><td>Reset signal (internal)</td></tr><tr><td></td><td>Interval timer interrupt</td></tr></table></td><td>• Specification overview<table><tr><td>Clock division ratio</td><td>Divide by 4, 64, 128, 512, 2048, or 8192</td></tr><tr><td>Number of bits</td><td>14</td></tr><tr><td>Operating mode</td><td>Watchdog timer mode</td></tr><tr><td></td><td>—</td></tr><tr><td>Operation start mode</td><td>Auto-start mode</td></tr><tr><td></td><td>Register start mode</td></tr><tr><td>Window function</td><td>Support for setting window start and end positions</td></tr><tr><td>Output signals</td><td>—</td></tr><tr><td></td><td>Reset signal (internal)</td></tr><tr><td></td><td>Interrupt request signal</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>• Timer counter (TCNT)
• Timer control/status register (TCSR)
• Reset control/status register (RSTCSR)
• Write window A register (WINA)
• Write window B register (WINB)
—</td><td>—
• WDT refresh register (WDTRR)
• WDT control register (WDTCR)
• WDT status register (WDTSR)
• WDT reset control register (WDTRCR)</td></tr>
</table>

Table 2.25 Differences in Functions and Specifications (25)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="2">Independent watchdog timer</td><td>Functions</td><td>• Specification overview<table><tr><td>Number of bits</td><td>14</td></tr><tr><td>Operating mode</td><td>Watchdog timer mode</td></tr><tr><td>Operation start mode</td><td>—
Register start mode</td></tr><tr><td>Window function</td><td>—</td></tr><tr><td>Output signals</td><td>Reset signal (internal)
—</td></tr></table></td><td>• Specification overview<table><tr><td>Number of bits</td><td>14</td></tr><tr><td>Operating mode</td><td>Watchdog timer mode</td></tr><tr><td>Operation start mode</td><td>Auto-start mode
Register start mode</td></tr><tr><td>Window function</td><td>Support for setting window start and end positions</td></tr><tr><td>Output signals</td><td>Reset signal (internal)
Interrupt request signal</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>• IWDT control register (IWDTCR)<table><tr><td>b0
b1</td><td>TOPS[1:0]</td><td>Time-out selection bits</td></tr><tr><td>b2
b3</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b4
b7</td><td>CKS[3:0]</td><td>Clock selection bits</td></tr><tr><td>b8
b9</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b12
b13</td><td>—</td><td>(Reserved bits)</td></tr></table>• IWDTCR.CKS[3:0]
00--b: IWDTCLK
0100b: IWDTCLK/16
0101b: IWDTCLK /32
0110b: IWDTCLK /64
0111b: IWDTCLK/128
1---b: IWDTCLK/256
• IWDT status register (IWDTSR)<table><tr><td>b0
b13</td><td>CNTVAL[13:0]</td><td>Down-counter bits</td></tr><tr><td>b14</td><td>UNDFF</td><td>Underflow flag</td></tr><tr><td>b15</td><td>—</td><td>(Reserved bit)</td></tr></table>—</td><td>• IWDT control register (IWDTCR)<table><tr><td>b0
b1</td><td>TOPS[1:0]</td><td>Time-out period selection bits</td></tr><tr><td>b2
b3</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b4
b7</td><td>CKS[3:0]</td><td>Clock division ratio selection bits</td></tr><tr><td>b8
b9</td><td>RPES[1:0]</td><td>Window end position selection bits</td></tr><tr><td>b12
b13</td><td>RPSS[1:0]</td><td>Window start position selection bits</td></tr></table>• IWDTCR.CKS[3:0]
0000b: IWDTCLK
0010b: IWDTCLK/16
0011b: IWDTCLK /32
0100b: IWDTCLK /64
1111b: IWDTCLK/128
0101b: IWDTCLK/256
Setting prohibited other than above
• IWDT status register (IWDTSR)<table><tr><td>b0
b13</td><td>CNTVAL[13:0]</td><td>Down-counter value bits</td></tr><tr><td>b14</td><td>UNDFF</td><td>Underflow flag</td></tr><tr><td>b15</td><td>REFEF</td><td>Refresh error flag</td></tr></table>• IWDT reset control register (IWDTRCR)
• IWDT count stop control register (IWDTCSTPR)</td></tr>
<tr><td>USB 2.0 Host/function module</td><td>Registers/ bits</td><td>—</td><td>• System configuration control register (SYSCFG)
• System configuration status register 0 (SYSSTS0)
• Device state control register 0 (DVSTCTR0)
• CFIFO port register (CFIFO)
• D0FIFO port register (D0FIFO)
• D1FIFO port register (D1FIFO)
• CFIFO port select register (CFIFOSEL)
• D0FIFO port select register (D0FIFOSEL)
• D1FIFO port select register (D1FIFOSEL)
• CFIFO port control register (CFIFOCTR)
• D0FIFO port control register (D0FIFOCTR)
• D1FIFO port control register (D1FIFOCTR)
• Interrupt enable register 0 (INTENB0)
• Interrupt enable register 1 (INTENB1)
• BRDY interrupt enable register (BRDYENB)
• NRDY interrupt enable register (NRDYENB)
• BEMP interrupt enable register (BEMPENB)</td></tr>
</table>

Table 2.26 Differences in Functions and Specifications (26)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>USB 2.0 Host/function module</td><td>Registers/ bits</td><td>—</td><td>• SOF output configuration register (SOFCFG)
• Interrupt status register 0 (INTSTS0)
• Interrupt status register 1 (INTSTS1)
• BRDY interrupt status register (BRDYSTS)
• NRDY interrupt status register (NRDYSTS)
• BEMP interrupt status register (BEMPSTS)
• Frame number register (FRMNUM)
• Device state change register (DVCHGR)
• USB address register (USBADDR)
• USB request type register (USBREQ)
• USB request value register (USBVAL)
• USB request index register (USBINDX)
• USB request length register (USBLENG)
• DCP configuration register (DCPCFG)
• DCP maximum packet size register (DCPMAXP)
• DCP control register (DCPCTR)
• Pipe window select register (PIPESEL)
• Pipe configuration register (PIPECFG)
• Pipe maximum packet size register (PIPEMAXP)
• Pipe cycle control register (PIPEPERI)
• PIPEn control registers (PIPEnCTR)
• PIPEn transaction counter enable registers (PIPEnTRE)
• PIPEn transaction counter registers (PIPEnTRN)
• Device address n configuration registers (DEVADDn)</td></tr>
<tr><td rowspan="2">Serial communications interface</td><td>Functions</td><td>• Specification overview (SCIb)<table><tr><td>Serial communication modes</td><td>Asynchronous
Clock synchronous
Smart card interface
—
—</td></tr></table></td><td>• Specification overview (SCIc)<table><tr><td>Serial communication modes</td><td>Asynchronous
Clock synchronous
Smart card interface
Simple I²C bus (MSB-first only)
Simple I²C bus</td></tr><tr><td>Hardware flow control</td><td>Asynchronous
Clock synchronous</td></tr></table>• Specification overview (SCId)<table><tr><td>Serial communication modes</td><td>Asynchronous
Clock synchronous
Smart card interface
Simple I²C bus (MSB-first only)
Simple I²C bus</td></tr><tr><td>Hardware flow control</td><td>Asynchronous
Clock synchronous</td></tr><tr><td>Extended serial mode</td><td>Start frame transmission/reception, timer function</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>• Serial mode register (SMR)
The channel name is SMCI when the SMIF bit in SCMR is set to 1.</td><td>—</td></tr>
</table>

Table 2.27 Differences in Functions and Specifications (27)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="4">Serial communications interface</td><td rowspan="4">Registers/ bits</td><td>
• Serial status register (SSR)
SCMR.SMIF bit = 0, 1
<table>
<tr><td>b0</td><td>MPBT</td><td>Multi-processor bit transfer bit</td></tr>
<tr><td>b1</td><td>MPB</td><td>Multi-processor bit</td></tr>
<tr><td>b2</td><td>TEND</td><td>Transmit end flag</td></tr>
<tr><td>b3</td><td>PER</td><td>Parity error flag</td></tr>
<tr><td>b4</td><td>FER</td><td>Framing error flag</td></tr>
<tr><td>b5</td><td>ORER</td><td>Overrun error flag</td></tr>
<tr><td>b6</td><td>RDRF</td><td>Receive data full flag</td></tr>
<tr><td>b7</td><td>TDRE</td><td>Transmit data empty flag</td></tr>
</table>
</td><td>
• Serial status register (SSR)
SCMR.SMIF bit = 0, 1
<table>
<tr><td>b0</td><td>MPBT</td><td>Multi-processor bit transfer bit</td></tr>
<tr><td>b1</td><td>MPB</td><td>Multi-processor bit</td></tr>
<tr><td>b2</td><td>TEND</td><td>Transmit end flag</td></tr>
<tr><td>b3</td><td>PER</td><td>Parity error flag</td></tr>
<tr><td>b4</td><td>FER</td><td>Framing error flag</td></tr>
<tr><td>b5</td><td>ORER</td><td>Overrun error flag</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
</table>
</td></tr>
<tr><td>
• Serial extended mode register (SEMR)
<table>
<tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>ABCS</td><td>Asynchronous mode clock source select bit</td></tr>
<tr><td>b5</td><td>NFEN</td><td>Noise Cancelling Function Select bit</td></tr>
</table>
</td><td>
• Serial extended mode register (SEMR)
<table>
<tr><td>b0</td><td>ACS0</td><td>Asynchronous mode clock source select bit</td></tr>
<tr><td>b4</td><td>ABCS</td><td>Asynchronous mode base clock select bit</td></tr>
<tr><td>b5</td><td>NFEN</td><td>Digital noise filter function enable bit</td></tr>
</table>
</td></tr>
<tr><td>—</td><td>
• Noise filter setting register (SNFR)
• I²C mode register 1 (SIMR1)
• I²C mode register 2 (SIMR2)
• I²C mode register 3 (SIMR3)
• I²C status register (SISR)
• SPI mode register (SPMR)
• Extended serial module enable register (ESMER)
• Control register 0 (CR0)
• Control register 1 (CR1)
• Control register 2 (CR2)
• Control register 3 (CR3)
• Port control register (PCR)
• Interrupt control register (ICR)
• Status register (STR)
• Status clear register (STCR)
• Control field 0 data register (CF0DR)
• Control field 0 compare enable register (CF0CR)
• Control field 0 receive data register (CF0RR)
• Primary control field 1 data register (PCF1DR)
</td></tr>
</table>

Table 2.28 Differences in Functions and Specifications (28)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>Serial communications interface</td><td>Registers/ bits</td><td>—</td><td>• Secondary control field 1 data register (SCF1DR)
• Control field 1 compare enable register (CF1CR)
• Control field 1 receive data register (CF1RR)
• Timer control register (TCR)
• Timer mode register (TMR)
• Timer prescaler register (TPRE)
• Timer count register (TCNT)</td></tr>
<tr><td>CAN module</td><td>Registers/ bits</td><td>• Bit configuration register (BCR)<table><tr><th>b0</th><th>—</th><th>(Reserved bit)</th></tr><tr><td>b8
b10</td><td>TSEG2[2:0]</td><td>Time segment 2 control bits</td></tr><tr><td>b12
b13</td><td>SJW[1:0]</td><td>Resynchronization jump width control bits</td></tr><tr><td>b16
b25</td><td>BRP[9:0]</td><td>Prescaler division ratio select bits</td></tr><tr><td>b28
b31</td><td>TSEG1[3:0]</td><td>Time segment 1 control bits</td></tr></table></td><td>• Bit configuration register (BCR)<table><tr><th>b0</th><th>CCLKS</th><th>CAN clock source selection bit</th></tr><tr><td>b8
b10</td><td>TSEG2[2:0]</td><td>Time segment 2 control bits</td></tr><tr><td>b12
b13</td><td>SJW[1:0]</td><td>Resynchronization jump width control bits</td></tr><tr><td>b16
b25</td><td>BRP[9:0]</td><td>Prescaler division ratio select bits</td></tr><tr><td>b28
b31</td><td>TSEG1[3:0]</td><td>Time segment 1 control bits</td></tr></table></td></tr>
</table>

Table 2.29 Differences in Functions and Specifications (29)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="4">Serial peripheral interface</td><td>Functions</td><td>• Specification overview
<table><tr><td>Number of channels</td><td>One channel</td></tr></table></td><td>• Specification overview
<table><tr><td>Number of channels</td><td>Two channels</td></tr></table></td></tr>
<tr><td rowspan="3">Registers/ bits</td><td>• RSPI status register (SPSR)
<table><tr><td>b0</td><td>OVRF</td><td>Overrun error flag</td></tr><tr><td>b1</td><td>IDLNF</td><td>RSPI idle flag</td></tr><tr><td>b2</td><td>MODF</td><td>Mode fault error flag</td></tr><tr><td>b3</td><td>PERF</td><td>Parity error flag</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>SPTEF</td><td>Transmit buffer empty flag</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>SPRF</td><td>Receive buffer full flag</td></tr></table></td><td>• RSPI status register (SPSR)
<table><tr><td>b0</td><td>OVRF</td><td>Overrun error flag</td></tr><tr><td>b1</td><td>IDLNF</td><td>RSPI idle flag</td></tr><tr><td>b2</td><td>MODF</td><td>Mode fault error flag</td></tr><tr><td>b3</td><td>PERF</td><td>Parity error flag</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
<tr><td>• RSPI data register (SPDR)
<table><tr><td>b0
b15</td><td>L[15:0]</td><td>—</td></tr><tr><td>b16
b31</td><td>H[15:0]</td><td>—</td></tr></table></td><td>• RSPI data register (SPDR)
<table><tr><td>b0

b31</td><td>SPD0

SPD31</td><td>—</td></tr></table></td></tr>
<tr><td>• RSPI data control register (SPDCR)
<table><tr><td>b0
b1</td><td>SPFC[1:0]</td><td>Number of frames specification bits</td></tr><tr><td>b2
b3</td><td>SLSEL[1:0]</td><td>SSL pin output selection bits</td></tr><tr><td>b4</td><td>SPRDTD</td><td>RSPI receive/transmit data selection bit</td></tr><tr><td>b5</td><td>SPLW</td><td>RSPI longword access/word access specification bit</td></tr><tr><td>b6
b7</td><td>—</td><td>(Reserved bits)</td></tr></table></td><td>• RSPI data control register (SPDCR)
<table><tr><td>b0
b1</td><td>SPFC[1:0]</td><td>Number of frames specification bits</td></tr><tr><td>b2
b3</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b4</td><td>SPRDTD</td><td>RSPI receive/transmit data selection bit</td></tr><tr><td>b5</td><td>SPLW</td><td>RSPI longword access/word access specification bit</td></tr><tr><td>b6
b7</td><td>—</td><td>(Reserved bits)</td></tr></table></td></tr>
<tr><td>LIN module</td><td>Registers/ bits</td><td>• LIN wake-up baud rate select register (LWBR)
• LIN baud rate prescaler 0 register (LBRP0)
• LIN baud rate prescaler 1 register (LBRP1)
• LIN self-test control register (LSTC)
• Mode register (L0MD)
• Break field setting register (L0BRK)
• Space setting register (L0SPC)
• Wake-up setting register (L0WUP)
• Interrupt enable register (L0IE)
• Error detection enable register (L0EDE)
• Control register (L0C)
• Transmission control register (L0TC)
• Mode status register (L0MST)
• Status register (L0ST)
• Error status register (L0EST)
• Response field set register (L0RFC)
• ID buffer register (L0IDB)
• Check sum buffer register (L0CBR)
• Data n buffer register (L0DBn) (n = 1 to 8)</td><td>—</td></tr>
</table>

Table 2.30 Differences in Functions and Specifications (30)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="2">12-bit A/D converter</td><td>Functions</td><td>
• Specification overview
<table>
<tr><td>Input channels</td><td>(1 unit × 4 channels) × 2</td></tr>
<tr><td>Conversion time</td><td>1.0 μs per 1 channel (when operating with A/D conversion clock ADCLK = 50 MHz and AVCC = 4.0 to 5.5V)
2.0 μs per 1 channel (when operating with A/D conversion clock ADCLK = 25 MHz and AVCC = 3.0 to 3.6V)</td></tr>
<tr><td>A/D conversion clock</td><td>PCLK, PCLK/2, PCLK/4, PCLK/8</td></tr>
<tr><td>Data registers</td><td>10 registers (S12AD0.ADDR0A, ADDR0B, S12AD0ADDR1 to S12AD0ADDR3)
8-, 10-, or 12-bit precision output of A/D conversion results</td></tr>
<tr><td>Operating mode</td><td>Single mode
Single-cycle scan mode
Continuous scan mode
2-channel scan mode</td></tr>
<tr><td>Start trigger</td><td>Software trigger
MTU3
GPT
External trigger (ADTRG0# pin)
External trigger (ADTRG1# pin)</td></tr>
<tr><td>Function</td><td>Sample and hold function
A/D converter self-diagnostic function
Input signal amplification function using programmable gain amplifier (3 channels/1 unit)
Window comparator function (3 channels/1 unit)
Variable sampling state (unit)
—
—
—
Double data register function</td></tr>
</table>
</td><td>
• Specification overview
<table>
<tr><td>Input channels</td><td>(1 unit × 4 channels) × 2</td></tr>
<tr><td>Conversion time</td><td>1.0 μs per 1 channel (when operating with A/D conversion clock ADCLK = 50 MHz)</td></tr>
<tr><td>A/D conversion clock</td><td>The following frequency ratios may be specified for PCLKB and ADCLK:
PCLKB:ADCLK = 1:1, 1:2, 1:4, or 1:8.</td></tr>
<tr><td>Data registers</td><td>14 registers (ADDR0 to ADDR3, ADDBLDR, ADDBLDRA, ADDBLDRB)
8-, 10-, or 12-bit precision output of A/D conversion results</td></tr>
<tr><td>Operating mode</td><td>—
Single-cycle scan mode
Continuous scan mode
Group scan mode</td></tr>
<tr><td>Start trigger</td><td>Software trigger
MTU3
GPT
External trigger (ADTRG0# pin)
External trigger (ADTRG1# pin)</td></tr>
<tr><td>Function</td><td>Channel (dedicated) sample and hold function
A/D converter self-diagnostic function
Input signal amplification function using programmable gain amplifier (3 channels/1 unit)
Window comparator function (3 channels/unit)
Variable sampling state (channel)
A/D conversion value addition
Discharge function
Double trigger mode (A/D conversion data redundancy function)
Double trigger mode extension</td></tr>
</table>
</td></tr>
<tr><td>Registers/ bits</td><td>
• A/D data registers n (ADDRn) (n = 0A, 0B, and 1 to 3)
—
• A/D data register diag (ADRD)
• A/D control register (ADCSR)
<table>
<tr><td>—</td><td>—</td><td>—</td></tr>
<tr><td>—</td><td>—</td><td>—</td></tr>
<tr><td>—</td><td>—</td><td>—</td></tr>
<tr><td>—</td><td>—</td><td>—</td></tr>
<tr><td>b0</td><td>EXTRG</td><td>Trigger select bit</td></tr>
<tr><td>b1</td><td>TRGE</td><td>Trigger enable bit</td></tr>
<tr><td>b2 b3</td><td>CKS[1:0]</td><td>Clock select bits</td></tr>
<tr><td>b4</td><td>ADIE</td><td>A/D conversion end interrupt enable bit</td></tr>
<tr><td>b5 b6</td><td>ADCS[1:0]</td><td>A/D conversion mode select bits</td></tr>
<tr><td>b7</td><td>ADST</td><td>A/D start bit</td></tr>
</table>
ADCSR.ADCS[1:0]
00b: Single mode
01b: Single-cycle scan mode
10b: Continuous scan mode
11b: 2-channel scan mode
</td><td>
• A/D data registers y (ADDRy)
• A/D data-doubling register (ADDBLDR)
• A/D data-doubling register A (ADDBLDRA)
• A/D data-doubling register B (ADDBLDRB)
• A/D self-diagnosis data register (ADRD)
• A/D control register (ADCSR)
<table>
<tr><td>b0 b4</td><td>DBLANS[4:0]</td><td>Double-trigger channel select bits</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>GBADIE</td><td>Group B scan end interrupt enable bit</td></tr>
<tr><td>b7</td><td>DBLE</td><td>Double Trigger mode select bit</td></tr>
<tr><td>b8</td><td>EXTRG</td><td>Trigger select bit</td></tr>
<tr><td>b9</td><td>TRGE</td><td>Trigger start enable bit</td></tr>
<tr><td>b10 b11</td><td>—</td><td>(Reserved bits)</td></tr>
<tr><td>b12</td><td>ADIE</td><td>Scan end interrupt enable bit</td></tr>
<tr><td>b13 b14</td><td>ADCS[1:0]</td><td>Scan mode select bits</td></tr>
<tr><td>b15</td><td>ADST</td><td>A/D conversion start bit</td></tr>
</table>
ADCSR.ADCS[1:0]
00b: Single-cycle scan mode
01b: Group scan mode
10b: Continuous scan mode
11b: Setting prohibited
</td></tr>
</table>

Table 2.31 Differences in Functions and Specifications (31)

Item		RX62T Group	RX63T Group
12-bit A/D converter	Registers/ bits	• A/D channel select register (ADANS) unit 0 b0 PG000EN AN000 programmable gain amplifier enable bit b1 PG001EN AN001 programmable gain amplifier enable bit b2 PG002EN AN002 programmable gain amplifier enable bit b3 to b7 — (Reserved bits) b8 PG000SEL AN000 programmable gain amplifier select bit b9 PG001SEL AN001 programmable gain amplifier select bit b10 PG002SEL AN002 programmable gain amplifier select bit b11 — (Reserved bit) b12, b13 CH[1:0] Channel set bits b14 — (Reserved bit) b15 — (Reserved bit)	• A/D channel select register A (ADANSA) b0 to b3 ANSA[3:0] A/D conversion channels select bits b4 to b7 — (Reserved bits) b8 PG000EN Programmable gain amplifier for AN000 enable bit b9 PG001EN Programmable gain amplifier for AN001 enable bit b10 PG002EN Programmable gain amplifier for AN002 enable bit b11 — (Reserved bit) b12 PG000SEL Programmable gain amplifier for AN000 select bit b13 PG001SEL Programmable gain amplifier for AN001 select bit b14 PG002SEL Programmable gain amplifier for AN002 select bit b15 — (Reserved bit)
		• A/D channel select register (ADANS) unit 1 b0 PG100EN AN100 programmable gain amplifier enable bit b1 PG101EN AN101 programmable gain amplifier enable bit b2 PG102EN AN102 programmable gain amplifier enable bit b3 to b7 — (Reserved bits) b8 PG100SEL AN100 programmable gain amplifier select bit b9 PG101SEL AN101 programmable gain amplifier select bit b10 PG102SEL AN102 programmable gain amplifier select bit b11 — (Reserved bit) b12, b13 CH[1:0] Channel set bits b14, b15 — (Reserved bits)	• A/D channel select register B (ADANSB) b0 to b3 ANSB[3:0] A/D conversion channels select bits b4 to b15 — (Reserved bits)
		—	• A/D-converted value addition mode select register (ADADS) • A/D-converted value addition count select register (ADADC)
		• A/D control extended register (ADCER) b0 SHBYP Dedicated sample-and hold circuit select bit b1, b2 ADPRC[1:0] A/D Data register bit precision set bits b3 — (Reserved bit) b4 — (Reserved bit) b5 ACE Automatic clearing enable bit b8, b9 DIAGVAL[1:0] Self diagnostic voltage select bits b10 DIAGLD Self diagnostic mode select bit b11 DIAGM Self diagnostic enable bit b12 ADIE2 2-channel scan interrupt select bit b13 ADIEW Double trigger interrupt select bit b14 — (Reserved bit) b15 ADRFMT A/D data register format select bit	• A/D control extended register (ADCER) b0 — (Reserved bit) b1, b2 ADPRC[1:0] A/D data-register bit-precision specification bit b3 — (Reserved bit) b4 DCE Discharge enable bit b5 ACE Automatic clearing enable bit b8, b9 DIAGVAL[1:0] Conversion voltage select for self diagnosis bits b10 DIAGLD Self-diagnosis mode select bit b11 DIAGM Self-diagnosis enable bit b12 to b14 — (Reserved bits) b15 ADRFMT A/D data register format select bit

Table 2.32 Differences in Functions and Specifications (32)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="5">12-bit A/D converter</td><td rowspan="5">Registers/ bits</td><td>• A/D start trigger select register (ADSTRGR)
<table>
<tr><td>b0
b4</td><td>ADSTRS0[4:0]</td><td>A/D start trigger group 0 select bits</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b8
b12</td><td>ADSTRS1[4:0]</td><td>A/D start trigger group 1 select bits</td></tr>
<tr><td>b13</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• A/D start trigger select register (ADSTRGR)
<table>
<tr><td>b0
b5</td><td>TRSB[5:0]</td><td>A/D conversion start trigger select for group B bits</td></tr>
<tr><td>b8
b13</td><td>TRSA[5:0]</td><td>A/D conversion start trigger select bits</td></tr>
</table></td></tr>
<tr><td>• A/D programmable gain amplifier register (ADPG)
<table>
<tr><td>b0
b3</td><td>PG000GAIN [3:0]</td><td>Gain select for AN000 programmable gain amplifier bits</td></tr>
<tr><td>b4
b7</td><td>PG001GAIN [3:0]</td><td>Gain select for AN001 programmable gain amplifier bits</td></tr>
<tr><td>b8
b11</td><td>PG002GAIN [3:0]</td><td>Gain select for AN002 programmable gain amplifier bits</td></tr>
</table></td><td>• A/D programmable gain amplifier register (ADPG)
<table>
<tr><td>b0
b3</td><td>PG0GAIN</td><td>Programmable gain amplifier 0 gain select bits</td></tr>
<tr><td>b4
b7</td><td>PG1GAIN</td><td>Programmable gain amplifier 1 gain select bits</td></tr>
<tr><td>b8
b11</td><td>PG2GAIN</td><td>Programmable gain amplifier 2 gain select bits</td></tr>
</table></td></tr>
<tr><td>• Comparator operating mode selection register 0 (ADCMPMD0)
<table>
<tr><td>b0
b1</td><td>CEN000[1:0]</td><td>AN000 comparator select bits</td></tr>
<tr><td>b2
b3</td><td>CEN001[1:0]</td><td>AN001 comparator select bits</td></tr>
<tr><td>b4
b5</td><td>CEN002[1:0]</td><td>AN002 comparator select bits</td></tr>
<tr><td>b8
b9</td><td>CEN100[1:0]</td><td>AN100 comparator select bits</td></tr>
<tr><td>b10
b11</td><td>CEN101[1:0]</td><td>AN101 comparator select bits</td></tr>
<tr><td>b12
b13</td><td>CEN102[1:0]</td><td>AN102 comparator select bits</td></tr>
</table></td><td>• Comparator operating mode selection register 0 (ADCMPMD0)
<table>
<tr><td>b0
b1</td><td>CEN000[1:0]</td><td>Comparator selection bits for AN000/AN100</td></tr>
<tr><td>b2
b3</td><td>CEN001[1:0]</td><td>Comparator selection bits for AN001/AN101</td></tr>
<tr><td>b4
b5</td><td>CEN002[1:0]</td><td>Comparator selection bits for AN002/AN102</td></tr>
<tr><td>b8
b13</td><td>—</td><td>(Reserved bits)</td></tr>
</table></td></tr>
<tr><td>• Comparator operating mode selection register 1 (ADCMPMD1)
<table>
<tr><td>b0
b2</td><td>REFL[2:0]</td><td>Internal voltage select for comparator low reference voltage bits</td></tr>
<tr><td>b4
b6</td><td>REFH[2:0]</td><td>Internal voltage select for comparator high reference voltage bits</td></tr>
<tr><td>b8</td><td>CSEL0</td><td>AN000 to AN002 comparator input select bit</td></tr>
<tr><td>b9</td><td>VSELH0</td><td>AN000 to AN002 comparator high reference voltage select bit</td></tr>
<tr><td>b10</td><td>VSELL0</td><td>AN000 to AN002 comparator low reference voltage select bit</td></tr>
<tr><td>b11</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b12</td><td>CSEL1</td><td>AN100 to AN102 comparator input select bit</td></tr>
<tr><td>b13</td><td>VSELH1</td><td>AN100 to AN102 comparator high reference voltage select bit</td></tr>
<tr><td>b14</td><td>VSELL1</td><td>AN100 to AN102 comparator low reference voltage select bit</td></tr>
<tr><td>b15</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Comparator operating mode selection register 1 (ADCMPMD1)
<table>
<tr><td>b0
b2</td><td>REFL[2:0]</td><td>Comparator low-side reference-voltage internal-voltage selection bits</td></tr>
<tr><td>b4
b6</td><td>REFH[2:0]</td><td>Comparator high-side reference-voltage internal-voltage selection bits</td></tr>
<tr><td>b8</td><td>CSEL0</td><td>Comparator input selection bit</td></tr>
<tr><td>b9</td><td>VSELH0</td><td>Comparator high-side reference-voltage selection bit</td></tr>
<tr><td>b10</td><td>VSELL0</td><td>Comparator low-side reference-voltage selection bit</td></tr>
<tr><td>b11
b15</td><td>—</td><td>(Reserved bits)</td></tr>
</table></td></tr>
<tr><td>• Comparator filter mode register 0 (ADCMPNR0)
<table>
<tr><td>b0
b3</td><td>C000NR[3:0]</td><td>AN000 comparator noise cancellation filter mode select bits</td></tr>
<tr><td>b4
b7</td><td>C001NR[3:0]</td><td>AN001 comparator noise cancellation filter mode select bits</td></tr>
<tr><td>b8
b11</td><td>C002NR[3:0]</td><td>AN002 comparator noise cancellation filter mode select bits</td></tr>
</table></td><td>• Comparator filter mode register 0 (ADCMPNR0)
<table>
<tr><td>b0
b3</td><td>C000NR[3:0]</td><td>Comparator noise-cancelling filter mode selection bits for AN000/AN100</td></tr>
<tr><td>b4
b7</td><td>C001NR[3:0]</td><td>Comparator noise-cancelling filter mode selection bits for AN001/AN101</td></tr>
<tr><td>b8
b11</td><td>C002NR[3:0]</td><td>Comparator noise-cancelling filter mode selection bits for AN002/AN102</td></tr>
</table></td></tr>
<tr><td>• Comparator filter mode register 1 (ADCMPNR1)</td><td>—</td></tr>
</table>

Table 2.33 Differences in Functions and Specifications (33)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="4">12-bit A/D converter</td><td rowspan="4">Registers/ bits</td><td>• Comparator detection flag register (ADCMPFR)
<table><tr><td>b0</td><td>C000FLAG</td><td>AN000 comparator detection flag</td></tr><tr><td>b1</td><td>C001FLAG</td><td>AN001 comparator detection flag</td></tr><tr><td>b2</td><td>C002FLAG</td><td>AN002 comparator detection flag</td></tr><tr><td>b3</td><td>C100FLAG</td><td>AN100 comparator detection flag</td></tr><tr><td>b4</td><td>C101FLAG</td><td>AN101 comparator detection flag</td></tr><tr><td>b5</td><td>C102FLAG</td><td>AN102 comparator detection flag</td></tr></table></td><td>• Comparator detection flag register (ADCMPFR)
<table><tr><td>b0</td><td>C000FLAG</td><td>Comparator detection flag for AN000/AN100</td></tr><tr><td>b1</td><td>C001FLAG</td><td>Comparator detection flag for AN001/AN101</td></tr><tr><td>b2</td><td>C002FLAG</td><td>Comparator detection flag for AN002/AN102</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>B5</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
<tr><td>• Comparator interrupt select register (ADCMPSEL)
<table><tr><td>b0</td><td>SEL000</td><td>AN000 comparator detection select bit</td></tr><tr><td>b1</td><td>SEL001</td><td>AN001 comparator detection select bit</td></tr><tr><td>b2</td><td>SEL002</td><td>AN002 comparator detection select bit</td></tr><tr><td>b3</td><td>SEL100</td><td>AN100 comparator detection select bit</td></tr><tr><td>b4</td><td>SEL101</td><td>AN101 comparator detection select bit</td></tr><tr><td>b5</td><td>SEL102</td><td>AN102 comparator detection select bit</td></tr><tr><td>b8</td><td>IE</td><td>Interrupt enable bit</td></tr><tr><td>b9</td><td>POERQ</td><td>POE request set bit</td></tr><tr><td>b10</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• Comparator interrupt select register (ADCMPSEL)
<table><tr><td>b0</td><td>IE000</td><td>Comparator detection-interrupt (CMP0/CMP4) enable bit for AN000/AN100</td></tr><tr><td>b1</td><td>IE001</td><td>Comparator detection-interrupt (CMP1/CMP5) enable bit for AN001/AN101</td></tr><tr><td>b2</td><td>IE002</td><td>Comparator detection-interrupt (CMP2/CMP6) enable bit for AN002/AN102</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b8</td><td>POERQ000</td><td>POE request generation on comparator detection setting bit for AN000/AN100</td></tr><tr><td>b9</td><td>POERQ001</td><td>POE request generation on comparator detection setting bit for AN001/AN101</td></tr><tr><td>b10</td><td>POERQ002</td><td>POE request generation on comparator detection setting bit for AN002/AN102</td></tr></table></td></tr>
<tr><td>—</td><td>• A/D sample and hold circuit control register (ADSHCR)
• A/D group scan priority control register (ADGSPCR)</td></tr>
<tr><td>10-bit A/D converter</td><td>Functions</td><td>• Specification overview
<table><tr><td>Input channel</td><td>12</td></tr><tr><td>Conversion time</td><td>Per channel 1.0 µs (ADCLK = 50 MHz, AVCC0 = 4.0 V to 5.5 V)
Per channel 2.0 µs (ADCLK = 25 MHz, AVCC0 = 3.0 V to 3.6 V)</td></tr><tr><td>A/D conversion clock</td><td>PCLK,PCLK/2,PCLK/4,PCLK/8</td></tr><tr><td>Data register</td><td>10 registers (ADDRA to ADDRL)</td></tr><tr><td rowspan="3">Operating mode</td><td>Single mode</td></tr><tr><td>Single-cycle scan mode</td></tr><tr><td>Continuous scan mode</td></tr><tr><td rowspan="4">Function</td><td>Sample and hold function</td></tr><tr><td>Variable sampling state (unit)</td></tr><tr><td>A/D converter self-diagnostic function</td></tr><tr><td>—</td></tr></table></td><td>• Specification overview
<table><tr><td>Input channel</td><td>20</td></tr><tr><td>Conversion time</td><td>AN0 to AN7: Per channel 0.5 µs (ADCLK = 100 MHz)
AN8 to AN19: Per channel 1.0 µs (ADCLK = 50 MHz)</td></tr><tr><td>A/D conversion clock</td><td>The following frequency ratios may be specified for the peripheral module clock and A/D conversion clock: PCLK:ADCLK frequency ratio = 1:1, 1:2, 1:4, 1:8, 2:1, or 4:1</td></tr><tr><td>Data register</td><td>21 registers (ADDRA to ADDRT, ADRD)</td></tr><tr><td rowspan="3">Operating mode</td><td>—</td></tr><tr><td>Single-cycle scan mode</td></tr><tr><td>Continuous scan mode</td></tr><tr><td rowspan="4">Function</td><td>Sample and hold function</td></tr><tr><td>Variable sampling state (channel)</td></tr><tr><td>A/D converter self-diagnostic function</td></tr><tr><td>A/D-converted value addition mode</td></tr></table></td></tr>
</table>

Table 2.34 Differences in Functions and Specifications (34)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="11">10-bit A/D converter</td><td rowspan="11">Registers/ bits</td><td>• A/D data register n (ADDRn) (n = A to L)</td><td>• A/D data register y (ADDRy) (y = A to T)</td></tr>
<tr><td>• A/D self-diagnostic register (ADDIAGR)
<table><tr><td>b0
b1</td><td>DIAG[1:0]</td><td>Self-diagnostic designation bits</td></tr><tr><td>b2
b7</td><td>—</td><td>(Reserved bits)</td></tr></table></td><td>• A/D self-diagnostic register (ADRD)
ADCER.ADPRC = 0, ADCER.ADRFMT = 0 (set to 10-bit right-aligned format)
<table><tr><td>b0
b9</td><td>AD[9:0]</td><td>Converted value[9:0]</td></tr><tr><td>b10
b13</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b14
b15</td><td>DIAGST[1:0]</td><td>Self-diagnostic status bits</td></tr></table></td></tr>
<tr><td>• A/D control / status register (ADCSR)
<table><tr><td>b0
b3</td><td>CH[3:0]</td><td>Channel select bits</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>ADST</td><td>A/D start bit</td></tr><tr><td>b6</td><td>ADIE</td><td>A/D interrupt enable bit</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• A/D control / status register (ADCSR)
<table><tr><td>b0
b7</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b8</td><td>EXTRG</td><td>Trigger select bit</td></tr><tr><td>b9</td><td>TRGE</td><td>Trigger start select enable bit</td></tr><tr><td>b10
b11</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b12</td><td>ADIE</td><td>Scan finished interrupt enable bit</td></tr><tr><td>b13</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b14</td><td>ADCS</td><td>Scan mode select bit</td></tr><tr><td>b15</td><td>ADST</td><td>A/D conversion start bit</td></tr></table></td></tr>
<tr><td>• A/D control register (ADCR)
—</td><td>—
• A/D channel select register 0 (ADANSA0)
• A/D channel select register 1 (ADANSA1)
• A/D-converted value addition mode select register 0 (ADADS0)
• A/D A/D-converted value addition mode select register 1 (ADADS1)
• A/D-converted value addition count select register (ADADC)</td></tr>
<tr><td>• A/D start trigger select register (ADSTRGR)
<table><tr><td>b0
b4</td><td>ADSTRS[4:0]</td><td>A/D start trigger select bits</td></tr><tr><td>b5
b7</td><td>—</td><td>(Reserved bits)</td></tr></table></td><td>• A/D start trigger select register (ADSTRGR)
<table><tr><td>b0
b7</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b8
b13</td><td>TRSA[5:0]</td><td>A/D conversion start trigger select bits</td></tr><tr><td>b14
b15</td><td>—</td><td>(Reserved bits)</td></tr></table></td></tr>
<tr><td>• ADDRn format select register (ADDPR) (n = A to L)
<table><tr><td>b0</td><td>DPPRC</td><td>Bit precision specification bit</td></tr><tr><td>b1
b6</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b7</td><td>DPSEL</td><td>ADDRn format select bit</td></tr></table></td><td>• A/D control extended register (ADCER)
<table><tr><td>b0
b1</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b2</td><td>ADPRC</td><td>A/D data register bit precision specification bit</td></tr><tr><td>b3
b4</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b5</td><td>ACE</td><td>Auto-clear enable bit</td></tr><tr><td>b6
b7</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b8
b9</td><td>DIAGVAL [1:0]</td><td>Self-diagnostic conversion voltage select bits</td></tr><tr><td>b10</td><td>DIAGLD</td><td>Self-diagnostic mode select bit</td></tr><tr><td>b11</td><td>DIAGM</td><td>Self-diagnostic enable bit</td></tr><tr><td>b12
b14</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b15</td><td>ADRFMT</td><td>A/D data register format select bit</td></tr></table></td></tr>
</table>

Table 2.35 Differences in Functions and Specifications (35)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td>10-bit A/D converter</td><td>Registers/ bits</td><td>• A/D sampling state register (ADSSTR)
—</td><td>• A/D sampling state register n (ADSSTRn) (n = 0 to 7)
• A/D sampling state register L (ADSSTRL)</td></tr>
<tr><td>D/A converter</td><td>Registers/ bits</td><td>—</td><td>• D/A data register m (DADRm)
• D/A control register (DACR)
• DADRm format select register (DADPR)
• D/A A/D synchronous start control register (DAADSCR)</td></tr>
<tr><td>Data operation circuit</td><td>Registers/ bits</td><td>—</td><td>• DOC control register (DOCR)
• DOC data input register (DODIR)
• DOC data setting register (DODSR)</td></tr>
<tr><td>RAM</td><td>Functions</td><td>• Specification overview
<table><tr><td>RAM capacity</td><td>16 KB/8 KB</td></tr><tr><td>Address</td><td>0000 0000h to 0000 3FFFh (16 KB)
0000 0000h to 0000 1FFFh (8 KB)</td></tr></table></td><td>• Specification overview
<table><tr><td>RAM capacity</td><td>48 KB/32 KB/24 KB</td></tr><tr><td>Address</td><td>0000 0000h to 0000 BFFFh (48 KB)
0000 0000h to 0000 7FFFh (32 KB)
0000 0000h to 0000 5FFFh (24 KB)</td></tr></table></td></tr>
<tr><td>Flash memory for code storage</td><td>Functions</td><td>• Specification overview
<table><tr><td>Memory space</td><td>User area: Maximum 256 KB (256 K, 128 K, 64 K)
—</td></tr><tr><td>Write unit</td><td>256-byte units</td></tr><tr><td>Block structure (reassure unit)</td><td>4 KB × 8 blocks (256 K, 128 K, 64 K)
—
—
16 KB × 14 blocks (256 K)
16 KB × 6 blocks (128 K)
16 KB × 2 blocks (64K)</td></tr><tr><td>On-board programming</td><td>Boot mode
—
—
User program mode</td></tr><tr><td>Off-board programming</td><td>The user MAT can be rewritten by using a PROM writer.</td></tr><tr><td>Protection functions</td><td>Software protection functions
Error protection functions</td></tr></table></td><td>• Specification overview
<table><tr><td>Memory space</td><td>User area: Maximum 512 KB (512 K, 384 K, 256 K)
User boot area: 16 KB</td></tr><tr><td>Write unit</td><td>128-byte units</td></tr><tr><td>Block structure (reassure unit)</td><td>4 KB × 8 blocks (512 K, 384 K, 256 K)
16 KB × 30 blocks (512 K)
16 KB × 22 blocks (384 K)
16 KB × 14 blocks (256 K)
—
—</td></tr><tr><td>On-board programming</td><td>Boot program
USB boot mode
User boot mode
User program mode</td></tr><tr><td>Off-board programming</td><td>The user area and user boot area can be rewritten by using a flash writer.</td></tr><tr><td>Protection functions</td><td>Software protection functions
FCU command lock function</td></tr></table></td></tr>
<tr><td></td><td>Registers/ bits</td><td>• Flash write erase protection register (FWEPROR)
<table><tr><td>b0
b1</td><td>FLWE[1:0]</td><td>Flach programming/erasure bits</td></tr></table>
• Flash access status register (FASTAT)
<table><tr><td>b0</td><td>DFLWPE</td><td>Data flash protect/erase protect violation bit</td></tr><tr><td>b1</td><td>DFLRPE</td><td>Data flash read protect violation bit</td></tr><tr><td>b3</td><td>DFLAE</td><td>Data flash access violation bit</td></tr><tr><td>b4</td><td>CMDLK</td><td>FCU command lock bit</td></tr><tr><td>b7</td><td>ROMAE</td><td>ROM access violation bit</td></tr></table></td><td>• Flash P/E protect register (FWEPROR)
<table><tr><td>b0
b1</td><td>FLWE[1:0]</td><td>Flash P/E bits</td></tr></table>
• Flash access status register (FASTAT)
<table><tr><td>b0</td><td>DFLWPE</td><td>E2 data flash P/E protect violation flag</td></tr><tr><td>b1</td><td>DFLRPE</td><td>E2 data flash read protect violation flag</td></tr><tr><td>b3</td><td>DFLAE</td><td>E2 data flash access violation flag</td></tr><tr><td>b4</td><td>CMDLK</td><td>FCU command lock flag</td></tr><tr><td>b7</td><td>ROMAE</td><td>ROM access violation flag</td></tr></table></td></tr>
</table>

Table 2.36 Differences in Functions and Specifications (36)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="5">Flash memory for code storage</td><td rowspan="5">Registers/ bits</td><td>• Flash Access error interrupt enable register (FAEINT)
<table><tr><td>b0</td><td>DFLWPEIE</td><td>Data flash protect/erase protect violation interrupt enable bit</td></tr><tr><td>b1</td><td>DFLRPEIE</td><td>Data flash read protect violation interrupt enable bit</td></tr><tr><td>b3</td><td>DFLAEIE</td><td>Data flash access violation interrupt enable bit</td></tr><tr><td>b4</td><td>CMDLKIE</td><td>FCU command lock interrupt enable bit</td></tr><tr><td>b7</td><td>ROMAEIE</td><td>ROM access violation interrupt enable bit</td></tr></table></td><td>• Flash access error interrupt enable register (FAEINT)
<table><tr><td>b0</td><td>DFLWPEIE</td><td>E2 data flash P/E protect violation interrupt enable bit</td></tr><tr><td>b1</td><td>DFLRPEIE</td><td>E2 data flash read protect violation interrupt enable bit</td></tr><tr><td>b3</td><td>DFLAEIE</td><td>E2 data flash access violation interrupt enable bit</td></tr><tr><td>b4</td><td>CMDLKIE</td><td>FCU command lock interrupt enable bit</td></tr><tr><td>b7</td><td>ROMAEIE</td><td>E2 data flash P/E protect violation interrupt enable bit</td></tr></table></td></tr>
<tr><td>• Flash status register 1 (FSTATR1)
<table><tr><td>b0
b1</td><td>—</td><td>(Reserved bit)
Note: The value when read is undetermined.</td></tr><tr><td>b4</td><td>FLOCKST</td><td>Lock bit status bit</td></tr><tr><td>b7</td><td>FCUERR</td><td>FCU error flag</td></tr></table></td><td>• Flash status register 1 (FSTATR1)
<table><tr><td>b0
b1</td><td>—</td><td>(Reserved bit)
Note: Value is 0 when read.</td></tr><tr><td>b4</td><td>FLOCKST</td><td>Lock bit status bit</td></tr><tr><td>b7</td><td>FCUERR</td><td>FCU error flag</td></tr></table></td></tr>
<tr><td>• Flash P/E mode entry register (FENTRYR)
<table><tr><td>b7</td><td>FENTRYD</td><td>Data flash P/E mode entry bit</td></tr></table></td><td>• Flash P/E mode entry register (FENTRYR)
<table><tr><td>b7</td><td>FENTRYD</td><td>E2 data flash P/E mode entry bit</td></tr></table></td></tr>
<tr><td>• Peripheral clock notification register (PCKAR)
These bits are used to set the peripheral clock (PCLK) at the programming/erasure of on-chip ROM/data flash.</td><td>• Peripheral clock notification register (PCKAR)
These bits are used to set the FlashIF clock (FCLK) at the programming/erasure of the on-chip ROM/E2 data flash.</td></tr>
<tr><td>• FCU RAM enable register (FCURAME)</td><td>—</td></tr>
<tr><td rowspan="2">Flash memory for data storage</td><td>Functions</td><td>• Specification overview
<table><tr><td>Memory space</td><td>32 KB /8 KB</td></tr><tr><td>Read via peripheral</td><td>Reading in a PCLK3 cycle using word or byte access</td></tr><tr><td>Write unit</td><td>8-byte or 128-byte units</td></tr><tr><td>Block structure (erase unit)</td><td>2 KB × 16 blocks (32 K)
2 KB × 4 blocks (8 K)</td></tr><tr><td>Programming command</td><td>2nd cycle data: 04h (8 bytes)
: 40h (128 bytes)</td></tr><tr><td>Blank check unit</td><td>8-byte or 2-KB units</td></tr><tr><td rowspan="4">On-board programming</td><td>Boot program</td></tr><tr><td>—</td></tr><tr><td>—</td></tr><tr><td>User program mode</td></tr><tr><td>Rewrite count</td><td>30,000 times</td></tr></table></td><td>• Specification overview
<table><tr><td>Memory space</td><td>32 KB</td></tr><tr><td>Read via peripheral</td><td>Reading in a PCLK6 cycle using word or byte access</td></tr><tr><td>Write unit</td><td>2-byte units</td></tr><tr><td>Block structure (erase unit)</td><td>32 bytes × 1024 blocks</td></tr><tr><td>Programming command</td><td>2nd cycle data: 01h (2 bytes)</td></tr><tr><td>Blank check unit</td><td>2-byte or 2-KB units</td></tr><tr><td rowspan="4">On-board programming</td><td>Boot program</td></tr><tr><td>USB boot mode</td></tr><tr><td>User boot mode</td></tr><tr><td>User program mode</td></tr><tr><td>Rewrite count</td><td>100,000 times</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>• Flash access status register (FASTAT)
<table><tr><td>b0</td><td>DFLWPE</td><td>Data flash protect/erase protect violation bit</td></tr><tr><td>b1</td><td>DFLRPE</td><td>Data flash read protect violation bit</td></tr><tr><td>b3</td><td>DFLAE</td><td>Data flash access violation bit</td></tr><tr><td>b4</td><td>CMDLK</td><td>FCU command lock bit</td></tr><tr><td>b7</td><td>ROMAE</td><td>ROM access violation bit</td></tr></table>• Flash access error interrupt enable register (FAEINT)
<table><tr><td>b0</td><td>DFLWPEIE</td><td>Data flash protect/erase protect violation interrupt enable bit</td></tr><tr><td>b1</td><td>DFLRPEIE</td><td>Data flash read protect violation interrupt enable bit</td></tr><tr><td>b3</td><td>DFLAEIE</td><td>Data flash access violation interrupt enable bit</td></tr><tr><td>b4</td><td>CMDLKIE</td><td>FCU command lock interrupt enable bit</td></tr><tr><td>b7</td><td>ROMAEIE</td><td>ROM access violation interrupt enable bit</td></tr></table></td><td>• Flash access status register (FASTAT)
<table><tr><td>b0</td><td>DFLWPE</td><td>Data flash protect/erase protect violation bit</td></tr><tr><td>b1</td><td>DFLRPE</td><td>Data flash read protect violation bit</td></tr><tr><td>b3</td><td>DFLAE</td><td>Data flash access violation bit</td></tr><tr><td>b4</td><td>CMDLK</td><td>FCU command lock bit</td></tr><tr><td>b7</td><td>ROMAE</td><td>ROM access violation bit</td></tr></table>• Flash access error interrupt enable register (FAEINT)
<table><tr><td>b0</td><td>DFLWPEIE</td><td>E2 data flash program/erase protect violation interrupt enable bit</td></tr><tr><td>b1</td><td>DFLRPEIE</td><td>E2 data flash read protect violation interrupt enable bit</td></tr><tr><td>b3</td><td>DFLAEIE</td><td>E2 data flash access violation interrupt enable bit</td></tr><tr><td>b4</td><td>CMDLKIE</td><td>FCU command lock interrupt enable bit</td></tr><tr><td>b7</td><td>ROMAEIE</td><td>E2 data flash P/E protect violation interrupt enable bit</td></tr></table></td></tr>
</table>

Table 2.37 Differences in Functions and Specifications (37)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="3">Flash memory for data storage</td><td rowspan="3">Registers/ bits</td><td>
• Data flash read enable register 0 (DFLRE0)
<table>
<tr><td>b0</td><td>DBRE00</td><td>DB00 block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE01</td><td>DB01 block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE02</td><td>DB02 block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE03</td><td>DB03 block read enable bi</td></tr>
<tr><td>b4</td><td>DBRE04*1</td><td>DB04 block read enable bit</td></tr>
<tr><td>b5</td><td>DBRE05*1</td><td>DB05 block read enable bit</td></tr>
<tr><td>b6</td><td>DBRE06*1</td><td>DB06 block read enable bit</td></tr>
<tr><td>b7</td><td>DBRE07*1</td><td>DB07 block read enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
Note: 1. These bits are reserved on the R5F562T7xxxx and R5F562T6xxxx.
</td><td>
• E2 data flash read enable register 0 (DFLRE0)
<table>
<tr><td>b0</td><td>DBRE00</td><td>0000-0063 block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE01</td><td>0064-0127 block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE02</td><td>0128-0191 block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE03</td><td>0192-0255 block read enable bit</td></tr>
<tr><td>b4</td><td>DBRE04</td><td>0256-0319 block read enable bit</td></tr>
<tr><td>b5</td><td>DBRE05</td><td>0320-0383 block read enable bit</td></tr>
<tr><td>b6</td><td>DBRE06</td><td>0384-0447 block read enable bit</td></tr>
<tr><td>b7</td><td>DBRE07</td><td>0448-0511 block read enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td></tr>
<tr><td>
• Data flash read enable register 1 (DFLRE1)
<table>
<tr><td>b0</td><td>DBRE08</td><td>DB08 block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE09</td><td>DB09 block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE10</td><td>DB10 block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE11</td><td>DB11 block read enable bit</td></tr>
<tr><td>b4</td><td>DBRE12*1</td><td>DB12 block read enable bit</td></tr>
<tr><td>b5</td><td>DBRE13*1</td><td>DB13 block read enable bit</td></tr>
<tr><td>b6</td><td>DBRE14*1</td><td>DB14 block read enable bit</td></tr>
<tr><td>b7</td><td>DBRE15*1</td><td>DB15 block read enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
Note: 1. These bits are reserved on the R5F562T7xxxx and R5F562T6xxxx.
</td><td>
• E2 data flash read enable register 1 (DFLRE1)
<table>
<tr><td>b0</td><td>DBRE08</td><td>0512-0575 block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE09</td><td>0576-0639 block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE10</td><td>0640-0703 block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE11</td><td>0704-0767 block read enable bit</td></tr>
<tr><td>b4</td><td>DBRE12</td><td>0768-0831 block read enable bit</td></tr>
<tr><td>b5</td><td>DBRE13</td><td>0832-0895 block read enable bit</td></tr>
<tr><td>b6</td><td>DBRE14</td><td>0896-0959 block read enable bit</td></tr>
<tr><td>b7</td><td>DBRE15</td><td>0960-1023 block read enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td></tr>
<tr><td>
• Data flash programming/erasure enable register 0 (DFLWE0)
<table>
<tr><td>b0</td><td>DBWE00</td><td>DB00 block programming/erasure enable bit</td></tr>
<tr><td>b1</td><td>DBWE01</td><td>DB01 block programming/erasure enable bit</td></tr>
<tr><td>b2</td><td>DBWE02</td><td>DB02 block programming/erasure enable bit</td></tr>
<tr><td>b3</td><td>DBWE03</td><td>DB03 block programming/erasure enable bit</td></tr>
<tr><td>b4</td><td>DBWE04*1</td><td>DB04 block programming/erasure enable bit</td></tr>
<tr><td>b5</td><td>DBWE05*1</td><td>DB05 block programming/erasure enable bit</td></tr>
<tr><td>b6</td><td>DBWE06*1</td><td>DB06 block programming/erasure enable bit</td></tr>
<tr><td>b7</td><td>DBWE07*1</td><td>DB07 block programming/erasure enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
Note: 1. These bits are reserved on the R5F562T7xxxx and R5F562T6xxxx.
</td><td>
• E2 data flash programming/erasure enable register 0 (DFLWE0)
<table>
<tr><td>b0</td><td>DBWE00</td><td>0000-0063 block P/E enable bit</td></tr>
<tr><td>b1</td><td>DBWE01</td><td>0064-0127 block P/E enable bit</td></tr>
<tr><td>b2</td><td>DBWE02</td><td>0128-0191 block P/E enable bit</td></tr>
<tr><td>b3</td><td>DBWE03</td><td>0192-0255 block P/E enable bit</td></tr>
<tr><td>b4</td><td>DBWE04</td><td>0256-0319 block P/E enable bit</td></tr>
<tr><td>b5</td><td>DBWE05</td><td>0320-0383 block P/E enable bit</td></tr>
<tr><td>b6</td><td>DBWE06</td><td>0384-0447 block P/E enable bit</td></tr>
<tr><td>b7</td><td>DBWE07</td><td>0448-0511 block P/E enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td></tr>
</table>

Table 2.38 Differences in Functions and Specifications (38)

<table>
<tr><th colspan="2">Item</th><th>RX62T Group</th><th>RX63T Group</th></tr>
<tr><td rowspan="4">Flash memory for data storage</td><td rowspan="4">Registers/ bits</td><td>
• Data flash programming/erasure enable register 1 (DFLWE1)
<table>
<tr><td>b0</td><td>DBWE08</td><td>DB08 block programming/erasure enable bit</td></tr>
<tr><td>b1</td><td>DBWE09</td><td>DB09 block programming/erasure enable bit</td></tr>
<tr><td>b2</td><td>DBWE10</td><td>DB10 block programming/erasure enable bit</td></tr>
<tr><td>b3</td><td>DBWE11</td><td>DB11 block programming/erasure enable bit</td></tr>
<tr><td>b4</td><td>DBWE12*1</td><td>DB12 block programming/erasure enable bit</td></tr>
<tr><td>b5</td><td>DBWE13*1</td><td>DB13 block programming/erasure enable bit</td></tr>
<tr><td>b6</td><td>DBWE14*1</td><td>DB14 block programming/erasure enable bit</td></tr>
<tr><td>b7</td><td>DBWE15*1</td><td>DB15 block programming/erasure enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
Note: 1. These bits are reserved on the R5F562T7xxxx and R5F562T6xxxx.
</td><td>
• E2 data flash programming/erasure enable register 1 (DFLWE1)
<table>
<tr><td>b0</td><td>DBWE08</td><td>0512-0575 block P/E enable bit</td></tr>
<tr><td>b1</td><td>DBWE09</td><td>0576-0639 block P/E enable bit</td></tr>
<tr><td>b2</td><td>DBWE10</td><td>0640-0703 block P/E enable bit</td></tr>
<tr><td>b3</td><td>DBWE11</td><td>0704-0767 block P/E enable bit</td></tr>
<tr><td>b4</td><td>DBWE12</td><td>0768-0831 block P/E enable bit</td></tr>
<tr><td>b5</td><td>DBWE13</td><td>0832-0895 block P/E enable bit</td></tr>
<tr><td>b6</td><td>DBWE14</td><td>0896-0959 block P/E enable bit</td></tr>
<tr><td>b7</td><td>DBWE15</td><td>0960-1023 block P/E enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td></tr>
<tr><td>
• Flash P/E mode entry register (FENTRYR)
<table>
<tr><td>b0</td><td>FENTRY0</td><td>ROM P/E mode entry bit 0</td></tr>
<tr><td>b7</td><td>FENTRYD</td><td>Data flash P/E mode entry bit</td></tr>
<tr><td>b8
b15</td><td>FEKEY[7:0]</td><td>Key code</td></tr>
</table>
</td><td>
• Flash P/E mode entry register (FENTRYR)
<table>
<tr><td>b0</td><td>FENTRY0</td><td>ROM P/E mode entry bit 0</td></tr>
<tr><td>b7</td><td>FENTRYD</td><td>E2 data flash P/E mode entry bit</td></tr>
<tr><td>b8
b15</td><td>FEKEY[7:0]</td><td>Key code</td></tr>
</table>
</td></tr>
<tr><td>
• Data flash blank check control register (DFLBCCNT)
<table>
<tr><td>b0</td><td>BCSIZE</td><td>Blank check size setting bit</td></tr>
<tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b3

b10</td><td>BCADR[7:0]</td><td>Blank check address setting bits</td></tr>
<tr><td>b11
b14</td><td>—</td><td>(Reserved bits)</td></tr>
<tr><td>b15</td><td>—</td><td>(Reserved bit)</td></tr>
</table>
</td><td>
• E2 flash blank check control register (DFLBCCNT)
<table>
<tr><td>b0

b10</td><td>BCADR [10:0]</td><td>Blank check size setting bits</td></tr>
<tr><td>b11
b14</td><td>—</td><td>(Reserved bits)</td></tr>
<tr><td>b15</td><td>BCSIZE</td><td>Blank check size setting bit</td></tr>
</table>
</td></tr>
<tr><td>
• Data flash blank check status register (DFLBCSTAT)
</td><td>
• E2 data flash blank check status register (DFLBCSTAT)
</td></tr>
</table>

3. Reference Documents

User's Manual: Hardware

RX62T Group User's Manual: Hardware Rev.1.31
RX63T Group User's Manual: Hardware Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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Inquiries

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REVISION HISTORY	RX62T Group, RX63T Group Application Note Differences between RX62T Group and RX63T Group (144, 120, 112, and 100-Pin Versions)

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 24, 2013	—	First edition issued
1.01	Jan. 08, 2018	19	Removed Functions column in Multi-function timer pulse unit 3.
		20	Remove “Active level register 1 (ALR1)”.
		31	Remove “Serial control register (SCR)” and “Smart card mode register (SCMR)”.
		33	Remove “RSPI control register (SPCR)” and “RSPI control register 2 (SPCR2)”.
		34	Fixed incorrect input channels in 12-bit A/D converter. Fixed from “(1 unit × 8 channels) × 1” to “(1 unit × 4 channels) × 2”.
		34	Fixed incorrect Data registers in 12-bit A/D converter. Fixed from “11 registers (ADDR0 to ADDR7, ADDBLDR, ADDBLDRA, ADDBLDRB)” to “14 registers (ADDR0 to ADDR3, ADDBLDR, ADDBLDRA, ADDBLDRB)” Add “8-, 10-, or 12-bit precision output of A/D conversion results”
		35-37	Fixed incorrect of the register name.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

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