Introduction
The RX62T Group has a general PWM timer (GPT) consisting of a four-channel 16-bit timer, the GPT operates at a maximum of 100 MHz. This application note is going to show the setting of three-phase saw-wave complementary PWM with automatic dead time setting in GPT function.

Target Device
RX62T

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1. Specification

- 16 bit x 4 channels
- Up-count or down-count operation (saw waves) or up/down-count operation (triangle waves) for each counter.
- Clock sources independently selectable for each channel.
- Two input/output pins per channel.
- Two output compare/input capture registers per channel.
- For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use.
- In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms.
- Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow).
- Synchronously operation of the several counters
- Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting).
- Generation of dead times in PWM operation.
- Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times.
- Starting, clearing, and stopping counters in response to external or internal triggers.
- Internal trigger sources: output of the internal comparator, software, and compare match.
- The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the IWDT-dedicated low-speed on-chip oscillator clock signal (to detect abnormal oscillation).

Fig. 1-1 is the block diagram of General PWM Timer (GPT).
### Table 1-1 Specifications of General PWM Timer (GPT) Register

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTSTR</td>
<td>General PWM timer software start register</td>
</tr>
<tr>
<td>GTHSCR</td>
<td>General PWM timer hardware source start control register</td>
</tr>
<tr>
<td>GTHCCR</td>
<td>General PWM timer hardware source clear control register</td>
</tr>
<tr>
<td>GTHSSR</td>
<td>General PWM timer hardware start source select register</td>
</tr>
<tr>
<td>GTHPSR</td>
<td>General PWM timer hardware stop/clear source select register</td>
</tr>
<tr>
<td>GTWP</td>
<td>General PWM timer write-protection register</td>
</tr>
<tr>
<td>GTSYNC</td>
<td>General PWM timer sync register</td>
</tr>
<tr>
<td>GTETINT</td>
<td>General PWM timer external trigger input interrupt register</td>
</tr>
<tr>
<td>GTBDR</td>
<td>General PWM timer buffer operation disable register</td>
</tr>
<tr>
<td>GTIOR</td>
<td>General PWM timer I/O control register</td>
</tr>
<tr>
<td>GTINTAD</td>
<td>General PWM timer interrupt output setting register</td>
</tr>
<tr>
<td>GTCR</td>
<td>General PWM timer control register</td>
</tr>
<tr>
<td>GTBER</td>
<td>General PWM timer buffer enable register</td>
</tr>
<tr>
<td>GTUDC</td>
<td>General PWM timer count direction register</td>
</tr>
<tr>
<td>GTITC</td>
<td>General PWM timer interrupt and A/D converter start request skipping setting</td>
</tr>
<tr>
<td>GTST</td>
<td>General PWM timer status register</td>
</tr>
<tr>
<td>GTCNT</td>
<td>General PWM timer counter value</td>
</tr>
<tr>
<td>GTCCRA</td>
<td>General PWM timer compare capture register A</td>
</tr>
<tr>
<td>GTCCRB</td>
<td>General PWM timer compare capture register B</td>
</tr>
<tr>
<td>GTCCRC</td>
<td>General PWM timer compare capture register C</td>
</tr>
<tr>
<td>GTCCRD</td>
<td>General PWM timer compare capture register D</td>
</tr>
<tr>
<td>GTCCRE</td>
<td>General PWM timer compare capture register E</td>
</tr>
<tr>
<td>GTCCRF</td>
<td>General PWM timer compare capture register F</td>
</tr>
<tr>
<td>GTPR</td>
<td>General PWM timer cycle setting register</td>
</tr>
<tr>
<td>GTPBR</td>
<td>General PWM timer cycle setting buffer register</td>
</tr>
<tr>
<td>GTPDBR</td>
<td>General PWM timer cycle setting double-buffer register</td>
</tr>
<tr>
<td>GTADTRA</td>
<td>A/D converter start request timing register A</td>
</tr>
<tr>
<td>GTADTBR</td>
<td>A/D converter start request timing buffer register A</td>
</tr>
<tr>
<td>GTADTDBRA</td>
<td>A/D converter start request timing double-buffer register A</td>
</tr>
<tr>
<td>GTADTRB</td>
<td>A/D converter start request timing register B</td>
</tr>
<tr>
<td>GTADTBBR</td>
<td>A/D converter start request timing buffer register B</td>
</tr>
<tr>
<td>GTADTDBBB</td>
<td>A/D converter start request timing double-buffer register B</td>
</tr>
<tr>
<td>GTONCR</td>
<td>General PWM timer output negate control register</td>
</tr>
<tr>
<td>GTDTCR</td>
<td>General PWM timer dead time control register</td>
</tr>
<tr>
<td>GTDVU</td>
<td>General PWM timer dead time value register</td>
</tr>
<tr>
<td>GTDVD</td>
<td>General PWM timer dead time value register</td>
</tr>
</tbody>
</table>
2. Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

2.1 Example Three Channel Synchronized Operation

Figure 2.1 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

By setting GTDTCR, a negative-phase waveform with dead time based on the dead time value registers GTDVU and GTDVD can be output from each pin.

Fig. 2-1 shows an example of Saw-Wave One-Shot Pulse Mode operation.

![Figure 2-1 Example of Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting](image)
2.2 Example of Procedure for Setting Three-Phase Saw-Wave Complementary
PWM Output with Automatic Dead Time Setting

Fig. 2-2 shows an example of the procedure for setting Saw-Wave One-Shot Pulse Mode.

![Diagram of procedure]

Figure 2-2  Example of Procedure for Setting Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting
3. General PWM Timer Software Register Setting

General PWM Timer Control Register (GTCR):

GTCR controls GTCNT.
GTCR should be set while GTCNT operation is stopped.

When synchronized clearing is selected, synchronized clearing is handled equally to clearing by the counter's overflow or underflow in saw-wave mode. The output of output compare is changed and buffer transfer performed. However, the overflow flag and underflow flag are not changed.

![Figure 3-1 GTCR Setting](image)

General PWM Timer I/O Control Register (GTIOR):

GPTn.GTIOR sets the functions of the GTIOCNnA and GTIOCNnB pins (n = 0 to 3). Each channel has one GTIOCNnA pin and one GTIOCNnB pin.

![Figure 3-2 GTIOR Setting](image)
General PWM Timer Cycle Setting Buffer Register (GTPBR):

The first have to set the counter cycle from GTPR register and the GTPBR is the buffer for GTPR.

General PWM Timer Compares Capture Register C (GTCCRC):

Set the compare match value.

General PWM Timer Dead Time Control Register (GTDTCR):

GTDTCR enables automatic setting of a negative-phase waveform with dead time.

From Fig. 3-3 the TDE have set to 1, compare match value of a negative-phase waveform with Dead time is automatically set to GPTn.GTCCRB and TDFER is also set to 1, TDBUE and TDBDE is also set to 1 that buffer operation enable.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>TDE</td>
<td>Negative-Phase Waveform Setting</td>
<td>0: Normal operation 1: Compare match value of a negative-phase waveform with dead time is automatically set to GPTn.GTCCRB</td>
</tr>
<tr>
<td>b3 to b1</td>
<td>(Reserved)</td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
<tr>
<td>b4</td>
<td>TDBUE</td>
<td>GTDVU Buffer Operation Enable</td>
<td>0: GPTn.GTDVU buffer operation is disabled 1: GPTn.GTDVU buffer operation is enabled</td>
</tr>
<tr>
<td>b5</td>
<td>TDBDE</td>
<td>GTDVU Buffer Operation Enable</td>
<td>0: GPTn.GTDVU buffer operation is disabled 1: GPTn.GTDVU buffer operation is enabled</td>
</tr>
<tr>
<td>b7 to b6</td>
<td>(Reserved)</td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
<tr>
<td>b8</td>
<td>TDFER</td>
<td>GTDVU Setting</td>
<td>0: Normal operation (GPTn.GTDVU and GPTn.GTDVD operate separately) 1: The value written to GPTn.GTDVU is set to GPTn.GTDVD</td>
</tr>
<tr>
<td>b15 to b9</td>
<td>(Reserved)</td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Figure 3-3  GTDTCR Setting**

General PWM Timer Dead Time Values Register (GTDVU):

Set the dead time value.

General PWM Timer Dead time Buffer Register (GTDBU):

This register is GTDVU buffer.

General PWM Timer Buffer Enable Register (GTBER):

GTBER makes settings for buffer operation. GTBER should be set while GTCNT operation is stopped.
From Fig. 3-4 The PR bits set 0x03 that GTPR is double buffer operation.

General PWM Timer Output Negate Control Register (GTONCR):

GTONCR controls negate of the GTIOCnA pin output and GTIOCnB pin output.

From Fig. 3-5 the OAE and OBE bits should set to 1, GTIOCnA and GTIOCnB Pin output enable.
4. Experiment Result

Fig. 4-1 to Fig. 4-3 the $f_{sw}$ is 20 kHz. Dead time is 2μs, Fig. 4-1 is GPT for 25% duty; Fig. 4-2 is GPT for 50% duty; and Fig. 4-3 is GPT for 75% duty.

![Figure 4-1 GPT output for 25% duty](image1)

![Figure 4-2 GPT output for 50% duty](image2)
4-3 GPT output for 75% duty

Fig. 4-4 shows the synchronized operation between GPT2 and GPT3.

4-4 Synchronized operation between GPT2 and GPT3

5. Conclusion
From experimental result, we can use General PWM Timer for Saw-Wave One-Shot Pulse Mode control.

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<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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<tbody>
<tr>
<td>1.00</td>
<td>October.01.11</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
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   Access to reserved addresses is prohibited.
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4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   - The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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