RX23T Group, RX62T Group

Points of Difference Between RX23T Group and RX62T Group

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Introduction

This application note is intended as a reference for confirming the points of difference between the I/O registers of the RX23T Group and RX62T Group.

Target Device

- RX23T Group 64-pin version, ROM capacity: 64 KB and 128 KB
- RX23T Group 52-pin version, ROM capacity: 64 KB and 128 KB
- RX23T Group 48-pin version, ROM capacity: 64 KB and 128 KB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Comparison of Functions of RX23T Group and RX62T Group

A comparison of the functions of the RX23T Group and RX62T Group is provided below. For details of the functions, see 2., Comparative Overview of Functions, and 3., Reference Documents.

Table 1.1 is a comparative listing of the functions of the RX23T and RX62T.

Table 1.1 Comparison of Functions of RX23T and RX62T

Function	RX62T	RX23T
Operating Modes	△	△
Reset	△	△
Option-setting memory	×	○
Voltage detection circuit (LVD): RX62T, (LVDAb): RX23T	△	△
Clock generation circuit	△	△
Clock frequency accuracy measurement circuit (CAC)	×	○
Low power consumption function	△	△
Register write protection function	×	○
Interrupt controller (ICU): RX62T, (ICUb): RX23T	△	△
Buses	△	△
Memory-protection unit (MPU)	△	△
Data transfer controller (DTC): RX62T, (DTCa): RX23T	△	△
I/O port	△	△
Multi-function pin controller (MPC)	×	○
Multi-function timer pulse unit 3 (MTU3): RX62T, (MTU3c): RX23T	△	△
Port output enable 3 (POE3): RX62T, (POE3b): RX23T	△	△
8-bit timer (TMR)	×	○
Compare match timer (CMT)	○	○
Watchdog timer (WDT)	○	×
Independent watchdog timer (IWDT): RX62T, (IWDTa): RX23T	△	△
Serial communications interface (SCIb): RX62T, (SCIg): RX23T	△	△
I^2C bus interface (RIIC): RX62T, (RIICa): RX23T	△	△
CAN module (CAN)	○	×
Serial peripheral interface (RSPI): RX62T, (RSPIa): RX23T	△	△
LIN module (LIN)	○	×
CRC calculator (CRC)	○	○
12-bit A/D converter (S12ADA): RX62T, (S12ADE): RX23T	△	△
10-bit A/D converter (ADA)	○	×
D/A converter (DA) for generating comparator C reference voltage	×	○
Comparator C (CMPC)	×	○
Data operation circuit (DOC)	×	○
RAM	△	△
Flash memory	△	△

Note: ○: Function implemented, ×: Function not implemented, △: Differences exist between implementation of function on RX62T and RX23T.

2. Comparative Overview of Functions

2.1 Operating Modes

Table 2.1 shows a comparative listing of the operating mode registers.

Table 2.1 Comparative Listing of Operating Mode Registers

Register	Bit	RX62T	RX23T
MDMONR	MD0	MD0 pin status flag	—
	MD	—	MD pin status flag
	MD1	MD1 pin status flag	—
	MDE	MDE pin status flag	—
MDSR	IROM	On-chip ROM startup status flag	—
	BOTS	Boot mode startup flag	—
SYSCR0	ROME	On-chip ROM enable bit	—
	KEY[7:0]	SYSCR0 key code	—

2.2 Resets

Table 2.2 shows a comparative listing of the reset specifications and Table 2.3 shows a comparative listing of the reset registers.

Table 2.2 Comparative Listing of Reset Specifications

Reset Name	RX62T	RX23T
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises or falls (voltage detection: VPOR).	VCC rises (voltage detection: VPOR).
Voltage monitoring reset	VCC falls (voltage detection: Vdet1 and Vdet2).	VCC falls (voltage detection: Vdet0, Vdet1, and Vdet2).
Deep software standby reset	Deep software standby mode is canceled by an interrupt.	—
Independent watchdog timer reset	The independent watchdog timer underflows.	The independent watchdog timer underflows or reflesh error.
Watchdog timer reset	The watchdog timer overflows.	—
Software reset	—	Register settings

Table 2.3 Comparative Listing of Reset Registers

Register	Bit	RX62T	RX23T
RSTSR0	PORF	—	Power-on reset detection flag
	LVD0RF	—	Voltage monitoring 0 reset detection flag
	LVD1RF	—	Voltage monitoring 1 reset detection flag
	LVD2RF	—	Voltage monitoring 2 reset detection flag
RSTSR1	CWSF	—	Cold/warm start determination flag
RSTSR2	IWDTRF	—	Independent watchdog timer reset detection flag
	SWRF	—	Software reset detection flag
SWRR	SWRR[15:0]	—	Software reset bits
RSTSR	PORF	Power-on reset flag	—
	LVD1F	LVD1 detection flag	—
	LVD2F	LVD2 detection flag	—
	DPSRSTF	Deep software standby reset flag	—
RSTCSR	RSTE	Reset enable bit	—
	WOVF	Watchdog timer overflow flag	—
IWDTSR	CNTVAL[13:0]	Down counter bits	—
	UNDFF	Underflow flag	—

2.3 Voltage Detection Circuit

Table 2.4 shows a comparative listing of the voltage detection circuit specifications and Table 2.5 shows a comparative listing of the voltage detection circuit registers.

Table 2.4 Comparative Listing of Voltage Detection Circuit Specifications

		RX62T (LVD)		RX23T (LVDAb)		
Item		**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage falls lower than Vdet1.	Voltage falls lower than Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
	Detection voltage	—	—	Selectable from two levels using OFS1.VDSEL[1:0] bits.	Selectable from nine levels using LVDLVLR.LVD1LVL[3:0] bits.	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits.
	Monitor flag	—	—	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.
		—	—		LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		—	—	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.
	Interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
		—	—		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
		—	—		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.

Table 2.5 Comparative Listing of Voltage Detection Circuit Registers

Register	Bit	RX62T (LVD)	RX23T (LVDAb)
RSTSR	PORF	Power-on reset flag	—
	LVD1F	LVD1 detection flag	—
	LVD2F	LVD2 detection flag	—
	DPSRSTF	Deep software standby reset flag	—
LVDKEYR	KEY[7:0]	LVDCR key code	—
LVDCR	LVD1RI	LVD1 reset/interrupt select bit	—
	LVD1E	LVD1 enable bit	—
	LVD2RI	LVD2 reset/interrupt select bit	—
	LVD2E	LVD2 enable bit	—
LVD1CR1	LVD1IDTSEL [1:0]	—	Voltage monitoring 1 interrupt generation condition select bits
	LVD1IRQSEL	—	Voltage monitoring 1 interrupt type select bit
LVD1SR	LVD1DET	—	Voltage monitoring 1 voltage change detection flag
	LVD1MON	—	Voltage monitoring 1 signal monitor flag
LVD2CR1	LVD2IDTSEL [1:0]	—	Voltage monitoring 2 interrupt generation condition select bits
	LVD2IRQSEL	—	Voltage monitoring 2 interrupt type select bit
LVD2SR	LVD2DET	—	Voltage monitoring 2 voltage change detection flag
	LVD2MON	—	Voltage monitoring 2 signal monitor flag
LVCMPCR	LVD1E	—	Voltage detection 1 enable bit
	LVD2E	—	Voltage detection 2 enable bit
LVDLVLR	LVD1LVL[3:0]	—	Voltage detection 1 level select bits (reference voltage when voltage falls)
	LVD2LVL[3:0]	—	Voltage detection 2 level select bits (reference voltage when voltage falls)
LVD1CR0	LVD1RIE	—	Voltage monitoring 1 interrupt/reset enable bit
	LVD1CMPE	—	Voltage monitoring 1 circuit comparison result output enable bit
	LVD1RI	—	voltage monitoring 1 circuit mode select bit
	LVD1RN	—	voltage monitoring 1 reset negate select bit
LVD2CR0	LVD2RIE	—	Voltage monitoring 2 interrupt/reset enable bit
	LVD2CMPE	—	Voltage monitoring 2 circuit comparison result output enable bit
	LVD2RI	—	voltage monitoring 2 circuit mode select bit
	LVD2RN	—	voltage monitoring 2 reset negate select bit

2.4 Clock Generation Circuit

Table 2.6 shows a comparative listing of the clock generation circuit specifications and Table 2.7 shows a comparative listing of the clock generation circuit registers.

Table 2.6 Comparative Listing of Clock Generation Circuit Specifications

Item	RX62T	RX23T
Uses	• Generates the system clock (ICLK) supplied to the CPU, DTC, MTU3, GPT, ROM, and RAM. • Generates the peripheral module clocks (PCLK) supplied to the peripheral modules. • IWDT-dedicated clock (IWDTCLK) supplied to the IWDT.	• Generates the system clock (ICLK) supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the CAC clock (CACCLK) supplied to the CAC.
Operating frequencies	• ICLK: 8 MHz to 100 MHz • PCLK: 8 MHz to 50 MHz • IWDTCLK: 125 kHz	• ICLK: 40 MHz (max.) • PCLKA: 40 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same frequency as each oscillator • IWDTCLK: 15 kHz
Main clock ocillator	• Resonator frequency: 8 MHz to 12.5 MHz • External clock input frequency: 8 MHz to 12.5 MHz • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source is switched to an internally generated clock, and the MTU3 and GPT pins can be forcedly driven to high-impedance.	• esonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function
PLL	• Input clock source: Main clock • Input frequency: 8 MHz to 12.5 MHz • Frequency multiplication ratio: 8 • Oscillation frequency: 64 MHz to 100 MHz	• Input clock source: Main clock • Input division ratio: Selectable among 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 10 (increments of 0.5) • Oscillation frequency: 24 MHz to 40 MHz
High-speed on-chip oscillator (HOCO)	—	Oscillation frequency: 32 MHz

Item	RX62T	RX23T
Low-speed on-chip oscillator (LOCO)	—	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 15 kHz
Internal oscillator circuit used when main clock oscillator is stopped	Oscillation frequency of internal oscillator circuit when oscillation stop detected: 0.5 MHz to 7.0 MHz	—

Table 2.7 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX62T	RX23T
SCKCR	PCK[3:0]	Peripheral module clock select bits	—
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
	PCKB[3:0]	—	Peripheral module clock B (PCLKB) select bits
	PCKD[3:0]	—	Peripheral module clock D (PCLKD) select bits
	FCK[3:0]	—	FlashIF clock (FCLK) select bits
SCKCR3	CKSEL[2:0]	—	Clock source select bits
PLLCR	PLIDIV[1:0]	—	PLL input frequency division ratio select bits
	STC[5:0]	—	Frequency multiplication factor select bits
PLLCR2	PLLEN	—	PLL stop control bit
MOSCCR	MOSTP	—	Main clock oscillator stop bit
LOCOCR	LCSTP	—	LOCO stop bit
ILOCOCR	ILCSTP	—	IWDT-dedicated on-chip oscillator stop bit
HOCOCR	HCSTP	—	HOCO stop
HOCOWTCR	HSTS[2:0]	—	High-Speed On-Chip Oscillator oscillation stabilization wait time
OSCOVFSR	MOOVF	—	Main clock oscillation stabilization flag
	PLOVF	—	PLL clock oscillation stabilization flag
	HCOVF	—	HOCO clock oscillation stabilization flag
OSTDCR	OSTDIE	—	Oscillation stop detection interrupt enable bit
	OSTDF	Oscillation stop detection flag	
	KEY[7:0]	OSTDCR key code	—
OSTDSR	OSTDF	—	Oscillation stop detection flag
MOSCWTCR	MSTS[4:0]	—	Main clock oscillator wait time setting bits
MOFCR	MODRV21	—	Main clock oscillator drive capability switch bit
	MOSEL	—	Main clock oscillator switch bit
MEMWAIT	MEMWAIT	—	Memory wait cycle setting bit

2.5 Low Power Consumption Functions

Table 2.8 shows a comparative listing of the low power consumption functions and Table 2.9 shows a comparative listing of the low power consumption function registers.

Table 2.8 Comparative Listing of Low Power Consumption Functions

Item	RX62T	RX23T
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK) and peripheral module clock (PCLK).	The frequency division ratio can be set independently for the system clock (ICLK), high-speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • Software standby mode • Deep sleep mode
Operating power reduction function	—	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Operating power control modes: 2 — High-speed operating mode — Low-speed operating mode

Table 2.9 Comparative Listing of Low Power Consumption Function Registers

Register	Bit	RX62T	RX23T
SBYCR	STS[4:0]	Standby timer select bits	—
MSTPCRA	MSTPA4	—	8-bit timer 3 and 2 (unit 1) module stop setting bit
	MSTPA5	—	8-bit timer 1 and 0 (unit 0) module stop setting bit
	MSTPA7	General PWM timer module stop setting bit	—
	MSTPA16	12-bit A/D converter (unit 1) module stop setting bit	—
	MSTPA17	12-bit A/D converter (unit 0) module stop setting bit	12-bit A/D converter module stop setting bit
	MSTPA19	—	D/A converter (DA) for generating comparator C reference voltage module stop setting bit
	MSTPA23	10-bit A/D converter module stop setting bit	—
	MSTPA24	12-bit A/D converter control section module stop setting bit	—
	ACSE	All-module clock stop mode mode enable bit	—
MSTPCRB	MSTPB0	CAN module stop setting bit	—
	MSTPB6	—	DOC module stop setting bit
	MSTPB7	LIN module stop setting bit	—
	MSTPB10	—	Comparator C module stop setting bit
	MSTPB17	Serial peripheral interface module stop setting bit	Serial peropheral interface 0 module stop setting bit
	MSTPB21	I^2C bus interface module stop setting bit	I^2C bus interface 0 module stop setting bit
	MSTPB26	—	Serial communication interface 5 module stop setting bit
	MSTPB29	Serial communication interface 2 module stop setting bit	—
	MSTPB31	Serial communication interface 0 module stop setting bit	—
MSTPCRC	MSTPC19	—	Clock frequency accuracy measurement circuit module stop setting bit
	DSLPE	—	Deep sleep mode enable bit
DPSBYCR	IOKEEP	I/O port retention bit	—
	DPSBY	Deep software standby bit	—
DPSWCR	WTSTS[5:0]	Deep software standby waiting time setting bits	—
DPSIER	DIRQ0E	IRQ0 pin enable bit	—
	DIRQ1E	IRQ1 pin enable bit	—
	DLVDE	LVD deep standby cancel signal enable bit	—
	DNMIE	NMI pin enable bit	—

Register	Bit	RX62T	RX23T
DPSIFR	DIRQ0F	IRQ0 deep standby cancel flag	—
	DIRQ1F	IRQ1 deep standby cancel flag	—
	DLVDF	LVD deep standby cancel flag	—
	DNMIF	NMI deep standby cancel flag	—
DPSIEGR	DIRQ0EG	IRQ0 edge select bit	—
	DIRQ1EG	IRQ1 edge select bit	—
	DNMIEG	NMI edge select bit	—
RSTSR	PORF	Power-on reset flag	—
	LVD1F	LVD1 detection flag	—
	LVD2F	LVD2 detection flag	—
	DPSRSTF	Deep software standby reset flag	—
DPSBKRy		Deep software standby backup register	—
OPCCR	OPCM[2:0]	—	Operating power control mode select bits
	OPCMTSF	—	Operating power control mode transition status flag

2.6 Interrupt Controller

Table 2.10 shows a comparative listing of the interrupt controller specifications and Table 2.11 shows a comparative listing of the interrupt controller registers.

Table 2.10 Comparative Listing of Interrupt Controller Specifications

Item		RX62T (ICU)	RX23T (ICUb)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Sources: 101 • Interrupt detection: Edge detection/level detection Edge detection or level detection is determined independently for each source of the connected peripheral modules.	• Interrupts from peripheral modules • Sources: 76 • Interrupt detection: Edge detection/level detection Edge detection or level detection is determined independently for each source of the connected peripheral modules.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source.	• Interrupts from pins IRQ0 to IRQ5 • Sources: 6 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register. • Source: 1	• Interrupt generated by writing to a register. • Source: 1
	Interrupt priority level	Priority is specified by register settings.	Priority is specified by register settings.
	Fast interrupt function	Faster interrupt processing by the CPU can be specified only for a single interrupt source.	Faster interrupt processing by the CPU can be specified only for a single interrupt source.
	DTC control	DTC activation sources: 87 (78 peripheral function interrupts + 8 external pin interrupts + 1 software interrupt)	DTC activation sources: 52 (45 peripheral function interrupts + 6 external pin interrupts + 1 software interrupt)
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt at oscillation stop detection	Interrupt at oscillation stop detection
	IWDT underflow/refresh error	—	Interrupt at an underflow of the down counter or at the occurrence of a refresh error
	Voltage monitoring 1 interrupt	—	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	—	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)
	Voltage monitoring interrupt	Interrupt during power voltage fall detection	—

Item	RX62T (ICU)	RX23T (ICUb)
Return from low power consumption modes	• Sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • All-module clock stop mode: Return is initiated by a non-maskable interrupts, interrupt IRQ7 to IRQ0, or WDT interrupt. • Software standby mode: Return is initiated by a non-maskable interrupt or interrupt IRQ7 to IRQ0.	• Sleep mode: Return is initiated by a deep sleep mode, non-maskable interrupt, or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt or interrupt IRQ5 to IRQ0.

Table 2.11 Comparative Listing of Interrupt Controller Registers

Register	Bit	RX62T (ICU)	RX23T (ICUb)
IRQFLTE0	FLTEN0	—	IRQ0 digital filter enable bit
	FLTEN1	—	IRQ1 digital filter enable bit
	FLTEN2	—	IRQ2 digital filter enable bit
	FLTEN3	—	IRQ3 digital filter enable bit
	FLTEN4	—	IRQ4 digital filter enable bit
	FLTEN5	—	IRQ5 digital filter enable bit
IRQFLTC0	FCLKSEL0[1:0]	—	IRQ0 digital filter sampling clock setting bits
	FCLKSEL1[1:0]	—	IRQ1 digital filter sampling clock setting bits
	FCLKSEL2[1:0]	—	IRQ2 digital filter sampling clock setting bits
	FCLKSEL3[1:0]	—	IRQ3 digital filter sampling clock setting bits
	FCLKSEL4[1:0]	—	IRQ4 digital filter sampling clock setting bits
	FCLKSEL5[1:0]	—	IRQ5 digital filter sampling clock setting bits
NMISR	IWDTST	—	IWDT underflow/refresh error status flag
	LVDST	Voltage monitoring interrupt status flag	—
	LVD1ST	—	Voltage monitoring 1 interrupt status flag
	LVD2ST	—	Voltage monitoring 2 interrupt status flag
NMIER	IWDTEN	—	IWDT underflow/refresh error enable bit
	LVDEN	Voltage monitoring interrupt enable bit	—
	LVD1EN	—	Voltage monitoring 1 interrupt enable bit
	LVD2EN	—	Voltage monitoring 2 interrupt enable bit
NMICLR	IWDTCLR	—	IWDT clear bit
	LVD1CLR	—	LVD1 clear bit
	LVD2CLR	—	LVD2 clear bit
NMIFLTE	NFLTEN	—	NMI digital filter enable bit
NMIFLTC	NFCLKSEL[1:0]	—	NMI digital filter sampling clock setting bits

2.7 Bus

Table 2.12 shows a comparative listing of the bus specifications and Table 2.13 shows a comparative listing of the bus registers.

Table 2.12 Comparative Listing of Bus Specifications

Item		RX62T	RX23T
CPU bus	Instruction bus	• Connected to the CPU (for instructions). • Connected to the on-chip memory (on-chip RAM and on-chip ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for instructions). • Connected to the on-chip memory (on-chip RAM and on-chip ROM). • Operates in synchronization with the system clock (ICLK).
	Operand bus	• Connected to the CPU (for operand). • Connected to the on-chip memory (on-chip RAM and on-chip ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for operand). • Connected to the on-chip memory (on-chip RAM and on-chip ROM). • Operates in synchronization with the system clock (ICLK).
Memory buses	Memory bus 1	Connected to the RAM.	Connected to the RAM.
	Memory bus 2	Connected to the ROM.	Connected to the ROM.
Internal main buses	Internal main bus 1	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).
	Internal main bus 2	• Connected to the DTC. • Connected to the on-chip memory (on-chip RAM and on-chip ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the DTC. • Connected to the on-chip memory (on-chip RAM and on-chip ROM). • Operates in synchronization with the system clock (ICLK).
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (interrupt controller and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).
	Internal peripheral bus 2	• Connected to peripheral modules (WDT, CMT, CRC, SCI, etc.) • Operates in synchronization with the peripheral module clock (PCLK).	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 3	—	• Connected to peripheral modules (CMPC). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3, GPT). • Operates in synchronization with the system clock (ICLK).	• Connected to peripheral modules (MTU3). • Operates in synchronization with the peripheral module clock (PCLKA).
	Internal peripheral bus 6	• Connected to the on-chip ROM (P/E) and data flash memory. • Operates in synchronization with the peripheral module clock (PCLK).	• Connected to the flash control module. • Operates in synchronization with the FlashIF clock (FCLK).

Table 2.13 Comparative Listing of Bus Registers

Register	Bit	RX62T	RX23T
BEREN	TOEN	—	Timeout detection enable bit
BERSR1	TO	—	Timeout bit
BUSPRI	BPRA[1:0]	—	Memory bus 1 (RAM) priority control bits
	BPRO[1:0]	—	Memory bus 2 (ROM) priority control bits
	BPIB[1:0]	—	Internal peripheral bus 1 priority control bits
	BPGB[1:0]	—	Internal peripheral bus 2 and 3 priority control bits
	BPHB[1:0]	—	Internal peripheral bus 4 priority control bits
	BPFB[1:0]	—	Internal peripheral bus 6 priority control bits

2.8 Memory Protection Unit

Table 2.14 shows a comparative listing of the memory protection unit registers.

Table 2.14 Comparative Listing of Memory Protection Unit Registers

Register	Bit	RX62T	RX23T
MPESTS	IA	Instruction memory protection error generated bit	—
	IMPER	—	Instruction memory protection error generated bit
	DA	Data memory protection error generated bit	—
	DMPER	—	Data memory protection error generated bit

2.9 Data Transfer Controller

Table 2.15 shows a comparative overview of the data transfer controller and Table 2.16 shows a comparative listing of the data transfer controller registers.

Table 2.15 Comparative Overview of Data Transfer Controller

Item	RX62T (DTC)	RX23T (DTCa)
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. The maximum repeat size is 256 data units. • Block transfer mode A single activation leads to the transfer of a single block. The maximum block size is 255 data units.	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. The maximum repeat size is 256 data units. • Block transfer mode A single activation leads to the transfer of a single block. The maximum block size is 256 data units.
Transfer channels	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.
Transfer space	• 16 MB in short-address mode (areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh, excepting reserved areas) • 4 GB in full-address mode (area from 0000 0000h to FFFF FFFFh, excepting reserved areas)	• 16 MB in short-address mode (areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh, excepting reserved areas) • 4 GB in full-address mode (area from 0000 0000h to FFFF FFFFh, excepting reserved areas)
Data transfer units	• 1 data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Number of data units per block: 1 to 255	• 1 data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Number of data units per block: 1 to 256
CPU interrupt requests	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of a specified number of data units.	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of a specified number of data units.
Read skip	Transfer data read skip can be enabled.	Transfer data read skip can be enabled.

Item	RX62T (DTC)	RX23T (DTCa)
Write-back skip	When “fixed” is selected as the transfer source address or transfer destination address, write-back skip execution is supported.	When “fixed” is selected as the transfer source address or transfer destination address, write-back skip execution is supported.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.16 Comparative Listing of Data Transfer Controller Registers

Register	Bit	RX62T (DTC)	RX23T (DTCa)
DTCVBR	—	DTC vector base address (lower 12 bits)	DTC vector base address (lower 10 bits)
	—	DTC vector base address (upper 20 bits)	DTC vector base address (lower 22 bits)

2.10 I/O Ports

Table 2.17 shows a comparative listing of the I/O port registers.

Table 2.17 Comparative Listing of I/O Port Registers

Register	Bit	RX62T	RX23T
PDR	B0 to B7	—	Pm0 to Pm7 direction control bits Note: m = 0 to 4, 7, 9, A, B, D
PODR	B0 to B7	—	Pm0 to Pm7 output data storage bits Note: m = 0 to 4, 7, 9, A, B, D
PIDR	B0 to B7	—	Pm0 to Pm7 bits Note: m = 0 to 4, 7, 9, A, B, D,
PMR	B0 to B7	—	Pm0 to Pm7 pin mode control bits Note: m = 0 to 3, 7, 9, A, B, D,
ODR0	B0, B2, B4, B6	—	Pm0 to Pm3 output type select bits Note: m = 0 to 3, 7, 9, A, B, D
ODR1	B0, B2, B4, B6	—	Pm4 to Pm7 output type select bits Note: m = 2, 3, 7, 9, A, B, D
PCR	B0 to B7	—	Pm0 to Pm7 input pull-up resistor control bits Note: m = 0 to 4, 7, 9, A, B, D
DSCR	B0 to B7	—	Pm0 to Pm7 drive capacity control bits Note: m = 0 to 3, 7, 9, A, B, D
DDR	B0 to B7	Pn0 to Pn7 I/O select bits Note: n = 1 to 3, 7, 9, A, B, D, E	—
DR	B0 to B7	Pn0 to Pn7 output data storage bits Note: n = 1 to 3, 7, 9, A, B, D, E	—
PORT	B0 to B7	Pn0 bit Note: n = 1 to 4, 7, 9, A, B, D, E	—
ICR	B0 to B7	Pn0 input buffer control bits Note: n = 1 to 4, 7, 9, A, B, D	—
PFCMTU	MTUS0	MTU3 pin select 0 bit	—
	MTUS1	MTU3 pin select 1 bit	—
	TCLKS[1:0]	MTCLK pin select bits	—
PFDGPT	GPTS	GPT pin select bit	—
PFGSPI	RSPCKE	RSPCK output enable bit	—
	MOSIE	MOSI output enable bit	—
	MISOE	MISO output enable bit	—
	SSL0E	SSL0 output enable bit	—
	SSL1E	SSL1 output enable bit	—
	SSL2E	SSL2 output enable bit	—
	SSL3E	SSL3 output enable bit	—
PFHSPI	RSPIS[1:0]	RSPI pin select bits	—
PFJCAN	CANE	CAN pin enable bit	—
	CANS[1:0]	CAN pin select bits	—
PFKLIN	LINE	LIN pin enable bit	—
PFMPOE	POE0E	POE0# input enable bit	—
	POE8E	POE8# input enable bit	—
	POE10E	POE10# input enable bit	—

2.11 Multi-Function Timer Pulse Unit 3

Table 2.18 shows a comparative overview of multi-function timer pulse unit 3 and Table 2.19 shows a comparative listing of the multi-function timer pulse unit 3 registers.

Table 2.18 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX62T (MTU3)	RX23T (MTU3c)
Pulse input/output	Maximum 24	Maximum 16
Pulse input	3	3
Count clocks	6 to 8 clocks for each channel (4 clocks for channel 5)	11 clocks for each channel (14 clocks for MTU0, 12 clocks for MTU1 and MTU2, and 10 clocks for MTU5, and four clocks for MTU1 & MTU2 (LWA = 1))
Opearting frequency	8 to 100 MHz	Up to 40 MHz
Available operations	[MTU0 to MTU4, MTU6, and MTU7] • Waveform output on compare match • Input capture function • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 12-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, and MTU7] Buffer operation specifiable	[MTU0, MTU3, and MTU4] Buffer operation specifiable
	[MTU1 and MTU2] • Phase counting mode can be specified independently. • Cascade connection operation available	[MTU1 and MTU2] • Phase counting mode can be specified independently. • Cascade connection operation available
	[MTU3, MTU4, MTU6, and MTU7] • Through interlocked operation of MTU3/MTU4 and MTU6/MTU7, the positive and negative signals in six phases, for a total of 12 phases, can be output in complementary PWM and reset PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers is supported at peaks and troughs of the timer-counter values or when writing to the buffer registers (MTU4.TGRD and MTU7.TGRD). • Double-buffering is selectable in complementary PWM mode.	[MTU3 and MTU4] • Through interlocked operation of MTU3/MTU4, the positive and negative signals in six phases, for a total of 6 phases, can be output in complementary PWM and reset PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers is supported at peaks and troughs of the timer-counter values or when writing to the buffer registers (MTU4.TGRD). • Double-buffering is selectable in complementary PWM mode.

Item	RX62T (MTU3)	RX23T (MTU3c)
Available operations	[MTU3 and MTU4] Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output can be enabled, allowing the selection between two types of waveform output (chopping or level).	[MTU3 and MTU4] Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output can be enabled, allowing the selection between two types of waveform output (chopping or level).
	[MTU5] Support for operation as a dead-time compensation counter	[MTU5] Support for operation as a dead-time compensation counter
Interrupt skipping function	In complementary PWM mode, interrupts at counter peaks and troughs and triggers to start conversion by the A/D converter can be skipped.	In complementary PWM mode, interrupts at counter peaks and troughs and triggers to start conversion by the A/D converter can be skipped.
Interrupt sources	38	28
Buffer operation	Automatic transfer of register data (transfer from the buffer register to the timer register)	Automatic transfer of register data (transfer from the buffer register to the timer register)
Trigger generation	A/D converter start triggers can be generated.	A/D converter start triggers can be generated.
	An A/D converter start request delaying function enables the A/D converter to be started at user-defined timing and to be synchronized with PWM output.	An A/D converter start request delaying function enables the A/D converter to be started at user-defined timing and to be synchronized with PWM output.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.19 Comparative Listing of Multi-Function Timer Pulse Unit 3 Registers

Register	Bit	RX62T (MTU3)	RX23T (MTU3c)
TCR2	TPSC2[2:0]	—	Timer prescaler select bits
	PCB[1:0]	—	Phase counting mode function expansion control bits
TMDR2B	DRS	Double buffer select bit	—
TMDR3	LWA	—	Longword access control bit
	PHCKSEL	—	External input phase clock select bit
TSR	TGFA	Input capture/output compare flag A	—
	TGFB	Input capture/output compare flag B	—
	TGFC	Input capture/output compare flag C	—
	TGFD	Input capture/output compare flag D	—
	TCFV	Overflow flag	—
	TCFU	Underflow flag	—
TSYCR	CE2B	Clear enable 2B bit	—
	CE2A	Clear enable 2A bit	—
	CE1B	Clear enable 1B bit	—
	CE1A	Clear enable 1A bit	—
	CE0D	Clear enable 0D bit	—
	CE0C	Clear enable 0C bit	—
	CE0B	Clear enable 0B bit	—
	CE0A	Clear enable 0A bit	—
TCNTLW	—	—	Timer longword counter
TGRnLW (n = A or B)	—	—	Timer longword general register
TCSYSTR	SCH7	Synchronous start 7 bit	—
	SCH6	Synchronous start 6 bit	—
TRWERB	RWE	Read/write enable bit	—
TOCR1B	OLSP	Output level select P bit	—
	OLSN	Output level select N bit	—
	TOCS	TOC select bit	—
	TOCL	TOC register write protection bit	—
	PSYE	PWM synchronous output enable bit	—
TOCR2B	OLS1P	Output level select 1P bit	—
	OLS1N	Output level select 1N bit	—
	OLS2P	Output level select 2P bit	—
	OLS2N	Output level select 2N bit	—
	OLS3P	Output level select 3P bit	—
	OLS3N	Output level select 3N bit	—
	BF[1:0]	TOLBR buffer transfer timing select bits	—
TOLBRB	OLS1P	Output level select 1P bit	—
	OLS1N	Output level select 1N bit	—
	OLS2P	Output level select 2P bit	—
	OLS2N	Output level select 2N bit	—
	OLS3P	Output level select 3P bit	—
	OLS3N	Output level select 3N bit	—
TCNTSB	—	Timer subcounter	—
TCDRB	—	Timer cycle data register	—
TCBRB	—	Timer cycle buffer register	—
TDDRB	—	Timer dead time data register	—

Register	Bit	RX62T (MTU3)	RX23T (MTU3c)
TDERB	TDER	Dead time enable bit	—
TBTERB	BTE[1:0]	Buffer transfer disable and interrupt skipping link setting bits	—
TWCRA	SCC	Synchronous clearing control bit	—
TWCRB	WRE	Waveform retain enable bit	—
	SCC	Synchronous clearing control bit	—
	CCE	Compare match clear enable bit	—
NFCRn (n = 0 to 4, C)	NFAEN	—	Noise filter A enable bit
	NFBEN	—	Noise filter B enable bit
	NFCEN	—	Noise filter C enable bit
	NFDEN	—	Noise filter D enable bit
	NFCS[1:0]	—	Noise filter clock select bits
NFCR5	NFUEN	—	Noise filter U enable bit
	NFVEN	—	Noise filter V enable bit
	NFWEN	—	Noise filter W enable bit
	NFCS[1:0]	—	Noise filter clock select bits
TITMRB	TITM	Interrupt skipping function select bit	—
TITCR1B	T4VCOR[2:0]	TCIV4 interrupt skipping count setting bits	—
	T4VEN	T4VEN bit	—
	T3ACOR[2:0]	TCIV3 interrupt skipping count setting bits	—
	T3AEN	T3AEN bit	—
TITCNT1B	T4VCNT[2:0]	TGIA4 interrupt counter bits	—
	T3ACNT[2:0]	TGIA3 interrupt counter bits	—
TITCR2B	TRG4COR [2:0]	TRG4AN/TRG4BN interrupt skipping count setting bits	—
TITCNT2B	TRG4CNT [2:0]	TRG4AN/TRG4BN interrupt counter bits	—
TADSTRGR0	TADSTRS0 [4:0]	—	A/D conversion start request select for ADSM0 pin output frame synchronization signal generation select bits

2.12 Port Output Enable 3

Table 2.20 shows a comparative overview of port output enable 3 and Table 2.21 shows a comparative listing of the port output enable 3 registers.

Table 2.20 Comparative Overview of Port Output Enable 3

Item	RX62T (POE3)	RX23T (POE3b)
Target pins to be placed in high-impedance state	• MTU output pins MTU0 pins (MTIOC0A-A, MTIOC0A-B, MTIOC0B-A, MTIOC0B-B, MTIOC0C, MTIOC0D) MTU3 pins (MTIOC3B, MTIOC3D) MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) MTU6 pins (MTIOC6B, MTIOC6D) MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) • GPT output pins GPT0 pins (GTIOC0A-A, GTIOC0B-A, GTIOC0A-B, GTIOC0B-B) GPT1 pins (GTIOC1A-A, GTIOC1B-A, GTIOC1A-B, GTIOC1B-B) GPT2 pins (GTIOC2A-A, GTIOC2B-A, GTIOC2A-B, GTIOC2B-B) GPT3 pins (GTIOC3A, GTIOC3B)	• MTU output pins MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) MTU3 pin (MTIOC3B, MTIOC3D) MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)
Conditions for high-impedance state	• Change to input pin When input is received on POE0#, POE4#, POE8#, POE10#, or POE11# • Shorting of output pins When a match (short circuit) occurs between the output signal levels (active level) over one or more cycles on the following combination of pins: 1. MTIOC3B and MTIOC3D 2. MTIOC4A and MTIOC4C 3. MTIOC4B and MTIOC4D 4. MTIOC6B and MTIOC6D 5. MTIOC7A and MTIOC7C 6. MTIOC7B and MTIOC7D 7. GTIOC0A-A and GTIOC0B-A 8. GTIOC1A-A and GTIOC1B-A 9. GTIOC2A-A and GTIOC2B-A • When a register setting is made • When clock generation circuit oscillation stop is detected • When comparator detection occurs in the comparator (S12ADA)	• Change to input pin When input is received on POE0#, POE8#, or POE10# • Shorting of output pins When a match (short circuit) occurs between the output signal levels (active level) over one or more cycles on the following combination of pins: 1. MTIOC3B and MTIOC3D 2. MTIOC4A and MTIOC4C 3. MTIOC4B and MTIOC4D • When a register setting is made • When clock generation circuit oscillation stop is detected • When comparator detection occurs in the comparator (CMPC)

Item	RX62T (POE3)	RX23T (POE3b)
Functions	• Each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling.	• Each of the POE0#, POE8#, and POE10# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling.
	• Pins for the MTU complementary PWM output, MTU0 pins, and GPT pins can be placed in the high-impedance state by the POE0#, POE4#, POE8#, POE10#, or POE11# pin falling-edge or low-level sampling.	• Pins for the MTU complementary PWM output and MTU0 pins can be placed in the high-impedance state by the POE0#, POE8#, or POE10# pin falling-edge or low-level sampling.
	• Pins for the MTU complementary PWM output, MTU0 pins, and GPT pins can be placed in the high-impedance state when the oscillation-stop detection circuit in the clock pulse generator detects stopped oscillation.	• Pins for the MTU complementary PWM output and MTU0 pins can be placed in the high-impedance state when oscillation stop is detected by the oscillation stop detection function of the clock generator.
	• Pins for the MTU complementary PWM output or the GPT large-current output pins can be placed in the high-impedance state when output levels of the MTU complementary PWM output pins or the GPT large-current output pins are compared and simultaneous active-level output continues for one cycle or more.	• Pins for the MTU complementary PWM output can be placed in the high-impedance state when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.
	• Pins for the MTU complementary PWM output, MTU0 pins, and GPT pins can be placed in the high-impedance state in response to comparator detection by the 12-bit A/D converter (S12ADA).	• Pins for the MTU complementary PWM output and MTU0 pins can be placed in the high-impedance state in response to comparator detection by the comparator (CMPC).
	• Pins for the MTU complementary PWM output, MTU0 pins, and GPT pins can be placed in the high-impedance state by modifying settings in the POE3 registers.	• Pins for the MTU complementary PWM output and MTU0 pins can be placed in the high-impedance state by modifying the settings in the POE3 registers.
	• Interrupts can be generated by input-level sampling or output-level comparison results.	• Interrupts can be generated by input-level sampling or output-level comparison results.

Table 2.21 Comparative Listing of Port Output Enable 3 Registers

Register	Bit	RX62T (POE3)	RX23T (POE3b)
ICSR2	POE4M[1:0]	POE4 mode select bits	—
	PIE2	Port interrupt enable bit	—
	POE4F	POE4 flag	—
OCSR2	OIE2	Output short interrupt enable 2 bit	—
	OCE2	Output short high-impedance enable 2 bit	—
	OSF2	Output short flag 2	—
ICSR5	POE11M[1:0]	POE11 mode select bits	—
	PIE5	Port interrupt enable bit	—
	POE11E	POE11 high-impedance enable bit	—
	POE11F	POE11 flag	—
ICSR6	OSTSTE	—	OSTST high-impedance enable bit
	OSTSTF	—	OSTST high-impedance flag
ALR1	OLSG0A	MTIOC3B/GTIOC0A-A active level setting bit	MTIOC3B active level setting bit
	OLSG0B	MTIOC3D/GTIOC0B-A active level setting bit	MTIOC3D active level setting bit
	OLSG1A	MTIOC4A/GTIOC1A-A active level setting bit	MTIOC4A active level setting bit
	OLSG1B	MTIOC4C/GTIOC1B-A active level setting bit	MTIOC4C active level setting bit
	OLSG2A	MTIOC4B/GTIOC2A-A active level setting bit	MTIOC4B active level setting bit
	OLSG2B	MTIOC4D/GTIOC2B-A active level setting bit	MTIOC4D active level setting bit
SPOER	MTUCH67HIZ	MTU6 and MTU7 output high-impedance enable bit	—
	GPT01HIZ	GPT0 and GPT1 output high-impedance enable bit	—
	GPT23HIZ	GPT2 and GPT3 output high-impedance enable bit	—
POECR1	MTU0AZE	MTU CH0A high-impedance enable bit	MTIOC0A PB3 pin high-impedance enable bit
	MTU0BZE	MTU CH0B high-impedance enable bit	MTIOC0B PB2 pin high-impedance enable bit
	MTU0CZE	MTU CH0C high-impedance enable bit	MTIOC0C PB1 pin high-impedance enable bit
	MTU0DZE	MTU CH0D high-impedance enable bit	MTIOC0D PB0 pin high-impedance enable bit
	MTU0A1ZE	—	MTIOC0A P31 pin high-impedance enable bit
	MTU0B1ZE	—	MTIOC0B P30 pin high-impedance enable bit
	MTU0B2ZE	—	MTIOC0B P93 pin high-impedance enable bit
	MTU0C1ZE	—	MTIOC0C P94 pin high-impedance enable bit

Register	Bit	RX62T (POE3)	RX23T (POE3b)
POECR2	MTU7BDZE	MTU CH7BD high-impedance enable bit	—
	MTU7ACZE	MTU CH7AC high-impedance enable bit	—
	MTU6BDZE	MTU CH6BD high-impedance enable bit	—
	MTU4BDZE	MTU CH4BD high-impedance enable bit	MTIOC4B/4D high-impedance enable bit
	MTU4ACZE	MTU CH4AC high-impedance enable bit	MTIOC4A/4C high-impedance enable bit
	MTU3BDZE	MTU CH3BD high-impedance enable bit	MTIOC3B/3D high-impedance enable bit
POECR3	GPT0ABZE	GPT CH0AB high-impedance enable bit	—
	GPT1ABZE	GPT CH1AB high-impedance enable bit	—
	GPT2ABZE	GPT CH2AB high-impedance enable bit	—
	GPT3ABZE	GPT CH3AB high-impedance enable bit	—
POECR4	CMADDMT34ZE	MTU CH34 high-impedance CFLAG add bit	MTU3 and MTU4 high-impedance CFLAG add bit
	IC2ADDMT34ZE	MTU CH34 high-impedance POE4F add bit	—
	IC3ADDMT34ZE	MTU CH34 high-impedance POE8F add bit	MTU3 and MTU4 high-impedance POE8F add bit
	IC4ADDMT34ZE	MTU CH34 high-impedance POE10F add bit	MTU3 and MTU4 high-impedance POE10F add bit
	IC5ADDMT34ZE	MTU CH34 high-impedance POE11F add bit	—
	CMADDMT67ZE	MTU CH67 high-impedance CFLAG add bit	—
	IC1ADDMT67ZE	MTU CH67 high-impedance POE0F add bit	—
	IC3ADDMT67ZE	MTU CH67 high-impedance POE8F add bit	—
	IC4ADDMT67ZE	MTU CH67 high-impedance POE10F add bit	—
	IC5ADDMT67ZE	MTU CH67 high-impedance POE11F add bit	—
POECR5	CMADDMT0ZE	MTU CH0 high-impedance CFLAG add bit	MTU0 high-impedance CFLAG add bit
	IC1ADDMT0ZE	MTU CH0 high-impedance POE0F add bit	MTU0 high-impedance POE0F add bit
	IC2ADDMT0ZE	MTU CH0 high-impedance POE4F add bit	—
	IC4ADDMT0ZE	MTU CH0 high-impedance POE10F add bit	MTU0 high-impedance POE10F add bit
	IC5ADDMT0ZE	MTU CH0 high-impedance POE11F add bit	—

Register	Bit	RX62T (POE3)	RX23T (POE3b)
POECR6	CMADDGPT01ZE	GPT CH01 high-impedance CFLAG add bit	—
	IC1ADDGPT01ZE	GPT CH01 high-impedance POE0F add bit	—
	IC2ADDGPT01ZE	GPT CH01 high-impedance POE4F add bit	—
	IC3ADDGPT01ZE	GPT CH01 high-impedance POE8F add bit	—
	IC5ADDGPT01ZE	GPT CH01 high-impedance POE11F add bit	—
	CMADDGPT23ZE	GPT CH23 high-impedance CFLAG add bit	—
	IC1ADDGPT23ZE	GPT CH23 high-impedance POE0F add bit	—
	IC2ADDGPT23ZE	GPT CH23 high-impedance POE4F add bit	—
	IC3ADDGPT23ZE	GPT CH23 high-impedance POE8F add bit	—
	IC4ADDGPT23ZE	GPT CH23 high-impedance POE10F add bit	—
POECMPFR	C0FLAG	—	Comparator channel 0 detection flag
	C1FLAG	—	Comparator channel 1 detection flag
	C2FLAG	—	Comparator channel 2 detection flag
	C3FLAG	—	Comparator channel 3 detection flag
POECMPSEL	POEREQ0	—	Comparator channel 0 POE request enable bit
	POEREQ1	—	Comparator channel 1 POE request enable bit
	POEREQ2	—	Comparator channel 2 POE request enable bit
	POEREQ3	—	Comparator channel 3 POE request enable bit

2.13 Independent Watchdog Timer

Table 2.22 shows a comparative overview of the independent watchdog timer and Table 2.23 shows a comparative listing of the independent watchdog timer registers.

Table 2.22 Comparative Overview of Independent Watchdog Timer

Item	RX62T (IWDT)	RX23T (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Counting starts automatically after a reset (auto-start mode). • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows is generated.	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. Counting restarts. (In auto-start mode, counting restarts automatically after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after a refresh.)
Window function		Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Reset output sources	• Down-counter underflow	• Down-counter underflow • Refresh occurring outside the refresh-permitted period (refresh error)
Non-maskable interrupt sources		• Down-counter underflow • Refresh occurring outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the IWDTSR register.	The down-counter value can be read by reading the IWDTSR register.
Output signals (internal signals)	• Reset output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX62T (IWDT)	RX23T (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	—	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

Table 2.23 Comparative Listing of Independent Watchdog Timer Registers

Register	Bit	RX62T (IWDT)	RX23T (IWDTa)
IWDTCR	RPES[1:0]	—	Window end position select bits
	RPSS[1:0]	—	Window start position select bits
IWDTSR	REFEF	—	Refresh error flag
IWDTRCR	RSTIRQS	—	Reset interrupt request select bit
IWDTCSTPR	SLCSTP	—	Sleep mode count stop control bit
OFS0	IWDTSTRT	—	IWDT start mode select bit
	IWDTTOPS[1:0]	—	IWDT timeout period select bits
	IWDTCKS[3:0]	—	IWDT clock frequency division ratio select bits
	IWDTRPES[1:0]	—	IWDT window end position select bits
	IWDTRPSS[1:0]	—	IWDT window start position select bits
	IWDTRSTIRQS	—	IWDT reset interrupt request select bit
	IWDTSLCSTP	—	IWDT sleep mode count stop control bit

2.14 Serial Communication Interface

Table 2.24 shows a comparative overview of the serial communication interface and Table 2.25 shows a comparative listing of the serial communication interface registers.

Table 2.24 Comparative Overview of Serial Communication Interface

Item	RX62T (SCIb)	RX23T (SCIg)
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed	Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication	• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.	• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.
I/O pins	• SCI/SMCI I/O pins SCK0, RXD0, TKD0, SCK1, RXD1, TXD1, SCK2, RXD2, and TKD2	• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK1, RXD1, TXD1, CTS1#/RTS1#, SCK5, RXD5, TXD5, and CTS5#/RTS5# • SCI I/O pins (simple I²C mode) SSCL1, SSDA1, SSCL5, and SSDA5 • SCI I/O pins (simple SPI mode) SCK1, SMISO1, SMOSI1, SS1#, SCK5, SMISO5, SMOSI5, and SS5#
Data transfer	Selectable between LSB-first or MSB-first transfer.	Selectable between LSB-first or MSB-first transfer.
Interrupt sources	Transmit end, transmit data empty, receive data full, or receive error	Transmit end, transmit data empty, receive data full, receive error Completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function	The module stop state can be specified for each channel.	The module stop state can be specified for each channel.

Item		RX62T (SCIb)	RX23T (SCIg)
Synchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	—	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Selectable between low level and falling edge.	Selectable between low level and falling edge.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	• An internal or external clock can be selected.	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	—	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	—	I^2C bus format
	Operatin mode	—	Master (single-master operation only)
	Transfer speed	—	Fast mode is supported.
	Noise canceler	—	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.

Item		RX62T (SCIb)	RX23T (SCIg)
Simple SPI mode	Data length	—	8 bits
	Error detection	—	Overrun error
	SS input pin function	—	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	—	Selectable among four clock phase and clock polarity settings.
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.

Table 2.25 Comparative Listing of Serial Communication Interface Registers

Register	Bit	RX62T (SCIb)	RX23T (SCIg)
RDRH	—	—	Receive data register H
RDRL	—	—	Receive data register L
RDRHL	—	—	Receive data register HL
TDRH	—	—	Transmit data register H
TDRL	—	—	Transmit data register L
TDRHL	—	—	Transmit data register HL
SSR	RDRF	Receive data full flag	—
	TDRE	Transmit data empty flag	—
SCMR	CHR1	—	Character length 1 bit
MDDR		—	Modulation duty register
SEMR	ACS0	—	Asynchronous mode clock source select bit
	BRME	—	Bit rate modulation enable bit
	BGDM	—	Baud rate generator double-speed mode select bit
SNFR	NFCS[2:0]	—	Noise filter clock select bits
SIMR1	IICM	—	Simple I^2C mode select bit
	IICDL[4:0]	—	SSDA output delay select bits
SIMR2	IICINTM	—	I^2C interrupt mode select bit
	IICCSC	—	Clock synchronization bit
	IICACKT	—	ACK transmission data bit
SIMR3	IICSTAREQ	—	Start condition generation bit
	IICRSTAREQ	—	Restart condition generation bit
	IICSTPREQ	—	Stop condition generation bit
	IICSTIF	—	Issuing of start, restart, or stop condition completed flag
	IICSDAS[1:0]	—	SSDA output select bits
	IICSCLS[1:0]	—	SSCL output select bits
SISR	IICACKR	—	ACK reception data flag
SPMR	SSE	—	SSn# pin function enable bit
	CTSE	—	CTS enable bit
	MSS	—	Master slave select bit
	MFF	—	Mode fault flag
	CKPOL	—	Clock polarity select bit
	CKPH	—	Clock phase select bit

2.15 I²C bus interface

Table 2.26 shows a comparative overview of the I²C bus interface and Table 2.27 shows a comparative listing of the I²C bus interface registers.

Table 2.26 Comparative Overview of I²C Bus Interface

Item	RX62T (RIIC)	RX23T (RIICa)
Communication format	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Fast mode is supported (up to 400 kbps).	Fast mode is supported (up to 400 kbps).
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detection conditions	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.
Slave addresses	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is loaded automatically. Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is loaded automatically. Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: Wait between the eighth and ninth clock cycles Wait between the ninth and first clock cycles	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: Wait between the eighth and ninth clock cycles Wait between the ninth and first clock cycles
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX62T (RIIC)	RX23T (RIICa)
Arbitration	• Multi-master support Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.	• Multi-master support Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.
Timeout detection function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise canceler	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources • Communication error or event occurrence Arbitration detection, NACK detection, timeout detection, start condition detection (including restart condition), stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end	Four sources • Communication error or event occurrence Arbitration detection, NACK detection, timeout detection, start condition detection (including restart condition), stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Transition to module stop state can be specified.	Transition to module stop state can be specified.
RIIC operating modes	Four Master transmit mode, master receive mode, slave transmit mode, and slave receive mode	Four Master transmit mode, master receive mode, slave transmit mode, and slave receive mode

Table 2.27 Comparative Listing of I²C Bus Interface Registers

Register	Bit	RX62T (RIIC)	RX23T (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNT		Timeout internal counter	—

2.16 Serial Peripheral Interface

Table 2.28 shows a comparative overview of the serial peripheral interface and Table 2.29 shows a comparative listing of the serial peripheral interface registers.

Table 2.28 Comparative Overview of Serial Peripheral Interface

Item	RX62T (RSPI)	RX23T (RSPIa)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Serial communication is available in master and slave mode. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.
Data format	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK
Buffer configuration	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection

Item	RX62T (RSPI)	RX23T (RSPIa)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay)Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified.	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function
Interrupt sources	Interrupt sources: Receive buffer full interrupt, transmit buffer empty interrupt, RSPI error interrupt (mode fault, overrun, parity error), RSPI idle interrupt (RSPI idle)	Interrupt sources: Receive buffer full interrupt, transmit buffer empty interrupt, RSPI error interrupt (mode fault, overrun, parity error), RSPI idle interrupt (RSPI idle)
Other functions	• Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.29 Comparative Listing of Serial Peripheral Interface Registers

Register	Bit	RX62T (RSPI)	RX23T (RSPIa)
SPDCR	SLSEL[1:0]	SSL pin output select bits	—
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit

2.17 12-Bit A/D Converter

Table 2.30 shows a comparative overview of the 12-bit A/D converter and Table 2.31 shows a comparative listing of the 12-bit A/D converter registers.

Table 2.30 Comparative Overview of 12-Bit A/D Converter

Item	RX62T (S12ADA)	RX23T (S12ADE)
Number of units	2 units	1 unit
Input channels	8 channels (4 channels × 2 units)	10 channels
Extended analog function	—	Internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	• 1.0 µs per channel (when operating with A/D conversion clock ADCLK = 50 MHz and AVCC0 = 4.0 V to 5.5 V) • 2.0 µs per channel (when operating with A/D conversion clock ADCLK = 25 MHz and AVCC0 = 3.0 V to 3.6 V)	• 1.0 µs per channel (when operating with A/D conversion clock ADCLK = 40 MHz)
A/D conversion clock	• Settable to PCLK divided by 1, 2, 4, or 8 (ADCSR.CKS[1:0]).	• Settable to ICLK divided by 1, 2, 4, 8, 16, 32, or 64 (SCKCR.PCKD[3:0]). • Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio is one of the following: PCLK:ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• 10 registers for analog input • 2 registers for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • Output with 12-bit accuracy supported for A/D conversion results.	• 10 registers for analog input, 1 for A/D-converted data duplication in double trigger mode, and 2 for A/D-converted data duplication during extended operation in double trigger mode • 1 register for internal reference voltage • 1 register for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • Output with 12-bit accuracy supported for A/D conversion results.

Item	RX62T (S12ADA)	RX23T (S12ADE)
Data register		• The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating mode	• Single mode: Analog inputs of one channel are converted only once. • Single-cycle scan mode: Analog inputs of up to four channels are converted only once. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 4 channels. • 2-channel scan mode: Channels in each unit are divided into two groups and the conversion startup source can be selected separately for each group.	• Single scan mode: A/D conversion is performed only once on the analog inputs of up to 10 channels arbitrarily selected. A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 10 channels. • Group scan mode: Analog inputs of up to 10 user-selected channels are divided into group A and group B, and A/D conversion of the analog input selected on a group basis is performed only once. The conditions for scanning start of group A and group B (synchronous trigger) can be selected independently, allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A has priority): If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be specified.

Item	RX62T (S12ADA)	RX23T (S12ADE)
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by multi-function timer pulse unit 3 (MTU3) or the general PWM timer (GPT). • Asynchronous trigger A/D conversion can be externally triggered from the ADTRG0# pin for S12AD0 and from the ADTRG1# pin for S12AD1.	• Software trigger • Synchronous trigger Conversion start is triggered by the multi-function timer pulse unit 3 (MTU3c) or the 8-bit timer (TMR). • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.
Functions	• Channel-dedicated sample-and-hold function (3 channels) • Self-diagnostic function for 12-bit A/D converter • Input signal amplification function using programmable gain amplifier (3 channels per unit) • Window comparator function (3 channels per unit)	• Channel-dedicated sample-and-hold function (3 channels) • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function for A/D data registers
Interrupt source	• An interrupt request (S12ADI) can be generated on completion of A/D conversion in each unit. • A S12ADI interrupt can activate the data transfer controller (DTC).	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of a group B scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a double scan of group A, whereas an A/D scan end interrupt request (GBADI) specifically for group B can be generated on completion of a group B scan. • The S12ADI and GBADI interrupts can activate the data transfer controller (DTC).

Item	RX62T (S12ADA)	RX23T (S12ADE)
Interrupt source	• An interrupt request (CMPI) can be generated when comparator detection occurs (can also be used for a POE source).	
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.31 Comparative Listing of 12-Bit A/D Converter Registers

Register	Bit	RX62T (S12ADA)	RX23T(S12ADE)
ADDBLDR		—	A/D data duplication register
ADDBLDRA		—	A/D data duplication register A
ADDBLDRB		—	A/D data duplication register B
ADOCDR		—	A/D internal reference voltage data register
ADCSR	CKS[1:0]	Clock select bits	—
	DBLANS[4:0]	—	Double trigger channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
ADANS	PG000EN	AN000 programmable gain amplifier enable bit	—
	PG001EN	AN001 programmable gain amplifier enable bit	—
	PG002EN	AN002 programmable gain amplifier enable bit	—
	PG000SEL	AN000 programmable gain amplifier select bit	—
	PG001SEL	AN001 programmable gain amplifier select bit	—
	PG002SEL	AN002 programmable gain amplifier select bit	—
	CH[1:0]	Channel setting bits	—

Register	Bit	RX62T (S12ADA)	RX23T(S12ADE)
ADANSA0	ANSA000	—	A/D conversion channel select select bits
	ANSA001	—	A/D conversion channel select select bits
	ANSA002	—	A/D conversion channel select select bits
	ANSA003	—	A/D conversion channel select select bits
	ANSA004	—	A/D conversion channel select select bits
	ANSA005	—	A/D conversion channel select select bits
	ANSA006	—	A/D conversion channel select select bits
	ANSA007	—	A/D conversion channel select select bits
ADANSA1	ANSA100	—	A/D conversion channel select select bits
	ANSA101	—	A/D conversion channel select select bits
ADANSB0	ANSB000	—	A/D conversion channel select select bits
	ANSB001	—	A/D conversion channel select select bits
	ANSB002	—	A/D conversion channel select select bits
	ANSB003	—	A/D conversion channel select select bits
	ANSB004	—	A/D conversion channel select select bits
	ANSB005	—	A/D conversion channel select select bits
	ANSB006	—	A/D conversion channel select select bits
	ANSB007	—	A/D conversion channel select select bits
ADANSB1	ANSB100	—	A/D conversion channel select select bits
	ANSB101	—	A/D conversion channel select select bits
ADADS0	ADS000	—	A/D-converted value addition/average channel select bits
	ADS001	—	A/D-converted value addition/average channel select bits
	ADS002	—	A/D-converted value addition/average channel select bits
	ADS003	—	A/D-converted value addition/average channel select bits
	ADS004	—	A/D-converted value addition/average channel select

Register	Bit	RX62T (S12ADA)	RX23T(S12ADE)
			bits
	ADS005	—	A/D-converted value addition/average channel select bits
	ADS006	—	A/D-converted value addition/average channel select bits
	ADS007	—	A/D-converted value addition/average channel select bits
ADADS1	ADS100	—	A/D-converted value addition/average channel select bits
	ADS101	—	A/D-converted value addition/average channel select bits
ADADC	ADC[2:0]	—	Addition count select bits
	AVEE	—	Average mode enable bit
ADCER	SHBYP	Dedicated sample-and-hold circuit select bit	—
	ADPRC[1:0]	A/D data register bit precision setting bits	—
	ADIE2	2-channel scan interrupt select select bit	—
	ADIEW	Double trigger interrupt select bit	—
ADSTRGR	ADSTRS0[4:0]	A/D start trigger group 0 select bits	—
	TRSB[5:0]	—	A/D conversion start trigger for group B select bits
	ADSTRS1[4:0]	A/D start trigger group 1 select bits	—
	TRSA[5:0]	—	A/D conversion start trigger select bits
ADPG	PG000GAIN[3:0]	AN000 programmable gain amplifier gain select bits	—
	PG001GAIN[3:0]	AN001 programmable gain amplifier gain select bits	—
	PG002GAIN[3:0]	AN002 programmable gain amplifier gain select bits	—
ADCMPMD0	CEN000[1:0]	AN000 comparator select bits	—
	CEN001[1:0]	AN001 comparator select bits	—
	CEN002[1:0]	AN002 comparator select bits	—
	CEN100[1:0]	AN100 comparator select bits	—
	CEN101[1:0]	AN101 comparator select bits	—
	CEN102[1:0]	AN102 comparator select bits	—
ADCMPMD1	REFL[2:0]	Internal voltage for comparator low reference voltage select bits	—
	REFH[2:0]	Internal voltage for comparator high reference voltage select bits	—
	CSEL0	AN000 to AN002 comparator input select bit	—
	VSELH0	AN000 to AN002 comparator high reference voltage select bit	—

Register	Bit	RX62T (S12ADA)	RX23T(S12ADE)
	VSELL0	AN000 to AN002 comparator low reference voltage select bit	—
	CSEL1	AN100 to AN102 comparator input select bit	—
	VSELH1	AN100 to AN102 comparator high reference voltage select bit	—
	VSELL1	AN100 to AN102 comparator low reference voltage select bit	—
ADCMPNR0	C000NR[3:0]	AN000 comparator noise cancellation filter mode select bits	—
	C001NR[3:0]	AN001 comparator noise cancellation filter mode select bits	—
	C002NR[3:0]	AN002 comparator noise cancellation filter mode select bits	—
ADCMPNR1	C100NR[3:0]	AN100 comparator noise cancellation filter mode select bits	—
	C101NR[3:0]	AN101 comparator noise cancellation filter mode select bits	—
	C102NR[3:0]	AN102 comparator noise cancellation filter mode select bits	—
ADCMPFR	C000FLAG	AN000 comparator detection flag	—
	C001FLAG	AN001 comparator detection flag	—
	C002FLAG	AN002 comparator detection flag	—
	C100FLAG	AN100 comparator detection flag	—
	C101FLAG	AN101 comparator detection flag	—
	C102FLAG	AN102 comparator detection flag	—
ADCMPSEL	SEL000	AN000 comparator detection select bit	—
	SEL001	AN001 comparator detection select bit	—
	SEL002	AN002 comparator detection select bit	—
	SEL100	AN100 comparator detection select bit	—
	SEL101	AN101 comparator detection select bit	—
	SEL102	AN102 comparator detection select bit	—
	IE	Interrupt enable setting bit	—
	POERQ	POE request setting bit	—
ADEXICR	OCSAD	—	Internal reference voltage A/D-converted value addition/average mode select bit
	OCSA	—	Internal reference voltage A/D conversion select bit
ADSHCR	SSTSH[7:0]	—	Channel-dedicated sample-and-hold circuit sampling time setting bits
	SHANS[2:0]	—	Channel-dedicated sample-and-hold circuit bypass select bits

Register	Bit	RX62T (S12ADA)	RX23T(S12ADE)
ADDISCR	ADNDIS[4:0]	—	A/D disconnection detection assist setting bits
ADGSPCR	PGS	—	Group A priority control setting bit
	GBRSCN	—	Group B restart setting bit
	GBRP	—	Group B single scan continuous start bit
ADHVREFCNT	HVSEL	—	High-potential reference voltage select bit
	LVSEL	—	Low-potential reference voltage select bit

2.18 RAM

Table 2.32 shows a comparative overview of the RAM.

Table 2.32 Comparative Overview of RAM

Item	RX62T	RX23T
RAM capacity	16 KB or 8 KB	12 KB
RAM address	0000 0000h to 0000 3FFFh (16 KB) 0000 0000h to 0000 1FFFh (8 KB)	0000 0000h to 0000 27FFh, 0000 4000h to 0000 4A7Fh (12 KB)
Access	• Single-cycle access is possible for both reading and writing. • The on-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The on-chip RAM can be enabled or disabled.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

2.19 Flash Memory

Table 2.33 shows a comparative listing of the flash memory specifications and Table 2.34 shows a comparative listing of the flash memory registers.

Table 2.33 Comparative Listing of Flash Memory Specifications

	RX62T		RX23T
Item	Flash Memory for Code Storage	Flash Memory for Data Storage	
Memory space	User area: 256 KB, 128 KB, or 64 KB	Data area: 32 KB or 8 KB	User area: Maximum 128 KB
Read cycle	High-speed read operation using 1 cycle of ICLK is supported.	A read operation in word or byte units takes 3 cycles of PCLK.	No ROM wait cycles when ICLK ≤ 32 MHz, ROM wait cycle when ICLK > 32 MHz
Value after erase	Can be read as FFFF FFFFh in 32-bit access.	Undetermined	FFh
Interrupt	A flash ready interrupt request (FRDYI) is generated upon completion of FCU command execution (program, P/E suspend, blank check, peripheral clock notify).	A flash ready interrupt request (FRDYI) is generated upon completion of FCU command execution (program, P/E suspend, lock bit read 2, peripheral clock notify).	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
Programming/ erasing method	—		• Software commands • The following software commands are implemented: Program, blank check, block erase, all-block erase • The following commands are implemented for programming the extra area:

Item	RX62T		RX23T
	Flash Memory for Code Storage	Flash Memory for Data Storage	
Programming/ erasing method	• On-chip dedicated sequencer (FCU) for programming of the ROM • Programming and erasing the ROM are handled by issuing commands to the FCU. • The ROM in the erased state can be read as FFFF FFFFh in 32-bit access.		—
Background operation (BGO) function	• The CPU is able to execute program code from areas other than the ROM or data flash while the ROM is being programmed or erased. • Execution of program code from the ROM is possible while the data flash memory is being programmed or erased.		—
Suspension and resumption functions	• The CPU is able to execute program code from the ROM when programming or erasure of the ROM is suspended. • Programming and erasure of the ROM can be restarted (resumed) after suspension.		—
Units of programming and erasure	• Unit of programming for the user area: 256 bytes • Units of erasure for the user area: 4 KB (8 blocks), 16 KB (when the ROM size is 256 KB: 14 blocks, when the ROM size is 128 KB: 6 blocks, and when the ROM size is 64 KB: 2 blocks)	• Unit of programming for the data area: 8 or 128 bytes • Unit of erasure for the data area: 2 KB (32 KB data flash: 16 blocks; 8 KB data flash: 4 blocks)	• Unit of programming for the user area: 8 bytes • Unit of erasure for the user area: 2 KB
On-board programming	Programming in boot mode • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. Programming by a routine for ROM/data flash programming within the user program • This allows ROM programming without resetting the system.		Programming in boot mode • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. • FINE is used. Programming by a routine for ROM/data flash programming within the user program
Off-board programming	A PROM programmer can be used to program the user area.	—	The user area can be programmed using a flash programmer compatible with this the RX23T Group.

Item	RX62T		RX23T
	Flash Memory for Code Storage	Flash Memory for Data Storage	
Software-controlled protection function	The FENTRYR.FENTRY0 bit, FWEPROR.FLWE[1:0] bits, and lock bits can be used to prevent unintentional programming.	The FENTRYR.FENTRYD bit, FWEPROR.FLWE[1:0] bits, and DFLREk and DFLWEk registers, can be used to prevent unintentional programming (k = 0 or 1).	The FENTRYR.FENTRY0 bit can be used to prevent unintentional programming.
Error protection function	Prevents further programming or erasure after the detection of abnormal operation during programming or erasure.		—
ID code protection	• This function can be used to prevent reading, writing, or erasing by the host. • ID codes can be used for control when connected to an on-chip debugging emulator.		• Connection with the serial programmer in boot mode can be enabled or disabled using ID codes in boot mode. • ID codes can be used for control when connected to an on-chip debugging emulator.
Start-up program protection function	—	—	This function is used to safely rewrite blocks 0 to 7.
Area protection	—	—	This function enables rewriting only the selected blocks in the user area and disables writing to the other blocks during self-programming.

Table 2.34 Comparative Listing of Flash Memory Registers

Register	Bit	RX62T	RX23T
FMODR	FRDMD	FCU read mode select bit	—
FASTAT	DFLWPE	Data flash programming/erasure protection violation bit	—
	DFLRPE	Data flash read protection violation bit	—
	DFLAE	Data flash access violation bit	—
	CMDLK	FCU command lock bit	—
	ROMAE	ROM access violation bit	—
FAEINT	DFLWPEIE	Data flash programming/erasure protection violation interrupt enable bit	—
	DFLRPEIE	Data flash read protection violation interrupt enable bit	—
	DFLAEIE	Data flash access violation interrupt enable bit	—
	CMDLKIE	FCU command lock interrupt enable bit	—
	ROMAEIE	ROM access violation interrupt enable bit	—

Register	Bit	RX62T	RX23T
FCURAME	FCRME	FCU RAM enable bit	—
	KEY[7:0]	Key code	—
FSTATR0	PRGSPD	Programming suspend status bit	—
	ERERR	—	Erase error flag
	ERSSPD	Erasure suspend status bit	—
	PRGERR	Programming error bit	Program error flag
	SUSRDY	Suspend ready bit	—
	BCERR	—	Blank check error flag
	ERSERR	Erasure error bit	
	EILGLERR	—	Extra area illegal command error flag
	FRDY	Flash ready bit	—
FSTATR1	FLOCKST	Lock bit status bit	—
	FRDY	—	Flash ready flag
	FCUERR	FCU error bit	—
	EXRDY	—	Extra area ready flag
FRDYIE	FRDYIE	Flash ready interrupt enable bit	—
FENTRYR	FENTRYD	Data flash P/E mode entry bit	—
FPROTR	FPROTCN	Lock bit protection cancel bit	—
	FPKEY[7:0]	Key code	—
FRESETR	FRKEY[7:0]	Key code	—
FCMDR	PCMDR[7:0]	Precommand	—
	CMDR[7:0]	Command	—
FCPSR	ESUSPMD	Erasure suspend mode bit	—
FPESTAT	PEERRST[7:0]	P/E error status bits	—
PCKAR	PCKA[7:0]	Peripheral clock notification bits	—
FWEPROR	FLWE[1:0]	Flash programming/erasure bits	—
DFLRE0	DBRE00	DB00 block read enable bit	—
	DBRE01	DB01 block read enable bit	—
	DBRE02	DB02 block read enable bit	—
	DBRE03	DB03 block read enable bit	—
	DBRE04	DB04 block read enable bit	—
	DBRE05	DB05 block read enable bit	—
	DBRE06	DB06 block read enable bit	—
	DBRE07	DB07 block read enable bit	—
	KEY[7:0]	Key code	—
DFLRE1	DBRE08	DB08 block read enable bit	—
	DBRE09	DB09 block read enable bit	—
	DBRE10	DB10 block read enable bit	—
	DBRE11	DB11 block read enable bit	—
	DBRE12	DB12 block read enable bit	—
	DBRE13	DB13 block read enable bit	—
	DBRE14	DB14 block read enable bit	—
	DBRE15	DB15 block read enable bit	—
	KEY[7:0]	Key code	—

Register	Bit	RX62T	RX23T
DFLWE0	DBWE00	DB00 block programming/erasure enable bit	—
	DBWE01	DB01 block programming/erasure enable bit	—
	DBWE02	DB02 block programming/erasure enable bit	—
	DBWE03	DB03 block programming/erasure enable bit	—
	DBWE04	DB04 block programming/erasure enable bit	—
	DBWE05	DB05 block programming/erasure enable bit	—
	DBWE06	DB06 block programming/erasure enable bit	—
	DBWE07	DB07 block programming/erasure enable bit	—
	KEY[7:0]	Key code	—
DFLWE1	DBWE08	DB08 block programming/erasure enable bit	—
	DBWE09	DB09 block programming/erasure enable bit	—
	DBWE10	DB10 block programming/erasure enable bit	—
	DBWE11	DB11 block programming/erasure enable bit	—
	DBWE12	DB12 block programming/erasure enable bit	—
	DBWE13	DB13 block programming/erasure enable bit	—
	DBWE14	DB14 block programming/erasure enable bit	—
	DBWE15	DB15 block programming/erasure enable bit	—
	KEY[7:0]	Key code	—
DFLBCCNT	BCSIZE	Blank check size setting bit	—
	BCADR[7:0]	Blank check address setting bits	—
DFLBCSTAT	BCST	Blank check status bit	—
FPR		—	Protection unlock register
FPSR	PERR	—	Protect error flag
FPMCR	FMS0	—	Flash operating mode select bit 0
	RPDIS	—	ROM P/E disable bit
	FMS1	—	Flash operating mode select bit 1
	LVPE	—	Low-voltage P/E mode enable bit
	FMS2	—	Flash operating mode select bit 2
FISR	PCKA[4:0]	—	Peripheral clock notification bits
	SAS[1:0]	—	Start-up area select bits
FASR	EXS	—	Extra area select bit
FCR	CMD[3:0]	—	Software command setting setting bits
	STOP	—	Forced processing stop bit
	OPST	—	Processing start bit

Register	Bit	RX62T	RX23T
FEXCR	CMD[2:0]	—	Software command setting bits
	OPST	—	Processing start bit
FSARH		—	Flash processing start address register H
FSARL		—	Flash processing start address register L
FEARH		—	Flash processing end address register H
FEARL		—	Flash processing end address register L
FWBn (n = 0 to 3)		—	Flash write buffer n register
FEAMH		—	Flash error address monitor register H
FEAML		—	Flash error address monitor register L
FSCMR	SASMF	—	Start-up area setting monitor flag
FAWSMR		—	Flash access window start address monitor register
FAWEMR		—	Flash access window end address monitor register
UIDRn (n = 0 to 3)		—	Unique ID register n

3. Reference Documents

User's Manual: Hardware

RX62T Group, RX62G Group User's Manual: Hardware Rev.2.00 (R01UH0034EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

RX23T Group User's Manual: Hardware Rev.1.10 (R01UH0520EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Aug. 4, 2015	—	First edition issued
1.01	Sep. 16, 2015	3	2.2 Resets Table 2.2 Comparative Listing of Reset Specifications Power-on reset description for RX23T amended
		7	2.4 Clock Generation Circuit Table 2.6 Comparative Listing of Clock Generation Circuit Specifications Error in PLL input frequency for RX62T amended. Frequency multiplication ratio description added
		9	2.5 Low Power Consumption Functions Table 2.8 Comparative Listing of Low Power Consumption Functions RSTSR register bit symbol error amended
		24	2.12 Port Output Enable 3 Table 2.20 Comparative Overview of Port Output Enable 3 Error related to GPT0 pins, target pins to be placed in high-impedance state, amended
		30	2.13 Independent Watchdog Timer Table 2.22 Comparative Overview of Independent Watchdog Timer Description of register start mode on RX62T added
		34	2.14 Serial Communication Interface Table 2.25 Comparative Listing of Serial Communication Interface Registers Errors in bit names in TDRH, TDRL, and TDRHL registers amended
		40	2.17 12-Bit A/D Converter Table 2.30 Comparative Overview of 12-Bit A/D Converter Errors in description of operating modes of RX62T amended
		45 to 47	2.19 Flash Memory Table 2.33 Comparative Listing of Flash Memory Specifications Description of of RX62T interrupt amended Description of on-board programming of RX62T and RX23T amended Error in description of area protection amended
1.10	Dec. 7, 2015	7	2.4 Clock Generation Circuit Table 2.6 Comparative Listing of Clock Generation Circuit Specifications High-Speed On-Chip Oscillator (HOCO) added
		9	2.4 Clock Generation Circuit Table 2.7 Comparative Listing of Clock Generation Circuit Registers High-Speed On-Chip Oscillator Control Register (HOCO) added High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR) added Oscillation Stabilization Flag Register (OSCOVFSR) HOCO clock oscillation stabilization flag added
		20	2.10 I/O Ports Table 2.17 Comparative Listing of I/O Port Registers Open Drain Control Register 1 (ODR1) changed

Rev.	Date	Description	
		Page	Summary
1.10	Dec. 7, 2015	21	2.11 Multi-Function Timer Pulse Unit 3 Table 2.18 Comparative Overview of Multi-Function Timer Pulse Unit 3 Description of of RX23T Count clock amended
		40	2.16 Serial Peripheral Interface Table 2.29 Comparative Listing of Serial Peripheral Interface Registers SPSR register deleted
		44, 45	2.17 12-Bit A/D Converter Table 2.31 Comparative Listing of 12-Bit A/D Converter Registers ADANSA0 register bit symbol amended ADANSB0 register bit symbol amended ADANSA1 register bit symbol amended ADANSB1 register bit symbol amended ADADS0 register bit symbol amended ADADS1 register bit symbol amended
		48	2.18 RAM Table 2.32 Comparative Overview of RAM Description of of RX23T RAM capacity amended Description of of RX23T RAM address amended

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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