RX210, RX21A, and RX220 Groups
HOCO Calibration Using the CAC

Abstract

This document describes the method to adjust frequencies of the high-speed on-chip oscillator (HOCO) using the clock frequency accuracy measurement circuit (CAC) during the RX210, RX21A or RX220 MCU operation.

Products

- RX210, RX21A, and RX220 Groups

Note: • 48-pin packages of the RX210 and RX220 Groups are not included as the target products.

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.
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1. Specifications

HOCO oscillation frequency may differ from the factory-configured frequency due to external factors such as ambient temperature. Calibration needs to be performed to compensate the frequency error. The high-speed on-chip oscillator trimming register (HOCOTRR\(n\) (\(n = 0\) to 3)) is used to adjust the HOCO oscillation frequency. Registers HOCOTRR0, HOCOTRR1, HOCOTRR2, and HOCOTRR3 correspond to oscillation frequencies 32 MHz, 36.864 MHz, 40 MHz, and 50 MHz, respectively. When the HOCO clock is 32 MHz, the HOCO frequency error can be compensated by adjusting the value of the HOCOTRR0 register in constant intervals.

In this application note, the HOCO oscillation frequency is measured in 1 second periods using the CAC. Then the value in the HOCOTRR0 register is adjusted with the obtained measurement result. Also a waveform which is equivalent to HOCO divided by 4 is output from the TMO3 pin.

Table 1.1 lists the Peripheral Functions and Their Applications and Figure 1.1 shows the Block Diagram.

### Table 1.1 Peripheral Functions and Their Applications

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAC</td>
<td>Measures the HOCO frequency based on the sub-clock.</td>
</tr>
<tr>
<td>RTC</td>
<td>Counter for 1 second period</td>
</tr>
<tr>
<td>TMR</td>
<td>Outputs a waveform which is equivalent to the HOCO clock divided by 4.</td>
</tr>
</tbody>
</table>

![Figure 1.1 Block Diagram](image-url)
2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU used</td>
<td>R5F5210BBDFP (RX210 Group)</td>
</tr>
<tr>
<td>Operating frequencies</td>
<td>• HOCO clock: 32 MHz&lt;br&gt;• Sub-clock: 32.768 kHz&lt;br&gt;• System clock (ICLK): 32 MHz (HOCO clock divided by 1)</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5.0 V</td>
</tr>
<tr>
<td>Integrated development</td>
<td>Renesas Electronics Corporation&lt;br&gt;High-performance Embedded Workshop Version 4.09.01</td>
</tr>
<tr>
<td>environment</td>
<td>C compiler&lt;br&gt;Renesas Electronics Corporation&lt;br&gt;C/C++ Compiler Package for RX Family V.1.02 Release 01</td>
</tr>
<tr>
<td></td>
<td>Compile options&lt;br&gt;-cpu=rx200 -output=obj=&quot;${(CONFIGDIR)$(FILELEAF).obj&quot; -debug -nologo&lt;br&gt;(The default setting is used in the integrated development environment.)</td>
</tr>
<tr>
<td>Endian</td>
<td>Little endian</td>
</tr>
<tr>
<td>Operating mode</td>
<td>Single-chip mode</td>
</tr>
<tr>
<td>Processor mode</td>
<td>Supervisor mode</td>
</tr>
<tr>
<td>Sample code version</td>
<td>Version 1.00</td>
</tr>
<tr>
<td>Board used</td>
<td>Renesas Starter Kit for RX210 (product part no.: R0K505210S003BE)</td>
</tr>
</tbody>
</table>

3. Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- RX210 Group Initial Setting Rev. 2.20 (R01AN1002EJ)
- RX21A Group Initial Setting Rev. 1.10 (R01AN1486EJ)
- RX220 Group Initial Setting Rev. 1.10 (R01AN1494EJ)

The initial setting functions in the reference application notes are used in the sample code accompanying this application note. The revision numbers of the reference application notes are as of when this application note was made. However the latest version is always recommended. Visit the Renesas Electronics Corporation website to check and download the latest version.
4. Hardware

4.1 Pin Used

Table 4.1 lists the Pin Used and Its Function.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P32/TMO3</td>
<td>Output</td>
<td>Outputs a waveform which is equivalent to the HOCO clock divided by 4.</td>
</tr>
</tbody>
</table>

5. Software

5.1 Operation Overview

In this application note, the HOCO clock (32 MHz) divided by 32 is used as the frequency measurement clock for the CAC and the sub-clock (32.768 kHz) divided by 1024 is used as the reference signal generation clock. The CAC counts valid edges of the HOCO in the period from a rising edge to the next rising edge of the sub-clock.

The measurement is triggered by the realtime clock (RTC) 1-second periodic interrupt and performed four times continuously.

The average of these four measurement results is calculated (measurement result for adjustment). If the difference (A) between the measurement result and the theoretical value is “A ≤ -256 counts” or “+256 counts ≤ A”, addition or subtraction is performed on the HOCOTRR0 register value. If the difference between the measurement result and the theoretical value is “-256 counts < A < +256 counts”, the HOCOTRR0 register value remains as it is.

Table 5.1 lists the Specifications of Register Value Adjustment, Figure 5.1 shows the Specification of Register Value Adjustment, and Figure 5.2 shows the Timing Diagram of Calibration.

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Condition</th>
<th>Adjustment Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X ≥ Z (Z + L)</td>
<td>-1</td>
</tr>
<tr>
<td>2</td>
<td>X ≤ (Z - L)</td>
<td>+1</td>
</tr>
<tr>
<td>3</td>
<td>(Z - L) &lt; X &lt; (Z + L)</td>
<td>As is</td>
</tr>
</tbody>
</table>

X: Measurement result, Z: Theoretical value, L: Allowable error range

Figure 5.1 Specification of Register Value Adjustment
Figure 5.2 Timing Diagram of Calibration

(1) Using the RTC 1-second periodic interrupt as a trigger, the CAC start setting is configured and a measurement is started.

(2) Valid edges of the HOCO divided by 32 are counted in the period from a rising edge to the next rising edge of the sub-clock divided by 1024. The measurement result is obtained in CAC measurement end interrupt handling. Four measurements are handled as a set of the measurement result.

(3) A set of the measurement result is averaged and the value in the HOCOTRR0 register is adjusted using the averaged value (1).

(4) When the adjustment of the HOCO oscillation frequency is completed, the CAC measurement is stopped. A wait for HOCO oscillation stabilization is processed until the next RTC 1-second periodic interrupt occurs while HOCO is being provided to the CPU or the peripheral functions such as ICLK.

Note:
1. The following errors are caused by errors between the HOCO and a crystal used for the sub-clock, and the allowable error range (±256 counts) of the theoretical value.
   - When the HOCO is 32 MHz, the maximum error is ±0.9%.
   - When the HOCO is 36.864 MHz, the maximum error is ±0.8%.
   - When the HOCO is 40 MHz, the maximum error is ±0.7%.
   - When the HOCO is 50 MHz, the maximum error is ±0.6%.
5.2 File Composition

Table 5.2 lists the Files Used in the Sample Code. Files generated by the integrated development environment are not included in this table.

<table>
<thead>
<tr>
<th>File Name</th>
<th>Outline</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>main.c</td>
<td>Main processing</td>
<td></td>
</tr>
<tr>
<td>r_init_stop_module.c</td>
<td>Stop processing for active peripheral functions after a reset</td>
<td></td>
</tr>
<tr>
<td>r_init_stop_module.h</td>
<td>Header file for r_init_stop_module.c</td>
<td></td>
</tr>
<tr>
<td>r_init_non_existent_port.c</td>
<td>Nonexistent port initialization</td>
<td></td>
</tr>
<tr>
<td>r_init_non_existent_port.h</td>
<td>Header file for r_init_non_existent_port.c</td>
<td></td>
</tr>
<tr>
<td>r_init_clock_an1706.c</td>
<td>Clock initialization</td>
<td></td>
</tr>
<tr>
<td>r_init_clock.h</td>
<td>Header file for r_init_clock.c</td>
<td></td>
</tr>
<tr>
<td>rtc_func.c</td>
<td>RTC initialization and 1-second periodic interrupt handling</td>
<td></td>
</tr>
<tr>
<td>rtc_func.h</td>
<td>Header file for rtc_func.c</td>
<td></td>
</tr>
<tr>
<td>cac_func.c</td>
<td>CAC initialization and measurement end interrupt handling</td>
<td></td>
</tr>
<tr>
<td>cac_func.h</td>
<td>Header file for cac_func.c</td>
<td></td>
</tr>
<tr>
<td>tmr_func.c</td>
<td>TMR initialization for PCLK output</td>
<td></td>
</tr>
</tbody>
</table>

5.3 Option-Setting Memory

Table 5.3 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Addresses</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFS0</td>
<td>FFFF FF8Fh to FFFF FF8Ch</td>
<td>FFFF FFFFh</td>
<td>The IWDT is stopped after a reset. The WDT is stopped after a reset.</td>
</tr>
<tr>
<td>OFS1</td>
<td>FFFF FF8Bh to FFFF FF88h</td>
<td>FFFF FFFFh</td>
<td>The voltage monitor 0 reset is disabled after a reset. HOCO oscillation is disabled after a reset.</td>
</tr>
<tr>
<td>MDES</td>
<td>FFFF FF83h to FFFF FF80h</td>
<td>FFFF FFFFh</td>
<td>Little endian</td>
</tr>
</tbody>
</table>
5.4 Constants

Table 5.4 lists the Constants Used in the Sample Code (Constants from the Initial Setting). Table 5.5 lists the Constants Used in the Sample Code.

<table>
<thead>
<tr>
<th>Constant Name</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEL_MAIN</td>
<td>B_NOT_USE</td>
<td>Selection of the main clock operation: The main clock is not used (main clock stopped).</td>
</tr>
<tr>
<td>SEL_SUB</td>
<td>B_USE</td>
<td>Selection of the sub-clock usage for the system clock: The sub-clock is used (1).</td>
</tr>
<tr>
<td>SEL_RTC</td>
<td>B_USE</td>
<td>Selection of the sub-clock usage for the RTC count source: The sub-clock is used.</td>
</tr>
<tr>
<td>SEL_PLL</td>
<td>B_NOT_USE</td>
<td>Selection of the PLL clock operation: The PLL clock is not used (PLL clock stopped).</td>
</tr>
<tr>
<td>SEL_HOCO</td>
<td>B_USE</td>
<td>Selection of the HOCO clock operation: The HOCO clock is used (HOCO clock oscillating).</td>
</tr>
<tr>
<td>SEL_SYSCLK</td>
<td>CLK_HOCO</td>
<td>Clock source selection for the system clock HOCO is selected.</td>
</tr>
</tbody>
</table>

Note:

1. For the clock setting, No. 4 is used in Table 1.3 Examples of Clock Selections in the Initial Setting application note except the SEL_SUB constant. In this application note, “B_USE (used)” is set to the SEL_SUB constant since the sub-clock is used for the CAC.
<table>
<thead>
<tr>
<th>Constant Name</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHECK_CNT</td>
<td>4</td>
<td>Number of measurements</td>
</tr>
<tr>
<td>MEND_FINISH</td>
<td>0</td>
<td>Frequency measurement counter: Measurement stopped</td>
</tr>
<tr>
<td>MEND_START</td>
<td>1</td>
<td>Frequency measurement counter: Measurement starts</td>
</tr>
<tr>
<td>MEND_CHECK_FINISH</td>
<td>CHECK_CNT</td>
<td>Frequency measurement counter: Measurement completed</td>
</tr>
<tr>
<td>ACCEPTABLE_RANGE</td>
<td>256</td>
<td>Allowable error range of the measurement result</td>
</tr>
<tr>
<td>MAIN_CLOCK_CYCLE</td>
<td>(1,000,000,000L / MAIN_CLOCK_Hz)</td>
<td>Main clock cycles (ns)</td>
</tr>
<tr>
<td>SUB_CLOCK_CYCLE</td>
<td>(1,000,000,000L / SUB_CLOCK_Hz)</td>
<td>Sub-clock cycles (ns)</td>
</tr>
<tr>
<td>FOR_CMT0_TIME</td>
<td>232727</td>
<td>Count cycles (ns) for the CMT0 timer to wait for the oscillation stabilization wait time: (1/LOCO) × 32, where LOCO = 137.5 kHz (max.), and 32 = PCLKB divided by 32</td>
</tr>
<tr>
<td>REG_HOCOTRR (when HOCO operates at 32 MHz)</td>
<td>SYSTEM.HOCOTRR0</td>
<td>HOCOTRR0 register</td>
</tr>
<tr>
<td>TYP_CAC_RESULT (when HOCO operates at 32 MHz)</td>
<td>31250</td>
<td>Measurement theoretical value when HOCO operates at 32 MHz.</td>
</tr>
<tr>
<td>REG_HOCOTRR (when HOCO operates at 36.864 MHz)</td>
<td>SYSTEM.HOCOTRR1</td>
<td>HOCOTRR1 register</td>
</tr>
<tr>
<td>TYP_CAC_RESULT (when HOCO operates at 36.864 MHz)</td>
<td>36000</td>
<td>Measurement theoretical value when HOCO operates at 36.864 MHz.</td>
</tr>
<tr>
<td>REG_HOCOTRR (when HOCO operates at 40 MHz)</td>
<td>SYSTEM.HOCOTRR2</td>
<td>HOCOTRR2 register</td>
</tr>
<tr>
<td>TYP_CAC_RESULT (when HOCO operates at 40 MHz)</td>
<td>39062</td>
<td>Measurement theoretical value when HOCO operates at 40 MHz.</td>
</tr>
<tr>
<td>REG_HOCOTRR (when HOCO operates at 50 MHz)</td>
<td>SYSTEM.HOCOTRR3</td>
<td>HOCOTRR3 register</td>
</tr>
<tr>
<td>TYP_CAC_RESULT (when HOCO operates at 50 MHz)</td>
<td>48828</td>
<td>Measurement theoretical value when HOCO operates at 50 MHz.</td>
</tr>
</tbody>
</table>
5.5 Variables
Table 5.6 lists the Global Variables.

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>static uint8_t</td>
<td>buffer_counter</td>
<td>Frequency measurement counter</td>
<td>INIT_CAC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Excep_CAC_MENDF</td>
</tr>
<tr>
<td>static uint32_t</td>
<td>result_buffer</td>
<td>Storage buffer for the frequency measurement</td>
<td>INIT_CAC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>result</td>
<td>Excep_CAC_MENDF</td>
</tr>
<tr>
<td>static int32_t</td>
<td>result_diff</td>
<td>Storage buffer for the result</td>
<td>INIT_CAC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Excep_CAC_MENDF</td>
</tr>
</tbody>
</table>

5.6 Functions
Table 5.7 lists the Functions.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>main</td>
<td>Main processing</td>
</tr>
<tr>
<td>R_INIT_StopModule</td>
<td>Stop processing for active peripheral functions after a reset</td>
</tr>
<tr>
<td>R_INIT_NonExistentPort</td>
<td>Nonexistent port initialization</td>
</tr>
<tr>
<td>R_INIT_Clock</td>
<td>Clock initialization</td>
</tr>
<tr>
<td>tmr_init</td>
<td>TMR initialization</td>
</tr>
<tr>
<td>CGC_oscillation_sub_an1706</td>
<td>Sub-clock oscillation setting</td>
</tr>
<tr>
<td>enable_RTC_an1706</td>
<td>RTC initialization</td>
</tr>
<tr>
<td>Excep_RTC_PRD</td>
<td>RTC periodic interrupt handling</td>
</tr>
<tr>
<td>cmt0_wait_16bit</td>
<td>CMT0 wait processing</td>
</tr>
<tr>
<td>INIT_CAC</td>
<td>CAC initialization</td>
</tr>
<tr>
<td>Excep_CAC_MENDF</td>
<td>CAC measurement end interrupt handling</td>
</tr>
</tbody>
</table>
### 5.7 Function Specifications

The following tables list the sample code function specifications.

<table>
<thead>
<tr>
<th>Function</th>
<th>Outline</th>
<th>Header</th>
<th>Declaration</th>
<th>Description</th>
<th>Arguments</th>
<th>Return Value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>main</strong></td>
<td>Main processing</td>
<td>None</td>
<td>void main(void)</td>
<td>Calls the following functions: Stop processing for active peripheral functions after a reset, nonexistent port initialization, clock initialization, and TMR initialization.</td>
<td>None</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td><strong>R_INIT_StopModule</strong></td>
<td>Stop processing for active peripheral functions after a reset</td>
<td>r_init_stop_module.h</td>
<td>void R_INIT_StopModule(void)</td>
<td>Configures the setting to enter the module stop state.</td>
<td>None</td>
<td>None</td>
<td>Transition to the module stop state is not performed in the sample code. For details on this function, refer to the Initial Setting application note for the product used.</td>
</tr>
<tr>
<td><strong>R_INIT_NonExistentPort</strong></td>
<td>Nonexistent port initialization</td>
<td>r_init_non_existent_port.h</td>
<td>void R_INIT_NonExistentPort(void)</td>
<td>Initializes port direction registers for ports that do not exist in products with less than 144 pins.</td>
<td>None</td>
<td>None</td>
<td>The number of pins in the sample code is set for the 100-pin package (PIN_SIZE=100). After this function is called, when writing in byte units to the PDR registers or PODR registers which have nonexistent ports, set the corresponding bits for nonexistent ports as follows: set the I/O select bits in the PDR registers to 1 and set the output data store bits in the PODR registers to 0. For details on this function, refer to the Initial Setting application note for the product used.</td>
</tr>
<tr>
<td><strong>R_INIT_Clock</strong></td>
<td>Clock initialization</td>
<td>r_init_clock.h</td>
<td>void R_INIT_Clock(void)</td>
<td>Initializes the clock.</td>
<td>None</td>
<td>None</td>
<td>The sample code selects processing which uses the HOCO as the system clock and the sub-clock for the RTC and CAC. For details on this function, refer to the Initial Setting application note for the product used.</td>
</tr>
</tbody>
</table>
### tmr_init

**Outline**  
TMR initialization

**Header**  
tmr_func.h

**Declaration**  
void tmr_init(void)

**Description**  
Configures channel 3 of the TMR to output PCLK divided by 2.

**Arguments**  
None

**Return Value**  
None

---

### CGC_oscillation_sub_an1706

**Outline**  
Sub-clock oscillation setting

**Header**  
r_init_clock.h

**Declaration**  
void CGC_oscillation_sub_an1706 (void)

**Description**  
Configures settings to use the sub-clock for either of the system clock or the RTC, or both.

**Arguments**  
None

**Return Value**  
None

---

### enable_RTC_an1706

**Outline**  
RTC initialization

**Header**  
rtc_func.h

**Declaration**  
void enable_RTC_an1706 (void)

**Description**  
Initializes the RTC (setting for clock provision and the RTC, and RTC software reset).

**Arguments**  
None

**Return Value**  
None

---

### Excep_RTC_PRD

**Outline**  
RTC periodic interrupt handling

**Header**  
rtc_func.h

**Declaration**  
static void Excep_RTC_PRD(void)

**Description**  
The CAC is initialized in this interrupt handling.

**Arguments**  
None

**Return Value**  
None

---

### cmt0_wait_16bit

**Outline**  
CMT0 wait processing

**Header**  
None

**Declaration**  
static void cmt0_wait_16bit(uint16_t cnt)

**Description**  
This function is used when waiting for RTC clock provision that is six clocks of the sub-clock.

**Arguments**  
uint16_t cnt:  
Oscillation stabilization wait time

\[
\text{cnt} = \text{oscillation stabilization wait time (ns)} \times \text{FOR_CMT0_TIME}
\]

**Return Value**  
None

**Remarks**  
1. The oscillation stabilization wait time varies depending on the crystal/ceramic resonator. Set the value based on the calculation method in the Initial Setting application note for the product used.

2. The value of FOR_CMT0_TIME is calculated where LOCO is 137.5 kHz (max.).

   The actual wait time may differ depending on the LOCO frequency.
### INIT_CAC

<table>
<thead>
<tr>
<th>Outline</th>
<th>CAC initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>cac_func.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void INIT_CAC(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Initializes the CAC.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
</tbody>
</table>

### Excep_CAC_MENDF

<table>
<thead>
<tr>
<th>Outline</th>
<th>CAC measurement end interrupt handling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>cac_func.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>static void Excep_CAC_MENDF(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Adjusts HOCO frequencies based on the measurement results.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
</tbody>
</table>
5.8 Flowcharts

5.8.1 Main Processing

Figure 5.3 shows the Main Processing.

![Main Processing Flowchart]

Figure 5.3 Main Processing

- Disable maskable interrupts
- Stop processing for active peripheral functions after a reset
  \( \text{R_INIT\_StopModule}() \)
- Nonexistent port initialization
  \( \text{R_INIT\_NonExistentPort}() \)
- Clock initialization
  \( \text{R_INIT\_Clock}() \)
- TMR initialization
  \( \text{tmr\_init()} \)
- Enable maskable interrupts

\( I \text{ flag} \leftarrow 0 \)

\( \text{PWM output of the TMR (TMO3) is configured to verify the adjusted HOCO clock.} \)

\( I \text{ flag} \leftarrow 1 \)
5.8.2 TMR Initialization

Figure 5.4 shows the TMR Initialization.

```
#pragma checksum 5.8.2 TMR Initialization

tmr_init

backup_PRCR ← PRCR register | A500h

PRC register ← A502h
PRC1 bit = 1: Enables writing to the registers related to the low power consumption function.

MSTPCR register
MSTPA4 bit ← 0: Cancels module stop state for TMR2 and TMR3.

PRCR register ← backup_PRCR

Select the I/O port function
PWPR register
B0WI bit ← 0
PFSWE bit ← 1
P32PFS register ← 05h
PSEL[3:0] bits = 0101b: Uses P32 as the TMO3 pin.
PWPR register
PFSWE bit ← 0
B0WI bit ← 1
PORT32.PMR register ← 04h
B2 bit = 1: Uses port 32 as I/O port for peripheral functions.

Stop the clock operation
TCCR register ← 00h
CSS[1:0] bits = 00b
CKS[2:0] bits = 000b: Clock input prohibited

Set the timing for compare match
TCORA register ← 00h: Compare match A used
TCORB register ← 01h: Compare match B used

Set the timing for counter clear
TCR register ← 10h
CCLR[1:0] bits = 10b: Counter cleared by compare match B

Set the counter
TCNT register ← 00h: Clears the counter.

Set the TMO3 pin output
TCSR register ← 1Fh
OSB[1:0] bits = 11b: Toggle output from TMO3 pin by compare match B
OSA[1:0] bits = 11b: Toggle output from TMO3 pin by compare match A

Start counting
TCCR register ← 08h
CSS[1:0] bits = 01b
CKS[2:0] bits = 000b: Uses PCLK as the frequency dividing clock.

return
```

Figure 5.4 TMR Initialization
### 5.8.3 Sub-Clock Oscillation Setting

Figure 5.5 shows the Sub-Clock Oscillation Setting.

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CGC_oscillation_sub_an1706</td>
</tr>
<tr>
<td>2</td>
<td>Enabling sub-clock oscillation oscilation_subclk()</td>
</tr>
<tr>
<td>3</td>
<td>RTC Initialization enable_RTC_an1706()</td>
</tr>
<tr>
<td>4</td>
<td>Reset the wait control register for the sub-clock resetting_wtcr_subclk()</td>
</tr>
<tr>
<td>5</td>
<td>Processing when the sub-clock is not used as the system clock no_use_subclk_as_sysclk()</td>
</tr>
<tr>
<td>6</td>
<td>Retains the setting when the sub-clock is used as the system clock to use the sub-clock for the CAC.</td>
</tr>
</tbody>
</table>

**Figure 5.5 Sub-Clock Oscillation Setting**
5.8.4 RTC Initialization

Figure 5.6 shows the RTC Initialization.

1. Set the RCR3 register
   - RTCEN bit ← 1: Sub-clock oscillator is operating.

2. CMT0 wait processing
   - cmt0_wait()

3. Stop counters and the prescaler
   - RCR2 register ← RCR2 register & 7EH
     - START bit = 0: Counters and prescaler are stopped

4. RTC software reset
   - RCR2 register
     - RESET bit ← 1: The prescaler and the target registers for RTC software reset are initialized

5. Is the RTC software reset completed?
   - No

6. Set the date and time to Tuesday, January 1, 2014, 00:00:00
   - RSECCNT register ← 00h: 00 is set to the second counter.
   - RMINCNT register ← 00h: 00 is set to the minute counter.
   - RWKCNT register ← 03h: 3 (Wednesday) is set to the day-of-week counter.
   - RDAYCNT register ← 01h: 01 is set to the date counter.
   - RMONCNT register ← 01h: 01 is set to the month counter.
   - RYRCNT register ← 0014h: 14 is set to the year counter.

7. Specify the time error adjustment
   - RAYJ register ← 00h
     - ADJ[5:0] bits = 000000b: Adjustment value not set
     - PMADJ[1:0] bits = 00b: Adjustment is not performed.

8. Set the RTC 1-second periodic interrupt
   - RCR1 register ← E4h
     - AIE bit = 0: An alarm interrupt request is disabled.
     - CIE bit = 0: A carry interrupt request is disabled.
     - PIE bit = 1: A periodic interrupt request is enabled.
     - PES[3:0] bits = 1110b: A periodic interrupt is generated every 1 second.

9. Set the automatic adjustment
   - RCR2 register ← 30h
     - START bit = 0: Year, month, day-of-week, date, hour, minute, second, and 64-Hz counters, and prescaler are stopped.
     - RTCOE bit = 0: RTCOUT output disabled.
     - AADJE bit = 1: Automatic adjustment is enabled.
     - AADJP bit = 1: The RADJ. ADJ[5:0] setting value is adjusted from the count value of the prescaler every 10 seconds.
     - HR24 bit = 0: The RTC operates in 12-hour mode.

10. Specify the RTC periodic interrupt settings
    - IRO93 register
      - IR flag ← 0: Interrupt request [ IR(RTC,PRD) ] is cleared.
    - IPR093 register
    - IER093 register
      - IENS5 bit ← 1: Interrupt request enable [ IEN(RTC,PRD) ] is enabled.

11. Start the RTC count operation
    - RCR2 register
      - START bit ← 1: Year, month, day-of-week, date, hour, minute, second, and 64-Hz counters, and prescaler operate normally.

return
5.8.5 RTC Periodic Interrupt Handling

Figure 5.7 shows the RTC Periodic Interrupt Handling.

![RTC Periodic Interrupt Handling Diagram]

Figure 5.7 RTC Periodic Interrupt Handling
5.8.6 CMT0 Wait Processing

Figure 5.8 shows the CMT0 Wait Processing.

- **cmt0_wait_16bit**
- **cnt** Clock oscillation stabilization wait time
- **backup_MSTP** ← MSTPCRA register
- **backup_PRCR** ← PRCR register | 0xA500

**Backup the protect register values**

**PRCR register** ← A502h
**PRC1 bit** = 1: Enables writing to the registers related to the low power consumption function.

**MSTPCRA register**
**MSTPA15 bit** = 0: The module-stop state is canceled for CMT0 and CMT1.

**Disable write protection**

**CMSTR0 register**
**STR0 bit** ← 0: CMT0.CMCNT count is stopped.

**Cancel the module-stop state**

**Set the CMT0 count source and enable the compare match interrupt**

**Clear the CMT0 counter**

**CMC0 register** ← 0000h

**Wait time ≠ 0?**

- **Yes** (wait time ≠ 0)
  - **Decrement the wait time**
  - **cnt** ← cnt - 1

- **No** (wait time = 0)

**Set the wait time for CMT0**

**CMCOR register** ← cnt

**Clear the CMT0 interrupt request**

**CMCR register** ← 0080h
**CMCNT register** ← 0000h
**CMCOR register** ← 0000h
**IR028 register**
**IR flag** ← 0: Clear the CMT0.CMI0 interrupt request.

**Start the CMT0 count**

**CMSTR0 register**
**STR0 bit** ← 1: CMT0.CMCNT count is started.

**Is the CMI0 interrupt request generated?**

- **No**
  - **See Note 1**
  - **CMSTR0 register**
  - **STR0 bit** ← 0: CMT0.CMCNT count is stopped.

- **Yes**
  - **CMSTR0 register**
  - **STR0 bit** ← 0: CMT0.CMCNT count is stopped.

**Stop the CMT0 count**

**Initialize CMT0**

**Restore the backed up values to the protect registers**

**MSTPCRA register** ← backup_MSTP
**PRCR register** ← backup_PRCR

**return**

**Note:**
1. When the counter of the watchdog timer (WDT) or independent watchdog timer (IWDT) is operating, refresh the counter in this loop as required.
5.8.7 CAC Initialization

Figure 5.9 shows the CAC Initialization.

```
INIC_CAC
No
Has 1 second elapsed?

Yes

Backup the protect register value
backup_PRCR ← PRCR register | A500h

Disable write protection
PRCR register ← A502h
PRC1 bit = 1: Enables writing to the registers related to the low power consumption function.

Cancel the module stop state
MSTPCR register
MSTPC19 bit ← 0: Cancels module stop state for the CAC.

Restore the backed up protect register value
PRCR register ← backup_PRCR

Select internally generated signal as reference signal
CACR2 register ← 01h
RPS bit ← 1: Internally generated signal

Specify the frequency measurement clock
CACR1 register ← 34h
CACREFE bit ← 0: CACREF pin input is disabled.
FMCS[2:0] bits ← 010b: High-speed on-chip oscillator is selected as the frequency measurement clock.
TCSS[1:0] bits ← 11b: Divide-by-32 is selected as the count clock.
EDGES[3:0] bits ← 00b: Rising edge is used as the valid edge.

Specify the reference signal generation clock
CACR2 register ← 63h
RPS bit ← 1: Internally generated signal is selected as the reference signal.
RSCS[2:0] bits ← 001b: The sub-clock is selected as the reference signal generation clock.
RCDS[1:0] bits ← 10b: ×1/1024 clock
DFS[1:0] bits ← 01b: The sampling clock for the digital filter is the frequency measuring clock.

Specify the CAC interrupt
CAICR register ← 72h
FERRIE bit = 0: Frequency error interrupt is disabled.
MENDIE bit = 1: Measurement end interrupt is enabled
OVFIE bit = 0: Overflow interrupt is disabled.
FERRFCL bit = 1: The FERRF flag is cleared.
MENDFCL bit = 1: The MENDF flag is cleared.
OVFFCL bit = 1: The OVFF flag is cleared.

Specify the upper-limit and lower limit values
CALLVR register ← (TYP_CAC_RESULT × 0.99)
CAULVR register ← (TYP_CAC_RESULT × 1.01)

Start the clock frequency measurement
CACR0 register ← 01h
CFME bit ← 1: Clock frequency measurement is enabled.

Specify the measurement end interrupt
IR033 register
IR flag ← 0: Interrupt request [IR(CAC,MENDF)] is cleared.
IPR033 register
IPR[3:0] bits ← 0010b: Interrupt priority level [IPR(CAC,MENDF)] is level 2.
IER04 register
IEN1 bit ← 1: Interrupt request enable [IEN(CAC,MENDF)] is enabled.

Clear the measurement result
buffer_counter ← MEND_START
result_buffer ← 00h
result_diff ← 00h

return
```

Figure 5.9 CAC Initialization
5.8.8 CAC Measurement End Interrupt Handling

Figure 5.10 shows the CAC Measurement End Interrupt Handling.

```plaintext
Excep_CAC_MENDF

Store the measurement result
result_buffer ← result_buffer + measurement result (CAC.CACNTBR)

Update the number of measurements
buffer_counter ← buffer_counter + 1

Clear the CAC interrupt
CAICR register ← 72h
FERRFCL bit = 1: The FERRF flag is cleared.
MENDFCL bit = 1: The MENDF flag is cleared.
OVFFCL bit = 1: The OVFF flag is cleared.

Is the measurement completed?
Yes
Calculate an average of the measurement results and extract data for the valid bits.
result_buffer ← (result_buffer / CHECK_CNT)

Calculate the difference between the measurement result and the theoretical value
result_diff ← result_buffer - TYP_CAC_RESULT.
0 - result_diff when the value of result_diff is negative.

No
256 ≤ difference between the measurement result and the theoretical value

Yes
Back up the protect register value
backup_PRCR ← PRCR register | A500h

PRCR register ← A501h
PRC0 bit = 1: Enables writing to the registers related to the clock generation circuit.

Disable write protection

Measurement value > Theoretical value?
No

Yes
Decrement the HOCOTR0 register by 1
Increment the HOCOTR0 register by 1

Set the measurement end
buffer_counter ← MEND_FINISH

Increment the CACR0 register to disable the clock frequency measurement
CACR0 register ← 00h
CFME bit ← 0: Clock frequency measurement is disabled.

Clear the CAC interrupt
CAICR register ← 70h
MENDIE bit = 0: Measurement end interrupt is disabled.
FERRFCL bit = 1: The FERRF flag is cleared.
MENDFCL bit = 1: The MENDF flag is cleared.
OVFFCL bit = 1: The OVFF flag is cleared.

Set the measurement end interrupt
IR033 register
IR flag ← 0: Interrupt request [ IR(CAC,MENDF) ] is cleared.

Restore the backed up protect register value
PRCR register ← backup_PRCR

Set the measurement end
buffer_counter ← MEND_FINISH

Disable the clock frequency measurement

Return
```

Figure 5.10 CAC Measurement End Interrupt Handling
6. Applying This Application Note to the RX21A or RX220 Group

The sample code accompanying this application note has been confirmed to operate with the RX210 Group. To make the sample code operate with the RX21A or RX220 Group, use this application note in conjunction with the Initial Setting application note for each group.

For details on using this application note with the RX21A and RX220 Groups, refer to “5. Applying the RX210 Group Application Note to the RX21A Group” in the RX21A Group Initial Setting application note, and “4. Applying the RX210 Group Application Note to the RX220 Group” in the RX220 Group Initial Setting application note.

Note: • Files r_init_clock.h and r_init_clock.c will be overwritten when applying the RX21A or RX220 Group Initial Setting. Make the settings in the overwritten files be same as the original settings in files r_init_clock.h and r_init_clock.c accompanying this application note.
7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

User’s Manual: Hardware
- RX210 Group User’s Manual: Hardware Rev.1.50 (R01UH0037EJ)
- RX21A Group User’s Manual: Hardware Rev.1.00 (R01UH0251EJ)
- RX220A Group User’s Manual: Hardware Rev.1.10 (R01UH0292EJ)
  The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
  The latest information can be downloaded from the Renesas Electronics website.

User’s Manual: Development Tools
- RX Family C/C++ Compiler Package V.1.01 User’s Manual Rev.1.00 (R20UT0570EJ)
  The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com

Inquiries
http://www.renesas.com/contact/
### REVISION HISTORY

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<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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<tr>
<td>1.00</td>
<td>Oct. 10, 2014</td>
<td>First edition issued</td>
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1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   - In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable.
   - When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal.
   - Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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