APPLICATION NOTE

RX100 Series

Design Guide for Sub-Clock Circuits

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Abstract

The sub-clock oscillation circuit is a circuit with a low gain used to reduce power consumption. Due to the low gain, there is a risk that noise may cause the MCU to operate erroneously. This document describes how to minimize the risk when using a 32.768 kHz crystal.

Products

RX100 Series (LQFP, LFQFP, HWQFN, WFLGA, TFLGA packages)

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Points on Board Design

1.1 Points on Stabilizing Oscillation

1.1.1 Points on XCIN and XCOUT Wiring

① to ⑥ below describe points on XCIN and XCOUT wiring for a board that is at least 1.2 mm thick. Figure 1.1 shows an Example of Preferred Trace for XCIN and XCOUT Wiring for LQFP, LFQFP, and HWQFN Packages. Figure 1.2 shows an Example of Preferred Trace for XCIN and XCOUT Wiring When Using the WFLGA and TFLGA Package. Figure 1.3 shows an Example of Alternate Trace for XCIN and XCOUT Wiring

① Do not cross the XCIN and XCOUT wires with other signal wires.

② Do not add an observation pin to XCIN and XCOUT.

③ Make the XCIN and XCOUT wire width between 0.1 and 0.3 mm. The wire length from the MCU pins to the crystal resonator pins should be less than 10 mm, or at least as close to 10 mm if longer.

④ The wire connected to the XCIN pin and the wire connected to the XCOUT pin should have as much space between them (at least 0.3 mm) as possible.

⑤ Connect external capacitors as close together as possible. Connect the wire for the capacitors to the ground trace (hereinafter referred to as ground shield) on the component side. For details on the ground shield, refer to section 1.1.2. When the capacitors cannot be laid out as shown in Figure 1.1 and Figure 1.2, use the layout shown in Figure 1.3.

⑥ In order to decrease the parasitic capacitance between XCIN and XCOUT, include a ground trace between the resonator and the MCU.

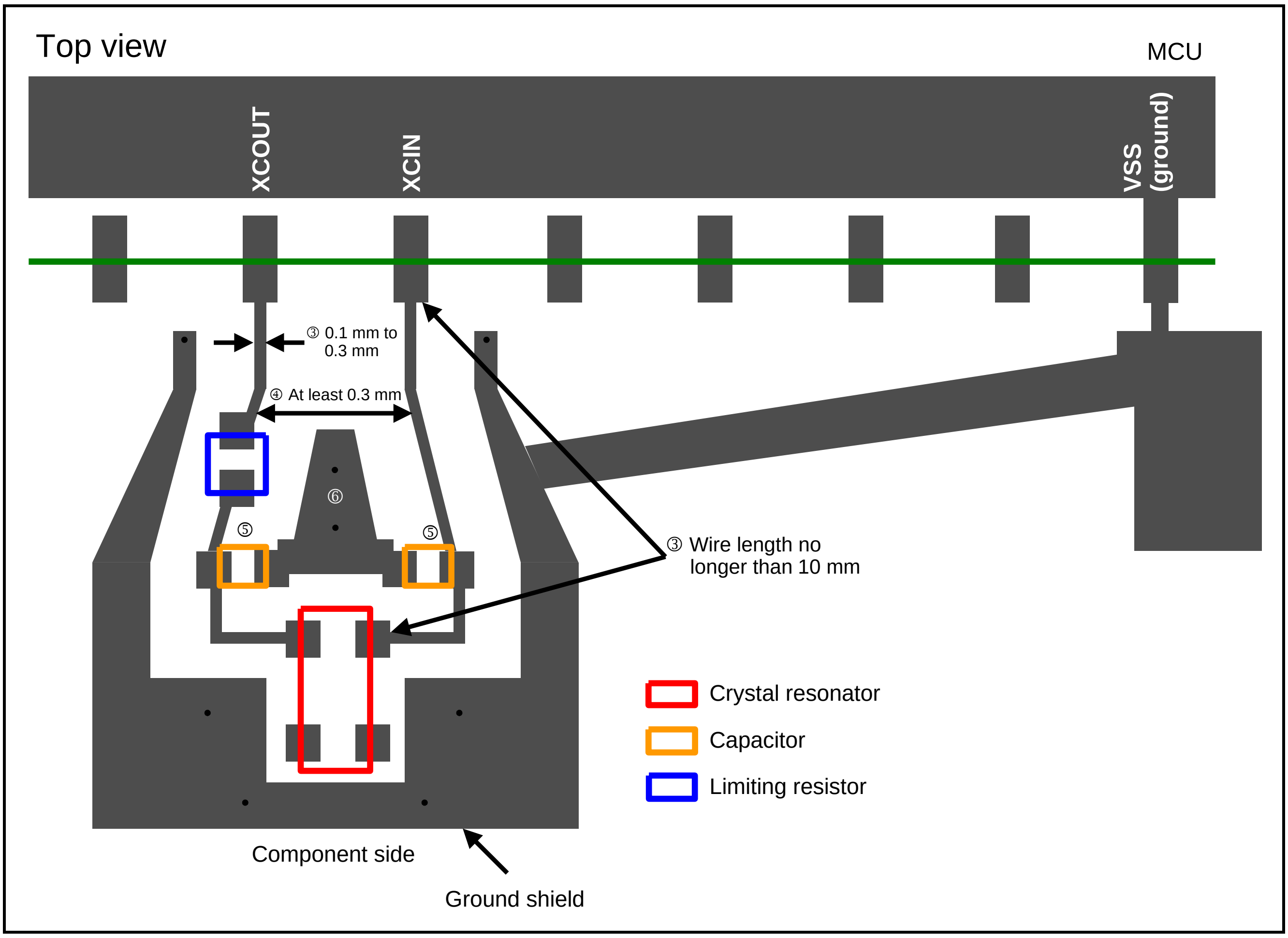

Figure 1.1 Example of Preferred Trace for XCIN and XCOUT Wiring for LQFP, LFQFP, and HWQFN Packages

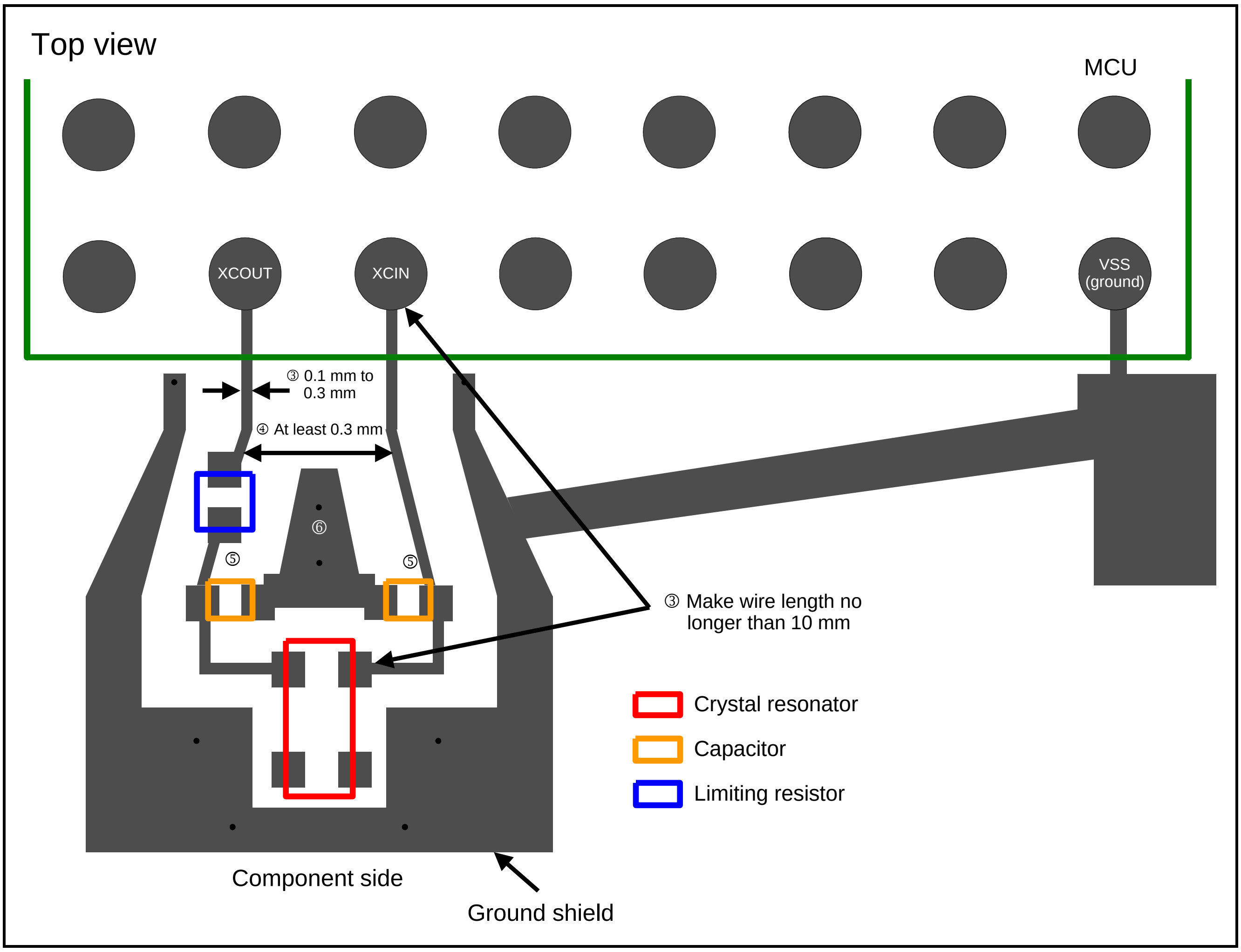

Figure 1.2 Example of Preferred Trace for XCIN and XCOUT Wiring When Using the WFLGA and TFLGA Packages

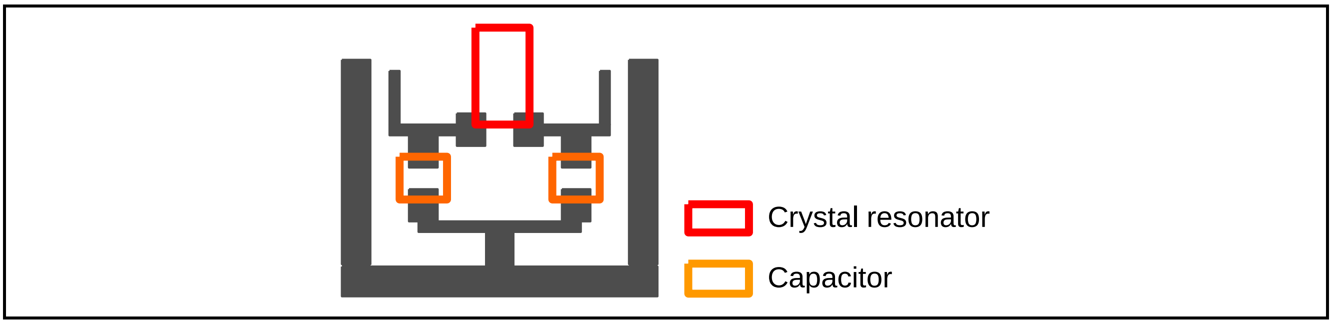

Figure 1.3 Example of Alternate Trace for XCIN and XCOUT Wiring

1.1.2 Points Regarding the Ground Shield

Shield the crystal resonator with a ground trace. ① to ④ below describe the points regarding the ground shield. Figure 1.4 and Figure 1.5 show trace examples.

① Lay out the ground shield on the same layer as the crystal resonator wiring.

② Wire the ground shield as close to the VSS pin on the MCU as possible, and ensure that the wire width is at least 0.3 mm.

③ To prevent current from running to the ground shield, branch the ground shield and the ground on the board near the VSS pin on the MCU.

④ Make the ground shield wire width at least 0.3 mm, and leave a 0.3 to 2.0 mm gap in between wires.

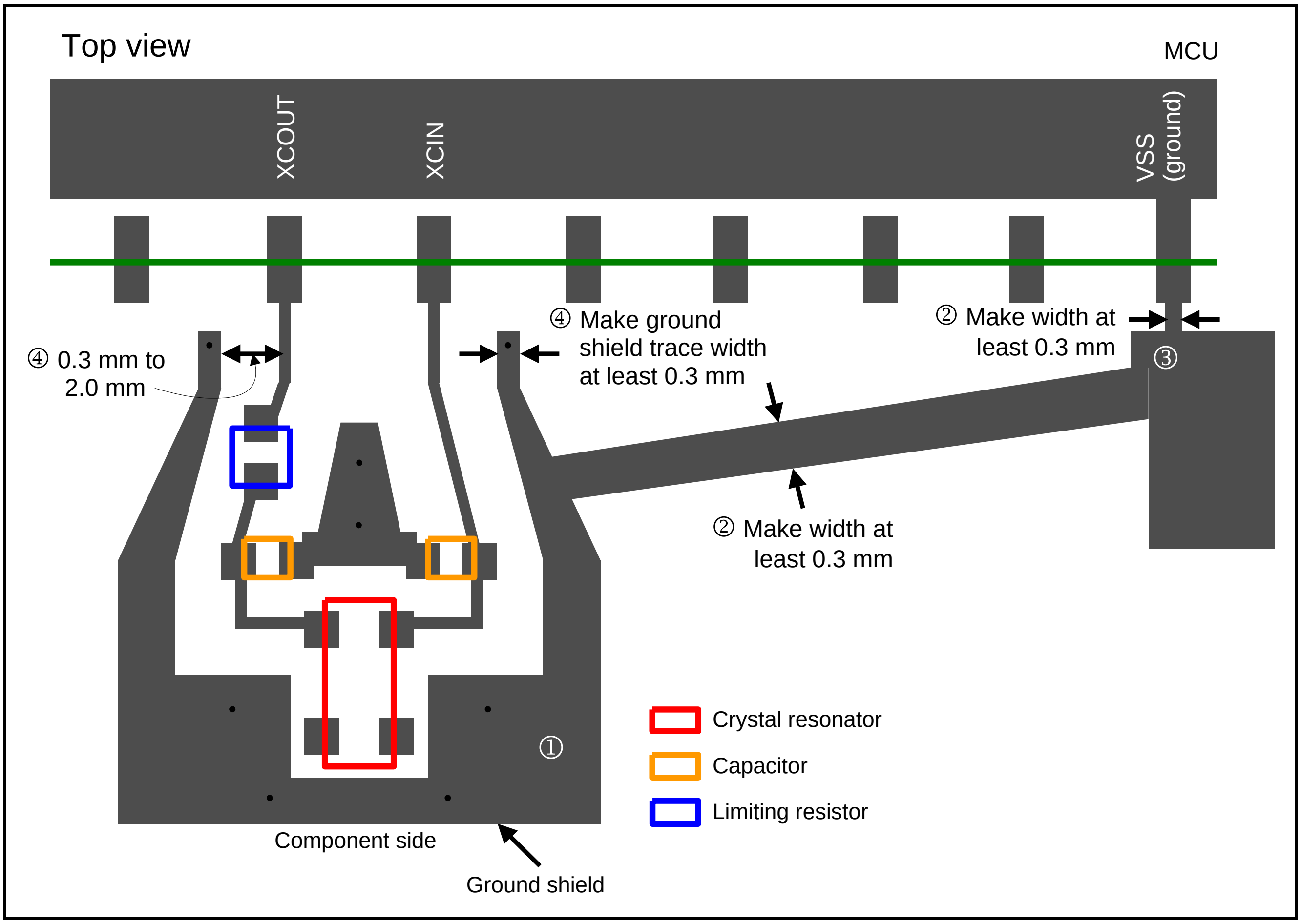

Figure 1.4 Trace Example for the Ground Shield When Using LQFP, LFQFP, and HWQFN Packages

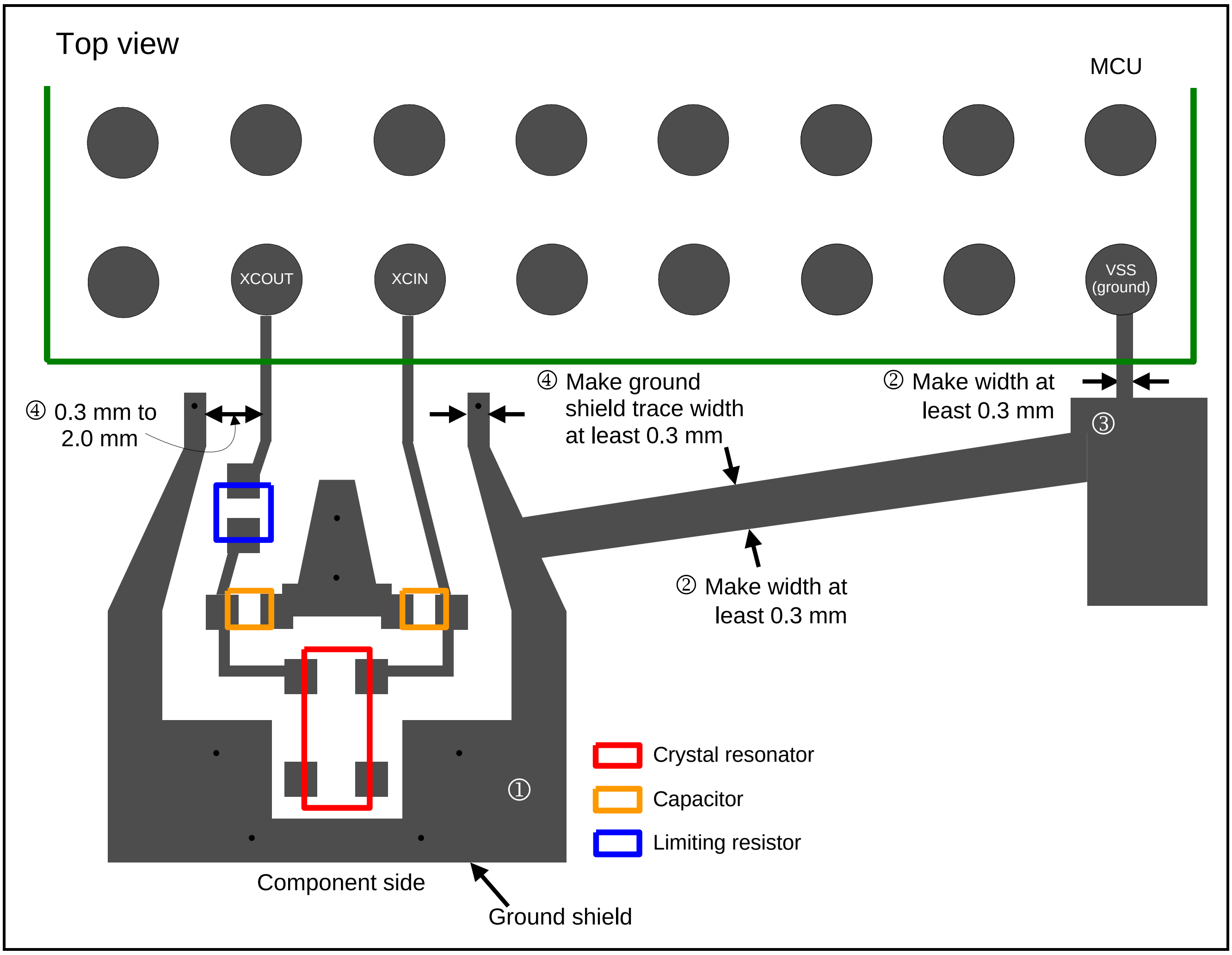

Figure 1.5 Trace Example for the Ground Shield When Using the WFLGA and TFLGA Packages

1.1.3 Points Regarding the Bottom Ground

1.1.3.1 Points When a Multilayered Board is at Least 1.2 mm

For boards that are at least 1.2 mm thick, lay out a ground trace on the solder side (hereinafter referred to as bottom ground) of the crystal resonator area (see Figure 1.6 and Figure 1.7).

① to ③ describe points when making a multilayered board that is at least 1.2 mm thick. Figure 1.6 and Figure 1.7 show trace examples.

① Do not lay out any traces in the middle layers of the crystal resonator area. Do not lay out power supply and ground traces in this area. Do not pass signal wires through this area either.

② Make the bottom ground at least 0.1 mm bigger than the ground shield. Connect the bottom ground on the solder side only to the ground shield on the component side connect the VSS pin through the ground shield.

③ Connect the ground shield terminator to the bottom ground.

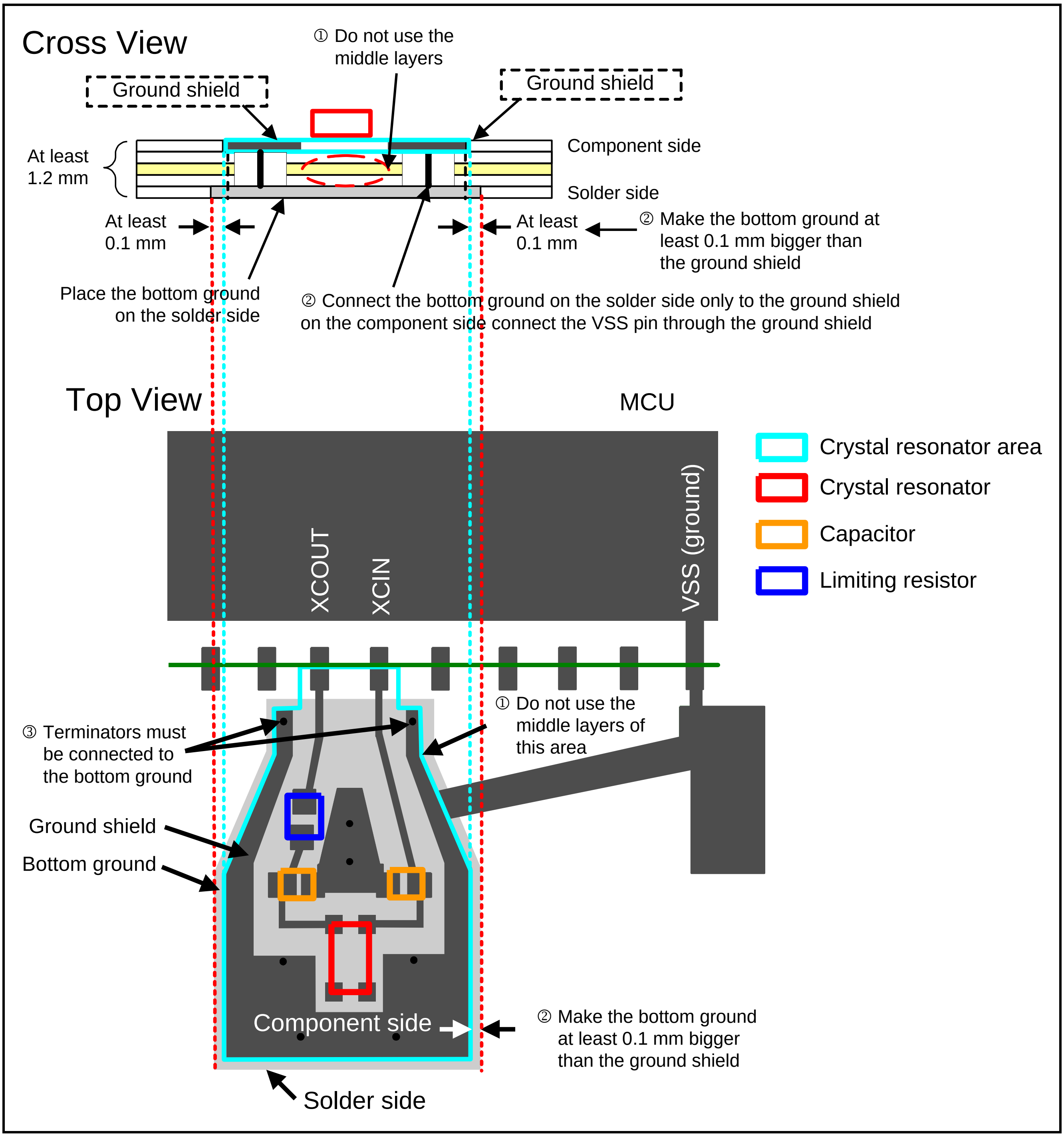

Figure 1.6 Trace Example If a Multilayered Board is at Least 1.2 mm Thick (When Using the LQFP, LFQFP, and HWQFN Packages)

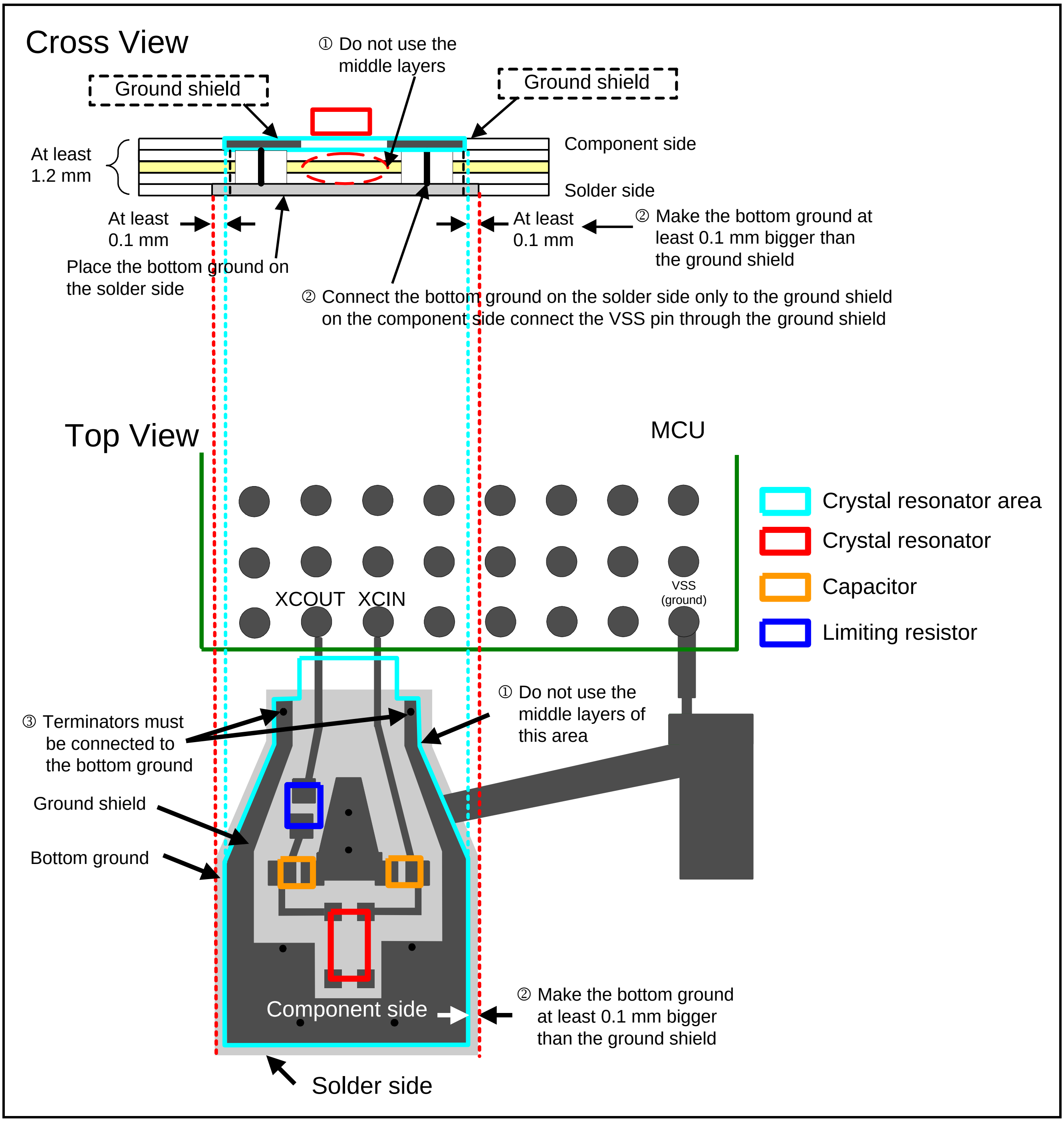

Figure 1.7 Trace Example If a Multilayered Board is at Least 1.2 mm Thick (When Using the WFLGA and TFLGA Packages)

1.1.3.2 Points When a Multilayered Board is Less Than 1.2 mm Thick

① describes points when making a multilayered board that is less than 1.2 mm thick. Figure 1.8 and Figure 1.9 show trace examples.

① Do not lay out any traces to layers other than the component side for the crystal resonator area. Do not lay out power supply and ground traces in this area. Do not pass signal wires through this area either.

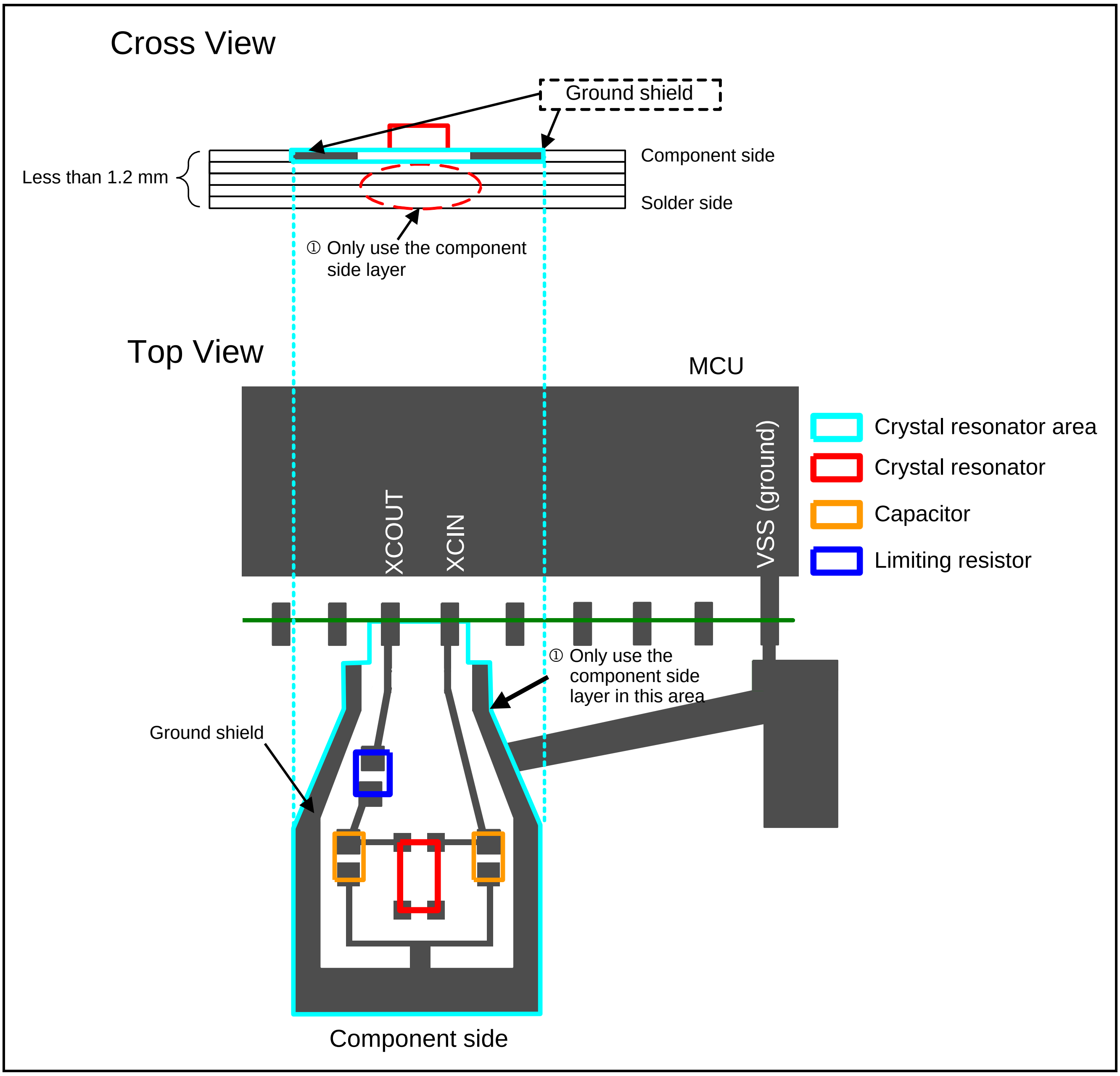

Figure 1.8 Trace Example If a Multilayered Board is Less Than 1.2 mm Thick (When Using the LQFP, LFQFP, and HWQFN Packages)

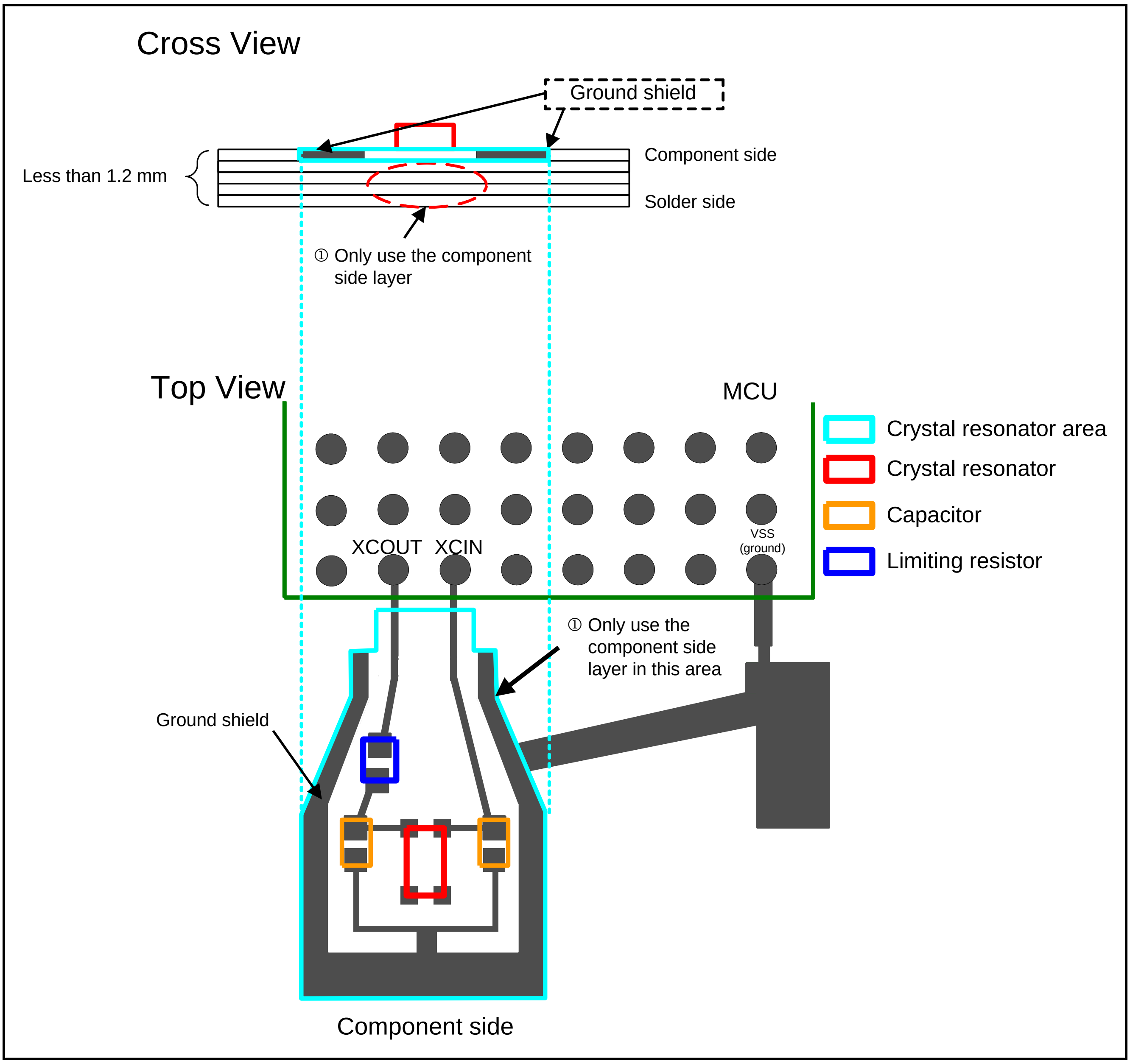

Figure 1.9 Trace Example If a Multilayered Board is Less Than 1.2 mm Thick (When Using the WFLGA and TFLGA Packages)

1.1.4 Other Points

① to ④ below describe other points. Figure 1.10 and Figure 1.11 show trace examples.

① Do not place the XCIN and XCOUT wires near wires that have big changes in current.

② Do not run the XCIN and XCOUT wires parallel to other signal wires like those for adjacent pins.

③ Pin wiring that runs adjacent to the XCIN and XCOUT pins should not directly be laid out outside the MCU. Lay out the wiring through the bottom side of the MCU first and then lay out the wiring to an area away from the XCIN and XCOUT pins (to avoid the wiring running parallel with the XCIN and XCOUT wiring).

④ Lay out as much of the ground trace on the bottom side of the MCU as possible.

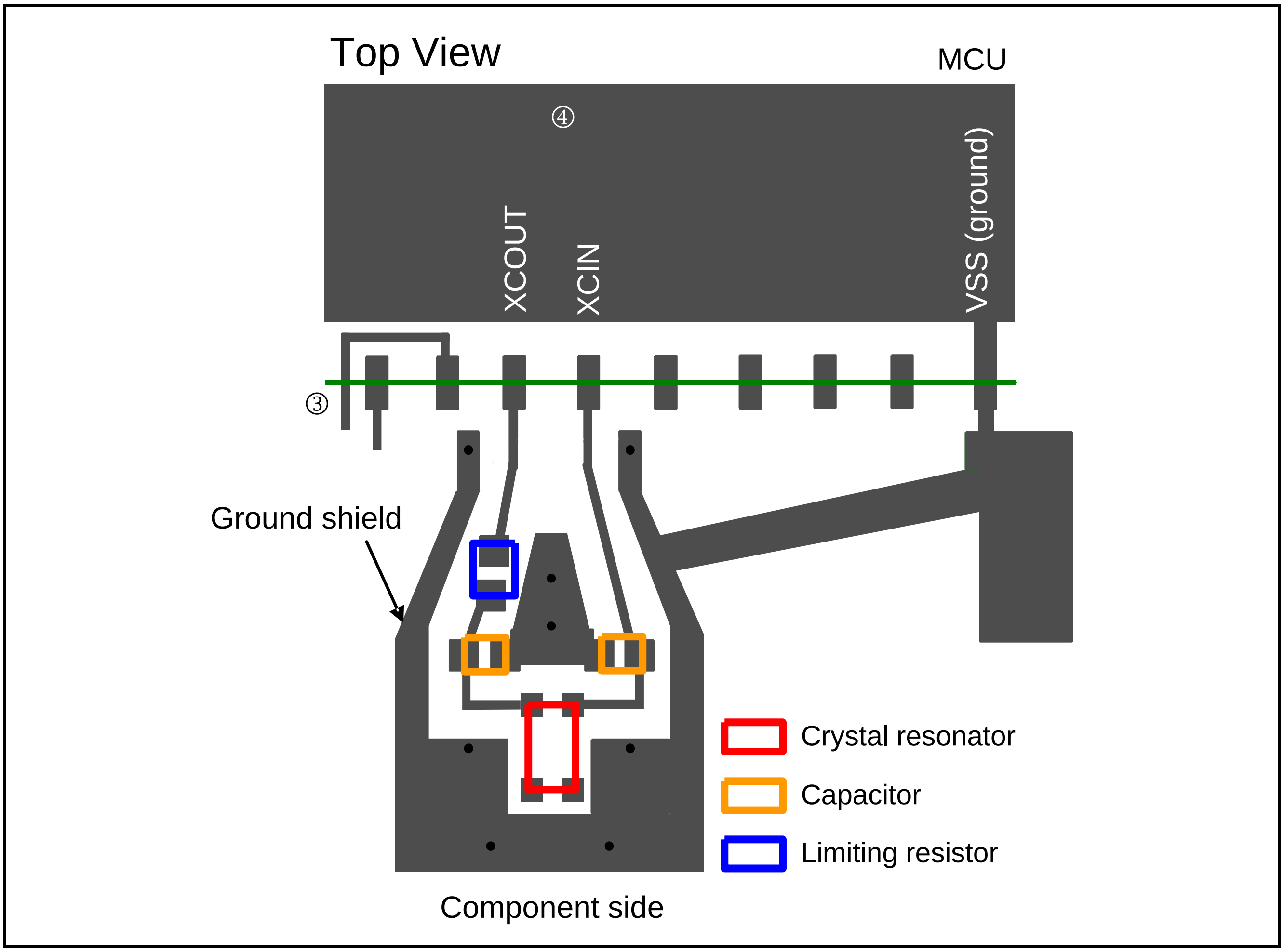

Figure 1.10 Trace Example for Other Points (When Using the LQFP, LFQFP, and HWQFN Packages)

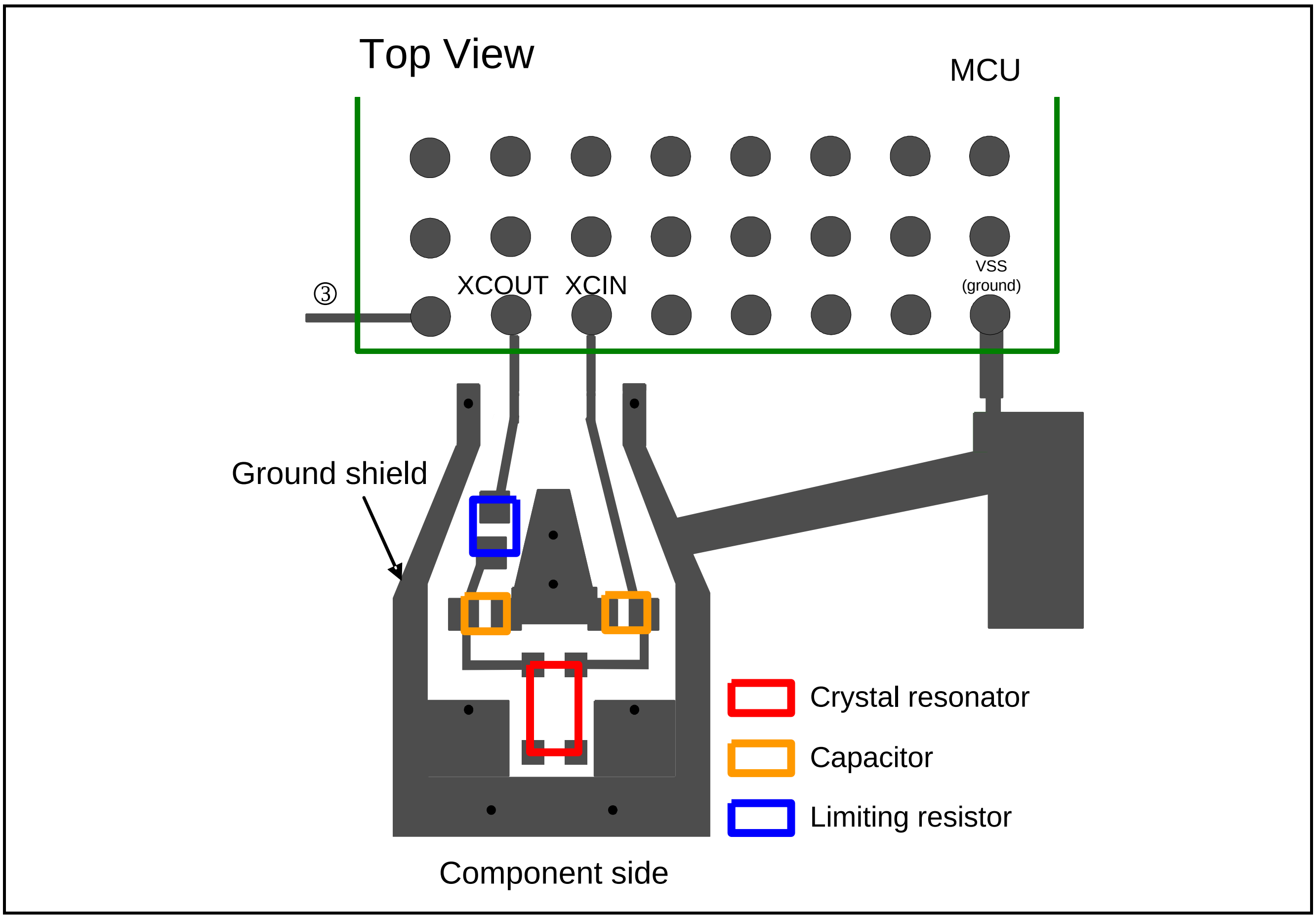

Figure 1.11 Trace Example for Other Points (When Using the WFLGA and TFLGA Packages)

1.1.5 Points on Wiring the Main Clock Resonator

① describes points on wiring the main clock resonator. Figure 1.12 shows a trace example.

① Shield the main clock resonator wiring with a ground. Branch the ground shield of the main clock and the sub-clock near the VSS pin. Note that if the main clock ground shield is connected directly to the sub-clock ground shield, there is a possibility that noise from the main clock resonator may transfer through and affect the sub-clock.

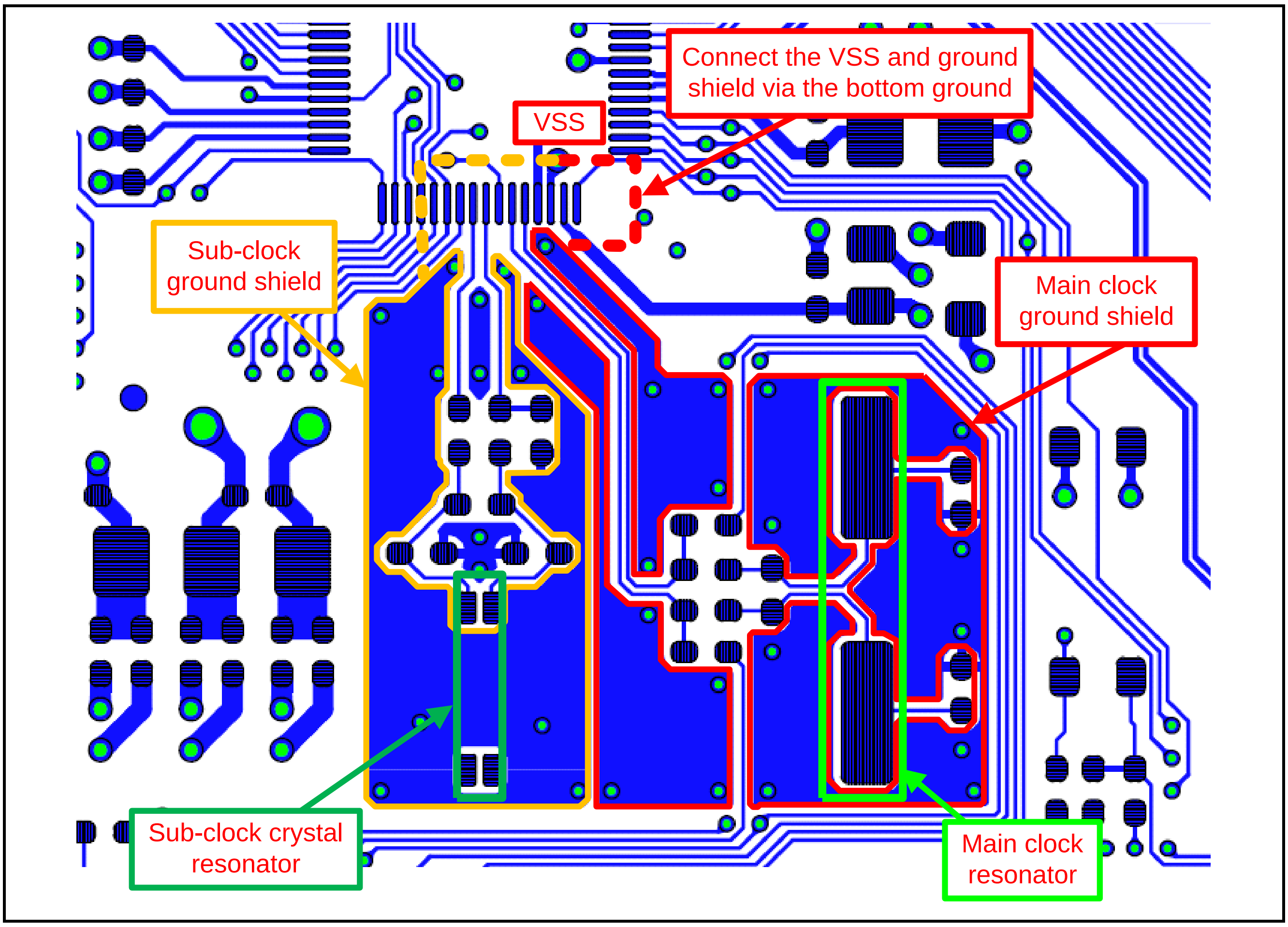

Figure 1.12 Trace Example When Shielding the Main Clock Resonator Wiring With a Ground

1.2 Trace Example Showing a High Risk of Erroneous Operation Due to Noise

Do not lay out traces described in ① through ⑨. Laying out the traces below may cause the 32.768 kHz crystal to operate erroneously. Figure 1.13 and Figure 1.14 show trace examples.

① XCIN and XCOUT wires cross other signal wires (risk of erroneous operation).

② Observation pins are attached to XCIN and XCOUT (risk of oscillation stopping).

③ XCIN and XCOUT wires are long (risk of erroneous operation or decreased accuracy).

④ The ground shield does not cover the entire area, and where there is a ground shield, the wiring is long or narrow (easily affected by noise, and there is a risk that accuracy will decrease due to the ground potential difference generated by the MCU and external capacitor).

⑤ Ground shield is not detached near VSS pin (risk of erroneous operation due to MCU current flowing to the ground shield).

⑥ Power supply or ground trace are under the XCIN and XCOUT wiring (risk of losing the clock or oscillation stopping).

⑦ A wire with a large current is routed nearby (risk of erroneous operation).

⑧ Parallel wiring for adjacent pins is close and long (risk of losing the clock or oscillation stopping).

⑨ The middle layers are used (risk of oscillation characteristics decreasing or signals operating erroneously).

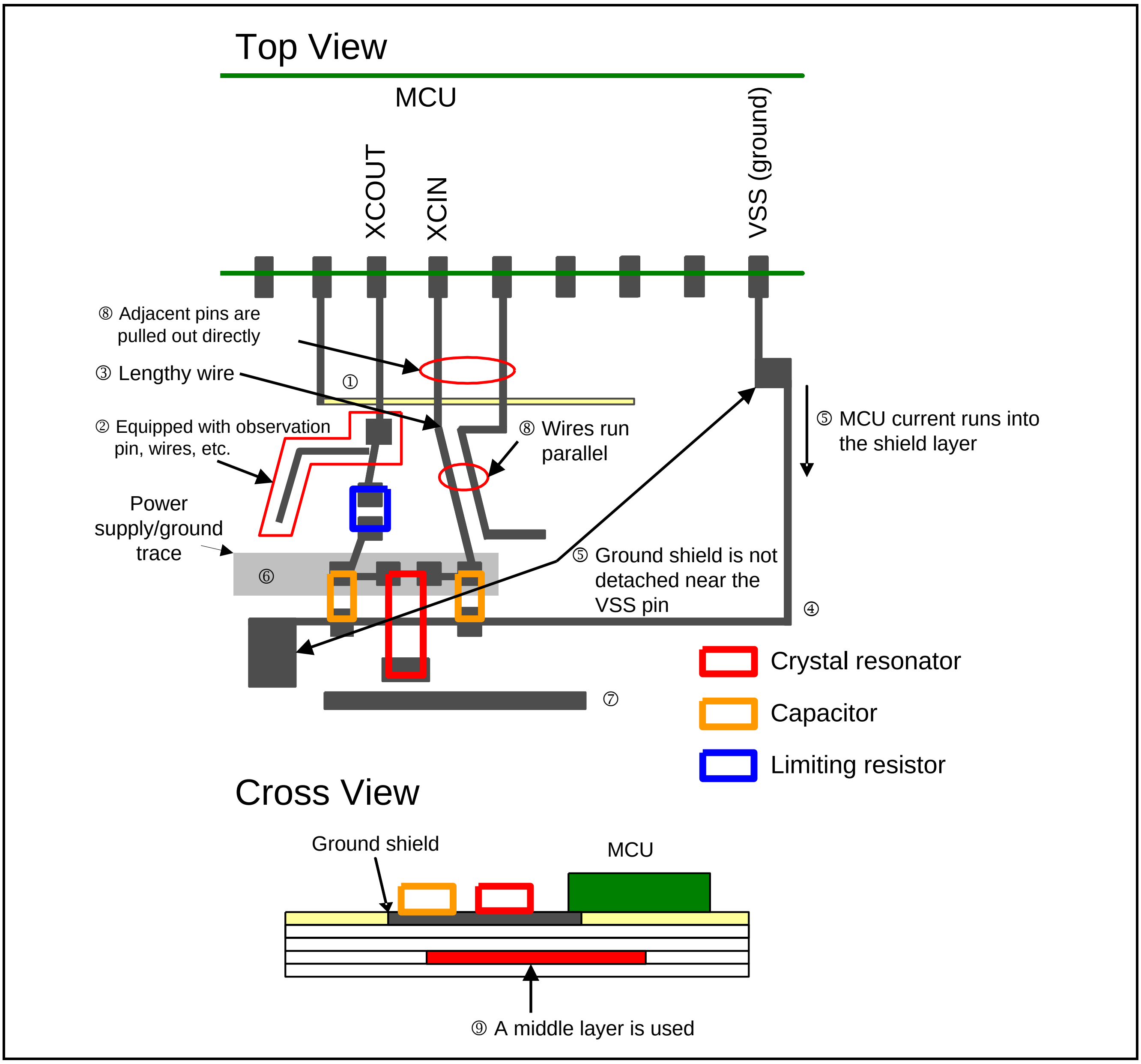

Figure 1.13 Trace Example Showing a High Risk of Erroneous Operation Due to Noise When Using the LQFP, LFQFP, and HWQFN Packages

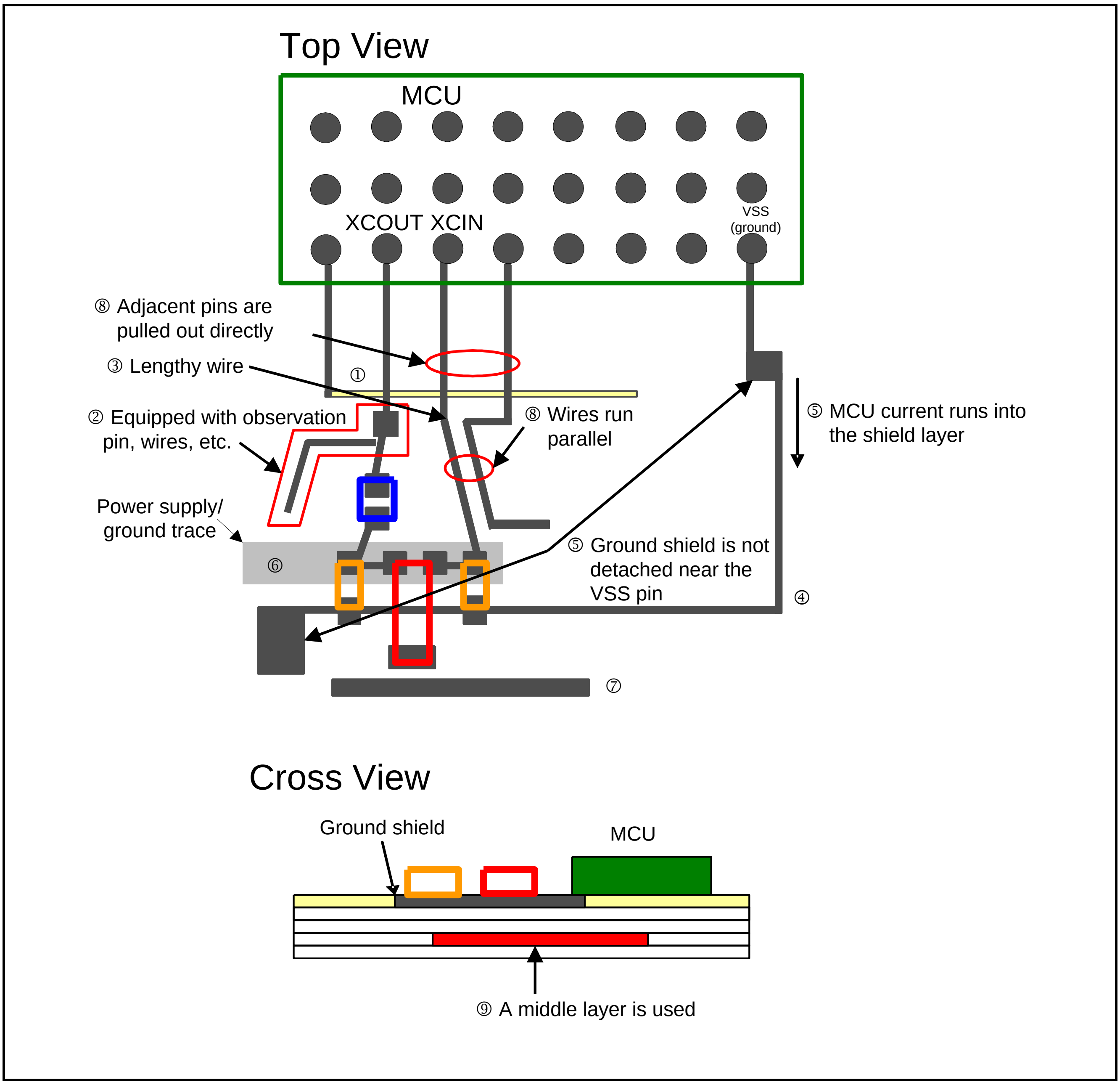

Figure 1.14 Trace Example Showing a High Risk of Erroneous Operation Due to Noise When Using the WFLGA and TFLGA Packages

1.3 Reference Oscillation Parameters and Confirmed Resonator Operation

1.3.1 Reference Oscillation Parameters and Confirmed Resonator Operation for the RX111 Group

Table 1.1 lists the Reference Oscillation Parameters for Confirmed Resonator Operation of the RX111 Group. Figure 1.15 shows the Trace Example for Confirmed Resonator Operation. The reference oscillation parameters in Table 1.1 have been confirmed for operation at 3.3 V and Ta = 25°C. Reference oscillation parameters are the same for the other RX100 Series.

Table 1.1 Reference Oscillation Parameters for Confirmed Resonator Operation of the RX111 Group

Manufacturer	Product	SMD/With Leads	Frequency (kHz)	Sub-Clock Oscillation Mode (RCR3.RTCDV[2:0] Bit Setting)	Load Capacity CL (pF)	Load Capacity Cg (1) (pF) ①	Load Capacity Cg (2) (pF) ②	Oscillation Stabilization Time (seconds)	Negative Resistance (kΩ)
Seiko Instruments Inc.	SSP-T7-F *1	SMD	32.768	Medium drive capacity (000b)	7.0	10	12	1.14	-407
Nihon Dempa Kogyo Co., Ltd.	NX3215SA *2	SMD	32.768	Medium drive capacity (000b)	6.0	8	8	0.5	-740
Nihon Dempa Kogyo Co., Ltd.	NX3215SA *2	SMD	32.768	Standard drive capacity (100b)	12.5	22	22	0.7	-530

Note 1. When using this resonator, contact Seiko Instruments for details on matching. (http://www.sii-crystal.com)

Note 2. When using this resonator, contact Nihon Dempa Kogyo for details on matching. (http://www.ndk.com/en/index.html)

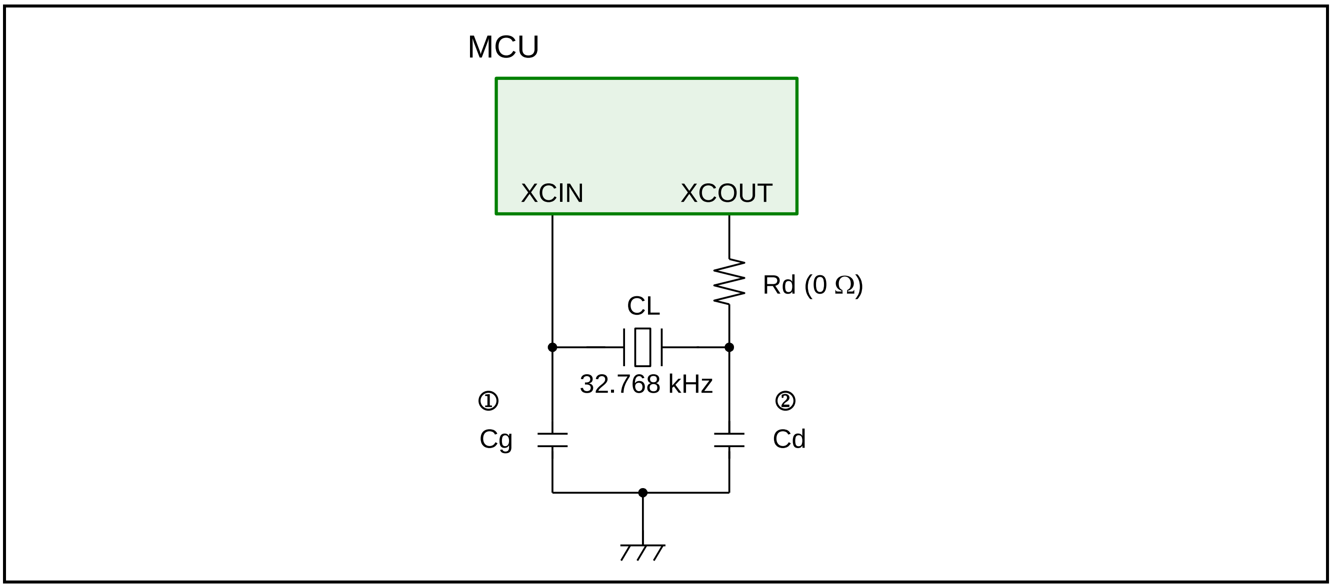

Figure 1.15 Trace Example for Confirmed Resonator Operation

The confirmed resonator operation and reference oscillation parameters listed here are based on information from the resonator manufacturer and are not guaranteed. As reference oscillation parameters are values evaluated under a given conditions by the manufacturer, values evaluated in the user system may vary. To achieve the optimum reference oscillation parameters for use in the actual user system, inquire with the resonator manufacturer to perform an evaluation on the actual circuit.

The conditions in the figure are conditions for oscillating the resonator connected to the MCU and are not operating conditions for the MCU itself. Refer to the specifications in the electrical characteristics for details on the MCU operating conditions.

2. Reference Documents

User's Manual: Hardware

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website

http://www.renesas.com

Inquiries

http://www.renesas.com/contact/

Revision History

Rev.	Date	Description: Page	Description: Summary
1.00	Apr. 1, 2014	-	First edition issued
1.01	Dec. 1, 2014	1	Deleted package information from Products
		1	Added the RX113 Group to Products
		18	Added reference oscillation parameters for the standard drive capacity to Table 1.1
		18	Added a sentence to explanation above Table 1.1 pertaining to the RX110 Group and RX113 having the same reference oscillation parameters as the RX111 Group.
		All	Changed the RX100 Series to individual groups
		All	Added LFQFP, HWQFN, and TFLGA packages
1.10	Mar. 7, 2016	1	Changed the target device to RX100 Series.
		19	Modified a sentence.
			Fixed the load capacity CL value of second line on Table 1.1. The value is changed from 8.0 pF to 6.0 pF.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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