

RX Family

Setting for Using Firmware Integration Technology with the Code Generator

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APPLICATION NOTE

Abstract

This application note describes procedures for setting firmware integration technology (FIT) and the code generator to be used together. The descriptions in this document assume that the product used is the RX64M Group. When using a product other than the RX64M Group, replace the description of the RX64M Group with the product used.

Products

RX Family

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.



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1. Overview

This document describes the setting procedures in three cases listed below when using the Board Support Package (BSP) FIT module for initial setting and clock settings, and using the code generator for setting the peripheral functions.

- 1. Procedure when starting a new project This is the procedure from generating a new project to the build. Refer to section 4.1 for details.
- 2. Procedure when changing the settings This procedure is used for setting the clocks and changing the conditions of peripheral functions for the project generated in (1) above. Refer to section 4.2 for details.
- Procedure when adding peripheral functions
 This procedure is used for adding peripheral functions to the project generated in (1) above. Refer to section 4.3 for details.

Restriction

The BSP FIT module cannot be used in conjunction with the code generator of the realtime clock (RTC)

2. Confirmed Operating Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below. Operation is not guaranteed if the e^2 studio or BSP module version is changed.

Item	Contents
MCU used	R5F564MLCDFC (RX64M Group)
Integrated development environment	Renesas Electronics Corporation e ² studio Version: 3.0.1.07
C compiler	Renesas Electronics Corporation C/C++ Compiler Package for RX Family V2.01.00
BSP module version	Version V.2.80
iodefine.h version	Version 0.9
Endian	Little endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Board used	Renesas Starter Kit+ for RX64M (product part no.: R0K50564MSxxxBE)

Table 2.1 Confirmed Operating Conditions

3. Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- Firmware Integration Technology User's Manual (R01AN1833EU)
- RX Family Board Support Package Module Using Firmware Integration Technology (R01AN1685EU)



4. Procedure When Using the BSP Module for Initial Settings and the Code Generator for the Peripheral Functions

Sections 4.1 to 4.3 describe setting procedures when using the Board Support Package (BSP) FIT module for initial setting and the code generator for the peripheral functions. The setting procedures in this section are described for the RX64M Group as an example. When using a product other than the RX64M Group, replace the description of the RX64M Group with the product used.

4.1 **Procedure for Creating a New Project**

This section describes the procedure from generating a new project, through setting the peripheral functions with the code generator, to the build. Figure 4.1 shows the flow for generating a new project. This section explains processing method described in the figure.



Figure 4.1 Procedure When Creating a New Project



1. Creating a new project.

Create a new project using project generation for the FIT

- (1) From the e^2 studio toolbar, select *File* > *New* > *C Project*.
- (2) Input a project name, select Renesas RXC toolchain as the toolchain, and click Next.
- (3) Select a target.
- (4) Uncheck the Release (no debug) in the configuration options and click Next.
- (5) Check the Use Peripheral code Generator box, and click Next.

e2 studio - Project Generation

Code Generator Settings

Use Peripheral code Generator

<u>Note</u>: When creating a project only for use with FIT, the box does not need to be checked, but in this case the code generator is used for the peripheral functions, so the box needs to be checked.

- (6) Change the Select Additional CPU Options and Global Options Settings as needed.
- (7) In the Standard Header Files, select 'C(C99)' for the library structure, and click Next.
- (8) Uncheck the Use User Stack, Use Heap Memory, Vector Definition Files, and I/O Register Definition Files, and click Finish.
- (9) When a project is created, delete the dbsct.c, project name.c, and typedefine.h files from the src folder.
- (10) Right click on the project, and select C/C++ Build > Settings > Linker > Section from Properties.
- (11) Click on *Remove Section* in the PResetPRG section and PIntPRG section.

(12) Change P section to "P* section".

(13) Click Apply.



2. Adding the BSP module.

The BSP module is added to the project created in step 1.

- (1) From the e2 studio toolbar, select *File > New > Renesas FIT Module*.
- (2) Select the project name to which the FIT module will be added.
- (3) Select the Family, Series, Group, and Target Board.
- (4) Select the r_bsp module.
- (5) Click Finish.

Add FIT Module		
IT Modules		
Select FIT Modules to	add to the	selected project
Name of the project f Family RX Series RX600 Group RX64M	to add FIT r Target Bo Toolchai	n Any RSKRX64M Application Any Reset
Module	Version	Description
r_bsp	2.80	Board Support Packages.

(6) Copy files r_bsp_config_reference.h and r_bsp_interruput_config_reference.h from the r_bsp\board\rskrx64m folder to the r_config folder and rename the files to "r_bsp_config.h" and "r_bsp_interruput_config.h", respectively.



(7) Configure the clock in r_bsp_config.h (select the clock source, set the frequency of the main clock, select the division ratios, etc.).

```
/* Clock source select (CKSEL)
  0 = Low Speed On-Chip Oscillator (LOCO)
  1 = High Speed On-Chip Oscillator (HOCO)
  2 = Main Clock Oscillator
  3 = Sub-Clock Oscillator
   4 = PLL Circuit
*/
#define BSP CFG CLOCK SOURCE (4)
/* Clock configuration options.
  The input clock frequency is specified and then the system clocks are set by
   specifying the multipliers used. The multiplier settings are used to set the clock
   registers in resetprg.c. If a 24MHz clock is used and the ICLK is 120MHz, PCLKA is
  120MHz, PCLKB is 60MHz, PCLKC is 60MHz, PCLKD is 60MHz, FCLK is 60MHz, USB Clock is
  48MHz, and BCLK is 120MHz then the settings would be:
  BSP CFG XTAL HZ = 24000000
  BSP CFG PLL DIV = 1 (no division)
  BSP CFG PLL MUL = 10.0 (24MHz x 10.0 = 240MHz)
  BSP CFG ICK DIV = 2: System clock (ICLK)
     (((BSP CFG XTAL HZ/BSP CFG PLL DIV) * BSP CFG PLL MUL) / (BSP CFG ICK DIV) = 120MHz
  BSP_CFG_PCKA_DIV = 2: Peripheral Clock A (PCLKA) =
     (((BSP CFG XTAL HZ/BSP CFG PLL DIV) * BSP CFG PLL MUL) / (BSP CFG PCKA DIV) = 120MHz
  BSP_CFG_PCKB_DIV = 4: Peripheral Clock B (PCLKB)
     (((BSP_CFG_XTAL HZ/BSP_CFG_PLL_DIV) * BSP_CFG_PLL_MUL) / (BSP_CFG_PCKB_DIV) = 60MHz
  BSP CFG PCKC DIV = 4: Peripheral Clock C (PCLKC) =
      (((BSP_CFG_XTAL_HZ/BSP_CFG_PLL_DIV) * BSP_CFG_PLL_MUL) / (BSP_CFG_PCKC_DIV) = 60MHz
  BSP CFG PCKD DIV = 4: Peripheral Clock D (PCLKD) =
     (((BSP_CFG_XTAL_HZ/BSP_CFG_PLL_DIV) * BSP_CFG_PLL_MUL) / (BSP_CFG_PCKD_DIV) = 60MHz
  BSP CFG FCK DIV = 4: Flash IF Clock (FCLK) =
     ((BSP_CFG_XTAL_HZ/BSP_CFG_PLL_DIV) * BSP_CFG_PLL_MUL) / (BSP_CFG_FCK_DIV) = 60MHz
  BSP CFG BCK DIV = 2: External Bus Clock (BCLK) =
     (((BSP CFG XTAL HZ/BSP CFG PLL DIV) * BSP CFG PLL MUL) / (BSP CFG BCK DIV) = 120MHz
  BSP CFG UCK DIV = 5: USB Clock (UCLK) =
     (((BSP_CFG_XTAL_HZ/BSP_CFG_PLL_DIV) * BSP_CFG_PLL_MUL) / (BSP_CFG_UCK_DIV) = 48MHz
*/
/* XTAL - Input clock frequency in Hz */
#define BSP CFG XTAL HZ (24000000)
/* The HOCO can operate at several difference frequencies. Choose which one using the
  macro below. Available frequency settings:
  0 = 16 MHz (default)
  1 = 18 MHz
  2 = 20 MHz
*/
#define BSP CFG HOCO FREQUENCY (0)
/* PLL clock source (PLLSRCEL). Choose which clock source to input to the PLL circuit.
  Available clock sources:
  0 = Main clock (default)
  1 = HOCO
*/
#define BSP_CFG_PLL_SRC (0)
/* PLL Input Frequency Division Ratio Select (PLIDIV).
  Available divisors = /1 (no division), /2, /3
*/
#define BSP_CFG_PLL_DIV (1)
/* PLL Frequency Multiplication Factor Select (STC).
  Available multipliers = x10.0 to x30.0 in 0.5 increments
   (e.g. 10.0, 10.5, 11.0, 11.5,..., 29.0, 29.5, 30.0)
*/
#define BSP_CFG_PLL_MUL (10.0)
```

(8) Select the platform. To select the platform, uncomment the *#include* for the board used.

Before

<u>After</u>

/* RDKRX63N */
//#include "./board/rdkrx63n/r_bsp.h"
/* RSKRX64M */
//#include "./board/rskrx64m/r_bsp.h"
/* RSKRX210 */
//#include "./board/rskrx210/r_bsp.h"

Atter	
/* RDKRX63N */ //#include "./board/rdkrx63n/r bsp.h	
/* RSKRX64M */	
<pre>#include "./board/rskrx64m/r_bsp.h" //* pswpy210 */</pre>	Uncommented
//#include "./board/rskrx210/r_bsp.h	

3. Changing the code generator properties.

Change the Generate File Mode in the Code Generator Property to Merge file.

(1) In the project created, right click on the *Code Generator* and select *Property*.

🍋 Project	Explorer 🔀			- 4	69		
a 😂 sar	mple_cg_fit						
⊳⊾	r bsp						
Þ 🖉	src						
▷ 🗁	r_config						
	sample cg f	it Debua	Jaunch				
	sample_cg_f	fit Hardw	areDebug.	launch			
⊳ 🛄	Code Genera	ator					
1	Generate Co	de					
8	Unload Cod	e Generat	tor				
	Property						

(2) In Properties view, change File generation control to Merge file.

sel	lected	
urce	Property	Value
	✓ Generate File Mode	
	API output control	Output all API functions according to the setting
	File generation control	Merge file
	Output folder	Do nothing if file exists
	Report type	Merge file
	 Microcontroller Information 	Overwrite file
	Microcontroller name	TOT JOHIVILEXI C
	Nick name	RX64M(4MB)
	Product Information	
	Release date	26/07/31 0:00:00
	Version	Code Generator 2, V1.01.00.02

The three options in the File Generation Control are explained in the following table.

File Generation Control	Processing After Code is Generated
Do nothing if file exists	If a file with the same name exists, a new file will not be output.
Merge file	If code is written in between the specified comments, that part is left as is and the code is updated.
Overwrite file	If a file with the same name exists, the existing file is overwritten by a new file.



4. Generating code for the peripheral functions

When code is generated, clocks and peripheral functions are set.

- (1) Click on the *Code Generator* in the project > *Peripheral Functions* > *Clock Generator*.
- (2) Configure the settings in those set to r_bsp_config.h in (7) of step 2.

Peripheral Functions 🔀			
Clock setting Block diagram			
Main clock oscillator and RTCMCLK setting			
Operation			
Main clock oscillator forced oscillation (only f	or RTC, software standby	and deep softwar	e standby mode)
Main clock oscillation source	Resonator		•
Frequency	24		(MHz)
Oscillator wait time	11000	(µs) (Actual v	alue: 11090.909 µs)
Oscillation stop detection function	Disabled		•
PLL circuit setting			
☑ Operation			
PLL clock source	Main clock oscillator		•
Input frequency division ratio	x 1 🔹		
Frequency multiplication factor	x 10.0 💌		
Frequency	240	(MHz)	
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting —	240	(MHz)	
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation	240	(MHz)	
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity	240 Drive capacity for low	(MHz)	•
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency	240 Drive capacity for low 32.768	(MHz)	• (kHz)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time	240 Drive capacity for low 32.768 2252.73	(MHz) v CL (ms) (Actual val	(kHz) ue: 2296.182 ms)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time High speed clock oscillator (HOCO) setting —	240 Drive capacity for low 32.768 2252.73	(MHz) v CL (ms) (Actual val	(kHz) ue: 2296.182 ms)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time High speed clock oscillator (HOCO) setting — Operation	240 Drive capacity for low 32.768 2252.73	(MHz) v CL (ms) (Actual val	(kHz) ue: 2296.182 ms)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time High speed clock oscillator (HOCO) setting Operation Frequency	240 Drive capacity for low 32.768 2252.73	(MHz) v CL (ms) (Actual val	 (kHz) ue: 2296.182 ms) (MHz)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time High speed clock oscillator (HOCO) setting — Operation Frequency Low speed clock oscillator (LOCO) setting —	240 Drive capacity for low 32.768 2252.73	(MHz) v CL (ms) (Actual val	 (kHz) ue: 2296.182 ms) (MHz)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time High speed clock oscillator (HOCO) setting — Operation Frequency Low speed clock oscillator (LOCO) setting — V Operation	240 Drive capacity for low 32.768 2252.73 16	(MHz) v CL (ms) (Actual val	 (kHz) ue: 2296.182 ms) (MHz)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time High speed clock oscillator (HOCO) setting Operation Frequency Low speed clock oscillator (LOCO) setting V Operation Frequency	240 Drive capacity for low 32.768 2252.73 16 240	(MHz) v CL (ms) (Actual val	 (kHz) ue: 2296.182 ms) (MHz) (kHz)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time High speed clock oscillator (HOCO) setting — Operation Frequency Low speed clock oscillator (LOCO) setting — Operation Frequency IwDPT-dedicated low-speed clock oscillator (IwDTLC	240 Drive capacity for low 32.768 2252.73 16 240 DCO) setting	(MHz) v CL (ms) (Actual val	 (kHz) ue: 2296.182 ms) (MHz) (kHz)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time High speed clock oscillator (HOCO) setting — Operation Frequency Low speed clock oscillator (LOCO) setting — Operation Frequency IWDT-dedicated low-speed clock oscillator (IWDTLCC Operation COPERATION	240 Drive capacity for low 32.768 2252.73 16 240 DCO) setting	(MHz)	 (kHz) ue: 2296.182 ms) (MHz) (kHz)
Frequency Sub-clock oscillator and RTC (RTCSCLK) setting — Operation Sub-clock oscillator drive capacity Frequency Oscillator wait time High speed clock oscillator (HOCO) setting — Operation Frequency Low speed clock oscillator (LOCO) setting — V Operation Frequency IWDT-dedicated low-speed clock oscillator (IWDTLC Operation Frequency	240 Drive capacity for low 32.768 2252.73 16 240 DCO) setting 120	(MHz)	 (kHz) ue: 2296.182 ms) (MHz) (kHz) (kHz)

NOTE: The peripheral function settings (counter value, bit rate, etc.) are calculated using the code generation settings. For proper operation under the BSP module settings, the clock generator setting of the code generator must match the setting of the BSP module.

- (3) In the project, click on Code Generator > Peripheral Functions > peripheral function used.
- (4) Use the graphic user interface (GUI) to select the desired conditions.
- (5) Click Generate Code.
- (6) Confirm that the source code has been generated in the project's src folder.

5. Modifying the file that includes the main function.

The file that was created by the code generator and includes the main function is modified. The default file name is r_{cg} main.c (hereinafter referred to as the main file). When adding code, refer to the following note.



(2) Add *#include* for platform.h.

Before change

After change



(3) Adding macro definitions

Copy the code and comments in the red box from r_cg_macrodriver.h and paste them in the main file.

(Extract part of the code for r_cg_macrodriver)

```
/************
                                             *****
         Macro definitions
         ******
                                           #ifndef __TYPEDEF__
                                                                                                                                              Copy
         /* Status list definition */
         #define MD_STATUSBASE (0x00U)
#define MD OK (MD_STATUSBASE + 0x00U) /* register setting OK */
        #define MD_STATUSBASE(MD_STATUSBASE + 0x00U) /* register sett.#define MD_SPT(MD_STATUSBASE + 0x01U) /* IIC stop */#define MD_NACK(MD_STATUSBASE + 0x02U) /* IIC no ACK */#define MD_BUSY1(MD_STATUSBASE + 0x03U) /* busy 1 */#define MD_BUSY2(MD_STATUSBASE + 0x04U) /* busy 2 */
         /* Error list definition */
         #define MD_ERRORBASE (0x80U)
#define MD_ERROR (MD_ERRORBASE + 0x00U) /* error */
        #defineMD_ERROR(MD_ERRORBASE + 0x00U) /* error */#defineMD_ARGERROR(MD_ERRORBASE + 0x01U) /* error argument input error */#defineMD_ERROR1(MD_ERRORBASE + 0x02U) /* error 1 */#defineMD_ERROR2(MD_ERRORBASE + 0x03U) /* error 2 */#defineMD_ERROR3(MD_ERRORBASE + 0x04U) /* error 3 */#defineMD_ERROR4(MD_ERRORBASE + 0x05U) /* error 4 */#defineMD_ERROR5(MD_ERRORBASE + 0x06U) /* error 5 */
         #endif
(Code for r cg main)
       Global variables and functions
       /* Start user code for global. Do not edit comment generated here */
                                                                                                                                           Paste
       /* Status list definition */
      #define MD_STATUSBASE (0x00U)
#define MD_OK (MD_STATUSBASE + 0x00U) /* register setting OK */
#define MD_SPT (MD_STATUSBASE + 0x01U) /* IIC stop */
#define MD_NACK (MD_STATUSBASE + 0x02U) /* IIC no ACK */
#define MD_BUSY1 (MD_STATUSBASE + 0x03U) /* busy 1 */
#define MD_BUSY2 (MD_STATUSBASE + 0x04U) /* busy 2 */
       /* Error list definition */
     #define MD_ERROR (MD_ERRORBASE + 0x00U) /* error */
#define MD_ARGERROR (MD_ERRORBASE + 0x01U) /* error argument input error */
#define MD_ERROR1 (MD_ERRORBASE + 0x02U) /* error 1 */
#define MD_ERROR2 (MD_ERRORBASE + 0x03U) /* error 2 */
#define MD_ERROR3 (MD_ERRORBASE + 0x04U) /* error 3 */
#define MD_ERROR4 (MD_ERRORBASE + 0x05U) /* error 4 */
#define MD_ERROR5 (MD_ERRORBASE + 0x06U) /* error 5 */
       /* End user code. Do not edit comment generated here */ Make sure to paste the code in between these two comments.
                                                                                                                     Make sure to paste the code in
```

(4) Adding the initialization function to peripheral functions

(4-1) Copy the code for the R_Systeminit function in r_cg_hardware_setup.c and paste it in the R_MAIN_UserInit function.

```
* Function Name: R_Systeminit
* Description : This function initializes every macro.
* Arguments
           : None
* Return Value : None
void R Systeminit (void)
                                                              (4-1) Copy
ł
   /* Enable writing to registers related to operating modes, LPC, CGC and software reset */
  SYSTEM, PRCR, WORD = 0xA50BU;
   /* Enable writing to MPC pin function control registers */
  MPC. PWPR. BTT. BOWT = 0U:
   MPC.PWPR.BIT.PFSWE = 1U;
   /* Initialize non-existent pins */
   PORT5.PDR.BYTE = 0x70U;
   /* Set peripheral settings */
   R CGC Create();
   R_MTU3_Create();
   /* Disable writing to MPC pin function control registers */
   MPC.PWPR.BIT.PFSWE = OU;
   MPC.PWPR.BIT.BOWI = 1U;
   /* Disable protection */
   SYSTEM. PRCR. WORD = 0xA500U;
}
```

(4-2) Delete the unused pin processing, and delete the call for the R CGC Create function.

```
* Function Name: R MAIN UserInit
* Description : This function initializes every macro.
* Arguments
             : None
* Return Value : None
                  void R Systeminit(void)
   /* Start user code. Do not edit comment generated here */
                                                                       (4-1) Paste
   /* Enable writing to registers related to operating modes, LPC, CGC and software reset */
   SYSTEM. PRCR. WORD = 0xA50BU;
   /* Enable writing to MPC pin function control registers */
   MPC.PWPR.BIT.BOWI = OU;
   MPC.PWPR.BIT.PFSWE = 1U;
   /* Initialize non-existent pins */ (4-2) Delete
   PORT5.PDR.BYTE = 0x70U;
    /* Set peripheral settings */
   R_CGC_Create(); (4-2) Delete
   R_MTU3_Create();
   /* Disable writing to MPC pin function control registers */
   MPC.PWPR.BIT.PFSWE = 0U;
   MPC.PWPR.BIT.BOWI = 1U;
   /* Disable protection */
   SYSTEM. PRCR. WORD = 0xA500U;
                                                            Make sure to paste the code in
   /* End user code. Do not edit comment generated here */\leftarrow
                                                            between these two comments.
}
```

(4-3) Add other processing

Add other processing that is executed before the infinite loop to (4-2). (e.g. start function call for timers, turning on LEDs, etc.)

6. Modifying files other than the main file

Modify files that were created at the code generation except the main file.

(1) Modify r_cg_macrodriver.h

Change the include path of iodefine.h (.././r_bsp/mcu/rx64m/register_access)

Before change

/**************************/ Includes ************************************
#include "iodefine.h"
<pre>#include <machine.h></machine.h></pre>

After change

7. Adding processing for interrupt functions

Interrupt handling for peripheral functions is performed in r_cg_*peripheral function name*_user.c. Interrupt functions are generated by the code generator. Add processing for the interrupt functions.

8. Deleting unnecessary files

The initial setting and clock setting can be set both by the BSP module and code generator. Since the settings are conflicting, delete the following files in the e^2 studio.

r_cg_cgc_user.c, r_cg_cgc.c, r_cg_cgc.h, r_cg_dbsct.c, r_cg_hardware_setup.c, r_cg_intprg.c, r_cg_resetprg.c, r_cg_sbrk.c, r_cg_sbrk.h, r_cg_stacksct.h, r_cg_vect.h, r_cg_vecttbl.c



Note on warnings displayed after the build

If *#includes* for stdint.h and $r_cg_macrodriver.h$ are added to the same file, the warnings below appear in *Problems* view after the build. This is because the same typedef is declared in both stdint.h generated by selecting C99 at project generation and $r_cg_macrodriver.h$ generated by the code generator.

escrip	rtion
ا 🚯 م	Warnings (6 items)
	W0520301: Typedef name has already been declared (with same type)
	M0520301: Typedef name has already been declared (with same type)
	M0520301: Typedef name has already been declared (with same type)
	W0520301: Typedef name has already been declared (with same type)
	W0520301: Typedef name has already been declared (with same type)
	W0520301: Typedef name has already been declared (with same type)

Follow the procedure below to delete these warnings. However, after regenerating the code in sections 4.2 Procedure When Changing the Settings and 4.3 Procedure When Adding Peripheral Functions, the procedure below must be performed again. Therefore, this procedure should be performed after all code generation is complete.

(1) Delete the following code from the r_cg_macrodriver.h file.

Typedef	definitions		
******	*****	*******	*
#ifndef	TYPEDEF		
typedef	signed char	<pre>int8_t;</pre>	
typedef	unsigned char	uint8_t;	
typedef	signed short	<pre>int16_t;</pre>	Delete
typedef	unsigned short	uint16_t;	Delete
typedef	signed long	int32 t;	
typedef	unsigned long	uint32 t;	
typedef	unsigned short	MD_STATUS	
#define	TYPEDEF	_	
#endif			

(2) Add #include for stdint.h to the r_cg_macrodriver.h file.





4.2 **Procedure When Changing the Settings**

This section describes the procedures for setting clocks and changing the conditions of the peripheral functions after a new project has been created (see section 4.1). Figure 4.2 shows the Procedure When Changing the Settings. This section also describes detailed processing for each step of the procedure.



Figure 4.2 Procedure When Changing the Settings

1. Modifying r_bsp_config.h

When changing the clock setting (PLL clock division and multiplication, PCLKB division, etc.), change r_bsp_config.h.

```
/* Peripheral Module Clock D Divider (PCKD).
Available divisors = /1 (no division), /2, /4, /8, /16, /32, /64
*/
#define BSP_CFG_PLL_SRC (4)
/* External Bus Clock Divider (BCLK).
Available divisors = /1 (no division), /2, /4, /8, /16, /32, /64
*/
#define BSP_CFG_BCK_DIV (4) Example: Change the BCLK division from divided by 2 to divided by 4.
/* Flash IF Clock Divider (FCK).
Available divisors = /1 (no division), /2, /4, /8, /16, /32, /64
*/
#define BSP_CFG_FCK_DIV (4)
```



2. Modifying the Code Generator

(1) When setting the clocks, set the *Clock Generator* to the same settings as those in r_bsp_config.h.

Clock source	PLL circu	it		•	
System clock (ICLK)	x 1/2	•	120	(MHz)	
Peripheral module clock (PCLKA)	x 1/2	•	120	(MHz)	
Peripheral module clock (PCLKB)	x 1/4	•	60	(MHz)	
Peripheral module clock for ADC (PCLKC)	x 1/4	•	60	(MHz)	
Peripheral module clock for ADC (PCLKD)	x 1/4	•	60	(MHz)	
External bus clock (BCLK)	x 1/4	•	60	(MHz)	Example: Change the BCLK division from divided by 2 to divided by 4
Flash IF clock (FCLK)	x 1/4	•	60	(MHz)	
USB clock (UCLK)	x 1/5	•	48	(MHz)	

(2) Change the peripheral functions as needed.

(3) Click *Generate Code*.

3. Modifying files that include the main function

When code generation is performed again, codes that are not placed between the comments described in "Note when adding code" in Step 5 of 4-1 Procedure When Creating a New Project are regenerated, so the modification below must be made. This modification is also performed when creating a new project, but they are regenerated when code generation is performed again.

(1) Delete *#includes* for r_cg_cgc.h.

4. Modifying files other than the main file

When code generation is performed again, the modification below must be made. These are also performed when creating a new project, but they are regenerated when code generation is performed again.

(1) Modify r_cg_macrodriver.h

Change the include path for iodefine.h (../../r_bsp/mcu/rx64m/register_access)

5. Changing processing for interrupt functions

Change processing for interrupt functions when necessary.

6. Deleting unnecessary files

Perform the same processing as step 8 in section 4.1 Procedure for Creating a New Project.



4.3 **Procedure When Adding Peripheral Functions**

This section describes the procedure for adding additional peripheral functions after a new project has been created (section 4.1 above). Figure 4.3 shows the Procedure When Adding Peripheral Functions. This section also describes detailed processing for each step of the procedure.



Figure 4.3 Procedure When Adding Peripheral Functions

1. Generating code for peripheral functions to be added

- (1) Configure settings for the peripheral functions to be added by the code generator.
- (2) Click Generate code.



2. Modifying Files That Include the main Function

Add code for the added peripheral function.

 Copy only the initial setting for the added peripheral function in the R_Systeminit function in r_cg_hardware_setup.c. (the initial setting function name for the peripheral functions is r_cg_<peripheral function>_Creat function).

```
* Function Name: R_Systeminit
* Description : This function initializes every macro.
* Arguments
            : None
* Return Value : None
void R_Systeminit(void)
ł
   /* Enable writing to registers related to operating modes, LPC, CGC, and software reset */
   SYSTEM. PRCR. WORD = 0xA50BU;
  /* Enable writing to MPC pin function control registers */
MPC.PWPR.BIT.BOWI = 0U;
   MPC. PWPR. BIT. PFSWE = 1U;
   /* Initialize non-existent pins */
   PORT5.PDR.BYTE = 0x70U;
   /* Set peripheral settings */
   R_CGC_Create();
  R_LVD1_Create(); Only copy the initial settings for the peripheral function added
   R MTU3 Create();
   /* Disable writing to MPC pin function control registers */
   MPC.PWPR.BIT.PFSWE = OU;
   MPC.PWPR.BIT.BOWI = 1U;
   /* Disable protection */
   SYSTEM. PRCR. WORD = 0xA500U;
}
```

(2) Add the function copied in (2-1) to the R_MAIN_UserInit function.

```
* Function Name: R MAIN UserInit
* Description : This function adds user code before implementing main function.
* Arguments : None
* Return Value : None
void R MAIN UserInit(void)
ł
   /* Start user code. Do not edit comment generated here */
   /* Enable writing to registers related to operating modes, LPC, CGC and software reset */
   SYSTEM. PRCR. WORD = 0xA50BU;
   /* Enable writing to MPC pin function control registers */
   MPC.PWPR.BIT.BOWI = OU;
   MPC.PWPR.BIT.PFSWE = 1U;
  /* Set peripheral settings */
R_LVD1_Create(); Add the copied function
   R_MTU3_Create();
   R_MTU3_C0_Start();
   LED0 = LED ON;
   /* Disable writing to MPC pin function control registers */
   MPC.PWPR.BIT.PFSWE = OU;
   MPC.PWPR.BIT.BOWI = 1U;
   /* Disable protection */
   SYSTEM. PRCR. WORD = 0xA500U;
   /* End user code. Do not edit comment generated here */
ł
```

The following processing needs to be performed every code generation.

(3) Delete *#includes* for r_cg_cgc.h.

3. Modifying Files Other Than the main File

When code generation is performed again, the modification below must be made. These are also performed when creating a new project, but they are regenerated when code generation is performed again.

(1) Modify r_cg_macrodriver.h

Change the include path for iodefine.h (../../r_bsp/mcu/rx64m/register_access)

4. Changing the Processing of the Interrupt Functions for the Added Peripheral Function

Add processing when the added peripheral function uses the interrupt functions.

Interrupt handling for peripheral functions is performed in "r_cg_name of peripheral function_user.c".

5. Deleting Unnecessary Files

Perform the same processing as step 8 in section 4.1 Procedure for Creating a New Project.



5. Reference Documents

User's Manual: Hardware

RX64M Group User's Manual: Hardware Rev.1.00 (R01UH0377EJ)

When using a product other than the RX64M Group, refer to User's Manual: Hardware for the product used. The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Environment

RX Family Compiler CC-RX V2.01.00 User's Manual: RX Coding Rev.1.00 (R20UT2748EJ) The latest version can be downloaded from the Renesas Electronics website.

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Inquiries http://www.renesas.com/contact/



REVISION HISTORY

RX Family Application Note Setting for Using Firmware Integration Technology with the Code Generator

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 26, 2014	—	First edition issued
1.10	Mar. 2, 2015	—	Changed the target device from the RX64M Group to the RX Family

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
 In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
- 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

— The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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