

RX Family

Sample Program for Open Source FAT File System Library M3S-TFAT-Tiny Module with Serial NOR Flash Memory

Abstract

This application note describes how to use the sample program for the open source FAT file system library M3S-TFAT-Tiny module with serial NOR flash memory. Hereinafter, the "M3S-TFAT-Tiny module" is referred to as the "TFAT library".

Target device

RX72N Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Outline

1.1 About This Application Note

This application note describes how to use the TFAT library with serial NOR flash memory. In this application note, you create a FAT file system work area in serial NOR flash memory by using the TFAT library, and then write files to, and read files from, the area.

This application note is bundled with a sample program that is compatible with the RX72N Envision Kit. If you want to use another device, refer to "5. Board-Dependent Settings".

1.2 Environment in Which Operation Was Verified

Operation of the sample program bundled with this application note was verified under the conditions shown below.

Item	Description
MCU used	R5F572NNHDFB (RX72N Group)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics e ² studio 2024-01
C compiler	Renesas Electronics C/C++ Compiler for RX Family V3.06.00
Compiler option	The "-lang=c99" and "-optimize=0" options were added with the default settings specified in the integrated development environment.
Endianness	Little endian
Operating mode	Single-chip mode
Sample program version	Rev.1.00
Board used	RX72N Envision Kit (model: RTK5RX72N0C00000BJ)
Serial NOR flash memory used	Macronix MX25L3233F (32 megabits)

 Table 1.1
 Operating Environment

1.3 Configuration of This Application Note

This application note consists of the items listed below.

Table 1.2 Configuration of This Application Note

Item		Description	
r01an7	7187jj0100_rx.pdf	Application note document (Japanese version)	
r01an7187ej0100_rx.pdf		Application note document (English version)	
worksp	Dace		
	TFAT_sample_RX72N_with_Flash	Sample program for the RX72N	
		(compatible with e ² studio) ^{*1}	

Note: 1. The e² studio project can be converted to a CS+ project.



1.4 Modules

Table 1.3 lists the FIT modules used in the sample program that is bundled with this application note. These FIT modules are provided by RX Driver Package v1.42.

Table 1.3	List of FIT	Modules Used
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Category	Application Note (Document Number)	FIT Module	Rev.
BSP	RX Family Board Support Package Module Using Firmware Integration Technology (R01AN1685)	r_bsp	7.42
Device driver	RX Family CMT Module Using Firmware Integration Technology (R01AN1856)	r_cmt_rx	5.60
	RX Family QSPI Clock Synchronous Single Master Control Module Using Firmware Integration Technology (R01AN1940)	r_qspi_smstr_rx	1.21
	RX Family Clock Synchronous Control Module for Serial NOR Flash Memory Access Firmware Integration Technology (R01AN2662)	r_flash_spi	3.30
Middleware	RX Family System Timer Module Firmware Integration Technology (R20AN0431)	r_sys_time_rx	1.01
	RX Family Memory Access Driver Interface Module Using Firmware Integration Technology (R01AN4548)	r_memdrv_rx	1.20
	RX Family M3S-TFAT-Tiny Memory Driver Interface Module Firmware Integration Technology (R20AN0335)	r_tfat_driver_rx	2.30
	RX Family Open Source FAT File System M3S-TFAT-Tiny Module Firmware Integration Technology (R20AN0038)	r_tfat_rx	4.10



2. Hardware Description

2.1 Hardware Configuration

The target board of this application note is equipped with Macronix serial NOR flash memory. Table 2.1 shows the pin connections between the MCU on the target board and the serial NOR flash memory.

Table	2.1	Pin	Connections
-------	-----	-----	-------------

Pin Name/Signal	Input/Output	Description
PD4/QSSL-B	Output	Chip Select
PD5/QSPCLK-B	Output	Clock
PD6/QIO0-B	Input/output	Bidirectional Data 0
PD7/QIO1-B	Input/output	Bidirectional Data 1
PD2/QIO2-B	Input/output	Bidirectional Data 2
PD3/QIO3-B	Input/output	Bidirectional Data 3

3. Executing the Sample Program

3.1 Launching the Workspace

- 1. Start e² studio. The dialog box for selecting the workspace opens. If the dialog box does not open, from the [File] menu, select [Switch Workspace] and then [Others].
- 2. Select any workspace of your choice, and then click [Launch].

		×
opment artifacts.		
	~	Browse
bace		
	opment artifacts.	~



3. From the [File] menu, select [Import].





4. Under the [General] node, select [Existing Projects into Workspace], and then select [Next].

Import				
Select Choose import wizard.			Ľ	
Select an import wizard:				
type filter text				
 ✓ Seneral 			^	
📮 File System	Select [Exis	tina Proiec	ts into Wo	orkspacel.
 Preferences Projects from Folder or Archive Rename & Import Existing C/C++ Project into Renesas CC-RX project conversion to Renesas Renesas CS+ Project for CA78K0R/CA78K0 Renesas CS+ Project for CC-RX, CC-RL and CC- Renesas GitHub FreeRTOS (with IoT libraries) P 	Workspace GCC RX -RH			
		Select	[Next >].	
O Kack Next	> Fini	ish	Cancel	-



- 5. Select [Browse] and specify the sample program bundled with this application note.
- 6. Select [Finish].

3 Import –	
Import Projects	
Select a directory to search for existing Eclipse projects.	
Select root directory: C:¥workspace¥TFAT_sample_RX72N_with_FLASH	Browse Select [Browse]
○ Select archive file:	Browse And specify the sample program
Projects:	bundle with this application note.
✓ TFAT_sample_RX72N_with_FLASH (C:¥workspace¥TFAT_sample_RX72N_with_FLAS	Select All
	Deserect All
	Refresh Select the sample project .
< >	
Options	
Search for nested projects	
Copy projects into workspace	
Close newly imported projects upon completion	
Hide projects that already exist in the workspace	
Working sets	
Add project to working sets	New Select [Finish].
Working sets:	Select
Compared and the second s	Cancel



3.2 Executing the Sample Program and Verifying Its Operation

This section describes how to execute the sample program that you imported and how to verify its operation.

1. Select the Build icon to build the imported sample program.





2. When the building is complete, perform debugging to verify operation. To perform debugging, open [Debug Configurations].





3. Open the debug configurations for the sample program that you built, and then start debugging it.

) 🖻 🕫 🔛 🗮 🖻 🏹 🔹	Name: TFAT_sample_RX72N_with_FLASH HardwareDebug	
C/C++ Application	Main Debugger Startup Common Source Project:	
C/C++ Remote Application EASE Script	TFAT_sample_RX72N_with_FLASH	Browse
GDB Hardware Debugging	C/C++ Application:	Diowse
C GDB Simulator Debugging (RH850)	HardwareDebug/TFAT sample RX72N with FLASH.x	
 C Renesas GDB Hardware Debugging TFAT_sample_RX72N_with_FLASH Hardw Renesas Simulator Debugging (RX, RL78) 	Variables Search Project Build (if required) before launching Build Configuration: Select Automatically Image: Disable auto build Image: Disable auto build Image: Disable auto build Image: Disable auto build	
Click	[Debug] button	
<	> Reyert	Apply

4. At this time, e² studio displays a pop-up window that confirms whether to switch the perspective. Switch it if necessary.

Confirm Perspective Switc	h	×
This kind of launch is configu	red to open the Debug perspective when it suspends.	
This Debug perspective supp debug stack, variables and br	orts application debugging by providing views for displaying the eakpoints.	
Switch to this perspective?	Click [Switch] button.	
Remember my decision	Switch No	





5. Open Renesas Debug Virtual Console so that you can view the operation results.



- 6. Execute the sample program. workspace - TFAT_sample_RX72N_with_FLASH/src/smc_gen/r_bsp/mcu/all/resetprg.c - e² studio \times _ Eile Edit Source Refactor Navigate Search Project Renesas Views Run Window Help Section 1 → Se 🔍 🔡 🗟 C/C++ 🦨 Smart Configurator 🎋 Debug Debug X 🖓 🗖 🗘 🕪 V 🂁 B 🗙 隆 P 🛠 E 📭 E 🔲 I 🤭 🗖 🗖 207 ffc000000 ⊖ R_BSP_POR_FUNCTION(R_BSP_STARTUP_FUNCTION) 💠 💥 💥 🧬 🕾 🔌 Þ 🕀 🕀 😂 😫 ^ ✓ C TFAT_sample_RX72N_with_F /* Stack pointers are setup prior to calling this f 209 ✓ ⑦ TFAT_sample_RX72N_with 210 211 Select [Resume] button. n this function but 212 213 214 * will be unavailable after you change the stack f PowerON_Reset_P(rx-elf-gdb -rx-force-isa= /* The bss sections have not been cleared and the d * and constructors of C++ objects have not been ex Renesas GDB server (Hos 216 217 #if defined(__GNUC__)
 #if BSP_CFG_USER_STACK_ENABLE == 1 218 INTERNAL_NOT_USED(ustack_area); INTERNAL_NOT_USED(istack_area); #endif 219 220 221 223 e #if defined(__CCRX__) || defined(__GNUC__) /* Initialize the Interrupt Table Register */ 226 ffc0000e 227 R_BSP_SET_INTB(R_BSP_SECTOP_INTVECTTBL); 228 Hifdef RSP MCII EXCEPTION TABLE > - 0 😑 Console 🔠 Registers 🔝 問題 🧠 Smart Browser 🖳 Debugger Console 📮 Renesas Debug Virtual Console 🗡 🚺 Memory r 📭 🖼 🖉 🖉 🚮 🥵 🖻 🖇 <
- 7. If the program execution was successful, the following messages are displayed in Renesas Debug Virtual Console:



If the following message is displayed, you must format the serial NOR flash memory: Error (FR_NO_FILESYSTEM) Drive mount Format the serial NOR flash memory by referring to "4.4.2 Formatting Process" and "7.1 About the Formatting Process".

If the program execution was successful,



4. Sample Program

4.1 Overview

The sample program is an e² studio project that is compatible with the target board shown in Table 1.1 Operating Environment.

4.2 Flowchart

Figure 4.1 shows the flowchart of the "main" function of the sample program.



Figure 4.1 Flowchart of the "main" Function



4.3 Module Initialization

Before you can use serial NOR flash memory with the TFAT library, you must initialize the following modules: • r_sys_time_rx

- r_flash_spi
- r_tfat_driver_rx

You must also initialize the settings of the pins that are connected to the serial NOR flash memory.

4.3.1 Flowchart



Figure 4.2 Flowchart of the Module Initialization Processes

4.3.2 System Timer Initialization

The system timer initialization process initializes the r_sys_time_rx module. This module is used to set the file update time.

4.3.3 Device Driver Initialization

The device driver initialization process initializes the r_flash_spi module. This module configures the communication with the serial NOR flash memory. It also registers the callback function that checks whether the flash memory is busy as a periodic timer callback for the r_sys_time_rx module at an interval of 10 ms.

4.3.4 Middleware Initialization

The middleware initialization process initializes the r_tfat_driver_rx module. This module also registers its own callback function that checks whether the flash memory is busy as a periodic timer callback for the r_cmt_rx module at an interval of 1 ms. For more detailed information, refer to "7.2 Timer Function for Serial NOR Flash Memory".



4.4 File Manipulation

4.4.1 Flowchart



Figure 4.3 Flowchart of File Manipulation Processes

4.4.2 Formatting Process

The open source FAT file system FatFs provides several optional settings that are defined in "ffconf.h". You can change the values of these settings to customize the API functions and FatFs features that are available to you. You cannot change these settings by using Smart Configurator.

These FatFs settings include the FF_USE_MKFS definition shown in Table 4.1 Formatting Option. This definition is an option to enable the f_mkfs function that performs the formatting process. If this option is set to 1, the TFAT library gives the users access to the f_mkfs function. In the sample program, when the formatting process is started, the f_mkfs function is called by changing the value of this option to 1.

Note that the formatting process erases the data existing on the serial NOR flash memory. Before the process starts, confirm that no important data is contained in the memory. For more detailed information about the formatting process, refer to "7.1 About the Formatting Process".



Table 4.1 Formatting Option

Definition Name	Possible Value	Value Meaning	Default
FF_USE_MKFS	"1"	Enables the f_mkfs function.	"0"
	"0"	Disables the f_mkfs function.	

4.4.3 File Manipulation Processes

After the formatting process (f_mkfs) is executed, file manipulation processes are sequentially executed as shown in Figure 4.3 Flowchart of File Manipulation Processes.

In these file manipulation processes, the following operations are performed:

- 1. Register the work area in the FAT file system (f_mount)
- 2. Create a folder named "FLD" in the root directory (f_mkdir)
- 3. Create a file named "TEXT.TXT" in the "FLD" folder and open the file in write mode (f_open)
- 4. Write text data of 2,048 bytes to the "TEXT.TXT" file (f_write)
- 5. Close the "TEXT.TXT" file (f_close)
- 6. Reopen the "TEXT.TXT" file in read mode (f_open)
- 7. Move the file pointer to the start address of the "TEXT.TXT" file (f_lseek)
- 8. Read the data in the file in units of 512 bytes from the file beginning and check whether each unit of data is identical to the written data (f_read)
- 9. Repeat step 8 to check whether all 2,048 bytes are identical to the 2,048-byte data that was written in step 4
- 10. Close the "TEXT.TXT" file (f_close)

The data to be written to the file is defined in "r_data_file.c". By default, repetitions of the string "Renesas," are written. You can change the data to be written and the relevant macro FILESIZE corresponding to the data size in "r_data_file.h", if necessary.

4.5 Memory Usage

This section shows the ROM size, RAM size, and the maximum stack size used by the sample program of this application note. "Table 4.2 Confirmation Conditions" shows the conditions under which memory usage was confirmed. "1.4 Modules" shows the modules that were used for confirmation and their revision numbers. "Table 4.3 Memory Usage" shows the confirmation results.

Table 4.2 Confirmation Con	ditions
----------------------------	---------

Condition	Description
Integrated development environment	Renesas Electronics e ² studio 2023-10
C compiler	Renesas Electronics C/C++ Compiler for RX Family V3.06.00
Endianness	Little endian
Compilation option	The "-lang=c99" and "-optimize=0" options were added with the default settings specified in the integrated development environment.

Table 4.3Memory Usage

Item	Memory Usage
ROM	69195 byte
RAM	48570 byte
Stack	5276 byte



5. Board-Dependent Settings

5.1 Modifying the Settings

This section describes how to modify the sample program of this application note if you use the sample program for a board other than the target board (RX72N Envision Kit).

In the sample program, the sections that are dependent on the target board are the settings of pins that are used for connections between the Macronix serial NOR flash memory and the MCU mounted on the board. For details about the pins that are used for connection between the serial NOR flash memory and MCU on the target board, refer to "2.1 Hardware Configuration".

The settings that are dependent on the target board and need to be modified are as follows:

1. The pin settings of the quad serial peripheral interface (QSPI). Change the pin settings according to the board that you want to use. In Smart Configurator, open the [Pins] page, and then select [QSPI]. You can then access the relevant QSPI pin settings.

int : This button 🟙 will assign pin functio	on to	the default b	oard pins if a bo	oard is selected.	Dor	n't Show Again
Hardware Resource 🛛 🕀 🖃 🖓	♣	Pin Functio	on		2	1 🔣 📑 🕹
Type filter text		type filter	r text (* = any st	ring, ? = any character)	All	
V CAN2	^	Enabled	Function	Assignment	Pin Number	Direction
 Serial peripheral interface RSPI0 RSPI1 RSPI2 Magnetic description of the serial peripheral interface QSPI0 Serial source interface enhanced 			QIO0 QIO1 QIO2 QIO3 QMI QMO QSPCLK	 PD6/D6/MTIC5V/MTIOC8A/POE4#/SSLC2-A/REF50C PD7/D7/MTIC5U/POE0#/SSLC3-A/RMII1_RX_ER/QMI PD2/D2/MTIOC4D/TIC2/GTIOC0B/MISOC-A/CRX0/E⁺ PD3/D3/MTIOC8D/TOC2/POE8#/GTIOC0A/RSPCKC-, Not assigned Not assigned PD5/D5/MTIC5W/MTIOC8C/MTCLKA/POE10#/SSLC1 	 119 (B) 124 (B) 123 (B) Not assigned Not assigned 	IO IO IO None None O
 SSIE0 SSIE1 MMC host interface SD host interface Parallel data capture unit 	~	<	QSSL	Not assigned	Not assigned	None

2. The SS# pin settings of the clock synchronous control module for serial NOR flash memory access (r_flash_spi). Change the settings to the MCU pins (on the board that you want to use) to which the SS# pins of the serial NOR flash memory are connected. In Smart Configurator, open the [Components] page, and then select [r_flash_spi]. In the properties list, [Device 0 Port Number] and [Device 0 Bit Number] are the relevant settings.



oftware component configuration			🛐 📄 Generate Code 🛛 Generate Repo
Components 🔌 🛃 🎝 🕞 🕀 🛟 🔻	Configure		G
te 😳	Property	Value	^
type filter text	# Device 1 1M-bit (128K Bytes)	Not control target	
V 🔁 Startup	# Device 1 2M-bit (256K Bytes)	Not control target	
✓ → Generic	# Device 1 4M-bit (512K Bytes)	Not control target	
r bsp	# Device 1 16M-bit (2M Bytes)	Not control target	
✓ ➢ Drivers	# Device 1 32M-bit (4M Bytes)	Not control target	
✓ ▷ Memory	# Device 1 64M-bit (8M Bytes)	Not control target	
💱 r_flash_spi	# Device 1 128M-bit (16M Bytes)	Not control target	
✓	# Device 1 256M-bit (32M Bytes)	Not control target	
💣 r gspi ymstr rx	# Device 1 512M-bit (64M Bytes)	Not control target	
✓ ➢ Timers	# Device 1 1G-bit (128M Bytes)	Not control target	
💁 r_cmt_rx	# Device 0 Port Number	PORTD	
✓ ➢ Middleware	# Device 0 Bit Number	PIN4	
✓ 🧁 Memory	# Device 1 Port Number	PORTX	
💁 r_memdrv_rx	# Device 1 Bit Number	PINO	
✓ (⇒ Timers			*
💣 r_sys_time_rx			~
✓ (⇒ Storage			\sim

3. The control-target serial NOR Flash memory settings of the clock synchronous control module for serial NOR flash memory access (r_flash_spi). Set the serial NOR flash memory device that you use as the control target. In Smart Configurator, open the [Components] page, and then select [r_flash_spi]. In the properties list, find the model name and memory size of the Macronix serial NOR flash memory device that you use. Make sure that "Control target" is displayed for only the model name and memory size of the flash memory device that you use.

oftware component conf	iguration	Generate C	Code Generate Repo
components 🚵 🛃 🎘 🕒 🕀 🛱	Configure		C
ت ت	Property	Value	^
type filter text	# Device 1 Included	Disabled	
✓ → Startup	# Device 0 Macronix MX25L	Control target	
✓ ➢ Generic	Device 0 Macronix MX66L	Not control target	
💣 r_bsp	# Device 0 Macronix MX25R	Not control target	
✓ → Drivers	# Device 0 Adesto AT25QF	Not control target	
V 🔁 Memory	# Device 1 Macronix MX25L	Not control target	
r_flash_spi	# Device 1 Macronix MX66L	Not control target	
✓	Device 1 Macronix MX25R	Not control target	
💣 r_qspi_smstr_rx	Device 1 Adesto AT25QF	Not control target	
✓ ➢ Timers	# Device 0 512K-bit (64K Bytes)	Not control target	
😫 r_cmt_rx	# Device 0 1M-bit (128K Bytes)	Not control target	
✓ ➢ Middleware	# Device 0 2M-bit (256K Bytes)	Not control target	
V 🗁 Memory	# Device 0 4M-bit (512K Bytes)	Not control target	
😫 r memdry r	# Device 0 16M-bit (2M Bytes)	Not control target	
V 🗁 Timers	# Device 0 32M-bit (4M Bytes)	Control target	
💣 r sys time rx	# Device 0 64M-bit (8M Bytes)	Not control target	
✓ ➢ Storage	# Device 0 128M-bit (16M Bytes)	Not control target	
r_tfat_driver_rx	# Device 0 256M-bit (32M Bytes)	Not control target	
r tfat rx	# Device 0 512M-bit (64M Bytes)	Not control target	
	# Device 0 1G-bit (128M Bytes)	Not control target	~
	<		>
			^



5.2 Changes to the Initial Settings of Smart Configurator

This section shows the Smart Configurator settings that have been changed from their initial values for use with the sample program of this application note.

5.2.1 BSP Module

Table 5.1 shows the relevant settings of the BSP module and their values that are currently set. For details about the "User stack size" and "Heap size" settings, refer to "7.3 About the Stack and Heap Sizes".

 Table 5.1 Changes to the "User stack size" and "Heap size" Settings

Item	Current Value
User stack size	0x2000
Heap size	0x1000

	c		
omponents 🚵 🛃 🎘 🕞 🕀 🊔 🔻	Configure		(
10 To	Property	Value	~
type filter text	🗙 🏟 Configurations		
✓ 🧁 Startup 🔨	# User stack setting	2 stacks	
V 🤁 Generic	# User stack size	0x2000	
r bsp	# Interrupt stack size	0x2000	
✓	# Heap size	0x4000	
✓	Initializes C input and output library functions	Enable	
😫 r_flash_spi	# Enable user stdio charget function	Use BSP charget() function	
✓	# User stdio charget function name	my_sw_charget_function	
r_qspi_smstr_rx	# Enable user stdio charput function	Use BSP charput() function	
✓	# User stdio charput function name	my_sw_charput_function	
😫 r_cmt_rx	# Processor Mode	Stay in Supervisor mode	
✓	# ID code 1	0×FFFFFFF	
✓	# ID code 2	0xFFFFFFF	~
😫 r_memdrv_rx			~
🗸 🗁 Timers			
💣 r_sys_time_rx			
✓ ➢ Timers			

5.2.2 Memory Access Driver Interface Module

Table 5.2 shows the relevant settings of the memory access driver interface module and their currently set values. These settings pertain to the communication mode and speed.

Table 5.2 Changes to the Settings of the Memory Access Driver Interface Module

Item	Current Value
Device 0 driver	QSPI clock synchronous single master control FIT module
Device 0 transfer rate for command transmission.	3000000 (30 Mbps)
Device 0 Transfer rate for date transmission.	3000000 (30 Mbps)
Device 0 Transfer rate for data reception.	3000000 (30 Mbps)



Software component configur	ation	🔂 📄 Generate Code Generate Re	eport
Components $\ge \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ $	Configure		í
type filter text	Property V 🏟 Configurations	Value	^
✓ 🧁 Startup 🔨	# Use device 0	enabled	
🗸 🧁 Generic	# Use device 1	disabled	
💣 r_bsp	# Device 0 data transfer mode	CPU transfer (Software transfer)	
✓	Pevice 1 data transfer mode Pevice 0 driver	CPU transfer (Software transfer)	
V 🗁 Memory	Device 0 driver	QSPI clock synchronous single-master control FIT m	
🍄 r_flash_spi		RSPI clock synchronous control FIT module	
🗸 🗁 Communications	# Device 0 driver channel number	Channel 0	
💣 r_qspi_smstr_rx	# Device 1 driver channel number	Channel 0	
✓	# Device 0 type	NOR FLASH or EEPROM	
💁 r_cmt_rx	# Device 1 type	NOR FLASH or EEPROM	
✓ ➢ Middleware	# Device 0 transfer rate for command transmission.	3000000	
V > Memory	# Device 0 Transfer rate for data transmission.	3000000	
Pr memdry rx	# Device 0 Transfer rate for data reception.	3000000	
V > Timers	# Device 1 transfer rate for command transmission.	1000000	~
r sys time rx			~
✓ ➢ Storage			~
Overview Board Clocks System Compon	ents Pins Interrupts		

5.2.3 Clock Synchronous Control Module for Serial NOR Flash Memory Access

Table 5.3 shows the relevant settings of the clock synchronous control module for serial NOR flash memory access. For this module, the settings for selection of the control-target serial NOR flash memory device and the pin that is connected to the Chip Select pin of the target memory device have been changed.

Table 5.3 Changes to the Settings of the Clock Synchronous Control Module for Serial NOR Flash Memory Access Memory Access

Item	Current Value
Device 0 Macronix MX25L	Control target
Device 0 32M-bit (4M Bytes)	Contral target
Device 0 Port Number	PORTD
Device 0 Bit Number	PIN4



mponents 🚵 🛃 📮 🕀 🚔	▼ Configure			(
٠	Propert	y	Value	^
ype filter text	#	Device 0 Macronix MX25L	Control target	
🗸 🗁 Startup	A #	Device 0 Macronix MX66L	Not control target	
✓ → Generic	#	Device 0 Macronix MX25R	Not control target	
e cenenc	#	Device 0 Adesto AT25QF	Not control target	
Drivers	#	Device 1 Macronix MX25L	Not control target	
✓ → Memory	#	Device 1 Macronix MX66L	Not control target	
r_flash_spi	#	Device 1 Macronix MX25R	Not control target	
✓ ➢ Communications	#	Device 1 Adesto AT25QF	Not control target	
r_qspi_smstr_rx	#	Device 0 512K-bit (64K Bytes)	Not control target	
✓ ➢ Timers	#	Device 0 1M-bit (128K Bytes)	Not control target	
r_cmt_rx	#	Device 0 2M-bit (256K Bytes)	Not control target	
Middleware	#	Device 0 4M-bit (512K Bytes)	Not control target	
V 🗁 Memory	#	Device 0 16M-bit (2M Bytes)	Not control target	
r_memdrv_rx	#	Device 0 32M-bit (4M Bytes)	Control target	
✓ ➢ Timers	#	Device 0 64M-bit (8M Bytes)	Not control target	~
r sys time rx				~
✓ → Storage				~

oftware component config	🐻 📄		
omponents 🚵 🛃 🎝 🕀 🕀 井	▼ Configure	(i	
ن 😜 ا	Property	Value	^
type filter text	# Device 1 1M-bit (128K Bytes)	Not control target	
🗸 🗁 Startup	# Device 1 2M-bit (256K Bytes)	Not control target	
	# Device 1 4M-bit (512K Bytes)	Not control target	
er bsp	# Device 1 16M-bit (2M Bytes)	Not control target	
✓ → Drivers	# Device 1 32M-bit (4M Bytes)	Not control target	
✓ ▷ Memory	# Device 1 64M-bit (8M Bytes)	Not control target	
r_flash_spi	# Device 1 128M-bit (16M Bytes)	Not control target	
✓ → Communications	# Device 1 256M-bit (32M Bytes)	Not control target	
r_qspi_smstr_rx	# Device 1 512M-bit (64M Bytes)	Not control target	
 Timers 	# Device 1 1G-bit (128M Bytes)	Not control target	
r_cmt_rx	# Device 0 Port Number	PORTD	
✓ ➢ Middleware	# Device 0 Bit Number	PIN4	
✓ ➢ Memory	# Device 1 Port Number	PORTX	
💕 r_memdrv_rx	# Device 1 Bit Number	PINO	
✓ ▷→ Timers			~
r sys time rx			~
✓ → Storage	,		\sim



6. Migration to CS+

Only an e² studio project sample program is bundled with this application note. If you use the sample program with CS+, load the e² studio project by using the following procedure.





7. Notes

7.1 About the Formatting Process

Make sure that the memory device (such as serial NOR flash memory) to be used with the TFAT library is formatted as a FAT file system (in FAT12, FAT16, or FAT32 format). If the serial NOR flash memory to be used for executing the sample program of this application note is not formatted (or formatted otherwise), appropriately format it by referring to "4.4.2 Formatting Process".

If you execute the sample program with a serial NOR flash memory device that is not formatted as a FAT file system (in FAT12, FAT16, or FAT32 format), the f_mount API function does not run correctly. As a result, the program fails to mount a file system and the following message appears in Renesas Debug Virtual Console: Error (FR_NO_FILESYSTEM) Drive mount

7.2 Timer Function for Serial NOR Flash Memory

To use the TFAT library with serial NOR flash memory, the disk_1ms_interval callback function included in the TFAT memory driver FIT module must be registered as a periodic timer callback at an interval of 1 ms. In the sample program, to perform this processing, the R_CMT_CreatePeriodic API function of the CMT module is used as follows:

```
R_CMT_CreatePeriodic((uint32_t)(1000), disk_1ms_interval,
&gs cmt channel);
```

7.3 About the Stack and Heap Sizes

To use the TFAT library with serial NOR flash memory, the sector size must be changed to 4,096. Set "4096" for FF_MIX_SS and FF_MAX_SS in ffconf.h.

Note that this change increases the sizes of local and global variables used in the TFAT library and therefore may cause a stack overflow or heap overflow. Change the stack and heap sizes if necessary. For details about how to change the stack and heap sizes and the stack and heap sizes that are set in the sample program of this application note, refer to "5.2.1 BSP Module".



8. Reference Documents

User's Manual: Hardware RX Family: RX72N Group User's Manual: Hardware (R01UH0824)

User's Manual: Evaluation Board RX72N Envision Kit User's Manual (R20UT4788) RX72N Envision Kit - Schematics (R20UT4789)

User's Guide: Development Environment RX Smart Configurator User's Guide (R20AN0451) RX Family: CC-RX Compiler User's Manual (R20UT3248)

The latest versions can be downloaded from the Renesas Electronics website. (www.renesas.com)



Revision History

		Description	
Rev.	Date	Page	Summary
1.00	May.01.24	—	Initial release



General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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