RX Family
RSPI Sequence Control and Interrupt Generation Timing

Abstract
This document describes the sequence control for the serial peripheral interface (hereinafter referred to as RSPI) and interrupt timing for the RX Family MCUs.

Products
RX Family

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.
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1. Peripheral Functions

1.1 RSPI Master Mode and Sequence Control

For RSPI master mode, in accordance with the sequence length set in the SPSCR register, data can be sequentially
transmitted or received switching up to eight transfer formats by hardware.

Figure 1.1 shows the Configuration Diagram of the RSPI Operating in Master Mode.

Output to an external device is determined by the transfer format setting specified by the RSPI command (hereinafter referred to as command) and the data written to the transmit buffer. The frame consists of data and commands that relate to output to an external device.

Figure 1.2 shows the Basic Concept of a Frame.
### 1.2 Number of Transmit/Receive Frames Per Sequence and Interrupt Generation Timing

The number of transmit/receive frames in a sequence is determined by a combination of sequence length set with the SPSCR.SPSLN[2:0] bits and number of frames set with the SPDCR.SPFC[1:0] bits.

The number of commands in a sequence is determined by the sequence length, and the transmit/receive frame commands are set in registers SPCMD0 to SPCMD7.

The timing to generate a transmit buffer empty interrupt request and a receive buffer full interrupt request for each sequence is determined by the number of frames. When data transmission starts for the frame of the set number, a transmit buffer empty interrupt request is generated; when data reception starts, a receive buffer full interrupt request is generated.

Figure 1.3 shows the Number of Frames Per Sequence and Interrupt Generation Timing. Operation is not guaranteed if settings other than those shown in the figure are made to the SPSCR.SPSLN[2:0] bits and SPDCR.SPFC[1:0] bits.

<table>
<thead>
<tr>
<th>Sequence Length</th>
<th>Number of Frames</th>
<th>Interrupt Generated</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>SPTX0/SPRX0</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>SPCMD0</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>SPTX0/SPRX0</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>SPCMD0</td>
</tr>
<tr>
<td>16</td>
<td>16</td>
<td>SPTX0/SPRX0</td>
</tr>
</tbody>
</table>

Figure 1.3 Number of Frames Per Sequence and Interrupt Generation Timing
Figure 1.4 shows the frame creation operation when the SPSLN[2:0] bits are 011b (sequence length is 4) and the SPFC[1:0] bits are 11b (4 frames).

Figure 1.4   Example of Frame Creation Operation
2. Application Example

2.1 Sequence Control Application Example

This section describes an operation example when the SPSCR.SPSLN[2:0] bits are set to 010b (sequence length is 3) and the SPDCR.SPFC[1:0] bits are set to 010b (3 frames).

Figure 2.1 shows an example of connecting the MCU to an external device using the sequence control.

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**Figure 2.1 Connection Example**

1. Set commands for the first and third to registers SPCMD0 to SPCMD2.
   - Command for the first frame of data: SPCMD0 register ← 0400h (MSB first, SSL0 signal asserted)
   - Command for the second frame of data: SPCMD1 register ← 0410h (MSB first, SSL1 signal asserted)
   - Command for the third frame of data: SPCMD2 register ← 1420h (LSB first, SSL2 signal asserted)

2. Transmit and receive operations start when data for three frames are written to the SPDR register.

3. In accordance with the SPCMD0 register setting (low signal output from the SSL0 pin (asserted) and MSB first), transfer the first frame of data.

4. After the first frame of data has been transferred, transfer the second frame of data in accordance with the SPCMD1 register setting (low signal output from the SSL1 pin (asserted) and MSB first).

5. After the second frame of transmit data has been output, data in the SPTX2 register (transmit buffer for the third frame of data) is transferred to the shift register, and a transmit buffer empty interrupt request is generated.

6. After the second frame of data has been transferred, transfer the third frame of data in accordance with the SPCMD2 register setting (low signal output from the SSL2 pin (asserted) and LSB first).

7. After the third frame of receive data has been transferred to the SPRX2 register (receive buffer for the third frame of data), a reception complete interrupt request is generated.
Figure 2.2 shows an Operation Example of the Sequence Control.

Figure 2.2  Operation Example of the Sequence Control
3. Reference Documents

User's Manual: Hardware
- RX630 Group User's Manual: Hardware Rev.1.60 (R01UH0040EJ)
- RX63N Group, RX631 Group User's Manual: Hardware Rev.1.80 (R01UH0041EJ)

When using products other than the RX630, RX63N, and RX631 Groups, refer to the User's Manual: Hardware for the product used.

The latest versions can be downloaded from the Renesas Electronics website.

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### Revision History

<table>
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<th>Date</th>
<th>Page</th>
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<tr>
<td>1.00</td>
<td>Aug. 1, 2012</td>
<td>1</td>
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<tr>
<td>1.01</td>
<td>July 1, 2014</td>
<td>1</td>
<td>Changed the target products to the RX family from RX630, RX63N, and RX631 Groups.</td>
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</tbody>
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   The state of the product is undefined at the moment when power is supplied.
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