RX Family

RSPI Sequence Control and Interrupt Generation Timing

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Abstract

This document describes the sequence control for the serial peripheral interface (hereinafter referred to as RSPI) and interrupt timing for the RX Family MCUs.

Products

RX Family

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Peripheral Functions

1.1 RSPI Master Mode and Sequence Control

For RSPI master mode, in accordance with the sequence length set in the SPSCR register, data can be sequentially transmitted or received switching up to eight transfer formats by hardware.

Figure 1.1 shows the Configuration Diagram of the RSPI Operating in Master Mode.

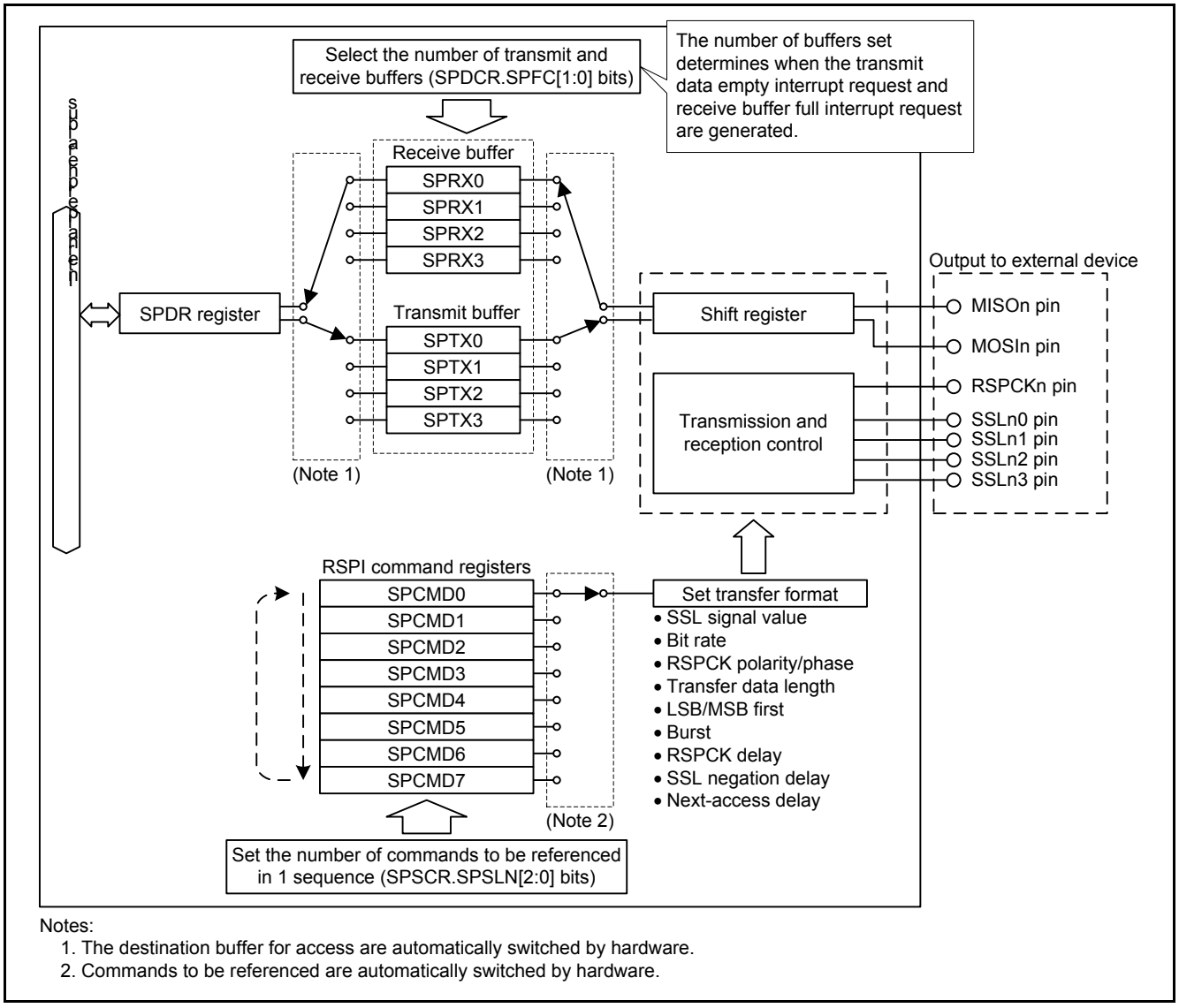

Figure 1.1 Configuration Diagram of the RSPI Operating in Master Mode

Output to an external device is determined by the transfer format setting specified by the RSPI command (hereinafter referred to as command) and the data written to the transmit buffer. The frame consists of data and commands that relate to output to an external device.

Figure 1.2 shows the Basic Concept of a Frame.

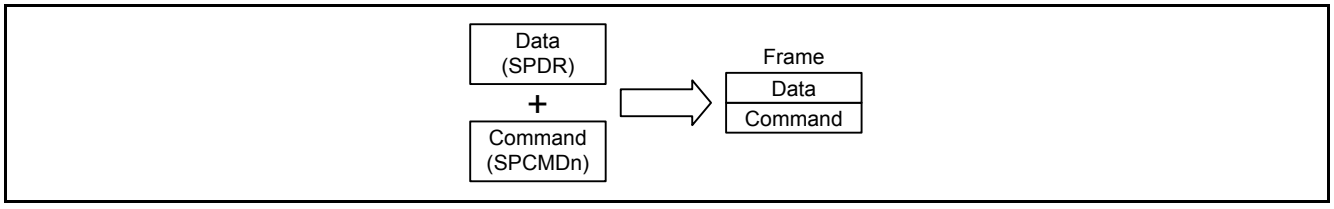

Figure 1.2 Basic Concept of a Frame

1.2 Number of Transmit/Receive Frames Per Sequence and Interrupt Generation Timing

The number of transmit/receive frames in a sequence is determined by a combination of sequence length set with the SPSCR.SPSLN[2:0] bits and number of frames set with the SPDCR.SPFC[1:0] bits.

The number of commands in a sequence is determined by the sequence length, and the transmit/receive frame commands are set in registers SPCMD0 to SPCMD7.

The timing to generate a transmit buffer empty interrupt request and a receive buffer full interrupt request for each sequence is determined by the number of frames. When data transmission starts for the frame of the set number, a transmit buffer empty interrupt request is generated; when data reception starts, a receive buffer full interrupt request is generated.

Figure 1.3 shows the Number of Frames Per Sequence and Interrupt Generation Timing. Operation is not guaranteed if settings other than those shown in the figure are made to the SPSCR.SPSLN[2:0] bits and SPDCR.SPFC[1:0] bits.

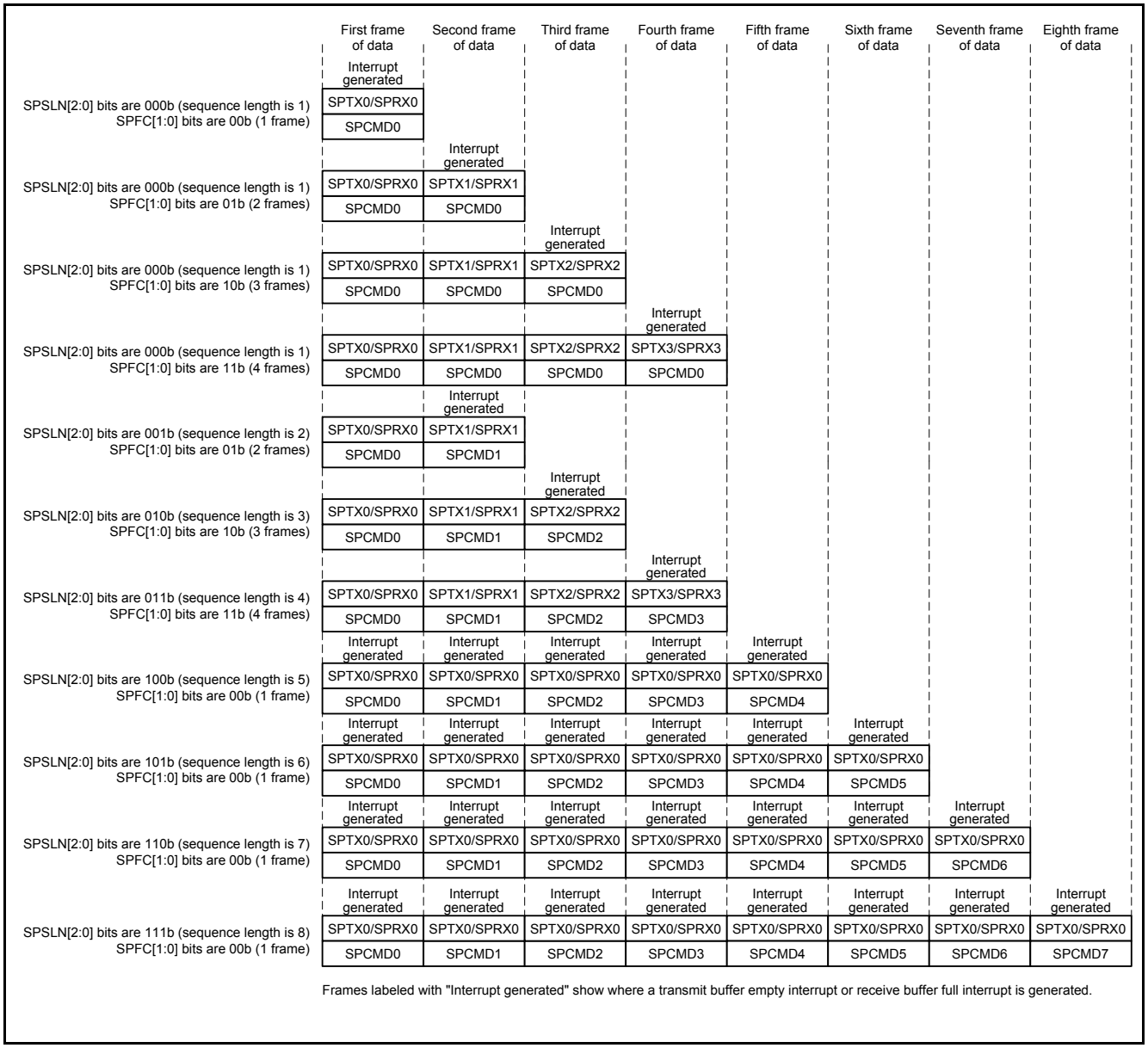

Figure 1.3 Number of Frames Per Sequence and Interrupt Generation Timing

Figure 1.4 shows the frame creation operation when the SPSLN[2:0] bits are 011b (sequence length is 4) and the SPFC[1:0] bits are 11b (4 frames).

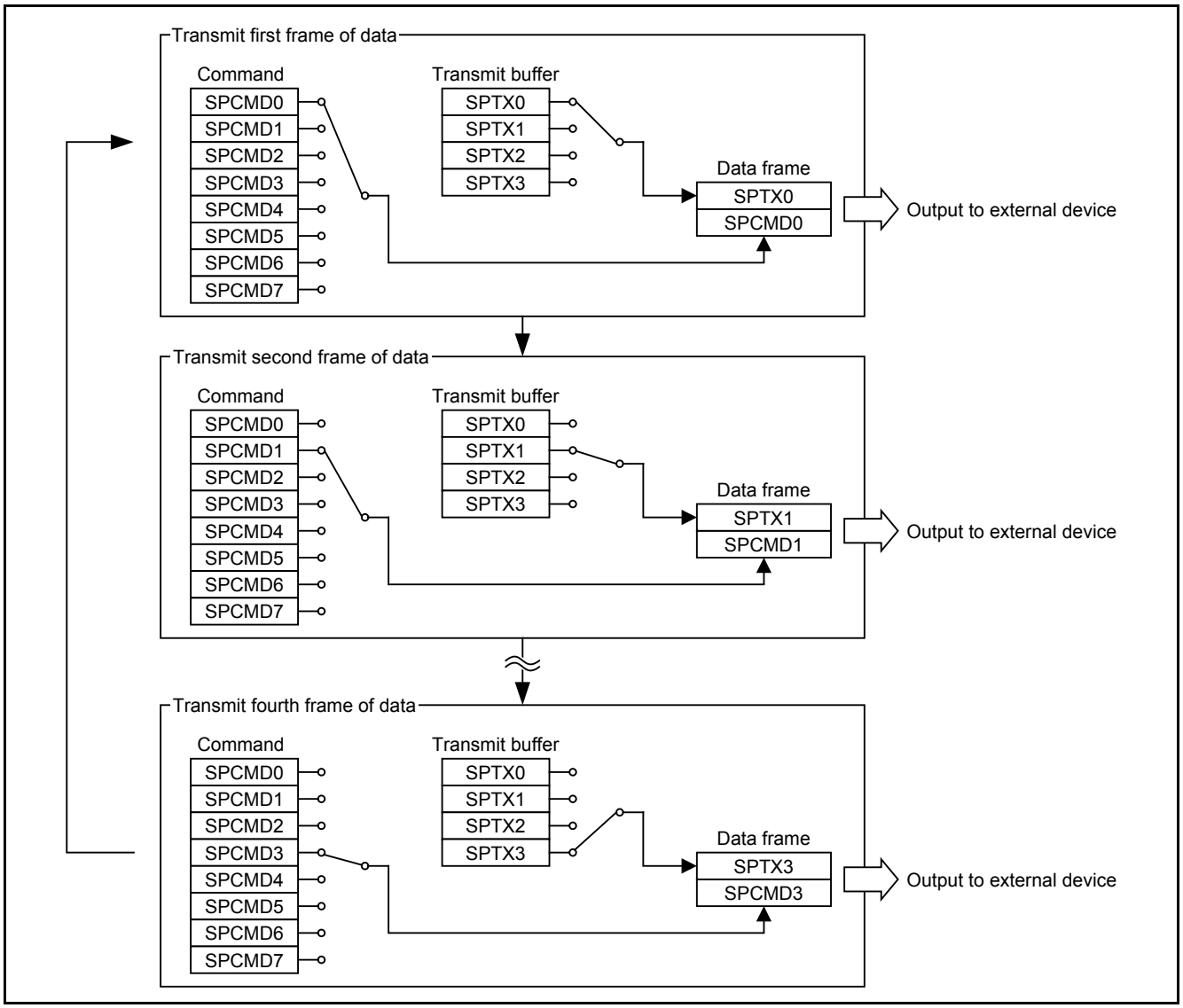

Figure 1.4 Example of Frame Creation Operation

2. Application Example

2.1 Sequence Control Application Example

This section describes an operation example when the SPSCR.SPSLN[2:0] bits are set to 010b (sequence length is 3) and the SPDCR.SPFC[1:0] bits are set to 010b (3 frames).

Figure 2.1 shows an example of connecting the MCU to an external device using the sequence control.

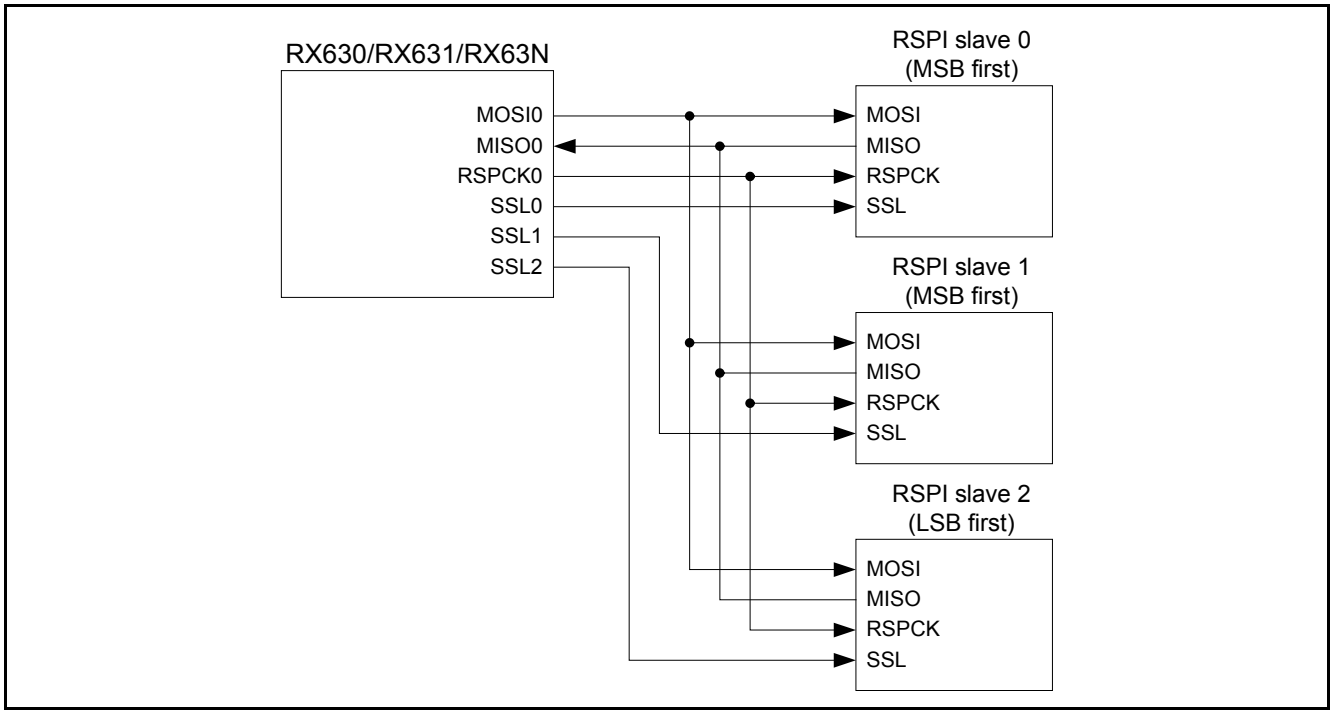

Figure 2.1 Connection Example

(1) Set commands for the first and third to registers SPCMD0 to SPCMD2.
Command for the first frame of data: SPCMD0 register ← 0400h (MSB first, SSL0 signal asserted)
Command for the second frame of data: SPCMD1 register ← 0410h (MSB first, SSL1 signal asserted)
Command for the third frame of data: SPCMD2 register ← 1420h (LSB first, SSL2 signal asserted)

(2) Transmit and receive operations start when data for three frames are written to the SPDR register.

(3) In accordance with the SPCMD0 register setting (low signal output from the SSL0 pin (asserted) and MSB first), transfer the first frame of data.

(4) After the first frame of data has been transferred, transfer the second frame of data in accordance with the SPCMD1 register setting (low signal output from the SSL1 pin (asserted) and MSB first).

(5) After the second frame of transmit data has been output, data in the SPTX2 register (transmit buffer for the third frame of data) is transferred to the shift register, and a transmit buffer empty interrupt request is generated.

(6) After the second frame of data has been transferred, transfer the third frame of data in accordance with the SPCMD2 register setting (low signal output from the SSL2 pin (asserted) and LSB first).

(7) After the third frame of receive data has been transferred to the SPRX2 register (receive buffer for the third frame of data), a reception complete interrupt request is generated.

Figure 2.2 shows an Operation Example of the Sequence Control.

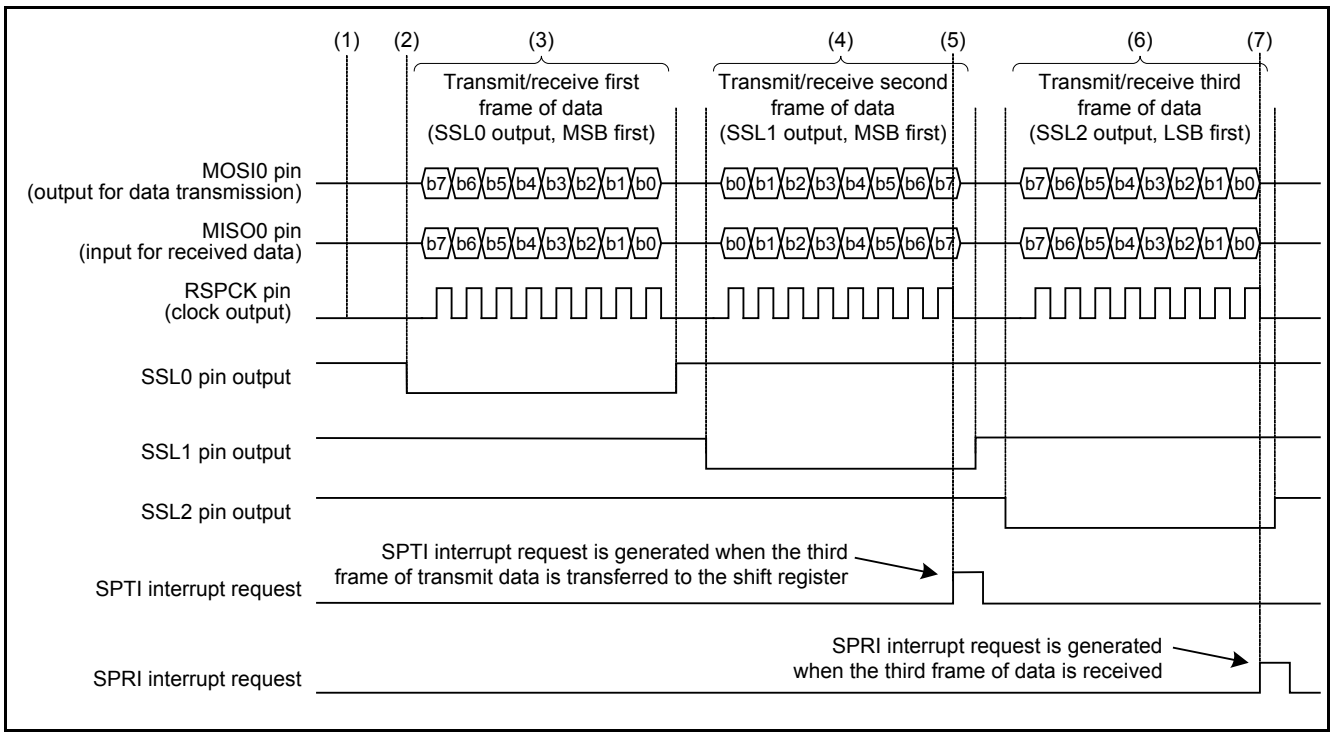

Figure 2.2 Operation Example of the Sequence Control

3. Reference Documents

User's Manual: Hardware

RX630 Group User's Manual: Hardware Rev.1.60 (R01UH0040EJ)

RX63N Group, RX631Group User's Manual: Hardware Rev.1.80 (R01UH0041EJ)

When using products other than the RX630, RX63N, and RX631 Groups, refer to the User's Manual:Hardware for the product used.

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

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Revision History	RX Family Application Note RSPI Sequence Control and Interrupt Generation Timing

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 1, 2012	—	First edition issued
1.01	July 1, 2014	1	Changed the target products to the RX family from RX630, RX63N, and RX631 Groups.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141