RX Family

Margin of Error for the Bit Rate in Asynchronous Communications

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Abstract

This document describes the procedure to calculate the allowable margin of error for the bit rate in asynchronous communications for the RX Family.

Products

RX Family

This document uses the RX210 Group to explain the margin of error for the bit rate. When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Peripheral Functions

1.1 Data Format

This section describes the data format in asynchronous communications mode. Table 1.1 lists the Transmit/Receive Data and Their Functions.

Table 1.1 Transmit/Receive Data and Their Functions

Name	Function	Remarks
ST (start bit)	1-bit low signal added before the character bits. Indicates the start of data transmission.	1-bit fixed
DATA (character bits)	Data signal in character units (7 bits or 8 bits)	Selectable from 7 bits or 8 bits
P (parity bit)	Signal added after the character bit to detect errors of communication data. The signal level changes so that the total number of 1s in this bit and the character bit can become odd or even depending on whether odd parity or even parity is selected.	Selectable from odd, even, or none
SP (stop bit)	1-bit or 2-bit high signal added after the character bits (or parity bit when parity is enabled) Indicates the end of data transmission. *1	Selectable from 1 bit or 2 bits

Note 1. In reception, only the first stop bit is checked regardless of the settings for the stop bit length. When the second stop bit is low, it is regarded as the start bit of the next transmit frame.

1.2 Receive Data Sampling Timing

In asynchronous mode, the SCI operates on an internal base clock (fBASE) with a frequency of 16 times[*1] the bit rate.

In reception, the low level of the RXDn pin for the start condition is detected by the falling edge of fBASE, and internal synchronization is started.

After synchronization, the start bit is sampled at the rising edge of the eighth cycle of fBASE. The time from input of the falling edge of the start bit to sampling of the start bit varies depending on the timing to input receive data. After receiving the start bit, data is sampled every 16 cycles of fBASE.

Note 1. This is an example when the SEMR.ABCS bit is 0. When the ABCS bit is 1, a frequency of eight times the bit rate is used as fBASE, and receive data is sampled at the rising edge of the fourth cycle of fBASE.

Figure 1.1 shows the Receive Data Sampling Timing in Asynchronous Mode When the SEMR.ABCS Bit is 0 for the following cases:

Case 1: Falling edge of the receive data is input near the rising edge of fBASE.
Case 2: Falling edge of the receive data is input immediately before the falling edge of fBASE.
Case 3: Falling edge of the receive data is input immediately after the falling edge of fBASE.

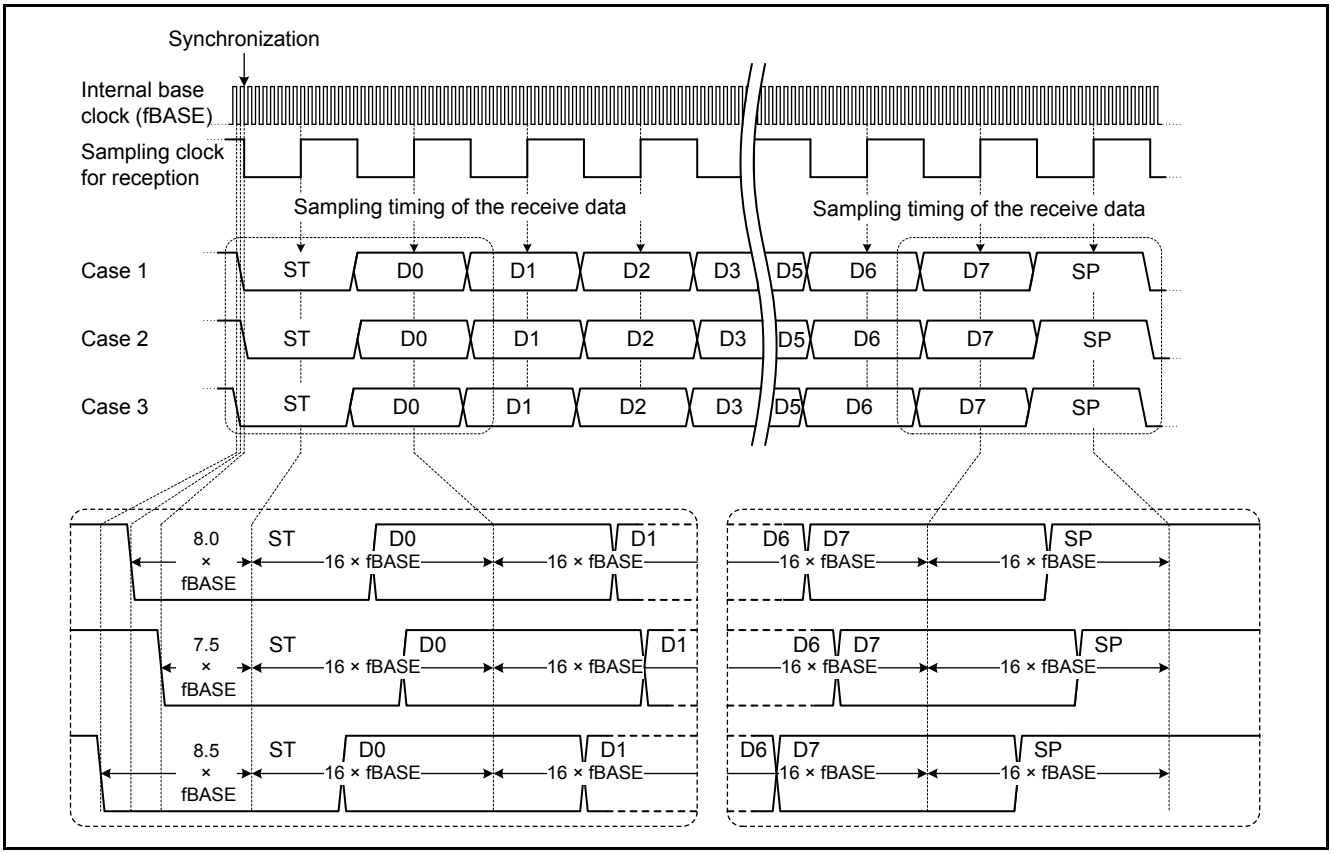

Figure 1.1 Receive Data Sampling Timing in Asynchronous Mode When the SEMR.ABCS Bit is 0

The time from input of the falling edge of the start bit to receiving the stop bit (tSTSP) in each case is as follows:

Case 1

$$tSTSP = \frac{8}{fBASE} + \frac{16}{fBASE} \times (b - 1)$$
$$= \frac{8}{fBASE} + \frac{1}{Br} \times (b - 1)$$

Case 2

$$tSTSP = \frac{7.5}{fBASE} + \frac{16}{fBASE} \times (b - 1)$$
$$= \frac{7.5}{fBASE} + \frac{1}{Br} \times (b - 1)$$

Case 3

$$tSTSP = \frac{8.5}{fBASE} + \frac{16}{fBASE} \times (b - 1)$$
$$= \frac{8.5}{fBASE} + \frac{1}{Br} \times (b - 1)$$

Br: Bit rate for reception
b: Total number of bits in one frame data (-1 when 2 bits are selected for SP)

As described above, tSTSP in case 2 is the shortest, and tSTSP in case 3 is the longest.

Note 1. When the SEMR.ABCS bit is 1, tSTSP is calculated by the following formulas:

Case 1

$$tSTSP = \frac{4}{fBASE} + \frac{1}{Br} \times (b - 1)$$

Case 2

$$tSTSP = \frac{3.5}{fBASE} + \frac{1}{Br} \times (b - 1)$$

Case 3

$$tSTSP = \frac{4.5}{fBASE} + \frac{1}{Br} \times (b - 1)$$

1.3 Relation Between the Receive Data Sampling Timing and Receive Data

In reception, the receive data that is input to the RXDn pin is received at the rising edge of the receive sampling clock in the RX. To receive data correctly, it is necessary to input the stop bit at the rising edge of the last sampling clock in a frame.

Figure 1.2 lists the Relation Between the Receive Sampling Clock and Receive Data.

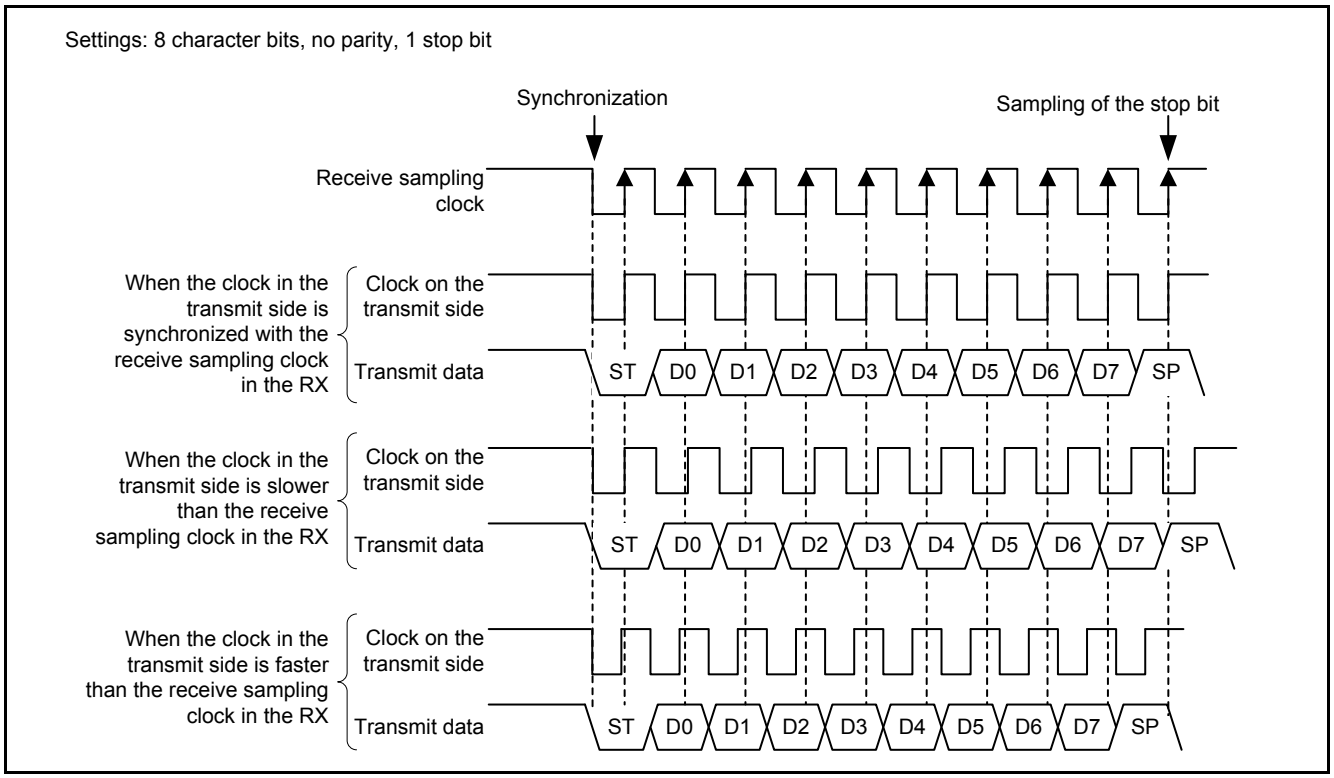

Figure 1.2 Relation Between the Receive Sampling Clock and Receive Data

Even if the clock on the transmit side is slower than the receive sampling clock in the RX, data can be received correctly when the stop bit on the transmit side is output (the falling edge of the last clock on the transmit side occurs) before the sampling of the stop bit in the RX.

If the clock on the transmit side is faster than the receive sampling clock in the RX, data can be received correctly when the start bit of the next data is output (0.5 clocks elapse after the rising edge of the last clock on the transmit side) after the sampling of the stop bit in the RX.

1.4 Calculating the Margin of Error for the Bit Rate

To transmit and receive data correctly, the bit rates for reception and transmission need to satisfy the formula below. Since the calculated value is the theoretical value, set an adequate margin. In addition, careful evaluation in the user application is recommended.

When the clock on the transmit side is slower than the receive sampling clock in the RX

Figure 1.3 lists the Relation Between the Clock on the Transmit Side and Receive Sampling Clock.

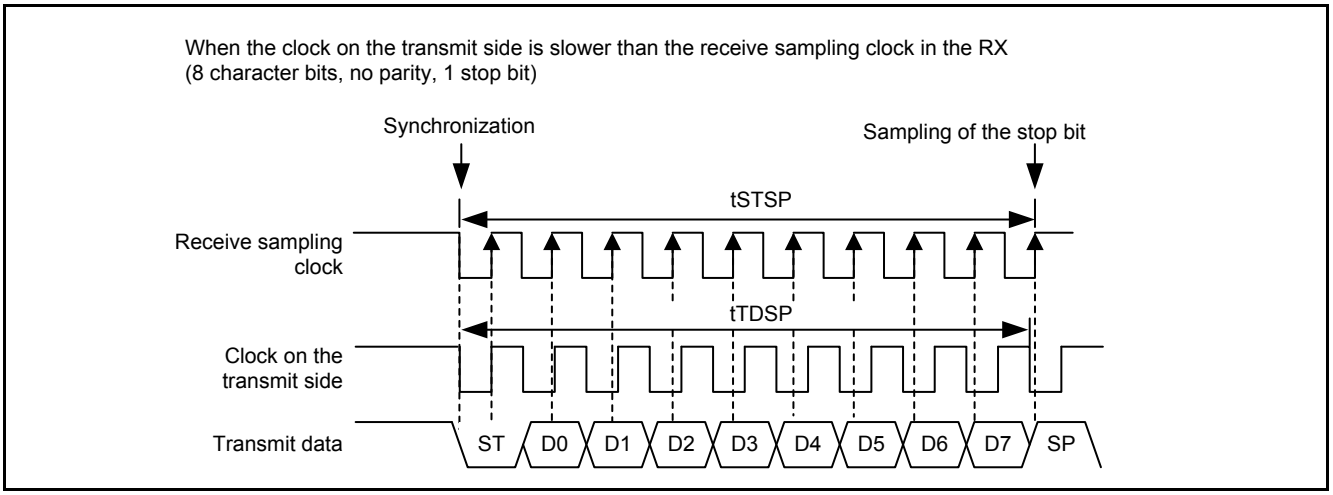

Figure 1.3 Relation Between the Clock on the Transmit Side and Receive Sampling Clock

When tTDSP represents the time from the start of outputting the start bit to the falling edge of the last clock for transmission, the falling edge of the last clock on the transmit side needs to occur before tSTSP elapses (tSTSP > tTDSP).

Since tTDSP is the time from the timing of outputting the start bit to the timing of outputting the start bit, it is calculated by the following formula:

$$tTDSP = \frac{1}{Bt} \times (b - 1)$$

When the SEMR.ABCS bit is 0, the minimum value for tSTSP is calculated by the following formula:

$$tSTSP = \frac{7.5}{fBASE} + \frac{1}{Br} \times (b - 1)$$

Accordingly, data can be transmitted and received correctly when the following formula is satisfied:

$$\frac{7.5}{fBASE} + \frac{1}{Br} \times (b - 1) > \frac{1}{Bt} \times (b - 1)$$

Bt: Bit rate for transmission [bps]
Br: Bit rate for reception [bps]
b: Total number of bits in one frame of data (-1 when 2 bits are selected for SP)

When the clock on the transmit side is faster than the receive sampling clock in the RX

Figure 1.4 lists the Relation Between the Clock on the Transmit Side and Receive Sampling Clock.

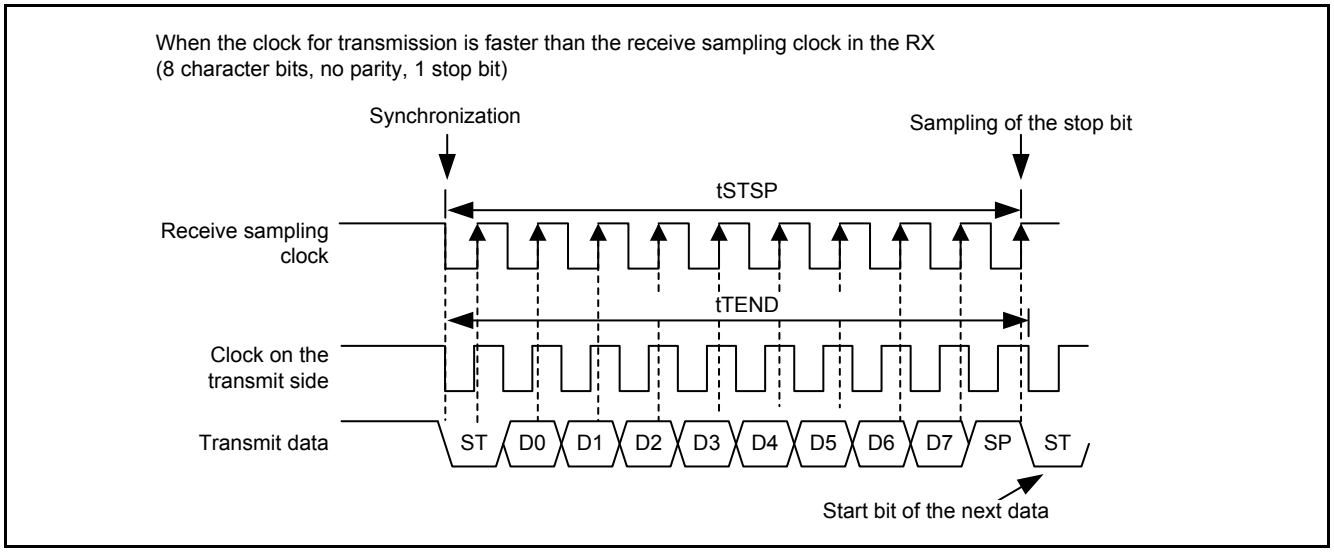

Figure 1.4 Relation Between the Clock on the Transmit Side and Receive Sampling Clock

When tTEND represents the time from the start of outputting the start bit to the completion of outputting the last data for transmission, the sampling timing of the stop bit needs to occur before the completion of the outputting last data (tSTSP > tTEND).

Since tTEND is the time from the start of outputting the start bit to the completion of outputting the start bit (outputting the start bit of the next data), it is calculated by the following formula:

$$tTEND = \frac{1}{Bt} \times b$$

When the SEMR.ABCS bit is 0, the minimum value for tSTSP is calculated by the following formula:

$$tSTSP = \frac{8.5}{fBASE} + \frac{1}{Br} \times (b - 1)$$

Accordingly, data can be transmitted and received correctly when the following formula is satisfied:

$$\frac{8.5}{fBASE} + \frac{1}{Br} \times (b - 1) < \frac{1}{Bt} \times b$$

Bt: Bit rate for transmission [bps]
Br: Bit rate for reception [bps]
b: Total number of bits in one frame of data (-1 when 2 bits are selected for SP)

Note: Even when the above formula is satisfied, data may not be received correctly due to delay in sampling of the start bit for the next data when data is continuously transmitted from the transmit side. To avoid this problem, select 2 as the stop bit length for transmission.

1.5 Example of Calculating the Transmit Bit Rate for Communication

This section describes an example of calculating the bit rate on the transmit side for communication when one frame of data is composed of the start bit, 8 character bits, and the stop bit, and the bit rate of the clock on the receive side is 9600 bps.

Conditions of the RX

PCLK: 25,000,000 Hz

SEMR.ABCS bit: 0 (16 base clock cycles for 1-bit period)

BRR register: 80

Bit rate: Approximately 9645.1 bps

Allowable margin on the transmit side

- Calculation for the lower limit of the transmit side

$$\frac{7.5}{fBASE} + \frac{1}{Br} \times (b - 1) > \frac{1}{Bt} \times (b - 1)$$

$fBASE = \text{bit rate} \times 16$

Accordingly,

$$\frac{7.5}{Br \times 16} + \frac{1 \times 16}{Br \times 16} \times (b - 1) > \frac{1}{Bt} \times (b - 1)$$

$$\frac{7.5 + 16\,(b - 1)}{Br \times 16} > \frac{1}{Bt} \times (b - 1)$$

$$Bt > \frac{(b - 1) \times Br \times 16}{7.5 + 16\,(b - 1)}$$

b = Start bit (1) + character length (8) + stop bit length (1) = 10

Accordingly,

$$Bt > \frac{(10 - 1) \times 9645.1 \times 16}{7.5 + 16\,(10 - 1)}$$

$$Bt > 9167.6 \text{ bps}$$

- Calculation for the upper limit on the transmit side (similar to the calculation for the lower limit)

$$\frac{8.5}{fBASE} + \frac{1}{Br} \times (b - 1) < \frac{1}{Bt} \times b$$

$$\frac{8.5 + 16\,(b - 1)}{Br \times 16} < \frac{1}{Bt} \times b$$

$$Bt < \frac{b \times Br \times 16}{8.5 + 16 \times (b - 1)}$$

$$Bt < 10119.4 \text{ bps}$$

According to the above formulas, data can be received correctly when the bit rate (Br) on the transmit side is between 9178 bps and 10119 bps (9178 bps < Br < 10119 bps).

Note that this value is the theoretical value, so set the adequate margin.

2. Appendix

Table 2.1 lists an example for RX Settings and the Corresponding Allowable Margin on the Transmit Side.

Table 2.1 RX Settings and the Corresponding Allowable Margin on the Transmit Side

RX Settings *1					Communication Format *2		Allowable Margin on the Transmit Side	
PCLK [MHz]	n	N	ABCS	Bit rate [bps]	Character	Parity	Lower limit [bps]	Upper limit [bps]
8	0	25	0	9615.4	8 bits	Not added	9140	10088
8	0	25	0	9615.4	8 bits	Added	9185	10043
8	0	25	0	9615.4	7 bits	Not added	9084	10143
8	0	25	0	9615.4	7 bits	Added	9140	10088
8	0	12	0	19230.8	8 bits	Not added	18279	20176
8	0	12	0	19230.8	8 bits	Added	18370	20086
8	0	12	1	38461.5	8 bits	Not added	37549	41440
8	0	12	1	38461.5	8 bits	Added	37639	41150
12	0	38	0	9615.4	8 bits	Not added	9140	10088
12	0	38	0	9615.4	8 bits	Added	9185	10043
12	0	19	0	18750.0	8 bits	Not added	17822	19672
12	0	19	0	18750.0	8 bits	Added	17911	19584
12	0	9	0	37500.0	8 bits	Not added	35644	39344
12	0	9	0	37500.0	8 bits	Added	35821	39169
20	0	64	0	9615.4	8 bits	Not added	9140	10088
20	0	64	0	9615.4	8 bits	Added	9185	10043
20	0	32	0	18939.4	8 bits	Not added	18002	19870
20	0	32	0	18939.4	8 bits	Added	18092	19782
20	0	15	0	39062.5	8 bits	Not added	37129	40983
20	0	15	0	39062.5	8 bits	Added	37314	40801
25	0	80	0	9645.1	8 bits	Not added	9168	10119
25	0	80	0	9645.1	8 bits	Added	9214	10074
25	0	40	0	19054.9	8 bits	Not added	18112	19992
25	0	40	0	19054.9	8 bits	Added	18202	19903
25	0	19	0	39062.5	8 bits	Not added	37129	40983
25	0	19	0	39062.5	8 bits	Added	37314	40801
30	0	97	0	9566.3	8 bits	Not added	9093	10036
30	0	97	0	9566.3	8 bits	Added	9138	9992
30	0	48	0	19132.7	8 bits	Not added	18186	20073
30	0	48	0	19132.7	8 bits	Added	18276	19984
30	0	23	0	39062.5	8 bits	Not added	37129	40983
30	0	23	0	39062.5	8 bits	Added	37314	40801

Note 1. N represents the BRR register value (0 ≤ N ≤ 255)
n varies depending on the SMR.CKS[1:0] bit value as follows:
When the SMR.CKS[1:0] bits are 00b, n is 0
When the SMR.CKS[1:0] bits are 01b, n is 1
When the SMR.CKS[1:0] bits are 10b, n is 2
When the SMR.CKS[1:0] bits are 11b, n is 3

Note 2. Regardless of the settings, the stop bit is fixed to 1 bit during a receive operation. The start bit is also fixed to 1 bit.

3. Reference Documents

User's Manual: Hardware

RX210 Group User's Manual: Hardware Rev.1.50 (R01UH0037EJ)
When using a product other than the RX210 Group, refer to the corresponding User's Manual: Hardware.
The latest version can be downloaded from the Renesas Electronics website.

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   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

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   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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