RX Family and M16C Family

Guide for Migration from the M16C to the RX: Asynchronous Serial Communications (UART)

Abstract

This document describes migration from the serial I/O UART mode in the M16C Family to the SCI asynchronous mode in the RX Family.

Products

RX Family

M16C Family

When this document explains migration from the M16C Family to the RX Family, the M16C/65C Group MCU is used as an example of the M16C Family MCU, and the RX231 Group and RX660 Group MCUs are used as examples of the RX Family MCU. When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Differences in Terminology Between the RX Family and M16C Family MCUs

Item	M16C Family	RX Family
Abbreviated name of the serial communication interface (SCI)	Serial I/O	SCI
Asynchronous serial communications mode	UART mode (Clock asynchronous serial I/O mode)	Asynchronous mode
SCI operating clock (clock source)	Count source	Clock source
Peripheral function operating clock	Peripheral function clocks: f1, fOCO40M, fOCO-F, fOCO-S, fC32	Peripheral module clocks: PCLKA, PCLKB, PCLKD
Transmit buffer	UiTB register (transmit buffer)	TDR registers: TDRH, TDRL, TDRHL
Transmit shift register	UART transmit shift register	TSR register
Receive buffer	UiRB register	RDR registers: RDRH, RDRL, RDRHL
Transmit interrupt	UARTi transmit interrupt (transmit buffer empty)	TXI interrupt
Transmit complete interrupt (M16C) Transmit end interrupt (RX)	UARTi transmit interrupt (transmission completed)	TEI interrupt
Receive interrupt	UARTi receive interrupt	RXI interrupt
Function to select I/O of peripheral functions for pins	Function select registers and input function select registers *2	MPC *1

Notes: 1. The MPC is not available in some groups.
2. Only available in the M32C Series and R32C Series.

Contents

1. General Differences in Asynchronous Serial Communications

Table 1.1 shows Differences in Asynchronous Serial Communications.

Table 1.1 Differences in Asynchronous Serial Communications

Item	M16C (M16C/65C)	RX (RX231)	RX (RX660)
Operation clock source	f1, fOCO40M, fOCO-F, fOCO-S, or fC32	PCLKB	PCLKB
Data length	7 bits, 8 bits or 9bits	7 bits, 8 bits or 9bits	7 bits, 8 bits or 9bits
Parity bit	Selectable from even, odd, or no parity	Selectable from even, odd, or no parity	Selectable from even, odd, or no parity
Stop bits	Selectable from 1 bit or 2 bits	Selectable from 1 bit or 2 bits	Selectable from 1 bit or 2 bits
Data format	Selectable from LSB first or MSB first	Selectable from LSB first or MSB first	Selectable from LSB first or MSB first
Hardware flow control	Available (selectable)	Available (selectable)	Available (selectable)
Separate CTS/RTS pins	Available (UART0)	Not available	Not available
Data match detection	Not available	Not available	Available
Start bit detection	Falling edge	Low level or falling edge can be selected.	Low level or falling edge can be selected.
Receive data sampling timing adjustment	Not available	Not available	Available
Transmit signal change timing adjustment	Not available	Not available	Available
Interrupt sources	Transmit interrupt Receive interrupt	Transmit data empty (TXI) interrupt Transmit end (TEI) interrupt Receive data full (RXI) interrupt Receive error (TRI) interrupt	Transmit data empty (TXI) interrupt Transmit end (TEI) interrupt Receive data full (RXI) interrupt Receive error (TRI) interrupt
Error detection	Overrun error Framing error Parity error	Overrun error Framing error Parity error	Overrun error Framing error Parity error
Double-speed mode	Not available	Available	Available
Multi-processor function	Not available	Available	Available
Noise cancellation	Not available	On-chip digital noise filter on the RXDn pin input route	On-chip digital noise filter on the RXDn pin input route
Data logic switch	Available	Available	Available
TXD, RXD I/O polarity switch	Available	Not available	Not available

2. Peripheral Functions Used

Table 2.1 shows Peripheral Functions and Modes Used When Performing Asynchronous Communications.

Table 2.1 Peripheral Functions and Modes Used When Performing Asynchronous Communications

No.	Operating Example	M16C		RX	
		Peripheral Function	Mode	Peripheral Function	Mode
1	Asynchronous serial communications (transmit/receive operations)	Serial I/O	UART mode	SCI	Asynchronous mode

3. Differences in Asynchronous Serial Communications

This section explains the functional differences in asynchronous serial communications between the RX and M16C under the example conditions shown in Table 3.1 Conditions for Asynchronous Serial Communications.

Table 3.1 Conditions for Asynchronous Serial Communications

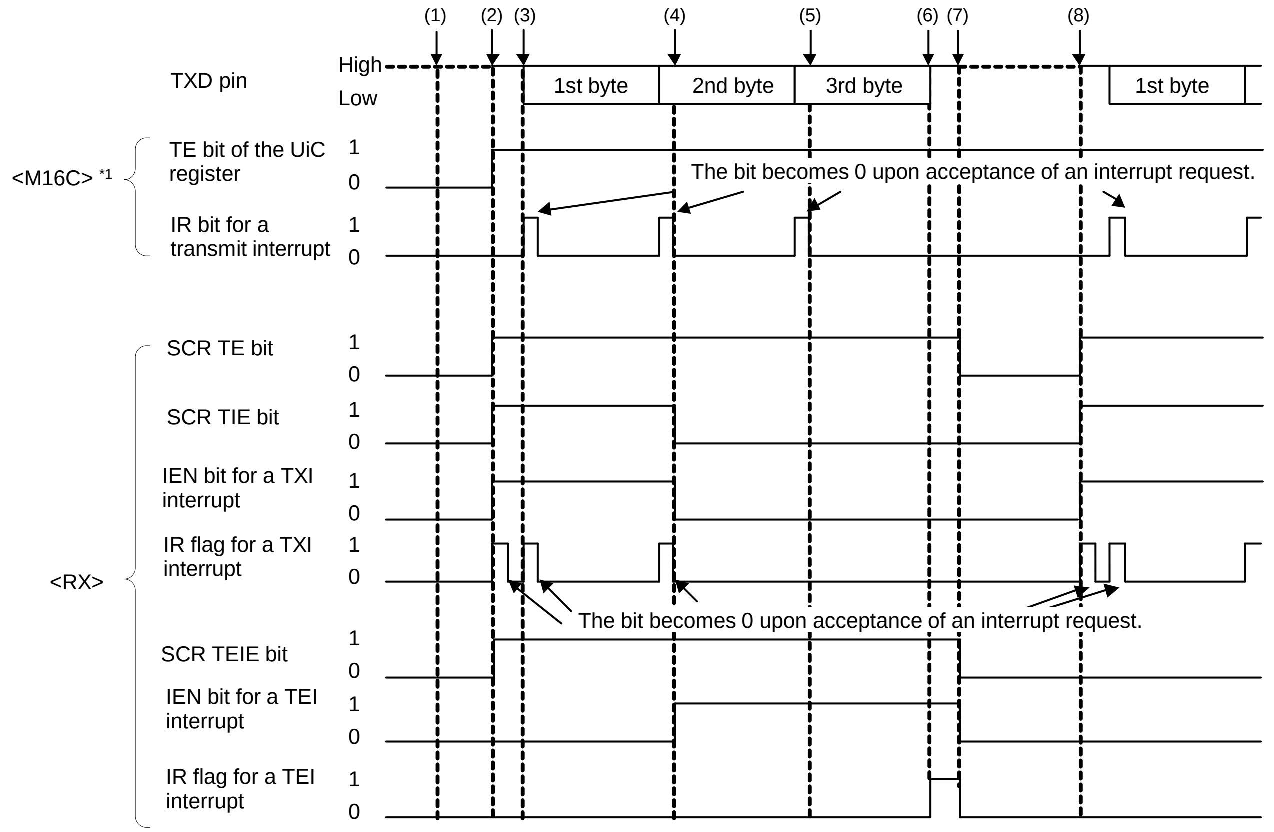
Item	Conditions for Transmission and Reception
Peripheral function operating clock	16 MHz
Transfer rate	9600 bps
Data length	8 bits
Stop bits	1 stop bit
Parity	None
Data format	LSB first
Hardware flow control	None
Channels used	RX Family: SCI0 M16C Family: UART0
Pin processing	Pull-up resistors are connected to the TXD and RXD pins. *1

Note: 1. In the RX Family, when the SCR.TE bit is 0 (serial transmission is disabled), the TXD pin is in the Hi-Z state. When a pull-up resistor is not connected, while serial transmission is disabled, switch the pin function to the output state of general I/O ports.

3.1 Transmit/Receive Timing

3.1.1 Differences in Transmitting

Figure 3.1 shows Differences in Timing Between the RX and the M16C
(When Transmitting 3 Bytes). Table 3.2 shows Differences in Operation and Processing at Various Timings Between the RX and the M16C (When Transmitting 3 Bytes).



Note 1. For the M16C, only either the time at which the transmit buffer becomes empty or the time at which transmission ends can be used as a trigger to generate a transmit interrupt.
The above timing chart is an example of operation when the time at which the transmit buffer becomes empty is selected as a trigger.

Figure 3.1 Differences in Timing Between the RX and the M16C (When Transmitting 3 Bytes)

Table 3.2 Differences in Operation and Processing at Various Timings Between the RX and the M16C (When Transmitting 3 Bytes)

<table>
<tr><th>Timing</th><th>M16C (M16C/65C)</th><th>RX (RX231/RX660)</th></tr>
<tr><td>(1) Before transmission starts</td><td>The pin status is determined when serial I/O mode is selected.</td><td>The TXD pin is in the Hi-Z until the SCR.TE bit is set to 1 (serial transmission is enabled).</td></tr>
<tr><td>(2) When transmission starts</td><td>The TE bit is set to 1 (transmission is enabled).
The transmit interrupt is not generated even if the TE bit is 1. The first byte of data is written in the main processing, etc.</td><td>Set the SCR.TE bit to 1, set the TIE bit to 1 (a TXI interrupt request is enabled), set the TEIE bit to 1 (a TEI interrupt request is enabled), and set the IEN bit for the TXI interrupt to 1 (TXI interrupt request enabled).
When the SCR.TE bit is set to 1, the IR flag for the transmit interrupt (TXI interrupt) becomes 1, and the transmit interrupt is generated. Write the first byte of transmit data in the transmit interrupt handling.</td></tr>
<tr><td>(3) When transmit data is transferred to the transmit shift register</td><td colspan="2">The IR flag (IR bit) for the transmit interrupt becomes 1, and the transmit interrupt is generated. The second byte of data is written in the transmit interrupt handling.</td></tr>
<tr><td>(4) Transmit interrupt when writing the last data</td><td>—</td><td>Set the IEN bit for the TEI interrupt to 1 (TEI interrupt enabled), set the SCR.TIE bit to 0 (a TXI interrupt request is disabled), and set the IEN bit for the TXI interrupt to 0 (TXI interrupt disabled).</td></tr>
<tr><td>(5) Transmit interrupt after writing the last data</td><td>Interrupt handling is completed without transmit data being written.</td><td>—
(The transmit interrupt is not generated.)</td></tr>
<tr><td>(6) After outputting the last data</td><td rowspan="2">—</td><td>The transmit end interrupt is generated.</td></tr>
<tr><td>(7) When transmission is complete</td><td>In the transmit end interrupt processing, set the SCR.TE bit to 0 (serial transmission is disabled), set the TEIE bit to 0 (a TEI interrupt request is disabled), and set the IEN bit for the TEI interrupt to 0 (TEI interrupt disabled) to disable transmission.
When transmission is disabled, the IR flag for the transmit end interrupt becomes 0, and the TXD pin becomes Hi-Z.</td></tr>
<tr><td>(8) When transmission restarts</td><td>The next data is written in the main processing, etc.</td><td>The same processing as in “(2) When transmission starts” occurs.</td></tr>
</table>

3.1.2 Differences in Receiving

Figure 3.2 shows Differences in Timing Between the RX and the M16C (During Reception). Table 3.3 shows Differences in Operation and Processing at Various Timings Between the RX and the M16C (During Reception).

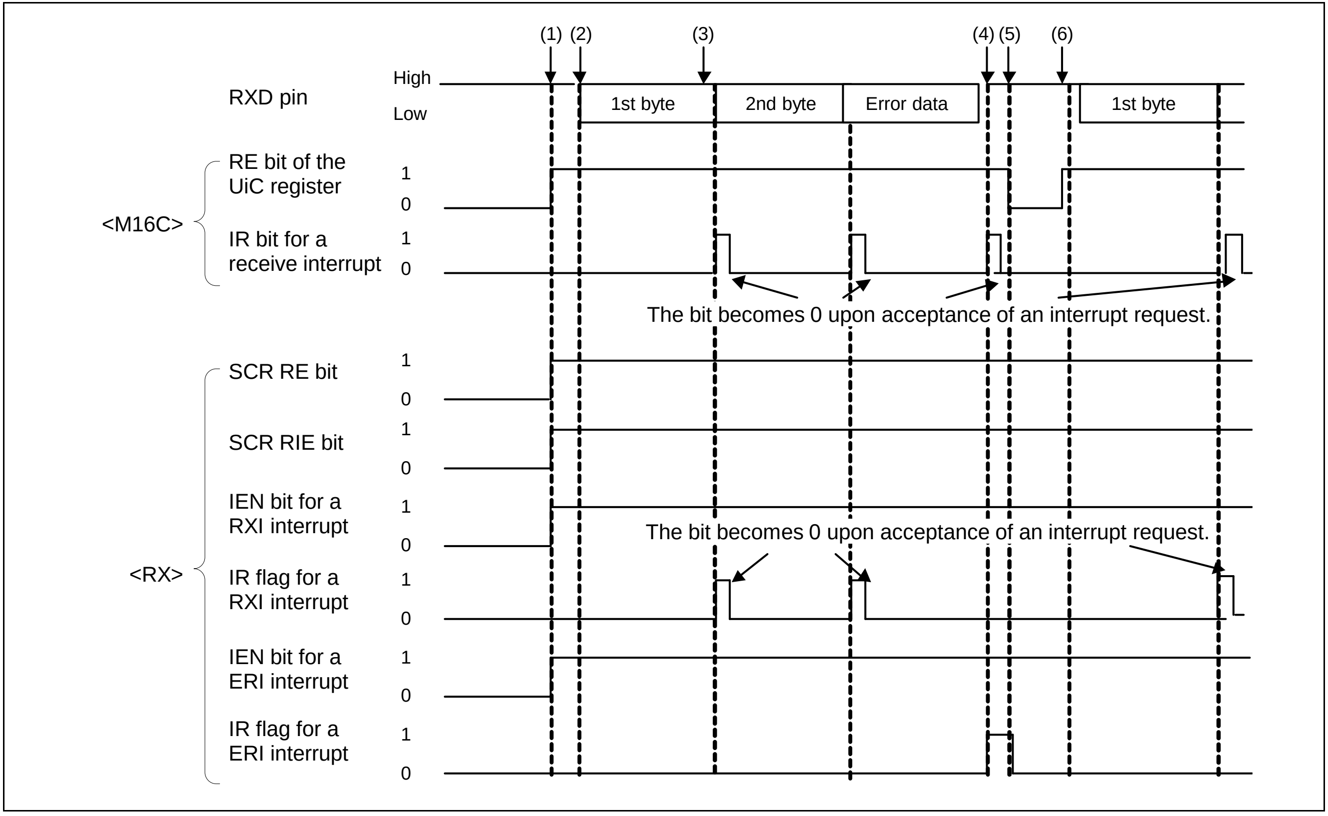


Figure 3.2 Differences in Timing Between the RX and the M16C (During Reception)

Table 3.3 Differences in Operation and Processing at Various Timings Between the RX and the M16C (During Reception)

<table>
<tr><th colspan="2">Timing</th><th>M16C (M16C/65C)</th><th>RX (RX231, RX660)</th></tr>
<tr><td>(1)</td><td>When reception is enabled</td><td>Set the RE bit to 1 (reception is enabled) to enable reception.</td><td>Set the SCR.RE bit to 1 (serial reception is enabled), the RIE bit to 1 (RXI interrupt request is enabled), the IEN bit for the RXI interrupt to 1 (RXI interrupt request enabled), and the IEN bit for the ERI interrupt to 1 (ERI interrupt request enabled) to enable reception.</td></tr>
<tr><td>(2)</td><td>When reception starts</td><td colspan="2">Receive operation starts when the start bit is input to the RXD pin.</td></tr>
<tr><td>(3)</td><td>When reception is completed</td><td colspan="2">When 1 byte of data is received, the received data is stored in the receive buffer, the IR flag (IR bit) for the receive interrupt (RXI interrupt) becomes 1, and the receive interrupt is generated. The value from the receive buffer is read in the receive interrupt handling.</td></tr>
<tr><td>(4)</td><td>When a receive error occurs</td><td>A receive interrupt occurs.
In the receive interrupt handling, read the error flag for the receive buffer register, and check to see if a receive error occurred.</td><td>The ERI interrupt is generated. Receive error processing is performed in the ERI interrupt handling.</td></tr>
<tr><td>(5)</td><td>Clear the receive error flag</td><td>Set the RE bit to 0 (reception disabled), and set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).</td><td rowspan="2">After reading the error flags in the SSR register, set the flags to 0 to clear them.
After all error flags have been cleared, the IR flag for the ERI interrupt becomes 0, and reception is enabled.</td></tr>
<tr><td>(6)</td><td>When reception is restarted</td><td>When bits SMD2 to SMD0 in the UiMR register are set to 101b (UART mode character length is 8 bits), and the RE bit is set to 1, reception is enabled.</td></tr>
</table>

3.2 Calculating the Bit Rate

There are differences in calculating the bit rate between the RX Family and M16C Family. Table 3.4 shows Differences in Calculating the Bit Rate.

Table 3.4 Differences in Calculating the Bit Rate

Item	M16C (M16C/65C)	RX (RX231)	RX (RX660)
Calculating the bit rate using the internal clock	Clock source / 16 (m + 1) Clock source: f1SIO, f2SIO, f8SIO, or f32SIO m: Value set in the UiBRG register	In the case where BGDM = 0 and ABCS = 0: Clock source / 32 (N + 1) *1 In the case where BGDM = 1 and ABCS = 0, or where BGDM = 0 and ABCS = 1: Clock source / 16 (N + 1) *1 In the case where BGDM = 1 and ABCS = 1: Clock source / 8 (N + 1) *1 Clock source: PCLK, PCLK/4, PCLK/16, or PCLK/64 N: Value set in the BRR register	In the case where BGDM = 0 and ABCS = 0: Clock source / 32 (N + 1) *1 In the case where BGDM = 1 and ABCS = 0, or where BGDM = 0 and ABCS = 1: Clock source / 16 (N + 1) *1 In the case where BGDM = 1 and ABCS = 1: Clock source / 8 (N + 1) *1 In the case where ABCSE = 1: Clock source / 6 (N + 1) *1 Clock source: PCLK, PCLK/4, PCLK/16, or PCLK/64 N: Value set in the BRR register
Calculating the bit rate using the external clock	fEXT/16 (m + 1) fEXT: Input from the CLKi pin m: Value set in the UiBRG register	fEXT/16 (when ABCS = 0) fEXT/8 (when ABCS = 0) fEXT: Input from the CLKi pin	fEXT/16 (when ABCS = 0) fEXT/8 (when ABCS = 0) fEXT: Input from the CLKi pin
Calculating the bit rate when the reference clock is generated by the TMR	—	Only when using SCI5, SCI6, and SCI12: The clock can be input from the TMR. (For details, refer to the User's Manual: Hardware).	Only when using SCI5, SCI6, and SCI12: The clock can be input from the TMR. (For details, refer to the User's Manual: Hardware).

Note: 1. Based on the "Relationships between N Setting in BRR and Bit Rate B" in the User's Manual: Hardware (in the case where BGDM = 0 and ABCS = 0):

$B = PCLK / (64 \times 2^{2n-1} \times (N + 1))$
$= PCLK / (32 \times 2^{2n} \times (N + 1))$
$= (PCLK / 2^{2n}) / (32 \times (N + 1))$
$= \text{Clock source} / (32 \times (N + 1))$

4. Appendix

4.1 Points on Migration From the M16C Family to the RX Family

This chapter explains points on migration from the M16C Family to the RX Family.

4.1.1 Interrupts

For the RX Family, when an interrupt request is received while all of the following conditions are met, the interrupt occurs.

- The I flag (PSW.I bit) is 1.
- Registers IER and IPR in the ICU are set to enable interrupts.
- The interrupt request is enabled by the interrupt request enable bit for the peripheral function.

Table 4.1 shows Comparison of Conditions for Interrupt Generation Between the RX and the M16C.

Table 4.1 Comparison of Conditions for Interrupt Generation Between the RX and the M16C

Item	M16C	RX
I flag	When the I flag is set to 1 (enabled), the maskable interrupt request can be accepted.	
Interrupt request flag	When there is an interrupt request from a peripheral function, the interrupt request flag becomes 1 (interrupt requested).	
Interrupt priority level	Selected by setting bits ILVL2 to ILVL0.	Selected by setting the IPR[3:0] bits.
Interrupt request enable	—	Specified by setting the IER register.
Interrupt enable for peripheral functions	—	Interrupt enable or disable can be specified in each peripheral function.

For more information, refer to sections Interrupt Controller (ICU), CPU, and sections for other peripheral functions used in the User’s Manual: Hardware.

4.1.2 I/O ports

In the RX Family, the MPC must be configured in order to assign I/O signals of peripheral functions to pins.

Before controlling the input and output pins in the RX Family, the following two items must be set.

- In the MPC.PFS register, select the peripheral functions that are assigned to the appropriate pins.
- In the PMR register for I/O ports, select the function for the pin to be used as a general I/O port or I/O port for a peripheral function.

Table 4.2 shows Comparison of I/O Settings for Peripheral Function Pins Between the RX and the M16C.

Table 4.2 Comparison of I/O Settings for Peripheral Function Pins Between the RX and the M16C

Function	M16C (in the case of the M16C/65C)	RX (in the case of the RX660/RX231)
Select the pin function	These are not available in the M16C. *1 When a mode of a peripheral function is selected, an appropriate pin is assigned as an I/O pin for the peripheral function.	A pin to which a peripheral I/O is assigned can be selected from multiple pins. The PFS register is used to select a peripheral function I/O that is assigned to a pin used.
Switch between general I/O port and peripheral function		With the PMR register, the pin function can be selected as a general I/O port or a peripheral function.

Note: 1. Register for similar functions are available in the M32C Series and R32C Series.

For more information, refer to the Multi-Function Pin Controller (MPC) and I/O port sections in the User's Manual: Hardware.

4.1.3 Module Stop Function

RX has the ability to stop each peripheral module individually.

By placing unused peripheral modules in the module stop state, power consumption can be reduced.

After a reset is released, all modules (with a few exceptions) are in the module stop state.

Registers for modules in the module stop state cannot be read or write accessed.

For more information, refer to the Low Power Consumption section in the User's Manual: Hardware.

4.2 I/O Register Macros

Macro definitions listed in Table 4.3 can be found in the RX I/O register definitions (iodefine.h).

The readability of programs can be achieved with these macro definitions.

Table 4.3 shows Macro Usage Examples.

Table 4.3 Macro Usage Examples

Macro	Usage Example
IR("module name", "bit name")	**IR(MTU0, TGIA0)** = 0 ; The IR bit corresponding to MTU0.TGIA0 is cleared to 0 (no interrupt request is generated).
DTCE("module name", "bit name")	**DTCE (MTU0, TGIA0)** = 1 ; The DTCE bit corresponding to MTU0.TGIA0 is set to 1 (DTC activation is enabled).
IEN("module name", "bit name")	**IEN(MTU0, TGIA0)** = 1 ; The IEN bit corresponding to MTU0.TGIA0 is set to 1 (interrupt enabled).
IPR("module name", "bit name")	**IPR(MTU0, TGIA0)** = 0x02 ; The IPR bit corresponding to MTU0.TGIA0 is set to 2 (interrupt priority level 2).
MSTP("module name")	**MSTP(MTU)** = 0 ; The MTU0 Module Stop bit is set to 0 (module stop state is canceled).
VECT("module name", "bit name")	#pragma interrupt (Excep_MTU0_TGIA0 (vect = **VECT(MTU0, TGIA0)**) The interrupt function is declared for the corresponding MTU0.TGIA0 register.

4.3 Intrinsic Functions

The RX Family has intrinsic functions for setting control registers and special instructions. When using intrinsic functions, include machine.h.

Table 4.4 shows Examples of Differences in the Settings of Control Registers and Descriptions of Special Instructions Between the RX and the M16C.

Table 4.4 Examples of Differences in the Settings of Control Registers and Descriptions of Special Instructions Between the RX and the M16C

Item	Description	
	M16C	RX
Set the I flag to 1	asm("fset i");	setpsw_i (); *1
Set the I flag to 0	asm("fclr i");	clrpsw_i (); *1
Expanded into the WAIT instruction	asm("wait");	wait(); *1
Expanded into the NOP instruction	asm("nop");	nop(); *1

Note: 1. The machine.h file must be included.

5. Reference Documents

User's Manual: Hardware

RX230/RX231 Group User's Manual: Hardware (R01UH0496EJ)

RX660 Group User's Manual: Hardware (R01UH0037EJ)

M16C/65C Group User's Manual: Hardware (R01UH0093EJ)

If you are using a product that does not belong to the RX231, RX660, or M16C/65C group, refer to the applicable user's manual for hardware.

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family CC-RX Compiler User's Manual (R20UT3248)

M16C Series, R8C Family C Compiler Package (M3T-NC30WA)

The latest versions can be downloaded from the Renesas Electronics website.

REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 1, 2014	—	First edition issued
2.00	June 12, 2023	—	The product model of the target device for the RX MCU was changed: From RX210 to RX231/RX660

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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