RX Family and M16C Family

Guide for Migration from the M16C to the RX: Simple I²C Mode

Abstract

This document describes migration from special mode 1 (I²C mode) for the serial I/O in the M16C Family to the simple I²C mode for the SCI in the RX Family.

Products

RX Family

M16C Family

When this document explains migration from the M16C Family to the RX Family, the M16C/65C Group MCU is used as an example of the M16C Family MCU, and the RX231 Group and RX660 Group MCUs are used as examples of the RX Family MCU. When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Differences in Terminology Between the RX Family and M16C Family MCUs

Item	M16C Family	RX Family
Serial communication interface (SCI)	Serial I/O	SCI
Simple I²C mode	Special mode 1 (I²C mode)	Simple I²C mode
SDA pin	SDAi pin	SSDAi pin
SCL pin	SCLi pin	SSCLi pin
SCI operating clock (clock source)	Count source	Clock source
Peripheral function operating clock	Peripheral function clocks: f1, fOCO40M, fOCO-F, fOCO-S, fC32	Peripheral module clocks: PCLKA, PCLKB, PCLKC, PCLKD
Transmit buffer	UiTB register (transmit buffer)	TDR registers: TDRH, TDRL, TDRHL
Transmit shift register	UART transmit shift register	TSR register
Receive buffer	UiRB register	RDR registers: RDRH, RDRL, RDRHL
Start condition	Start condition	Start condition
Stop condition	Stop condition	Stop condition
Restart condition	Restart condition	Restart condition
Interrupt after generating the start condition and stop condition	Start/stop condition detection interrupt *1	STI interrupt
Transmit interrupt	UARTi transmit interrupt (transmit buffer empty)	TXI interrupt
Transmit complete interrupt (M16C) Transmit end interrupt (RX)	UARTi transmit interrupt (transmission completed)	TEI interrupt
Receive interrupt	UARTi receive interrupt	RXI interrupt
Function to select I/O of peripheral functions for pins	Function select registers and input function select registers *3	MPC *2

Notes: 1. In the M16C Family, an interrupt request occurs when a start condition, restart condition, or stop condition is generated.
2. The MPC is not available in some groups.
3. Only available in the M32C Series and R32C Series.

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1. Differences in Simple I²C Mode

Table 1.1 shows General Differences in Simple I²C Mode.

Table 1.1 General Differences in Simple I²C Mode

Item	M16C (M16C/65C)	RX (RX231)	RX (RX660)
Operating mode	Master, slave	Master *1	Master *1
Data length	8 bits	8 bits	8 bits
Data format	MSB first fixed	MSB first fixed	MSB first fixed
Interrupt sources	Transmit, NACK (TXI) interrupt Receive, ACK detection (RXI) interrupt Start condition, stop condition detection interrupt	Transmit, NACK (TXI) interrupt Receive, ACK detection (RXI) interrupt Completion of generating a start, restart, or stop condition interrupt (STI interrupt)	Transmit, NACK (TXI) interrupt Receive, ACK detection (RXI) interrupt Completion of generating a start, restart, or stop condition interrupt (STI interrupt)
Error detection	Overrun error Arbitration lost	Not available	Not available
Noise cancellation	Not available	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. The noise elimination width can be adjusted.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. The noise elimination width can be adjusted.
Clock phase setting	Clock delay available or no clock delay selectable	Clock delay available	Clock delay available

Note: 1. Use the RIIC when performing slave operation with the RX Family.

2. Peripheral Functions Used

Table 2.1 shows Peripheral Functions and Modes to Be Used for Example Operations in Simple I²C Mode.

Table 2.1 Peripheral Functions and Modes to Be Used for Example Operations in Simple I²C Mode

No.	Operating Example	M16C		RX	
		Peripheral Function	Mode	Peripheral Function	Mode
1	Master transmit operation in simple I²C mode	Serial I/O	Special mode 1 (I²C mode)	SCI	Simple I²C mode
2	Master receive operation in simple I²C mode				

3. Differences in Simple I²C Mode

This section describes the differences in simple I²C mode between the RX and the M16C, using the conditions listed in Table 3.1 Conditions for Simple I²C Communication as an example.

Table 3.1 Conditions for Simple I²C Communication

Item	Conditions for Transmission and Reception
Peripheral function operating clock	16 MHz
Transfer rate	100 kbps
Channels used	RX Family: SCI0 M16C Family: UART0

3.1 Differences in Master Transmission

This section describes the differences in master transmission in simple I²C mode.

3.1.1 Differences in Timings During Master Transmission

Figure 3.1 shows Differences in Timings During Master Transmission Between the RX and the M16C (When Transmitting 3 Bytes).

Table 3.2 shows Differences in Operation and Processing at Various Timings Between the RX and the M16C (During Master Transmission).

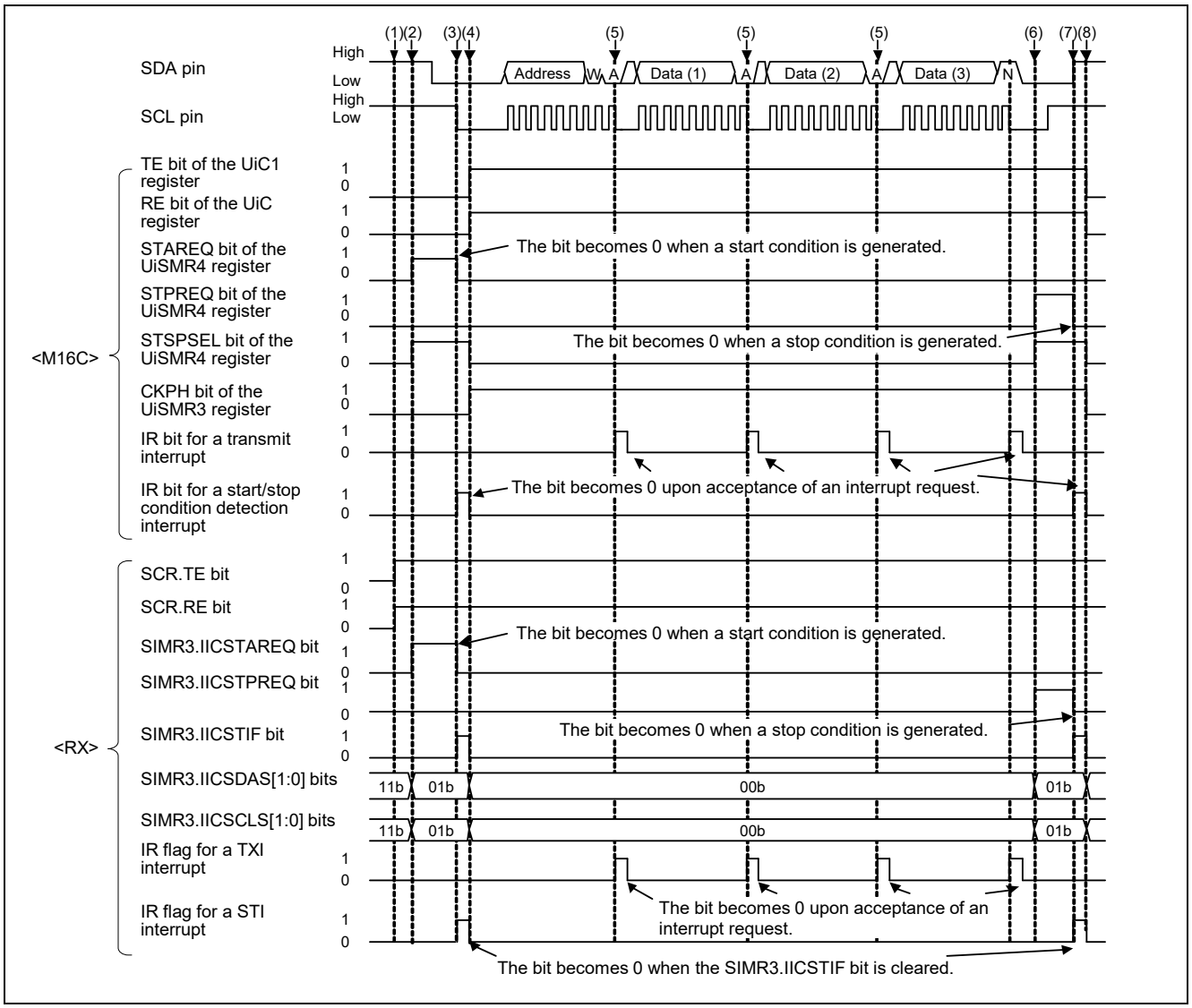

Figure 3.1 Differences in Timings During Master Transmission Between the RX and the M16C (When Transmitting 3 Bytes)

Table 3.2 Differences in Operation and Processing at Various Timings Between the RX and the M16C (During Master Transmission)

Timing	M16C (M16C/65C)	RX (RX231, RX660)
(1) Before transmission starts	Bits ILVL2 to ILVL0 in the UiBCNIC register are set and the start condition/stop condition interrupt is enabled.	The SCR.TE bit is set to 1 (serial transmission is enabled), the SCR.RE bit is set to 1 (serial reception is enabled), the SCR.TIE bit is set to 1 (TXI interrupt request is enabled), and the SCR.TEIE bit is set to 1 (STI interrupt request is enabled).
(2) Output of a start condition	After the STAREQ bit is set to 1, the STSPSEL bit is set to 1 (select start condition/stop condition generate circuit).	At the same time the SIMR3.IICSTAREQ bit is set to 1 (start condition is generated), the SIMR3.IICSCLS[1:0] bits and the SIMR3.IICSDAS[1:0] bits are set to 01b (generate a start, restart, or stop condition).
(3) Generation of a start condition detection interrupt	The STAREQ bit becomes 0, and the IR bit for the start condition/stop condition detection interrupt becomes 1.	The SIMR3.IICSTAREQ bit is set to 0 (start condition is not generated), the SIMR3.IICSTIF bit is set to 1 (all request generation has been completed), and the IR flag for the STI interrupt becomes 1.
(4) Handling of the start condition detection interrupt	The CKPH bit is set to 1 (with clock delay), the TE bit is set to 1 (transmission enabled), the RE bit is set to 1 (reception enabled), and the STSPSEL bit is set to 0 (select serial I/O circuit). In addition, bits ILVL2 to ILVL0 in the SiTIC register are set and the transmit interrupt is enabled. Then, the first byte of transmit data (slave address and W bit) is written to the transmit buffer.	The SIMR3.IICSTIF bit is set to 0, the SIMR3.IICSCLS[1:0] bits are set to 00b (serial clock output), and the SIMR3.IICSDAS[1:0] bits are set to 00b (serial data output). When the SIMR3.IICSTIF bit is set to 0, the IR flag for the STI interrupt becomes 0. Then, the first byte of transmit data (slave address and R/W bit) is written to the transmit buffer.
(5) When transmission is complete	The IR flag (IR bit) for the transmit interrupt (TXI interrupt) becomes 1, and the transmit interrupt is generated. In the transmit interrupt handling, after ACK or NACK is confirmed, the second byte and successive data is written to the transmit buffer.	
(6) Handling of a transmit interrupt after the last data is output	After the STPREQ bit is set to 1, the STSPSEL bit is set to 1 (select start condition/stop condition generate circuit).	At the same time the SIMR3.IICSTPREQ bit is set to 1 (stop condition is generated), the SIMR3.IICSCLS[1:0] bits and the SIMR3.IICSDAS[1:0] bits are set to 01b.
(7) When transmission ends	The STPREQ bit becomes 0, and the IR bit for the start condition/stop condition detection interrupt becomes 1.	The SIMR3.IICSTPREQ bit becomes 0 (stop condition is not generated), the SIMR3.IICSTIF bit becomes 1, and the IR flag for the STI interrupt becomes 1.
(8) Handling of a stop condition detection interrupt	The TE bit is set to 0 (transmission disabled), the RE bit is set to 0 (reception disabled), the CKPH bit is set to 0 (no clock delay), the STSPSEL bit is set to 0 (select serial I/O circuit), and bits SMD2 to SMD0 in the UiMR register are set to 000b.	The SIMR3.IICSTIF bit is set to 0, and bits SIMR3.IICSCLS[1:0] and SIMR3.IICSDAS[1:0] are set to 11b (high-impedance). When the SIMR3.IICSTIF bit is set to 0, the IR flag for the STI interrupt becomes 0.

3.2 Differences in Master Reception

This section describes the differences in master reception in simple I²C mode.

3.2.1 Differences in Timings During Master Reception

Figure 3.2 shows Differences in Timings During Master Reception Between the RX and the M16C (When Receiving 3 Bytes).

Table 3.3 shows Differences in Operation and Processing at Various Timings Between the RX and the M16C (During Master Reception) (1/2).

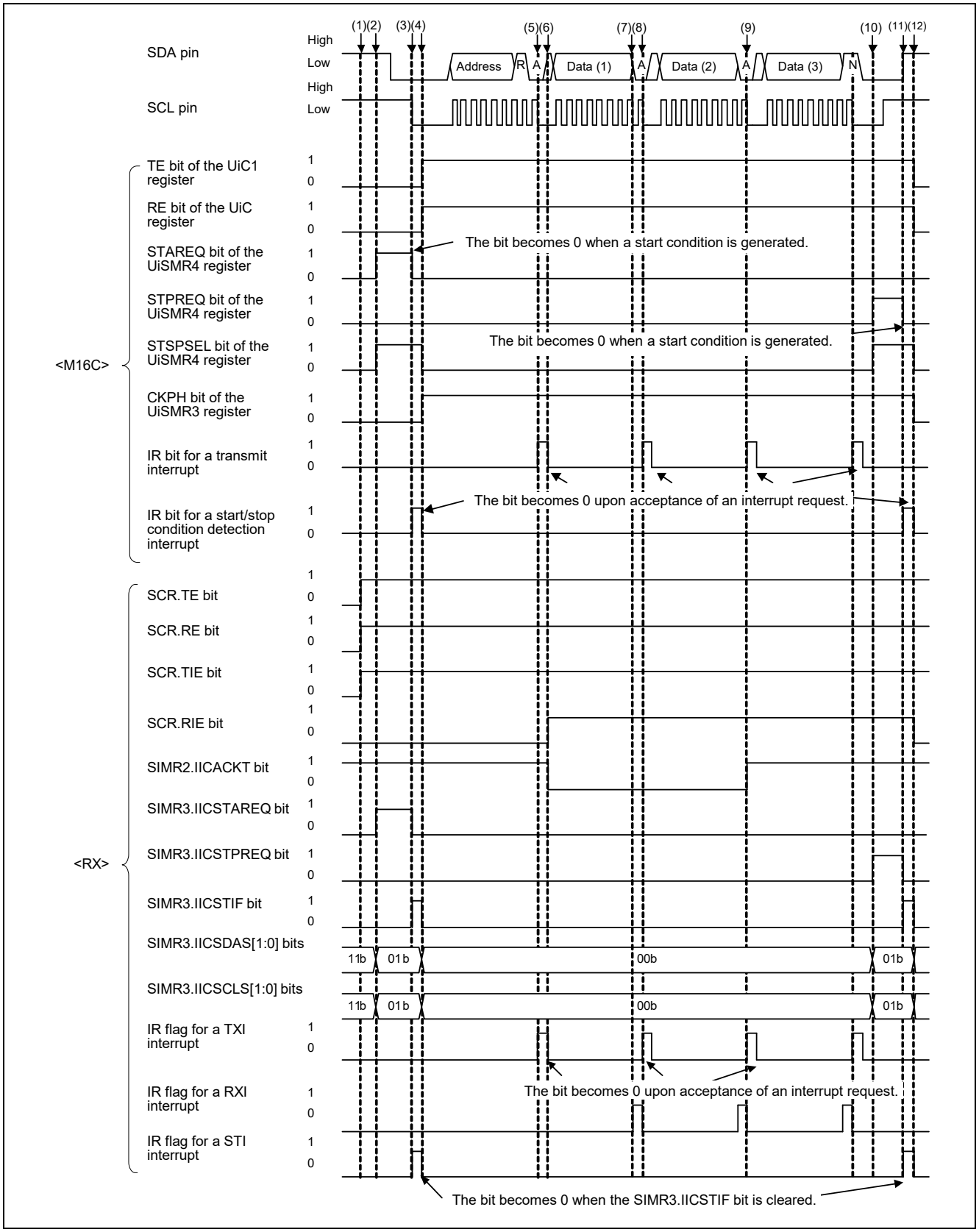

Figure 3.2 Differences in Timings During Master Reception Between the RX and the M16C (When Receiving 3 Bytes)

Table 3.3 Differences in Operation and Processing at Various Timings Between the RX and the M16C (During Master Reception) (1/2)

Timing		M16C (M16C/65C)	RX (RX231, RX660)
(1)	When reception is enabled	Bits ILVL2 to ILVL0 in the UiBCNIC register are set and the start condition/stop condition interrupt is enabled.	The SCR.TE bit is set to 1 (serial transmission is enabled), the SCR.RE bit is set to 1 (serial reception is enabled), the SCR.TIE bit is set to 1 (TXI interrupt request is enabled), and the SCR.TEIE bit is set to 1 (STI interrupt request is enabled).
(2)	When reception starts	After the STAREQ bit is set to 1, the STSPSEL bit is set to 1 (select start condition/stop condition generate circuit).	At the same time the SIMR3.IICSTAREQ bit is set to 1 (start condition is generated), the SIMR3.IICSCLS[1:0] bits and the SIMR3.IICSDAS[1:0] bits are set to 01b (generate a start, restart, or stop condition).
(3)	When reception is complete	The STAREQ bit becomes 0, and the IR bit for the start condition/stop condition detection interrupt becomes 1.	The SIMR3.IICSTAREQ bit is set to 0 (start condition is not generated), the SIMR3.IICSTIF bit is set to 1 (all request generation has been completed), and the IR flag for the STI interrupt becomes 1.
(4)	When a receive error occurs	The CKPH bit is set to 1 (with clock delay), the TE bit is set to 1 (transmission enabled), the RE bit is set to 1 (reception enabled), and the STSPSEL bit is set to 0 (select serial I/O circuit). Then, the first byte of transmit data (slave address and R bit) is written to the transmit buffer.	The SIMR3.IICSTIF bit is set to 0, the SIMR3.IICSCLS[1:0] bits are set to 00b (serial clock output), and the SIMR3.IICSDAS[1:0] bits are set to 00b (serial data output). When the SIMR3.IICSTIF bit is set to 0, the IR flag for the STI interrupt becomes 0. Then, the first byte of transmit data (slave address and R/W bit) is written to the transmit buffer.
(5)	Clearance of receive error flags	The IR flag (IR bit) for the transmit interrupt (TXI interrupt) becomes 1, and the transmit interrupt is generated.	
(6)	When reception is restarted	0x00FF is written as dummy data to the transmit buffer.	The SCR.RIE bit is set to 1 (RXI interrupt request is enabled), the SIMR2.IICACKT bit is set to 0 (ACK transmission), and dummy data (0xFF) is written to the transmit buffer.
(7)	When data is received	—	The IR flag for the RXI interrupt becomes 1. Data received is read in the RXI interrupt handling.
(8)	ACK transmission complete	The IR bit for the transmit interrupt becomes 1. After the transmit interrupt is used to read the receive data, dummy data (0x00FF) is written to the transmit buffer.	The IR flag for the TXI interrupt becomes 1. Dummy data (0xFF) is written to the transmit buffer in the TXI interrupt handling.
(9)	Handling of a transmit complete interrupt before the last data is written	After reading the data received, 0x01FF is written to the transmit buffer as dummy data.	The SIMR2.IICACKT bit is set to 1 (NACK transmission), and dummy data (0xFF) is written to the transmit buffer.
(10)	Handling of a transmit interrupt after the last data is output	After the STPREQ bit is set to 1, the STSPSEL bit is set to 1 (select start condition/stop condition generate circuit).	At the same time the SIMR3.IICSTPREQ bit is set to 1 (stop condition is generated), the SIMR3.IICSCLS[1:0] bits and the SIMR3.IICSDAS[1:0] bits are set to 01b.

Table 3.4 Differences in Operation and Processing at Various Timings Between the RX and the M16C (During Master Reception) (2/2)

Timing	M16C (M16C/65C)	RX (RX231, RX660)
(11) Stop condition detection interrupt generation	The STPREQ bit becomes 0, and the IR bit for the start condition/stop condition detection interrupt becomes 1.	The SIMR3.IICSTPREQ bit becomes 0 (stop condition is not generated), the SIMR3.IICSTIF bit becomes 1, and the IR flag for the STI interrupt becomes 1.
(12) Handling of a stop condition detection interrupt	The TE bit is set to 0 (transmission disabled), the RE bit is set to 0 (reception disabled), the CKPH bit is set to 0 (no clock delay), the STSPSEL bit is set to 0 (select serial I/O circuit), and bits SMD2 to SMD0 in the UiMR register are set to 000b.	The SCR.RIE bit is set to 0 (RXI interrupt request is disabled), the SIMR3.IICSTIF bit is set to 0, and bits SIMR3.IICSCLS[1:0] and SIMR3.IICSDAS[1:0] are set to 11b (high-impedance). When the SIMR3.IICSTIF bit is set to 0, the IR flag for the STI interrupt becomes 0.

3.3 Calculating the Bit Rate

There are differences in calculating the bit rate between the RX Family and M16C Family. Table 3.5 shows Differences in Calculating the Bit Rate.

Table 3.5 Differences in Calculating the Bit Rate

Item	M16C (M16C/65C)	RX (RX231)	RX (RX660)
Calculating the bit rate using the internal clock	Clock source / 2(*n* + 1) Clock source: f1SIO, f2SIO, f8SIO, or f32SIO *n*: Value set in the UiBRG register	Clock source / 32(*N*+1) *1 Clock source: PCLK, PCLK/4, PCLK/16, or PCLK/64 *N*: Value set in the BRR register	Clock source / 32(*N*+1) *1 Clock source: PCLK, PCLK/4, PCLK/16, or PCLK/64 *N*: Value set in the BRR register

Note: 1. Based on the “Relationships between N Setting in BRR and Bit Rate B” in the User’s Manual: Hardware:

$B = PCLK / (64 \times 2^{2n-1} \times (N + 1))$

$= PCLK / (32 \times 2^{2n} \times (N + 1))$

$= (PCLK / 2^{2n}) / (32 \times (N + 1))$

$=$ Clock source $/ (32 \times (N + 1))$

4. Appendix

4.1 Points on Migration From the M16C Family to the RX Family

This chapter explains points on migration from the M16C Family to the RX Family.

4.1.1 Interrupts

For the RX Family, when an interrupt request is received while all of the following conditions are met, the interrupt occurs.

- The I flag (PSW.I bit) is 1.
- Registers IER and IPR in the ICU are set to enable interrupts.
- The interrupt request is enabled by the interrupt request enable bits for the peripheral function.

Table 4.1 shows Comparison of Conditions for Interrupt Generation Between the RX and the M16C.

Table 4.1 Comparison of Conditions for Interrupt Generation Between the RX and the M16C

Item	M16C	RX
I flag	When the I flag is set to 1 (enabled), the maskable interrupt request can be accepted.	
Interrupt request flag	When there is an interrupt request from a peripheral function, the interrupt request flag becomes 1 (interrupt requested).	
Interrupt priority level	Selected by setting bits ILVL2 to ILVL0.	Selected by setting the IPR[3:0] bits.
Interrupt request enable	—	Specified by setting the IER register.
Interrupt enable for peripheral functions	—	Interrupt enable or disable can be specified in each peripheral function.

For more information, refer to sections Interrupt Controller (ICU), CPU, and sections for other peripheral functions used in the UMH.

4.1.2 I/O Ports

In the RX Family, the MPC must be configured in order to assign I/O signals of peripheral functions to pins.

Before controlling the input and output pins in the RX Family, the following two items must be set.

- In the MPC.PFS register, select the peripheral functions that are assigned to the appropriate pins.
- In the PORT.PMR register, select the function for the pin to be used as a general I/O port or I/O port for a peripheral function.

Table 4.2 shows Comparison of I/O Settings for Peripheral Function Pins Between the RX and the M16C.

Table 4.2 Comparison of I/O Settings for Peripheral Function Pins Between the RX and the M16C

Function	M16C (in the case of the M16C/65C)	RX (in the case of the RX660/RX231)
Select the pin function	These are not available in the M16C. *1 When a mode is set for a peripheral function, appropriate pins are assigned as I/O pins for the peripheral function.	With the PFS register, I/O ports for peripheral functions can be assigned by selecting from multiple pins.
Switch between general I/O port and peripheral function		With the PMR register, the corresponding pin function can be selected as a general I/O port or a peripheral function.

Note: 1. Register for similar functions are available in the M32C Series and R32C Series.

For more information, refer to the Multi-Function Pin Controller (MPC) and I/O port sections in the UMH.

4.1.3 Module Stop Function

The RX Family has the ability to stop each peripheral module individually.

By transitioning unused peripheral modules to the module stop state, power consumption can be reduced.

After a reset is released, all modules (with a few exceptions) are in the module stop state.

Registers for modules in the module stop state cannot be written to or read.

For more information, refer to the Low Power Consumption section in the User's Manual: Hardware.

4.2 I/O Register Macros

Macro definitions listed in Table 4.3 can be found in the RX I/O register definitions (iodefine.h).

The readability of programs can be achieved with these macro definitions.

Table 4.3 shows Macro Usage Examples.

Table 4.3 Macro Usage Examples

Macro	Usage Example
IR("module name", "bit name")	**IR(MTU0, TGIA0)** = 0 ; The IR bit corresponding to MTU0.TGIA0 is cleared to 0 (no interrupt request is generated).
DTCE("module name", "bit name")	**DTCE (MTU0, TGIA0)** = 1 ; The DTCE bit corresponding to MTU0.TGIA0 is set to 1 (DTC activation is enabled).
IEN("module name", "bit name")	**IEN(MTU0, TGIA0)** = 1 ; The IEN bit corresponding to MTU0.TGIA0 is set to 1 (interrupt enabled).
IPR("module name", "bit name")	**IPR(MTU0, TGIA0)** = 0x02 ; The IPR bit corresponding to MTU0.TGIA0 is set to 2 (interrupt priority level 2).
MSTP("module name")	**MSTP(MTU)** = 0 ; The MTU0 Module Stop bit is set to 0 (module stop state is canceled).
VECT("module name", "bit name")	#pragma interrupt (Excep_MTU0_TGIA0 (vect = **VECT(MTU0, TGIA0)**) The interrupt function is declared for the corresponding MTU0.TGIA0 register.

4.3 Intrinsic Functions

The RX Family has intrinsic functions for setting control registers and special instructions. When using intrinsic functions, include machine.h.

Table 4.4 shows Examples of Differences in the Settings of Control Registers and Descriptions of Special Instructions Between the RX and the M16C.

Table 4.4 Examples of Differences in the Settings of Control Registers and Descriptions of Special Instructions Between the RX and the M16C

Item	Description	
	M16C	RX
Set the I flag to 1	asm("fset i");	setpsw_i (); *1
Set the I flag to 0	asm("fclr i");	clrpsw_i (); *1
Expanded into the WAIT instruction	asm("wait");	wait(); *1
Expanded into the NOP instruction	asm("nop");	nop(); *1

Note: 1. The machine.h file must be included.

5. Reference Documents

User's Manual: Hardware

RX230/RX231 Group User's Manual: Hardware (R01UH0496EJ)
RX660 Group User's Manual: Hardware (R01UH0037EJ)
M16C/65C Group User's Manual: Hardware (R01UH0093EJ)
If you are using a product that does not belong to the RX231, RX660, or M16C/65C Group, refer to the applicable user's manual for hardware.
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family CC-RX Compiler User's Manual (R20UT3248)
M16C Series, R8C Family C Compiler Package (M3T-NC30WA)
The latest versions can be downloaded from the Renesas Electronics website.

REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 18, 2014	—	First edition issued
2.00	June 12, 2023	—	The product model of the target device for the RX MCU was changed: From RX210 to RX231/RX660

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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