RX Family, M16C Family

Migrating From the M16C Family to the RX Family: External Bus

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Abstract

This document describes migrating the external bus in the M16C Family to the RX Family.

Products

RX Family

M16C Family

As an example of migrating from the M16C to the RX, the explanation in this document uses the RX210 Group in the RX Family and the M16C/65C Group in the M16C Family. When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Differences in Terminology

Item	RX Family	M16C Family
Operating mode to access the external memory device	● Internal ROM enabled expansion mode ● Internal ROM disabled expansion mode	● Memory expansion mode ● Microprocessor mode
External memory area	External address space CSn area	External area
Peripheral function registers	I/O registers	Special function registers (SFRs)

Contents

1. Differences in the Functions of the External Bus

Table 1.1 lists the Differences in the Functions of the External Bus.

Table 1.1 Differences in the Functions of the External Bus

Item	RX (RX210)	M16C (M16C/65C)
Memory size	16 MB	1 MB/4 MB
Bus type	Separate bus/multiplexed bus	Separate bus/multiplexed bus
Data bus width	8-bit/16-bit	8-bit/16-bit
Data bus width setting	Set using the CSn control register (n = 0 to 3)	Set using the BYTE pin
Address buses	8 to 24 buses selectable	12, 16, or 20 buses selectable
Chip select outputs	4	4
Write access mode	• 1-write strobe mode • Byte strobe mode	Write signal combinations • $\overline{BHE}/\overline{WR}$ • $\overline{WRL}/\overline{WRH}$
Wait cycle	WAIT pin	RDY pin
Software wait	Wait for up to 31 cycles	0 to 8 waits can be inserted (selectable from 1ϕ + 1ϕ, 1ϕ + 2ϕ, 1ϕ + 3ϕ, 2ϕ + 3ϕ, 2ϕ + 4ϕ, 3ϕ + 4ϕ, 4ϕ + 5ϕ)
Recovery cycles	Maximum of 15 cycles can be inserted (select from 8 patterns)	0 to 3 cycles inserted (retain the last accessed address for address output)
Page access	Supported	N/A

From this point forward, the application note describes a separate bus.

1.1 Example of Connecting to an External Bus

Connecting to bus pins on the M16C and RX is the same. However, note that pin names for the bus control pins differ. Figure 1.1 shows Example of Bus Connection When the Bus Width is 16 Bits. Figure 1.2 shows Example of Bus Connection When the Bus Width is 8 Bits.

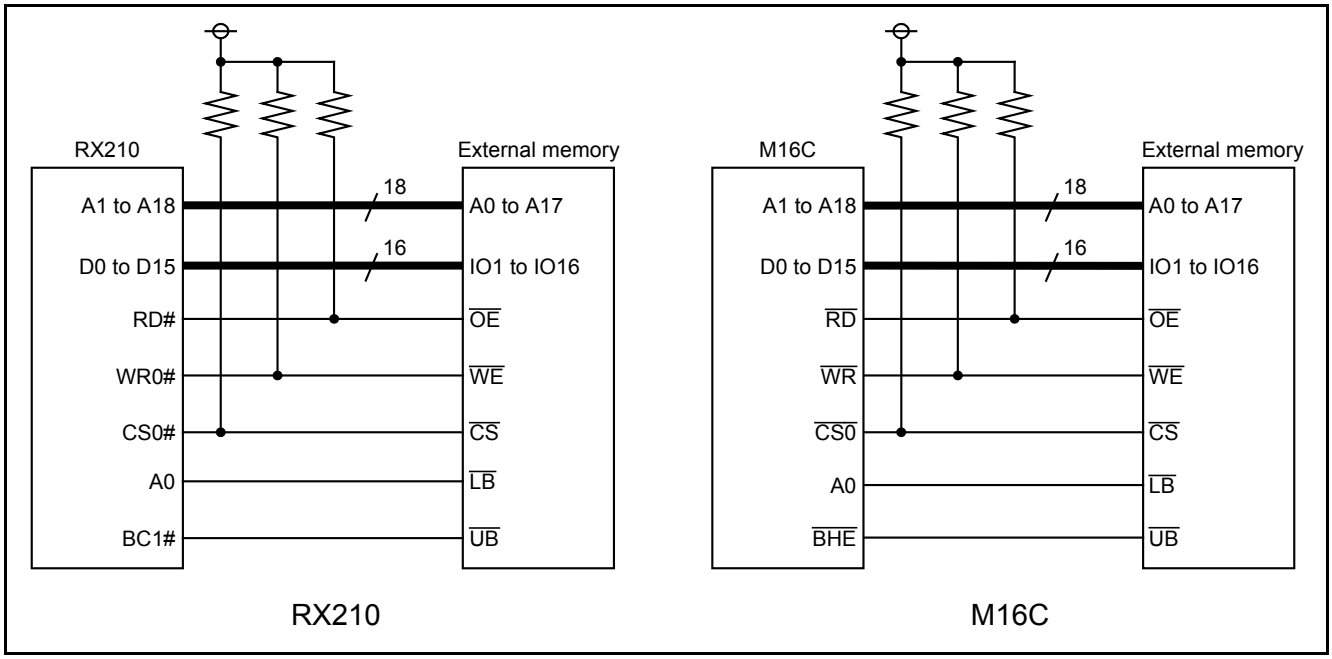


Figure 1.1 Example of Bus Connection When the Bus Width is 16 Bits

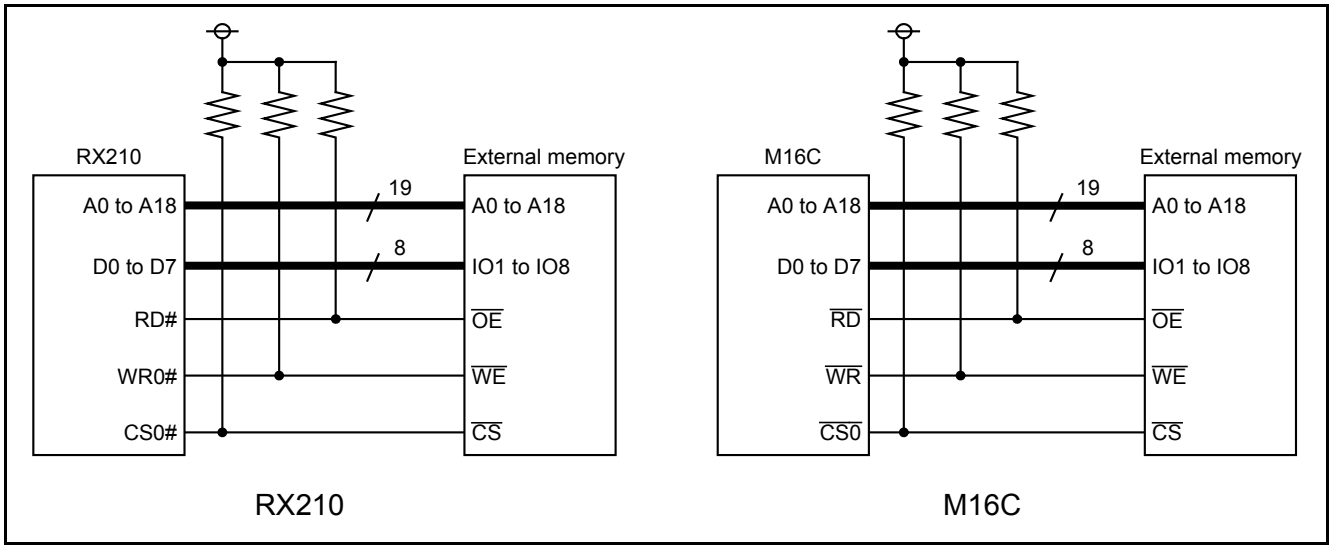


Figure 1.2 Example of Bus Connection When the Bus Width is 8 Bits

1.2 Calculating the Number of Bus Cycles

1.2.1 Calculating the Number of Bus Cycles When Reading

This section shows the differences in the bus timing (when reading) based on the timing shown in Figure 1.3.

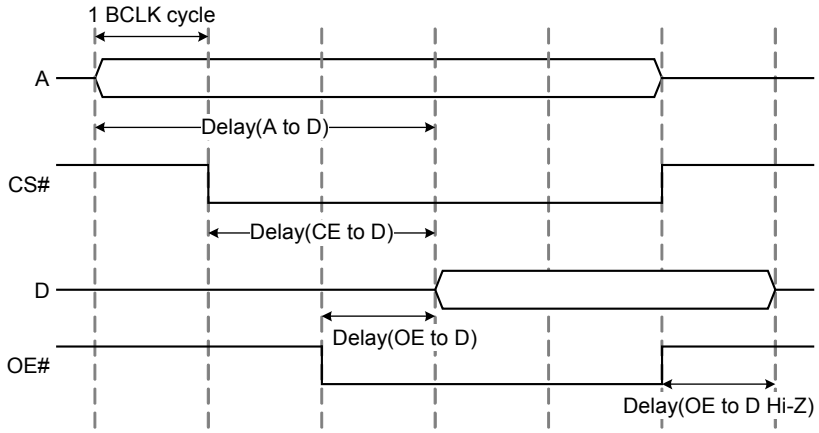
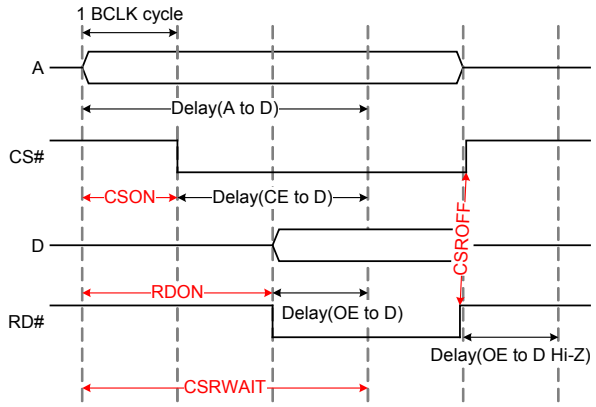
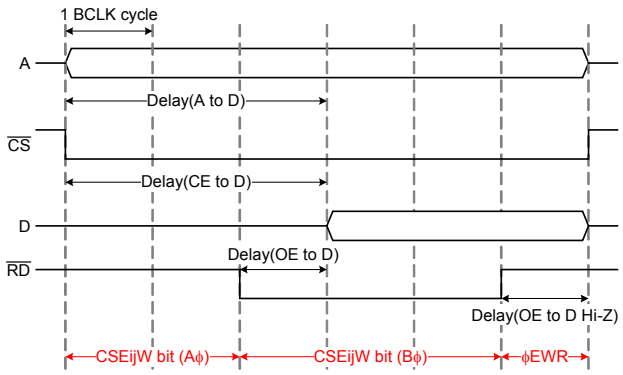


Figure 1.3 Example of Basic Bus Timing When Reading

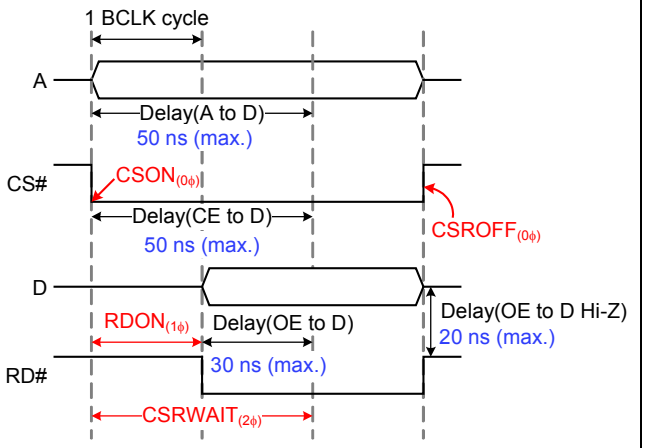
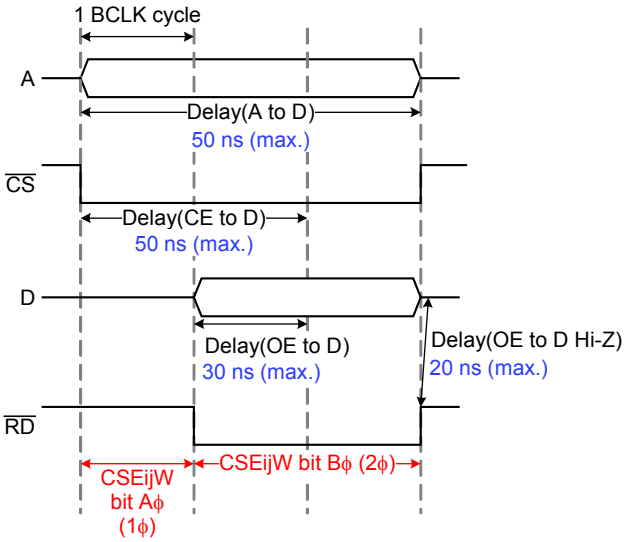
Table 1.2 Differences in the Bus Timing Settings When Reading

<table>
<tr><th colspan="2">RX (RX210)</th><th colspan="2">M16C (M16C/65C)</th></tr>
<tr><td colspan="2"> 
</td><td colspan="2"> 
</td></tr>
<tr><td>CSON</td><td>Sets the number of wait cycles to be inserted before asserting the CSn# signal</td><td colspan="2" rowspan="4">CSEijW bit (Aϕ + Bϕ) (i = 0 to 3, j = 0, 1)
Aϕ sets the number of cycles from the start of the bus access to the falling edge of the RD signal.
Bϕ sets the number of cycles from falling edge of the RD signal to the rising edge.</td></tr>
<tr><td>RDON</td><td>Sets the number of wait cycles to be inserted before asserting the RD# signal</td></tr>
<tr><td>CSRWAIT</td><td>Sets the number of cycles to be inserted in the first access of the normal read cycle</td></tr>
<tr><td>CSROFF</td><td>Sets the number of cycles from negating the RD# signal during a read access, to negating the CSn# signal</td></tr>
<tr><td colspan="2">N/A</td><td>EWR</td><td>Sets the number of recovery cycles according to the number of needed idle cycles</td></tr>
</table>

When reading the connected external memory has the following attributes, values set to the M16C and RX registers are shown in Table 1.3.

- Delay(A to D) = 50 ns (max.)
- Delay(CE to D) = 50 ns (max.)
- Delay(OE to D) = 30 ns (max.)
- Delay(OE to D Hi-Z) = 20 ns (max.)

Table 1.3 Differences in the External Bus Register Setting (When Reading and BCLK = 16 MHz)

<table>
<tr><th colspan="2">RX (RX210)</th><th colspan="2">M16C (M16C/65C)</th></tr>
<tr><td>CSON</td><td>CS0WCR2.BIT.CSON = 0; *1</td><td colspan="2" rowspan="4">CSEijW bit (Aϕ + Bϕ) *2 (i = 0 to 3, j = 0, 1)
CSE = 0x01; /* 2 waits (1ϕ + 2ϕ) */</td></tr>
<tr><td>RDON</td><td>CS0WCR2.BIT.RDON = 1; *1</td></tr>
<tr><td>CSRWAIT</td><td>CS0WCR1.BIT.CSRWAIT = 2; *1</td></tr>
<tr><td>CSROFF</td><td>CS0WCR2.BIT.CSROFF = 0;</td></tr>
<tr><td colspan="2">N/A</td><td>EWR</td><td>EWR = 0x00; / * No recovery cycles */</td></tr>
<tr><td colspan="2"> 
</td><td colspan="2"> 
</td></tr>
</table>

Note 1. Satisfy the following condition: CSnWCR2.CSON bit ≤ CSnWCR2.RDON bit ≤ CSnWCR1.CSRWAIT bit.

Note 2. Select from 1ϕ + 1ϕ, 1ϕ + 2ϕ, 1ϕ + 3ϕ, 2ϕ + 3ϕ, 2ϕ + 4ϕ, 3ϕ + 4ϕ, or 4ϕ + 5ϕ.

1.2.2 Calculating the Number of Bus Cycles When Writing

This section shows the differences in the bus access timing (when writing) based on the timing shown in Figure 1.4.

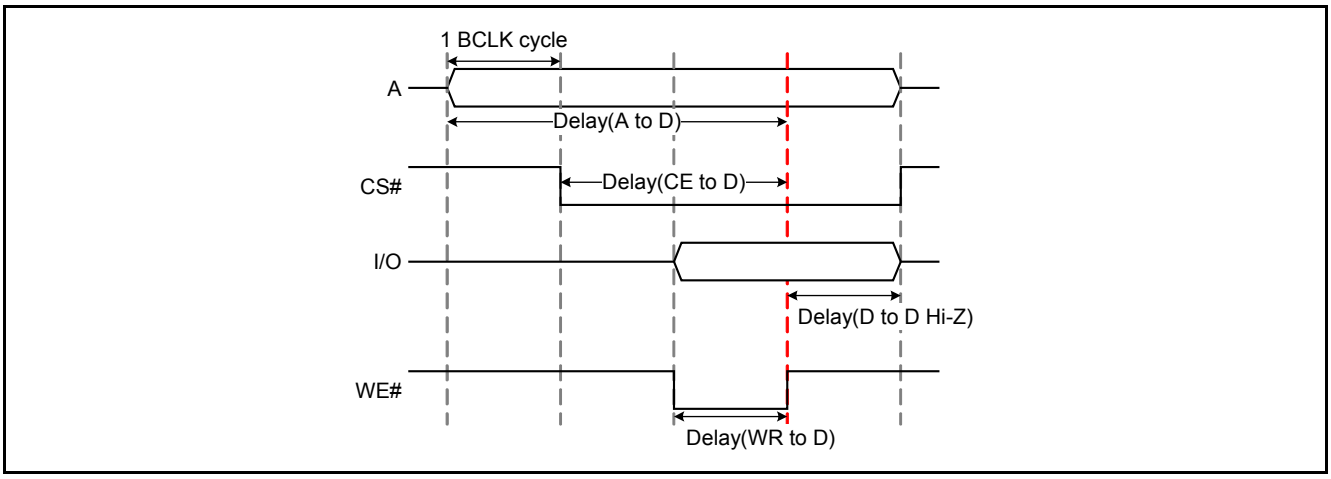
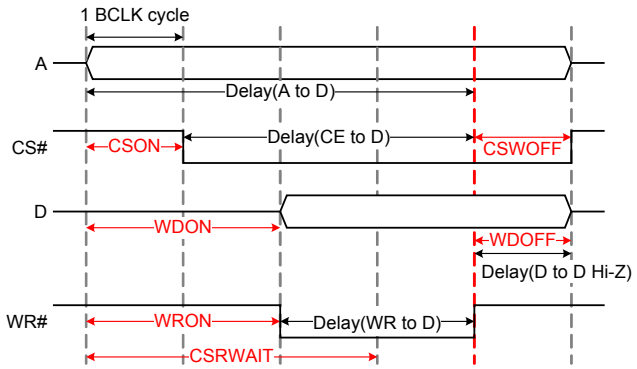
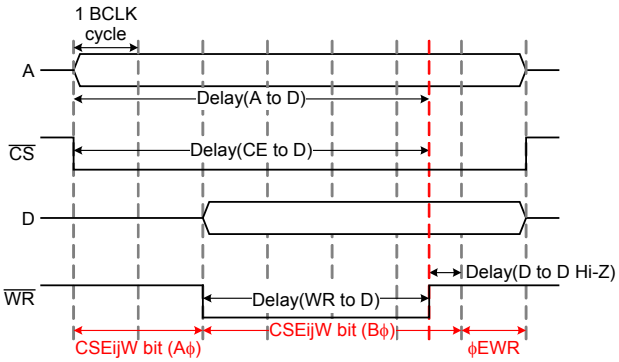


Figure 1.4 Example of Basic Bus Timing When Writing

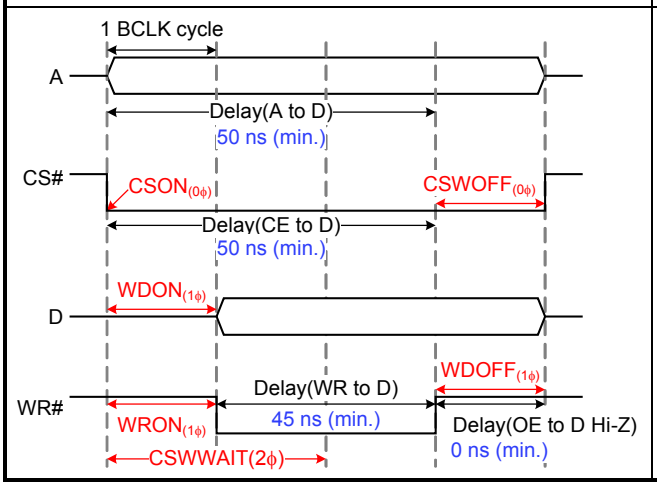
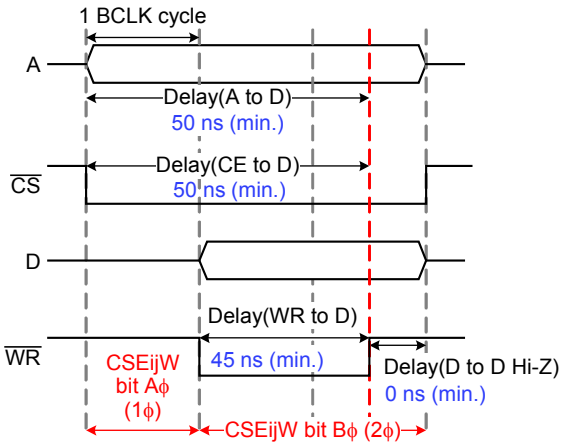
Table 1.4 Differences in the Bus Timing Settings When Writing

RX (RX210)		M16C (M16C/65C)	
			
CSON	Sets the number of wait cycles to be inserted before asserting the CSn# signal	CSEijW bit (Aϕ + Bϕ) (i = 0 to 3, j = 0, 1) Aϕ sets the number of cycles from the start of the bus access to the falling edge of the $\overline{WR}$ signal. Bϕ sets the number of cycles from falling edge of the $\overline{WR}$ signal to the rising edge.	
WDON	Sets the number of wait cycles to be inserted before outputting write data		
WRON	Sets the number of wait cycles to be inserted before asserting the WRn# signal		
WDOFF	Sets the number of cycles from negating the WRn# signal during a write access, to write data output completion		
CSWWAIT	Sets the number of cycles to be inserted in the first access of the normal read cycle		
CSWOFF	Sets the number of cycles from negating the WRn# signal during a write access, to negating the CSn# signal		
N/A		EWR	Sets the number of recovery cycles according to the number of needed idle cycles

When writing to the connected external memory has the following attributes, values set to the M16C and RX registers are shown in Table 1.5.

- Delay(A to D) = 50 ns (min.)
- Delay(CE to D) = 50 ns (min.)
- Delay(WR to D) = 45 ns (min.)
- Delay(D to D Hi-Z) = 0 ns (min.)

Table 1.5 Differences in the External Bus Register Setting (When Writing and BCLK = 16 MHz)

<table>
<tr><th colspan="2">RX (RX210)</th><th colspan="2">M16C (M16C/65C)</th></tr>
<tr><td>CSON</td><td>CS0WCR2.BIT.CSON = 0; *1</td><td colspan="2" rowspan="6">CSEijW bit (Aϕ + Bϕ) *3 (i = 0 to 3, j = 0, 1)
CSE = 0x01; /* 2 waits (1ϕ + 2ϕ) */</td></tr>
<tr><td>WDON</td><td>CS0WCR2.BIT.WDON = 1; *1</td></tr>
<tr><td>WRON</td><td>CS0WCR2.BIT.WRON = 1; *1</td></tr>
<tr><td>WDOFF</td><td>CS0WCR2.BIT.WDOFF = 1; *2</td></tr>
<tr><td>CSWWAIT</td><td>CS0WCR1.BIT.CSWWAIT = 2; *1</td></tr>
<tr><td>CSWOFF</td><td>CS0WCR2.BIT.CSWOFF = 1; *2</td></tr>
<tr><td colspan="2">N/A</td><td>EWR</td><td>EWR = 0x00; / * No recovery cycles */</td></tr>
<tr><td colspan="2"> 
</td><td colspan="2"> 
</td></tr>
</table>

Note 1. Satisfy the following conditions: 1 ≤ CSnWCR2.WDON bit ≤ CSnWCR2.WRON bit ≤ CSnWCR1.CSWWAIT bit, and CSnWCR2.CSON bit ≤ CSnWCR2.WRON bit ≤ CSnWCR1.CSWWAIT bit.

Note 2. Satisfy the following condition: CSnWCR2.WDOFF bit ≤ CSnWCR2.CSWOFF bit.

Note 3. Select from 1ϕ + 1ϕ, 1ϕ + 2ϕ, 1ϕ + 3ϕ, 2ϕ + 3ϕ, 2ϕ + 4ϕ, 3ϕ + 4ϕ, or 4ϕ + 5ϕ.

1.2.3 Recovery Cycles

The differences in the recovery cycle specifications are that in the M16C Family, recovery cycles are inserted before CS is negated, while in the RX Family, recovery cycles are inserted after CS is negated.

In the RX Family, 1 to 15 recovery cycles can be inserted. The condition for inserting a recovery cycle can be selected from the following:

- After a read access, the same external bus area is read accessed.
- After a read access, the same external bus area is write accessed.
- After a read access, a different external bus area is read accessed.
- After a read access, a different external bus area is write accessed.
- After a write access, the same external bus area is read accessed.
- After a write access, the same external bus area is write accessed.
- After a write access, a different external bus area is read accessed.
- After a write access, a different external bus area is write accessed

In the M16C Family, 1 to 3 recovery cycles can be inserted. When a recovery cycle is inserted, output for the data bus, address bus, and CS is extended.

2. Differences in Operating Modes

Table 2.1 lists the Differences in the Functions of Operating Modes Used by the External Memory and Internal Memory, and Table 2.2 lists the Differences in the Functions of Operating Modes Used Only by the External Memory.

Table 2.1 Differences in the Functions of Operating Modes That Use the External Memory and Internal Memory

Item	RX (RX210) On-chip ROM Enabled Extended Mode	M16C (M16C/65C) Memory Expansion Mode
Access area	I/O registers, on-chip RAM, on-chip ROM, external areas	SFRs, internal RAM, internal ROM, external areas
External memory area	0500 0000h to 07FF FFFFh (CS1, CS2, CS3)	Addresses 04000h to CFFFFh

Table 2.2 Differences in the Functions of Operating Modes That Use Only the External Memory

Item	RX (RX210) On-Chip ROM Disabled Extended Mode	M16C (M16C/65C) Microprocessor Mode
Access area	I/O registers, on-chip RAM, on-chip ROM (only enabled on start-up), external areas	SFRs, internal RAM, external areas
External memory area	0500 0000h to 07FF FFFFh (CS1, CS2, CS3) FF00 0000h to FFFF FFFFh (CS0)	Addresses 04000h to CFFFFh

3. Peripheral Functions Used

Table 3.1 lists the Operating Modes Used With the External Bus.

Table 3.1 Operating Modes Used With the External Bus

No.	RX Mode	M16C Mode	Operating Example	Description
1	On-chip ROM enabled extended mode	Memory expansion mode	Read the data for the external memory from program in the on-chip ROM.	Section 3.2
2	On-chip ROM disabled extended mode	Microprocessor mode	Read the data for the external memory from program in the external ROM.	Section 3.3

3.1 Device Operating Modes

The RX Family has three operating modes – single-chip mode, on-chip ROM enabled extended mode, and on-chip ROM disabled extended mode. Set the user program to enter each mode.

Table 3.2 Entering Modes in the RX Family

Mode	Program Setting
Single-chip mode	N/A
On-chip ROM enabled extended mode	Set the SYSCR0.ROME bit to 0, and the SYSCR0.EXBE bit to 1
On-chip ROM disabled extended mode	Set the SYSCR0.ROME bit to 1, and the SYSCR0.EXBE bit to 1 *2

Note 1. Set the bus width in the CSn control register (CSnCR register).
Note 2. Set this register in an area other than the external memory and ROM.

The RX Family's on-chip ROM disabled extended mode differs from the M16C Family's processor mode, and requires a program to transition to the mode on the on-chip ROM.

The M16C Family has three processor modes – single-chip mode, memory expansion mode, and microprocessor mode. The pin and program must be set to enter each processor mode.

Table 3.3 Entering Modes in the M16C Family *1

Mode	Mode Pin (CNVSS)	Program Setting
Single-chip mode	Low	N/A (when the MCU starts-up, bits PM01 and PM00 become 00b)
Memory expansion mode	Low	Set bits PM01 and PM00 to 01b *2
Microprocessor mode	High	N/A *3 (when the MCU starts-up, bits PM01 and PM00 become 11b)

Note 1. The bus width is set by the BYTE pin. Configure settings so the bus width is 8 bits when the BYTE pin is high, and 16 bits when the BYTE pin is low.
Note 2. The bus must be set. Configure settings in accordance with the external memory.
Note 3. The bus does not need to be set. Configure the bus when using a setting other than 1ϕ + 1ϕ for reading the external memory.

3.2 Differences in the Setting Procedure When Using the Program in the On-chip ROM to Read Data From the External Memory

Table 3.4 lists the Differences in Executing the Program in On-chip ROM and Reading Data From the External Memory (16-bit Bus Width).

Table 3.4 Differences in Executing the Program in On-chip ROM and Reading Data From the External Memory (16-bit Bus Width)

Step		RX Family (RX210)	M16C Family (M16C/65C)
1	Set pins	Input a high signal to the MD pin	Input a low signal to the CNVSS pin Input a low signal to the BYTE pin
2	Exit the reset state	Change the signal to the RESET pin from low to high	Change the signal to the RESET pin from low to high
3	Set clocks	Set the frequency of the operating clock.	
4	Set write access mode, external waits, and page access	BSC.CS1MOD.WORD = 0x0000;	N/A (no processing)
5	Set the bus timing (write)	BSC.CS1WCR1.BIT.CSWWAIT = 7; BSC.CS1WCR2.BIT.CSWOFF = 0; BSC.CS1WCR2.BIT.WDON = 0; BSC.CS1WCR2.BIT.WRON = 0; BSC.CS1WCR2.BIT.WDOFF = 0;	CSE = 0x00; EWC = 0x00;
6	Set the bus timing (read)	BSC.CS1WCR1.BIT.CSRWAIT = 7; BSC.CS1WCR2.BIT.CSROFF = 7; BSC.CS1WCR2.BIT.CSON = 0; BSC.CS1WCR2.BIT.RDON = 0;	
7	Set the number of recovery cycles	BSC.CS1REC.BIT.RRCV = 0; BSC.CS1REC.BIT.WRCV = 0; BSC.CSRECEN.WORD = 0x0000;	EWR = 0x00;
8	Set the bus pins	MPC.PFCSE.BIT.CS1E = 1; MPC.PFAOE0.BYTE = 0xFF; MPC.PFAOE1.BYTE = 0x0F; MPC.PFBCR0.BYTE = 0x11;	CSR = 0x01;
9	Select the bus width, endian, and bus mode, and start operation	BSC.CS1CR.WORD = 0x0001;	N/A (no processing)

10	Switch the operating mode	SYSTEM.PRCR.WORD = 0xA502;
		SYSTEM.SYSCR0.WORD = 0x5A03;
		SYSTEM.PRCR.WORD = 0xA500;
			prcr = 0x02;
			pm0 = 0x01;
			prcr = 0x00;

Table 3.5 lists the Differences in Executing the Program in On-chip ROM and Reading Data From the External Memory (8-bit Bus Width).

Table 3.5 Differences in Executing the Program in On-chip ROM and Reading Data From the External Memory (8-bit Bus Width)

Step		RX Family (RX210)	M16C Family (M16C/65C)
1	Set pins	Input a high signal to the MD pin	Input a low signal to the CNVSS pin Input a high signal to the BYTE pin
2	Exit the reset state	Change the signal to the RESET pin from low to high	Change the signal to the RESET pin from low to high
3	Set clocks	Set the frequency of the operating clock.	
4	Set write access mode, external waits, and page access	BSC.CS1MOD.WORD = 0x0000;	N/A (no processing)
5	Set the bus timing (write)	BSC.CS1WCR1.BIT.CSWWAIT = 7; BSC.CS1WCR2.BIT.CSWOFF = 0; BSC.CS1WCR2.BIT.WDON = 0; BSC.CS1WCR2.BIT.WRON = 0; BSC.CS1WCR2.BIT.WDOFF = 0;	CSE = 0x00; EWC = 0x00;
6	Set the bus timing (read)	BSC.CS1WCR1.BIT.CSRWAIT = 7; BSC.CS1WCR2.BIT.CSROFF = 7; BSC.CS1WCR2.BIT.CSON = 0; BSC.CS1WCR2.BIT.RDON = 0;	
7	Set the number of recovery cycles	BSC.CS1REC.BIT.RRCV = 0; BSC.CS1REC.BIT.WRCV = 0; BSC.CSRECEN.WORD = 0x0000;	EWR = 0x00;
8	Set the bus pins	MPC.PFCSE.BIT.CS1E = 1; MPC.PFAOE0.BYTE = 0xFF; MPC.PFAOE1.BYTE = 0x0F; MPC.PFBCR0.BYTE = 0x11;	CSR = 0x01;
9	Select the bus width, endian, and bus mode, and start operation	BSC.CS1CR.WORD = 0x0021;	N/A (no processing)

10	Switch the operating mode	SYSTEM.PRCR.WORD = 0xA503;
		SYSTEM.SYSCR0.WORD = 0x5A03;
		SYSTEM.PRCR.WORD = 0xA500;
			prcr = 0x02;
			pm0 = 0x01;
			prcr = 0x00;

3.3 Differences in the Setting Procedure When Using the Program in the External Memory to Read Data From the External Memory

Table 3.6 lists the Differences in Executing the Program in the External Memory (16-bit Bus Width) Without Using the On-chip ROM.

Table 3.6 Differences in Executing the Program in the External Memory (16-bit Bus Width) Without Using the On-chip ROM

Step		RX Family (RX210)	M16C Family (M16C/65C)
1	Set pins	Input a high signal to the MD pin	Input a high signal to the CNVSS pin Input a low signal to the BYTE pin
2	Exit the reset state	Change the signal to the RESET pin from low to high	Change the signal to the RESET pin from low to high
3	Set write access mode, external waits, and page access	BSC.CS1MOD.WORD = 0x0000;	N/A (no processing)
4	Set the bus timing (write)	BSC.CS0WCR1.BIT.CSWWAIT = 7; BSC.CS0WCR2.BIT.CSWOFF = 0; BSC.CS0WCR2.BIT.WDON = 0; BSC.CS0WCR2.BIT.WRON = 0; BSC.CS0WCR2.BIT.WDOFF = 0;	
5	Set the bus timing (read)	BSC.CS0WCR1.BIT.CSRWAIT = 7; BSC.CS0WCR2.BIT.CSROFF = 7; BSC.CS0WCR2.BIT.CSON = 0; BSC.CS0WCR2.BIT.RDON = 0;	
6	Set the number of recovery cycles	BSC.CS0REC.BIT.RRCV = 0; BSC.CS0REC.BIT.WRCV = 0; BSC.CSRECEN.WORD = 0x0000;	
7	Set the bus pins	MPC.PFCSE.BIT.CS0E = 1; MPC.PFAOE0.BYTE = 0xFF; MPC.PFAOE1.BYTE = 0x0F; MPC.PFBCR0.BYTE = 0x11;	
8	Select the bus width, endian, and bus mode, and start operation	BSC.CS0CR.WORD = 0x0001;	
9	Execute the program on the RAM	Transfer the program to be executed in steps 10 and 11 to the RAM. After transferring the program to the RAM, set the program counter in step 9.	
10	Switch the operating mode	SYSTEM.PRCR.WORD = 0xA502; SYSTEM.SYSCR0.WORD = 0x5A02; SYSTEM.PRCR.WORD = 0xA500;	
11	Jump to the program in the external memory that is to be executed first	Jump to the predetermined external memory address	Read the reset vector (FFFFCh to FFFFEh) from the external memory, and jump to the specified address
—	Set the bus to be used when accessing the external memory	Access the CS0 area using the specified number of cycles	Access the CS0 area with 1 wait (1ϕ + 1ϕ)
—	Set clocks	Set the frequency of the operating clock.	

Table 3.7 lists the Differences in Executing the Program in the External Memory (8-bit Bus Width) Without Using the On-chip ROM.

Table 3.7 Differences in Executing the Program in the External Memory (8-bit Bus Width) Without Using the On-chip ROM

Step		RX Family (RX210)	M16C Family (M16C/65C)
1	Set pins	Input a high signal to the MD pin	Input a high signal to the CNVSS pin Input a high signal to the BYTE pin
2	Exit the reset state	Change the signal to the RESET pin from low to high	Change the signal to the RESET pin from low to high
3	Set write access mode, external waits, and page access	BSC.CS1MOD.WORD = 0x0000;	N/A (no processing)
4	Set the bus timing (write)	BSC.CS0WCR1.BIT.CSWWAIT = 7; BSC.CS0WCR2.BIT.CSWOFF = 0; BSC.CS0WCR2.BIT.WDON = 0; BSC.CS0WCR2.BIT.WRON = 0; BSC.CS0WCR2.BIT.WDOFF = 0;	
5	Set the bus timing (read)	BSC.CS0WCR1.BIT.CSRWAIT = 7; BSC.CS0WCR2.BIT.CSROFF = 7; BSC.CS0WCR2.BIT.CSON = 0; BSC.CS0WCR2.BIT.RDON = 0;	
6	Set the number of recovery cycles	BSC.CS0REC.BIT.RRCV = 0; BSC.CS0REC.BIT.WRCV = 0; BSC.CSRECEN.WORD = 0x0000;	
7	Set the bus pins	MPC.PFCSE.BIT.CS0E = 1; MPC.PFAOE0.BYTE = 0xFF; MPC.PFAOE1.BYTE = 0x0F; MPC.PFBCR0.BYTE = 0x11;	
8	Select the bus width, endian, and bus mode, and start operation	BSC.CS0CR.WORD = 0x0021;	
9	Execute the program on the RAM	Transfer the program to be executed in steps 10 and 11 to the RAM. Then, set the program counter to the address for step 10 of the transferred program.	
10	Switch the operating mode	SYSTEM.PRCR.WORD = 0xA502; SYSTEM.SYSCR0.WORD = 0x5A02; SYSTEM.PRCR.WORD = 0xA500;	
11	Jump to the program in the external memory that is to be executed first	Jump to the predetermined external memory address	Read the reset vector (FFFFCh to FFFFEh) from the external memory, and jump to the specified address
—	Set the bus to be used when accessing the external memory	Access the CS0 area using the specified number of cycles	Access the CS0 area with 1 wait (1ϕ + 1ϕ)
—	Set clocks	Set the frequency of the operating clock.	

4. Appendix

4.1 Points on Migrating From the M16C Family to the RX Family

This chapter explains points on migrating from the M16C Family to the RX Family.

4.1.1 Interrupts

For the RX Family, when an interrupt request is received while all of the following conditions are met, the interrupt occurs.

- The I flag (PSW.I bit) is 1.
- Registers IER and IPR in the ICU are set to interrupt enabled.
- The interrupt request is enabled in the interrupt request enable bit for peripheral functions.

Table 4.1 lists a Comparison of Conditions for Interrupt Generation.

Table 4.1 Comparison of Conditions for Interrupt Generation

Item	RX210	M16C/65C
I flag	When the I flag is set to 1 (enabled), the maskable interrupt request can be accepted.	
Interrupt request flag	When an interrupt request is generated by a peripheral function, the interrupt request flag becomes 1 (interrupt requested).	
Interrupt priority level	Selected by setting the IPR[3:0] bits.	Selected by setting bits ILVL2 to ILVL0.
Interrupt request enable	Specified by setting the IER register.	N/A
Interrupt enable for peripheral functions	Interrupts can be enabled or disabled in each peripheral function.	N/A

For more information, refer to sections Interrupt Controller (ICU), CPU, and sections for other peripheral functions used in the User's Manual: Hardware.

4.1.2 I/O Ports

In the RX Family, the MPC must be configured in order to assign I/O signals from peripheral functions to pins. Before controlling the I/O pins in the RX Family, the following two items must be set.

- In the MPC.PFS register, select the peripheral functions that are assigned to the pins.
- In the PORTn.PMR register, select the pin function from a general I/O port or peripheral function.

Table 4.2 lists a Comparison of I/O Settings for Peripheral Function Pins.

Table 4.2 Comparison of I/O Settings for Peripheral Function Pins

Function	RX210	M16C/65C
Select the pin function	With the PFS register, I/O ports for peripheral functions can be assigned by selecting from multiple pins.	These are not available in the M16C Family. *1 When a mode is set for a peripheral function, appropriate pins are assigned as I/O pins for the peripheral function.
Switch between general I/O port and peripheral function	With the PMR register, the corresponding pin function can be selected as a general I/O port or a peripheral function.	

Note 1. Register for similar functions are available in the M32C Group and R32C Group.

For more information, refer to the Multi-Function Pin Controller (MPC) and I/O port sections in the User's Manual: Hardware.

4.1.3 Module Stop Function

The RX Family has the ability to stop each peripheral module individually. By transitioning unused peripheral modules to the module stop state, power consumption can be reduced. After a reset is released, all modules (with a few exceptions) are in the module stop state. Registers for modules in the module stop state cannot be written to or read.

For more information, refer to the Low Power Consumption section in the User's Manual: Hardware.

4.2 I/O Register Macros

Macro definitions listed in Table 4.3 can be found in the RX I/O register definitions (iodefine.h).
The readability of programs can be achieved with these macro definitions.
Table 4.3 lists examples of macros.

Table 4.3 Using Macros

Macro	Usage Example
IR("module name", "bit name")	**IR(MTU0,TGIA0)** = 0 ; The IR bit corresponding to MTU0.TGIA0 is cleared to 0 (no interrupt request is generated).
DTCE("module name", "bit name")	**DTCE (MTU0, TGIA0)** = 1 ; The DTCE bit corresponding to MTU0.TGIA0 is set to 1 (DTC activation is enabled).
IEN("module name", "bit name")	**IEN(MTU0, TGIA0)** = 1 ; The IEN bit corresponding to MTU0.TGIA0 is set to 1 (interrupt request enabled).
IPR("module name", "bit name")	**IPR(MTU0, TGIA0)** = 0x02 ; The IPR[3:0] bits corresponding to MTU0.TGIA0 are set to 0010b (interrupt priority level 2).
MSTP("module name")	**MSTP(MTU)** = 0 ; The MTU0 Module Stop bit is set to 0 (module stop state is canceled).
VECT("module name", "bit name")	#pragma interrupt (Excep_MTU0_TGIA0 (vect=**VECT(MTU0, TGIA0)**) The interrupt function is declared for the corresponding MTU0.TGIA0.

4.3 Intrinsic Functions

The RX Family has intrinsic functions for setting control registers and special instructions. When using intrinsic functions, include machine.h.

Table 4.4 lists examples of Descriptions of Special Instructions and Control Register Settings.

Table 4.4 Differences in the Descriptions of Special Instructions and Control Register Settings

Item	Description	
	RX	M16C
Set the I flag to 1	setpsw_i (); *1	asm("fset i");
Set the I flag to 0	clrpsw_i (); *1	asm("fclr i");
Expanded into the WAIT instruction	wait(); *1	asm("wait");
Expanded into the NOP instruction	nop(); *1	asm("nop");

Note 1. "machine.h" must be included.

5. Reference Documents

User's Manual: Hardware

RX210 Group User's Manual: Hardware Rev.1.50 (R01UH0037EJ)
M16C/65C Group User's Manual: Hardware Rev.1.10 (R01UH0093)
Refer to the corresponding User's Manual: Hardware when using products other than the RX210 Group and M16C/65C Group.
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family C/C++ Compiler Package V.1.01 User's Manual Rev.1.00 (R20UT0570EJ)
M16C Series, R8C Family C Compiler Package V5.45
C Compiler User's Manual Rev.3.00
The latest versions can be downloaded from the Renesas Electronics website.

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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