

# RX Family

R01AN1411EJ0101

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## Hardware Design Guide

### Abstract

This document describes notes on board design using the RX Family.

### Products

RX Family

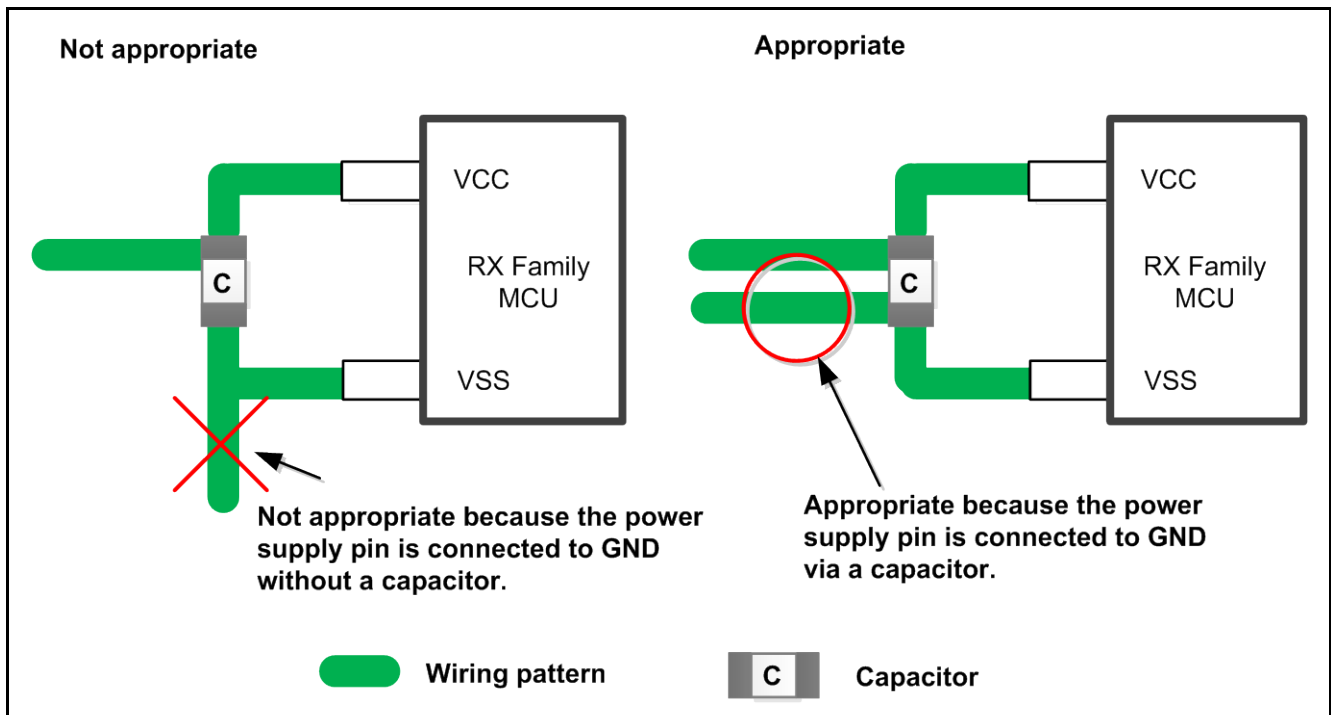
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## 1. Specifications

### 1.1 Power Supply Pins

Connect power supply pins to GND via a bypass capacitor (decoupling capacitor). Use a capacitor with good frequency characteristics, such as a ceramic capacitor. The wiring length between each power supply pin and a capacitor must be equal and as short as possible. In addition, pair the appropriate pins. For example, the VCC pin, AVCC pin, and VREFH pin must be paired with the VSS pin, AVSS pin, and VREFL pin, respectively. Refer to User's Manual: Hardware of the product used for more details. The pattern for power supply pins must be wider than patterns for other signal lines and must be connected to power supply and GND via a bypass capacitor. Figure 1.1 shows a Connection Example of a Power Supply Pin and Bypass Capacitor.



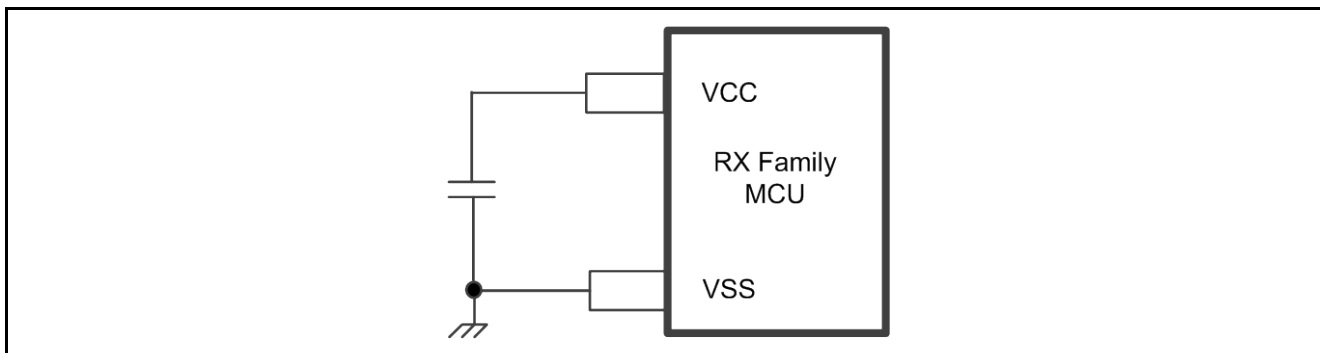
**Figure 1.1 Connection Example of a Power Supply Pin and Bypass Capacitor**

Refer to the application notes below for the analog power-supply pins. The latest versions and documents for new products can be downloaded from the Renesas Electronics website.

- RX610 Group Notes on Analog Power Supply Printed Circuit Board Patterns (R01AN0271EJ)
- RX62N Group, RX621 Group Notes on Analog Power Supply Printed Circuit Board Patterns (R01AN0269EJ)
- RX62T Group Notes on Analog Power Supply Printed Circuit Board Patterns (R01AN0638EJ)

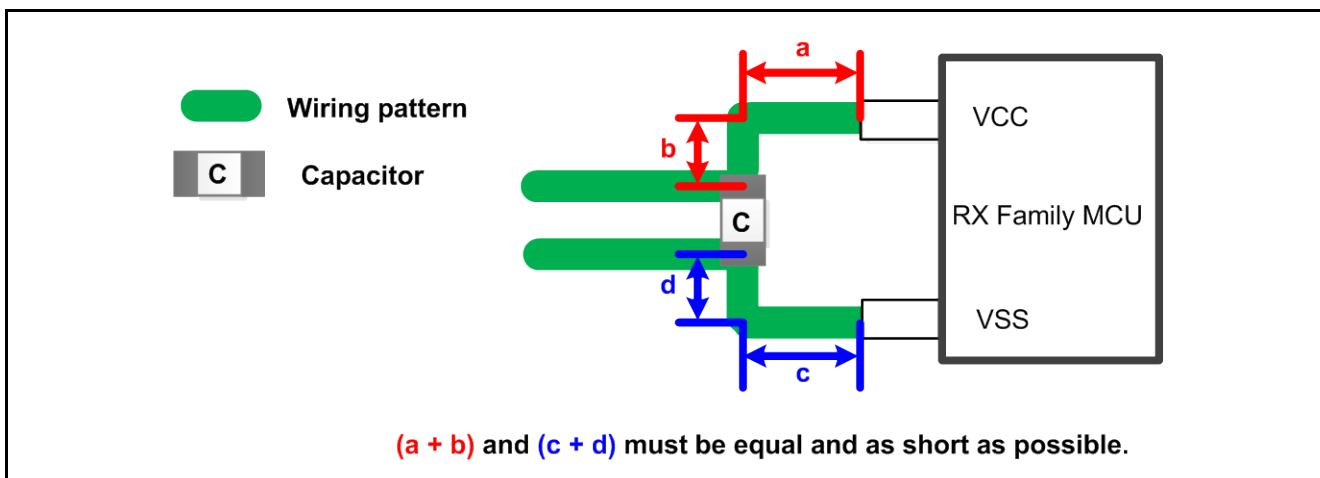
Reason: A bypass capacitor connected to power supply pins is placed for bypassing noise to GND during MCU operation.

Figure 1.2 shows a Circuit Structure Example for Power Supply Pins.



**Figure 1.2 Circuit Structure Example for Power Supply Pins**

Figure 1.3 shows a Pattern Example for Power Supply Pins.

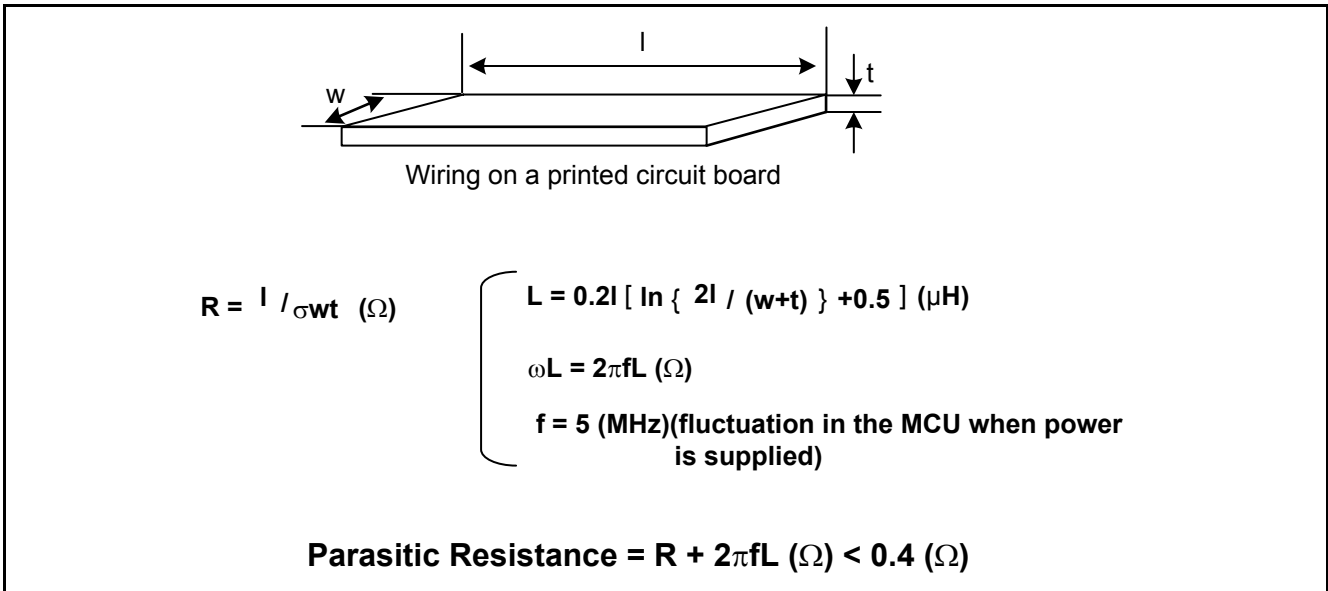


**Figure 1.3 Pattern Example for Power Supply Pins**

### 1.2 VCL Pin

Connect the VCL pin to GND via a capacitor with a capacity described in User’s Manual of the device used. The wiring length between the VCL pin and the capacitor must be 10 mm or less (5 mm or less if possible). Note that GND wiring varies depending on the number of board layers. Sections 1.2.1, 1.2.2, and 1.2.3 describe examples for one layer, two layers, and four or more layers, respectively.

Reason: If the wiring length between the VCL pin and capacitor is longer than 10 mm, the parasitic resistance increases, which can cause noise. When the wiring length is longer than 10 mm, wiring must be designed so that the parasitic resistance is less than 0.4 Ω. Figure 1.4 shows a Formula for Calculating the Parasitic Resistance.



**Figure 1.4 Formula for Calculating the Parasitic Resistance**

The following example uses the formula shown in Figure 1.4 to calculate the parasitic resistance.

Example

Wiring length (l): 0.01 m (10 mm)

Wiring width (w): 0.00015 m (0.15 mm)

Wiring thickness (t): 0.000035 (0.035 mm)

Resistivity of copper ( $\rho = 1 / \sigma$ ): 0.0000000169 Ω·m

$$\begin{aligned} \text{Parasitic resistance} &= R + 2\pi f L \\ &= (l / \sigma w t) + 2 \times \pi \times 5 \times (0.2 \times l ( \log_e ( 2 \times l / ( w + t ) ) + 0.5 )) \\ &= 0.03219 + 2 \times 3.1415 \times 5 \times 0.01036 \\ &\approx 0.35764 \ (\Omega) \end{aligned}$$

Figure 1.5 shows a Circuit Structure Example for the VCL Pin.

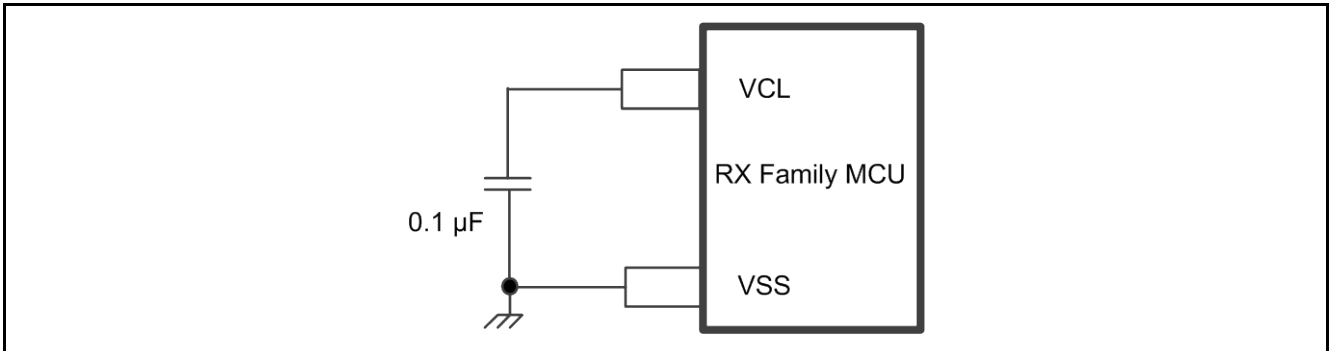


Figure 1.5 Circuit Structure Example for the VCL Pin

1.2.1 One-Layer Board or Multi-Layer Board with No GND Layer

Widen the GND pattern width.

Figure 1.6 shows a Pattern Example for the VCL Pin on the One-Layer Board.

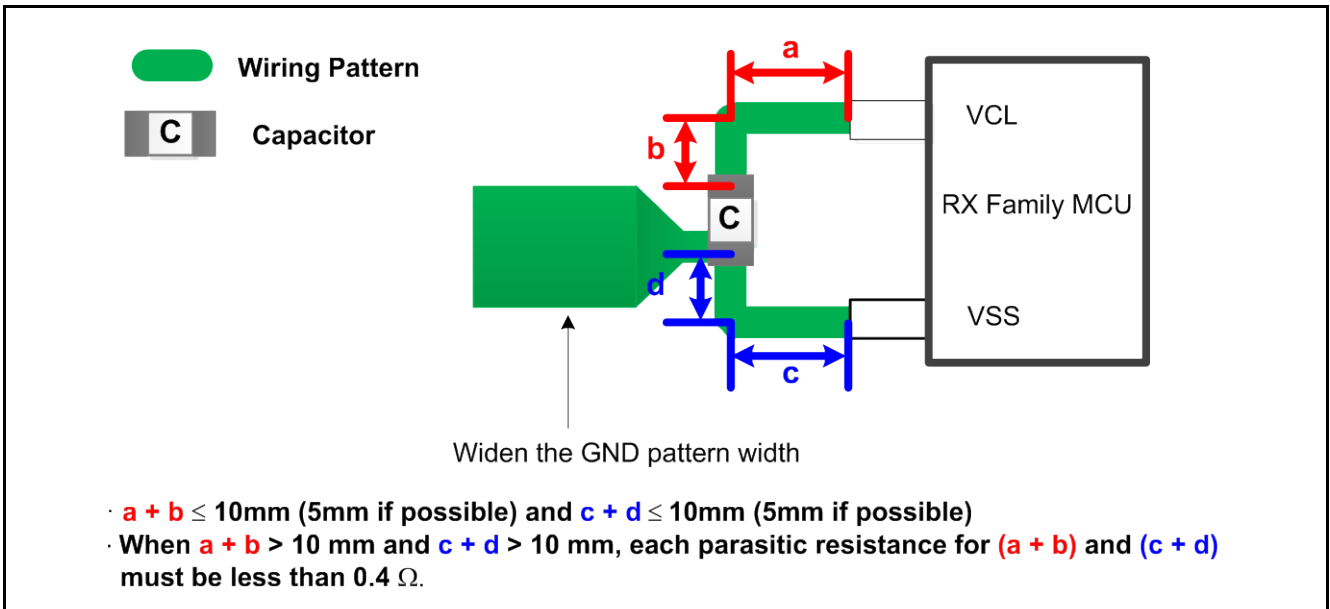


Figure 1.6 Pattern Example for the VCL Pin on the One-Layer Board

### 1.2.2 Two-Layer Board

Place a GND pattern on the back side of the part between the VCL pin and capacitor.

When the GND pattern on the back side is connected, connect via at least four through holes.

When the GND pattern on the back side is not connected, widen the GND pattern width on the front.

Figure 1.7 shows a Pattern Example for the VCL Pin on the Two-Layer Board.

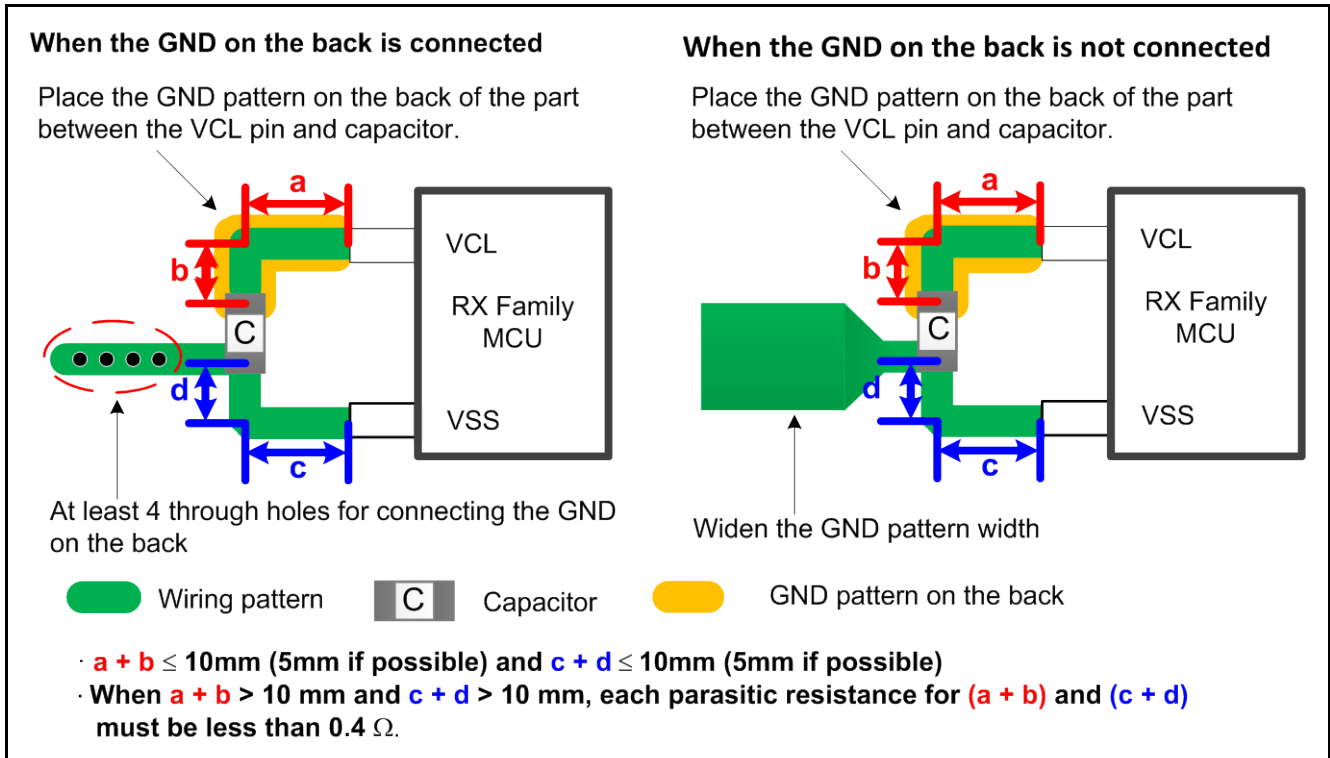


Figure 1.7 Pattern Example for the VCL Pin on the Two-Layer Board

### 1.2.3 Board With Four or More Layers

Connect to the GND layer via at least four through holes.

Figure 1.8 shows a Pattern Example for the VCL Pin on the Board with Four or More Layers.

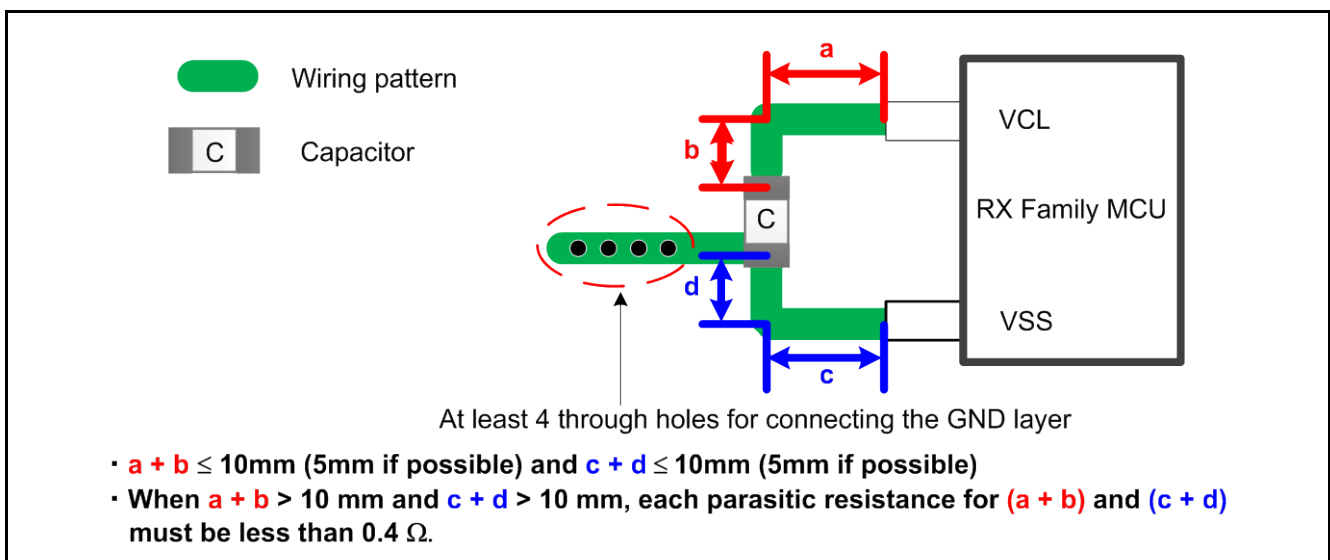


Figure 1.8 Pattern Example for the VCL Pin on the Board with Four or More Layers

### 1.3 Reset Pin

When directly connecting the reset pin to the reset IC, place the reset IC as close as possible. Noise also can be reduced by inserting a low-pass filter. Shield the pattern for the reset pin with the GND pattern. Do not place the pattern for the reset pin in parallel with other patterns where a large current flows or the level changes frequently.

Reason: The pulse width input to the reset pin is specified in the timing requirement. If the noise input to the reset pin has a shorter width than the specified width, the reset is released before the MCU initialization is completed, which may cause program runaway.

Figure 1.9 shows a Circuit Structure Example for the Reset Pin. Figure 1.10 shows a Pattern Example for the Reset Pin for a Multi-Layer Board.

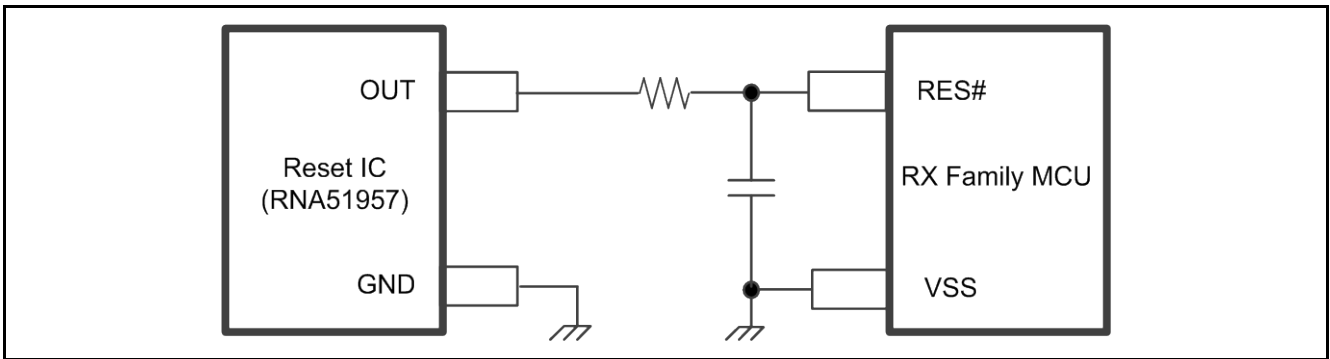


Figure 1.9 Circuit Structure Example for the Reset Pin

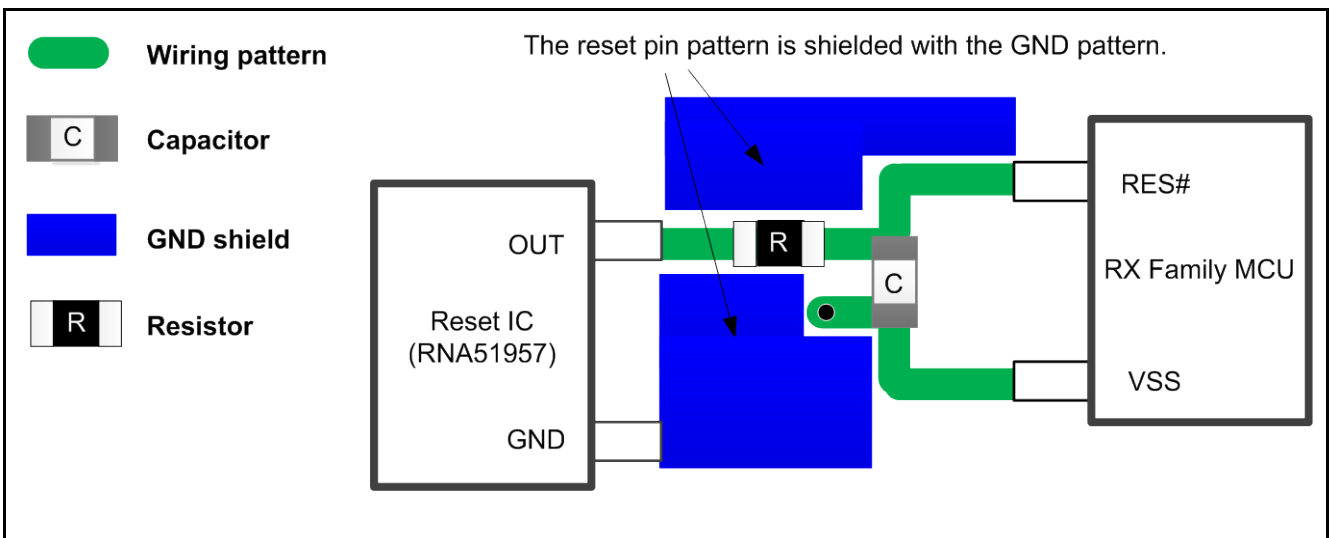


Figure 1.10 Pattern Example for the Reset Pin for a Multi-Layer Board



### 1.4 Clock I/O Pins

Wiring for clock I/O pins (EXATL, XTAL, XCIN, XCOU) should be as short as possible, including the peripheral circuits. Shield the pattern for the clock I/O pins with the GND pattern. Do not place the pattern for the clock I/O pins in parallel with or across other patterns where a large current flows or the level changes frequently. In addition, do not place the GND pattern and power supply pattern in layers under the external circuit where a crystal is placed.

Refer to the application notes below for the low CL crystal. The latest versions and documents for new products can be downloaded from the Renesas Electronics website.

- RX210, RX21A, and RX220 Groups Design Guide for Low CL Sub-Clock Circuits (R01AN1012EJ)
- RX63N/RX631 Groups Design Guide for Low CL Sub-Clock Circuits (R01AN1187EJ)

Reason: If noise is applied to the clock I/O pin, the clock waveform is distorted, which may cause the MCU malfunction and runaway. In addition, if there is a potential difference between the MCU VSS level and crystal VSS level due to noise, accurate clock cannot be input to the MCU.

Figure 1.11 shows a Circuit Structure Example for the Clock I/O Pin. Figure 1.12 shows a Pattern Example for the Clock I/O Pin.

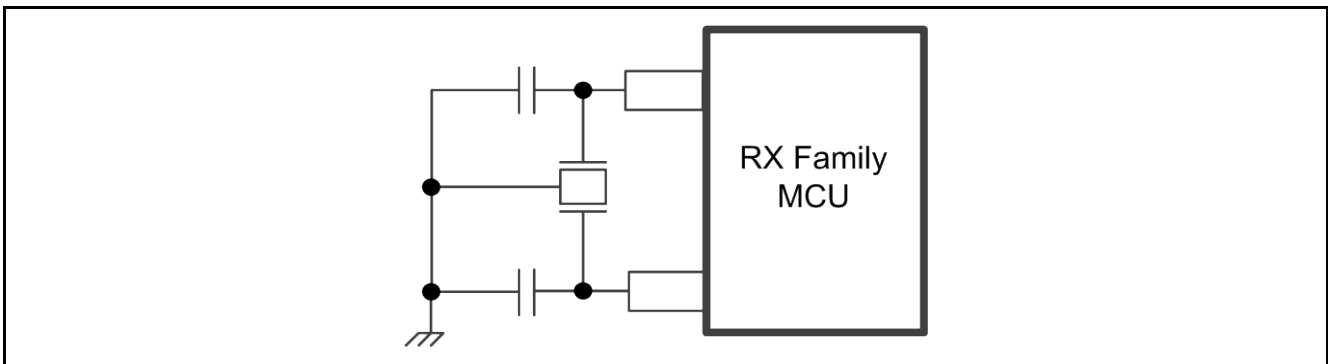


Figure 1.11 Circuit Structure Example for the Clock I/O Pin

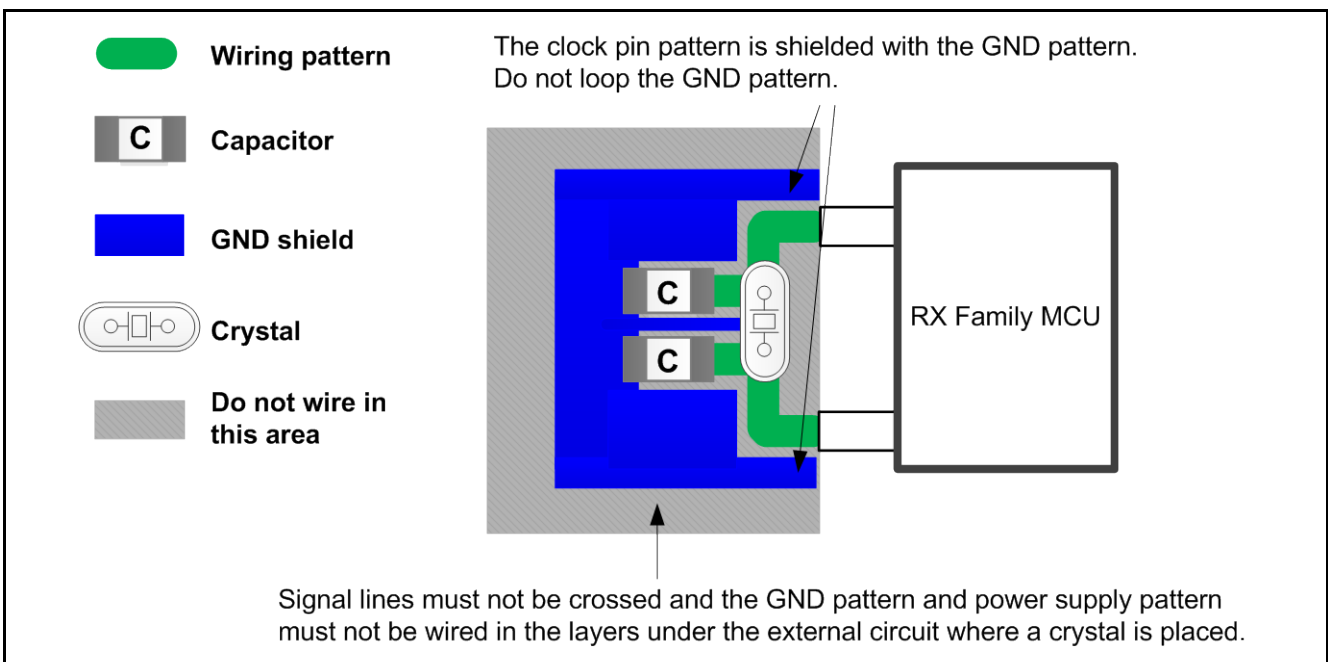


Figure 1.12 Pattern Example for the Clock I/O Pin

### 1.5 Analog Input Pins

Connect an analog input pin to GND via a capacitor. Wiring between the analog input pin and capacitor and wiring between the AVSS pin and capacitor must be equal and as short as possible. Shield the pattern for the analog input pins with the GND pattern. Do not place the pattern for the analog input pins in parallel with or across other patterns where a large current flows or the level changes frequently.

Reason: If noise is applied to the analog input pin, the waveform is distorted, and the accuracy of the A/D converter is decreased. An external capacitor is used to reduce noise.

An external capacitor is also used to achieve high-speed conversion. An adequate electrical charge must be stored in the external capacitor before conversion starts in order to reduce the signal source impedance of the input capacitor in the sample and hold circuit. Note that, if the voltage level of the analog input pin changes (e.g. in continuous scan mode) and the external capacitor charge is updated, an adequate electrical charge cannot be stored. In this case, do not connect an external capacitor.

Figure 1.13 shows a Circuit Structure Example for the Analog Input Pin. Figure 1.14 shows a Pattern Example for the Analog Input Pin.

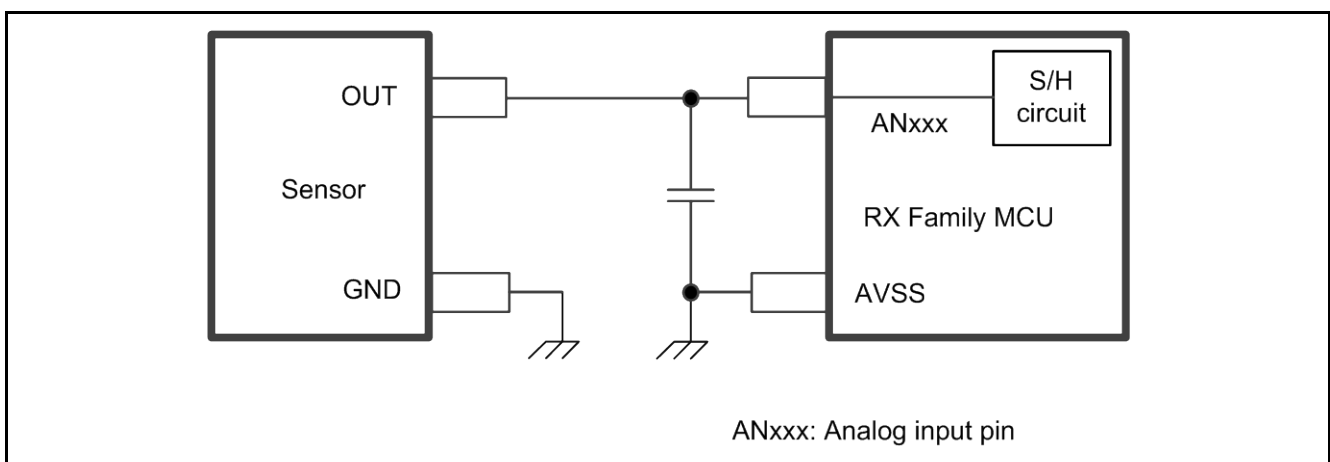


Figure 1.13 Circuit Structure Example for the Analog Input Pin

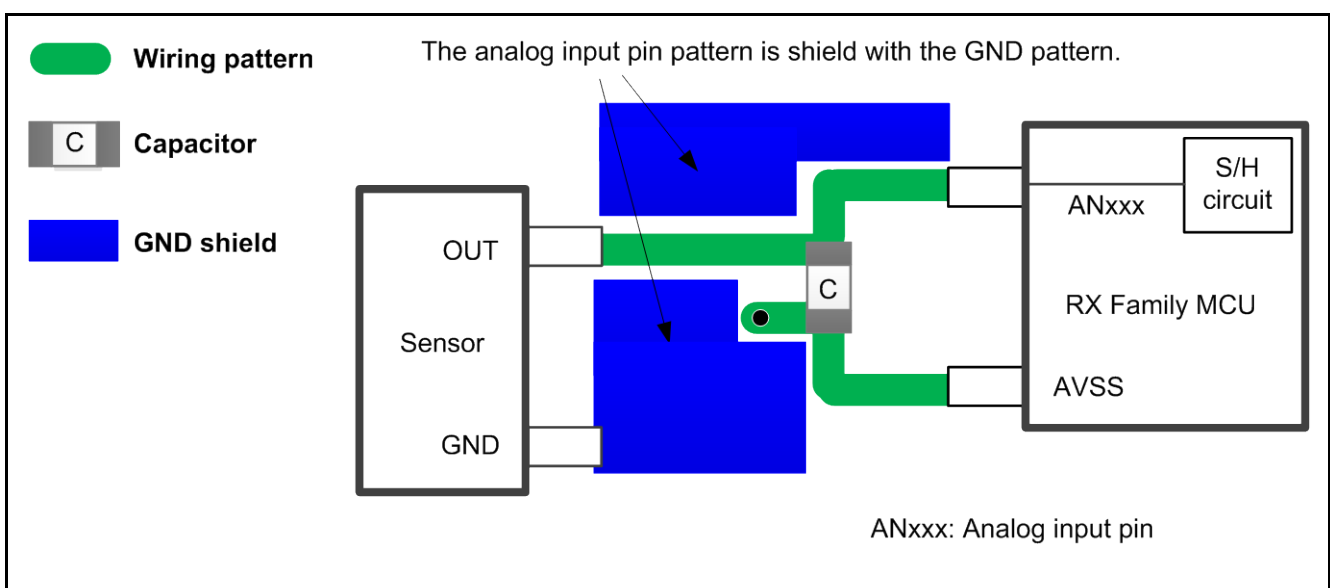


Figure 1.14 Pattern Example for the Analog Input Pin

## 1.6 Signal Pins Where a Large Current Flows

When a large current exceeding the current range supported by the MCU flows in a signal line, place the signal line as far from the MCU (especially a crystal) as possible. In addition, do not place the pattern of a signal pin where a large current flows in parallel with or across patterns of the reset pin, clock I/O pin, and analog input pins.

Reason: In a system using the MCU, there are signal lines that control a motor, LEDs, a thermal head, etc. If a large current flows in these signal lines, mutual inductance causes noise.

## 1.7 Signal Pins Where the Level Changes Frequently

Place a signal line where the level changes frequently as far from a crystal and the wiring pattern of the crystal as possible. Do not place a long signal line where the level changes frequently in parallel with or across the clock signal lines or other lines that are easily influenced by noise.

Reason: Signal lines where the level changes frequently can easily influence other signal lines when the level changes at the rising or falling edge. Especially when the signal lines are placed across the clock signal lines, the waveform of the clock is distorted, which may cause the malfunction or runaway.

2. Board Pattern Example

Figure 2.1 shows a Pattern Example using the RX Family for the One-Layer Board. Figure 2.2 shows a Pattern Example using the RX Family for the Multi-Layer Board.

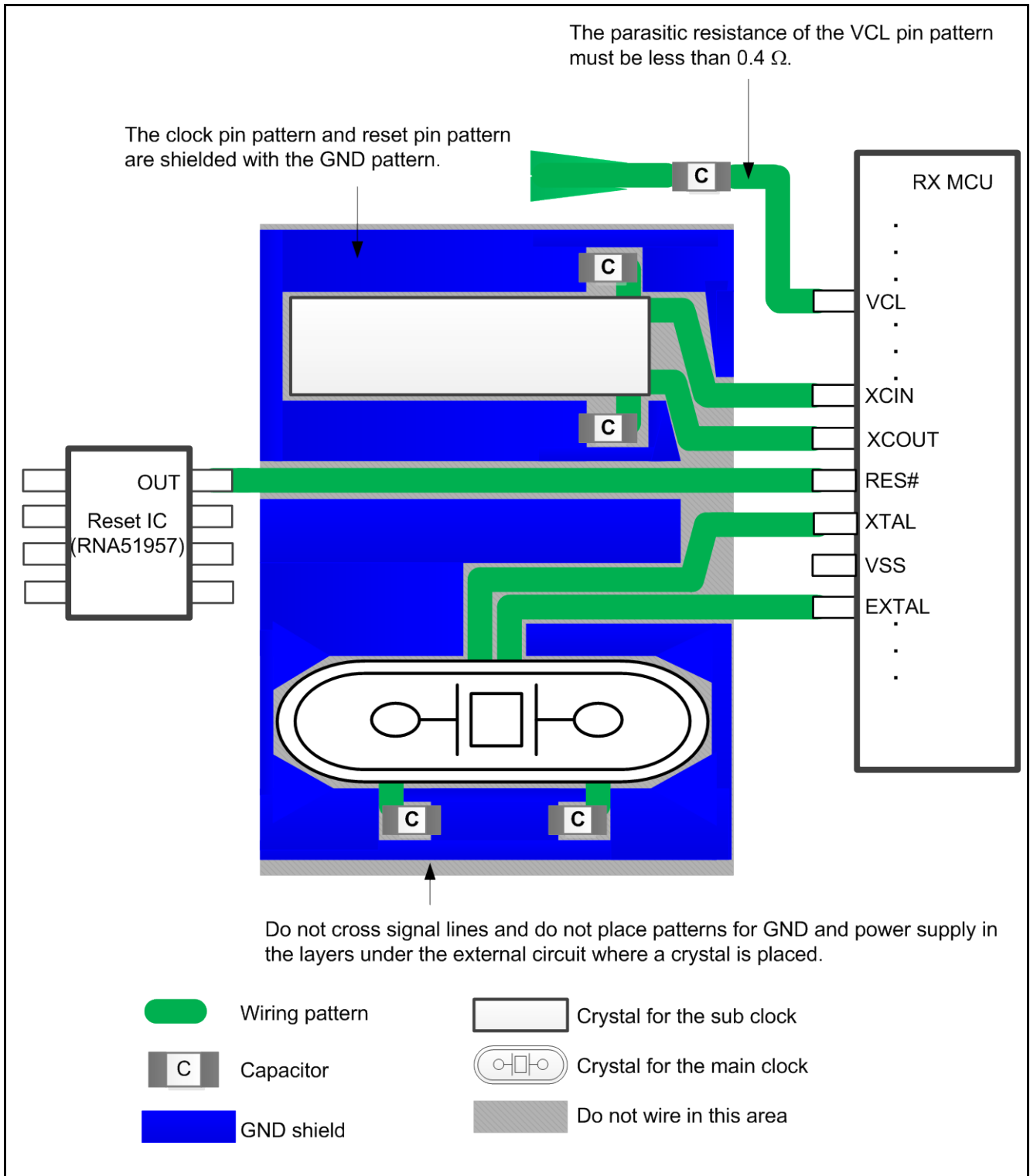


Figure 2.1 Pattern Example for the One-Layer Board

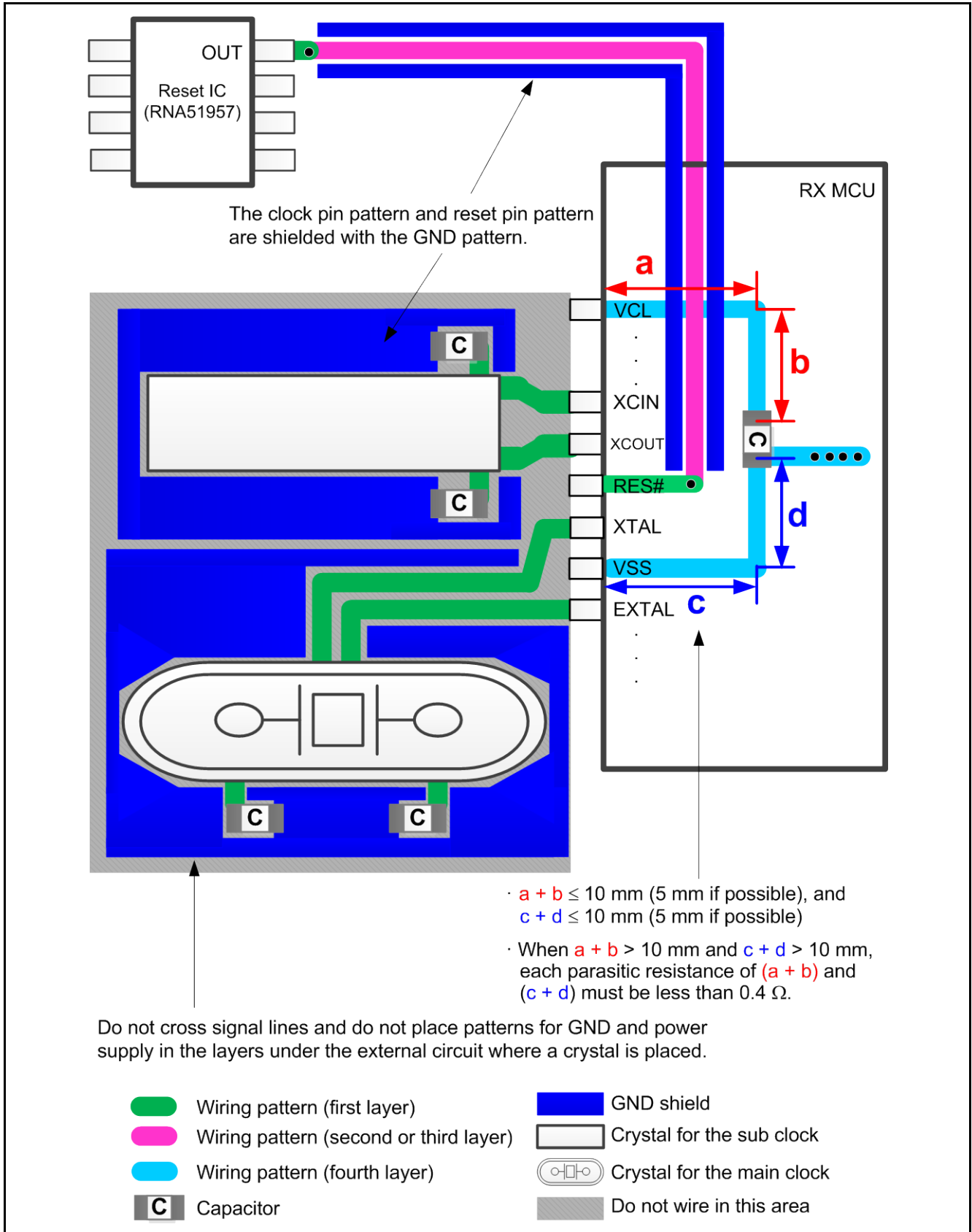


Figure 2.2 Pattern Example for the Multi-Layer Board

### 3. Reference Documents

User's Manual: Hardware

RXxxx User's Manual: Hardware

The latest versions can be downloaded from the Renesas Electronics website.

### Website and Support

Renesas Electronics website

<http://www.renesas.com>

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<b>REVISION HISTORY</b>	RX Family Application Note Hardware Design Guide
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Rev.	Date	Description	
		Page	Summary
1.01	Mar. 2, 2015	—	First edition issued

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.  
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.



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