RX Family, H8S Family

Points of Difference between HCAN (H8S Family) and CAN (RX Family)

Summary

This application note is intended as a reference document for customers using the controller area network (HCAN) module on the H8S Family who are considering migrating to the RX Family. It details points of difference between the HCAN module of the H8S Family and the CAN module of the RX Family.

Of the products listed as target devices, this application note compares the CAN modules of the groups listed in Table 1. For details of devices not listed in Table 1, refer to the applicable user’s manual.

In addition, the RSCAN module of the RX200 Series is not covered in this application note because it completely lacks software compatibility with the CAN module used as the comparison source. Refer to section 5, Related Documents, regarding differences between RSCAN and CAN modules of RX Family MCUs.

Table 1 CAN Specification Comparison Target Devices

Subject of Comparison	Family	Group	CAN Module
Comparison source	H8S Family	H8S/2636 Group	HCAN
Comparison target	RX Family	RX65N Group and RX651 Group	CAN

Target Devices

Devices among the following products equipped with CAN modules.

Devices with HCAN modules

H8S/2600 Series, H8S/2556 Group, and H8S/2282 Group

Devices with CAN modules

RX600 Series and RX700 Series

Contents

1. Differences between Functions

Differences between functions are shown below. Items that exist only on one group but not the other or that exist on both groups but with points of difference are indicated in **red**.

Table 1.1 Differences between Functions of H8S/2636 (HCAN) and RX65N (CAN)

Item		H8S/2636 (HCAN)	RX65N (CAN)
Protocol		Bosch 2.0B active compatible (ISO 11898-1 standard)	
Bit rate	Communication speed	Max. 1 Mbps	
	Bit rate equation	fCLK / (2 × (BRP + 1) × (3 + TSEG1 + TSEG2)) fCLK: System clock BRP: Baud rate prescaler (fCLK divided by (2 × (setting value + 1))) TSEG1 and TSEG2: Time segment 1 and time segment 2	fCAN / ((BRP + 1) × (1 + TSEG1 + TSEG2)) fCAN: Peripheral clock or main clock BRP: Baud rate prescaler (fCAN divided by (setting value + 1)) TSEG1 and TSEG2: Time segment 1 and time segment 2
Channels		2 channels	
ID Format		Specify standard ID or extended ID can be by the MCx.IDE bit of each mailbox.	• Specify ID format of all mailboxes with ID format mode bit (IDFM) • When Mixed ID mode is selected in ID format mode bit (IDFM), specify standard ID or extended ID by the MBj.IDE bit of each mailbox.
Mailboxes	Buffer configuration	16 buffers per channel (receive-only × 1, settable for transmission/reception × 15)	32 buffers per channel (settable for transmission/reception × 32)
	FIFO mailbox mode	No	Settable for transmission/reception × 24, ability to set 4 FIFO stages for transmission and 4 FIFO stages for reception
Data transmission	Transmission priority selection	Mailbox (buffer) number order (low-to-high) Message priority (identifier) high-to-low order	
	Ability to cancel transmission requests	Supported	Supported Note: The register manipulation method differs. Refer to 2.5, Mailbox Transmission/Reception Setting Details.
	One-shot transmission function	No	Single transmission only (no retransmission even in case of CAN bus error or arbitration lost)

Item		H8S/2636 (HCAN)	RX65N (CAN)
Data reception	Data frame and remote frame reception	Ability to receive both data frames and remote frames	Ability to receive either data frames or remote frames Note: In FIFO mailbox mode, reception of both types of frames can be enabled by setting the FIDCR0.RTR and FIDCR1.RTR bits in combination.
	Message ID masking function	One masking setting only, affecting mailbox 0 only.	Ability to make 8 masking settings (each affecting 4 mailboxes). All mailboxes are covered.
Data reception	Selectable between overwrite mode and overrun mode	No (Overwrite mode only)	Selectable
	One-shot reception function	No	Single reception only (Mailbox does not operate for reception after reception completes.)
Transmission interrupts	Message transmission completion interrupt	Yes	
	Message transmission cancellation completion interrupt	Yes	No Note: It is possible to use the transmission abort complete flag (TRMABT) for confirmation.
	Transmit FIFO interrupt	No	Yes
Reception interrupts	Message reception interrupt	Yes	
	Remote frame reception interrupt	Yes	Yes Note: A message reception interrupt request is generated when a remote frame is received by a mailbox for which remote frame was selected by the remote transmission request bit (RTR).
	Reception FIFO interrupt	No	Yes
Error interrupts	Error passive interrupt (TEC ≥ 128 or REC ≥ 128)	Yes	
	Bus-off entry interrupt (TEC ≥ 256)	Yes	

Item		H8S/2636 (HCAN)	RX65N (CAN)
	Bus-off recovery interrupt (normal recovery from bus-off state (detection of 11 consecutive recessive bits 128 times))	No	Yes
	Error warning interrupt (TEC ≥ 96 or REC ≥ 96)	Yes (Separate interrupts are generated for transmission errors and reception errors.)	Yes (Combined interrupts are generated for transmission errors and reception errors.)
	Overload frame transmission interrupt	Yes	
Error interrupts	Unread message overwrite interrupt	Yes	No Note: It is possible to use the message lost flag (MSGLOST) for confirmation.
	Reception overrun interrupt	No	Yes
	Bus lock interrupt (detection of 32 consecutive dominant bits on CAN bus)	No	Yes
	Bus error interrupt (detection of stuff error, form error, etc., on CAN bus)	No	Yes
Other interrupts	Reset processing interrupt	Reset processing completion interrupt generated by power on reset or software standby.	No Note: It is possible to use the power-on reset detect flag (PORF) or deep software standby reset flag (DPSRSTF) to determine the reset type.
	CAN bus operation interrupt	An interrupt is generated when CAN bus operation (dominant bit detection) occurs when in sleep mode.	No
Hardware reset	Initialized registers	All registers except mailboxes	All registers except MKRk, FIDCR, MKIVLR, MIER, TFPCR, RFPCR, CSSR, AFSR, and mailboxes.
	State transition after reset	Configuration mode (reset mode)	Sleep mode
	Initial setting process after reset	Perform in configuration mode (reset mode).	Perform in reset mode after cancelling sleep mode.

Item		**H8S/2636 (HCAN)**	**RX65N (CAN)**
Software reset	Initialized registers	TEC, REC	MCTLj, STR (except SLPST and TFST bits), EIFR, RECR, TECR, TSR, MSSR, MSMR, RFCR, TFCR, TCR, and ECSR (except EDPM bit)
Default state (error active or error passive)	Transition method	Transition by means of control register	
Bus-off state	Transition method	Transition when transmission error counter TEC ≥ 256	
	Mode transition after recovery	Transition to error active at detection of 11 consecutive recessive bits 128 times in bus-off state	Four selections are available: 1) Transition to error active at detection of 11 consecutive recessive bits 128 times in bus-off state 2) Switch to halt mode after transition to bus-off state (no interrupt) 3) Switch to halt mode when bus-off recovery occurs (interrupt generated) 4) Selection of manual transition (by a program) to error active state or halt mode from bus-off state
Configuration mode (reset mode)	Transition method	Transition after hardware reset or by means of control register	Transition by means of control register
Sleep mode	Transition method	Transition by means of control register	Transition by means of control register or after a reset
	Mode transition after cancellation	Transition to error active state by means of control register setting or CAN bus operation (dominant bit) detection	Transition to reset mode or halt mode by means of control register setting
Halt mode	Transition method	Transition by means of control register	
Error status monitoring	CAN bus error status monitoring	Not supported (no dedicated flags)	Ability to monitor generation of CAN bus errors such as stuff errors, form errors, and ACK errors
	Reading the error counter	Ability to read reception and transmission error counters	
DTC/DMAC transfer function		Ability to start the DTC when a message is received	No
Time stamp function		No	• Time stamp function using a 16-bit counter • Ability to select reference clock among 1-, 2-, 4- and 8-bit time periods
Software support unit		No	• Acceptance filter support • Mailbox search support • Channel search support

Item		**H8S/2636 (HCAN)**	**RX65N (CAN)**
Test control	Self-diagnostic function	No	• Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Module stop	Clock supply by means of module stop register	Yes	

2. Differences between Registers

Differences between registers are shown below. Items that exist only on one group but not the other or that exist on both groups but with points of difference are indicated in **red**.

2.1 Registers

Table 2.1 H8S/2636 (HCAN) and RX65N (CAN) Registers

Item	H8S/2636 (HCAN)	RX65N (CAN)
Control register	Master control register (MCR)	Control register (CTLR)
Status flags	General status register (GSR)	• Status register (STR) • Error interrupt factor judge register (EIFR)
Bit timing and communication speed settings	Bit configuration register (BCR)	Bit configuration register (BCR)
Mailbox transmission/reception settings	Mailbox configuration register (MBCR)	RECREQ and TRMREQ bits in message control register j (MCTLj) (j = 0 to 31)
Transmit wait settings	Transmit wait register (TXPR)	TRMREQ bit in message control register j (MCTLj) (j = 0 to 31)
Transmission completion status flags	Transmit acknowledge register (TXACK)	SENTDATA bit in message control register j (MCTLj) (j = 0 to 31)
Transmit wait cancel settings	Transmit wait cancel register (TXCR)	TRMREQ bit in message control register j (MCTLj) (j = 0 to 31)
Transmit message cancellation completion status flags	Abort acknowledge register (ABACK)	SENTDATA and TRMABT bits in message control register j (MCTLj) (j = 0 to 31)
Receive complete status flags	Receive complete register (RXPR)	NEWDATA bit in message control register j (MCTLj) (j = 0 to 31)
Remote frame receive complete status flags	Remote request register (RFPR)	—
Interrupt source status flags	Interrupt register (IRR) Note: Write 1 to clear a flag.	• RECREQ and TRMREQ bits in message control register j (MCTLj) (j = 0 to 31) • Error interrupt factor judge register (EIFR) Note: Write 0 to clear a flag.
Mailbox (buffer) interrupt request enable/disable flags	Mailbox interrupt mask register (MBIMR)	Mailbox interrupt enable register (MIER)
Interrupt source request enable/disable flags	Interrupt mask register (IMR)	• Interrupt request enable register m (IERm) • Error interrupt enable register (EIER)
Reception error counter	Receive error counter (REC)	Receive error count register (RECR)
Transmission error counter	Transmit error counter (TEC)	Transmit error count register (TECR)
Overwrite status flags	Unread message status register (UMSR)	MSGLOST bit in message control register j (MCTLj) (j = 0 to 31)
Settings for filtering using receive message identifier	Local acceptance filter masks (LAFML and LAFMH)	• Mask register k (MKRk) (k = 0 to 7) • Mask invalid register (MKIVLR)

Item	H8S/2636 (HCAN)	RX65N (CAN)
Mailboxes	Message control (MC0 to MC15)	Mailbox register j (MBj) (j = 0 to 31)
	Message data (MD0 to MD15)	Mailbox register j (MBj) (j = 0 to 31)
Module stop control	Module stop control register C (MSTPCRC)	Module stop control register B (MSTPCRB) Note: Settings must be made to the protect register (PRCR) before making settings to this register.
FIFO received ID compare settings	—	FIFO received ID compare registers 0 and 1 (FIDCR0 and FIDCR1)
Receive FIFO enable/disable settings	—	Receive FIFO control register (RFCR)
Receive FIFO pointer control settings	—	Receive FIFO pointer control register (RFPCR)
Transmit FIFO control settings	—	Transmit FIFO control register (TFCR)
Mailbox search mode settings	—	Mailbox search mode register (MSMR)
Mailbox search status register	—	Mailbox search status register (MSSR)
Channel search mode settings	—	Channel search support register (CSSR)
Multiple received ID masking function support	—	Acceptance filter support register (AFSR)
CAN bus error monitoring	—	Error code store register (ECSR)
CAN test mode control	—	Test control register (TCR)

2.2 Control Register Details

Table 2.2 H8S/2636 (HCAN) and RX65N (CAN) Control Registers

H8S/2636 (HCAN)			RX65N (CAN)		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
Master control register (MCR)			Control register (CTLR)		
MCR0	Reset request	0: Normal operating mode 1: Reset mode (initial value)	CANM [1:0]	CAN operating mode select bits	0 0: Normal operating mode 0 1: Reset mode (initial value) 1 0: Halt mode 1 1: Reset mode (forcible transition) Note: Forcible transition is a transition mode that does not wait for transmission to finish.
MCR1	Halt request	0: Normal operating mode (initial value) 1: Halt mode			
MCR2	Message transmission method	0: Message ID priority (initial value) 1: Mailbox number priority	TPM	Transmission priority mode select bit	0: Message ID priority (initial value) 1: Mailbox number priority
MCR5	HCAN sleep mode	0: Sleep mode released (initial value) 1: Sleep mode	SLPM	CAN sleep mode bit	0: Sleep mode released 1: Sleep mode (initial value) Note: Automatic transition to sleep mode after a hardware reset.
MCR7	HCAN sleep mode release	0: Sleep mode release by CAN bus operation disabled (initial value) 1: Sleep mode release by CAN bus operation enabled	—	—	—
—	—	—	IDFM [1:0]	ID Format Mode Select bit	0 0: Standard ID mode 0 1: Extended ID mode 1 0: Mixed ID mode 1 1: (setting prohibited) Note: When Mixed ID mode is selected in IDFM bit, specify standard ID or extended ID by the MBj.IDE bit of each mailbox.

2.3 Status Flag Details

Table 2.3 H8S/2636 (HCAN) and RX65N (CAN) Status Flags

H8S/2636 (HCAN)			**RX65N (CAN)**		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
General status register (GSR)			Error interrupt factor judge register (EIFR)		
GSR0	Bus off flag	0: Not in bus off state (initial value) 1: Bus off state (when TEC ≥ 256) [Clearing condition] Recovery from bus off state	BOEIF	Bus-off entry detect flag	0: Not in bus off state (initial value) 1: Bus off state (when TEC ≥ 256) [Clearing condition] 0 is written.
GSR1	Transmit/ receive warning flag	0: Error warning not detected (initial value) 1: Error warning detected (when TEC ≥ 96 or REC ≥ 96)	EWIF	Error-warning detect flag	0: Error warning not detected (initial value) 1: Error warning detected (when TEC ≥ 96 or REC ≥ 96)
General status register (GSR)			Status register (STR)		
GSR2	Message transmission status flag	0: Transmission in progress 1: Bus idle (initial value)	TRMST	Transmit status flag (transmitter)	0: Bus idle or reception in progress (initial value) 1: Transmission in progress or bus-off state Note: The status can be checked by reading this bit in combination with RECST. Bus idle: TRMST = 0, RECST = 0 Transmission in progress: TRMST = 1, RECST = 0 Reception in progress: TRMST = 0, RECST = 1
			RECST	Receive status flag (receiver)	0: Bus idle or transmission in progress (initial value) 1: Reception in progress
GSR3	Reset status bit	0: Normal operating state 1: Configuration mode (reset mode) (initial value)	RSTST	CAN reset status flag	0: Not in CAN reset mode 1: CAN reset mode (initial value)

2.4 Bit Timing and Communication Speed Setting Details

Table 2.4 H8S/2636 (HCAN) and RX65N (CAN) Bit Timing and Communication Speed Settings

H8S/2636 (HCAN)			**RX65N (CAN)**		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
Bit configuration register (BCR)			Bit configuration register (BCR)		
TSEG1 [3:0]	Time segment 1 bits	b3 b0 0 0 0 0: (setting prohibited) (initial value) 0 0 0 1: (setting prohibited) 0 0 1 0: (setting prohibited) 0 0 1 1: 4Tq 0 1 0 0: 5Tq : 1 1 1 1: 16Tq	TSEG1 [3:0]	Time segment 1 control bits	b31 b28 0 0 0 0: (setting prohibited) (initial value) 0 0 0 1: (setting prohibited) 0 0 1 0: (setting prohibited) 0 0 1 1: 4Tq 0 1 0 0: 5Tq : 1 1 1 1: 16Tq
TSEG2 [2:0]	Time segment 2 bits	b6 b4 0 0 0: (setting prohibited) (initial value) 0 0 1: 2Tq : 1 1 1: 8Tq	TSEG2 [2:0]	Time segment 2 control bits	b10 b8 0 0 0: (setting prohibited) (initial value) 0 0 1: 2Tq : 1 1 1: 8Tq
BSP	Bit sample point bit	0: Bit sampling at one point (initial value) 1: Bit sampling at three points	—	—	—
BRP [5:0]	Baud rate prescaler bits	Division ratio of 2 × (setting value P + 1) Note: The initial value is 0 (division by 2)	BRP [9:0]	Prescaler division ratio select bits	Division ratio of (setting value P + 1) Note: The initial value is 0 (division by 1)
SJW [1:0]	Re-Synchronization Jump Width	b15 b14 0 0: 1Tq (initial value) 0 1: 2Tq 1 0: 3Tq 1 1: 4Tq	SJW [1:0]	Resynchronization jump width control bits	b13 b12 0 0: 1Tq (initial value) 0 1: 2Tq 1 0: 3Tq 1 1: 4Tq

2.5 Mailbox Transmission/Reception Setting Details

Table 2.5 H8S/2636 (HCAN) and RX65N (CAN) Mailbox Transmission/Reception Settings

H8S/2636 (HCAN)			**RX65N (CAN)**		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
Mailbox configuration register (MBCR)			Message control register j (MCTLj) (j = 0 to 31)		
MBCR [15:1]	Mailbox configuration register	0: Set as transmit mailbox (initial value) 1: Set as receive mailbox	TRMREQ	Transmit mailbox request bit	0: Not configured for transmission (initial value) 1: Configured as transmit mailbox Note: The transmission and reception configuration settings are separate.
			RECREQ	Receive mailbox request bit	0: Not configured for reception (initial value) 1: Configured as receive mailbox Note: The transmission and reception configuration settings are separate.
Transmit wait register (TXPR)			Message control register j (MCTLj) (j = 0 to 31)		
TXPR [15:1]	Transmit wait register	0: Idle state (initial value) 1: Transmit wait (CAN bus arbitration) Notes: Transmission starts when TXPR is set to 1. The corresponding bit is cleared to 0 automatically after message transmission completion or cancellation completion.	TRMREQ	Transmit mailbox request bit	0: Not configured for transmission (initial value) 1: Configured as transmit mailbox Notes: Transmission starts when TRMREQ is set to 1 (equivalent to function of MBCR and TXPR combined on HCAN). The corresponding bit is not cleared to 0 even after message transmission completion.

H8S/2636 (HCAN)			**RX65N (CAN)**		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
Transmit acknowledge register (TXACK)			Message control register j (MCTLj) (j = 0 to 31)		
TXACK [15:1]	Transmit acknowledge register	0: Transmission in progress or no transmission (initial value) 1: Transmission complete [Clearing condition] 1 is written.	SENTDATA	Transmission complete flag	0: Transmission in progress or no transmission (initial value) 1: Transmission complete [Clearing condition] 0 is written.
Transmit wait cancel register (TXCR)			Message control register j (MCTLj) (j = 0 to 31)		
TXCR [15:1]	Transmit wait cancel register	0: Transmit message cancellation idle state (initial value) 1: Transmit message canceled [Clearing condition] 1 is written.	TRMREQ	Transmit mailbox request bit	0: Not configured for transmission (initial value) 1: Configured as transmit mailbox Note: Transmission is canceled when the value of TRMREQ changes from 1 to 0.
Abort acknowledge register (ABACK)			Message control register j (MCTLj) (j = 0 to 31)		
ABACK [15:1]	Abort acknowledge register	0: Cancellation failure due to transmission completion or no cancellation request (initial value) 1: Transmit message cancellation completion [Clearing condition] 1 is written.	TRMABT	Transmission abort complete flag	0: Cancellation failure due to transmission completion or no cancellation request (initial value) 1: Transmit message cancellation completion [Clearing condition] 0 is written.
Receive complete register (RXPR)			Message control register j (MCTLj) (j = 0 to 31)		
RXPR [15:0]	Receive complete register	0: Reception in progress or no reception (initial value) 1: Data frame or remote frame receive complete [Clearing condition] 1 is written.	NEWDATA	Reception complete flag	0: Reception in progress or no reception (initial value) 1: Data frame or remote frame receive complete [Clearing condition] 0 is written.

H8S/2636 (HCAN)			**RX65N (CAN)**		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
Remote request register (RFPR)			—		
RFPR [15:0]	Remote request register	0: Reception in progress or no reception (initial value) 1: Remote frame receive complete [Clearing condition] 1 is written.	—	—	—

2.6 Interrupt Source Status Flag Details

Table 2.6 H8S/2636 (HCAN) and RX65N (CAN) Interrupt Source Status Flags

H8S/2636 (HCAN)			**RX65N (CAN)**		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
Interrupt register (IRR)			Message control register j (MCTLj) (j = 0 to 31)		
IRR8	Mailbox empty interrupt flag	0: Transmission in progress or no transmission (initial value) 1: Transmission complete or transmission cancellation complete [Clearing condition] 1 is written.	SENTDATA	Transmission complete flag	0: Transmission in progress or no transmission (initial value) 1: Transmission complete [Clearing condition] 0 is written.
IRR1	Receive message interrupt flag	0: Reception in progress or no reception (initial value) 1: Data frame and remote frame receive complete [Clearing condition] When all mailbox bits in receive complete register (RXPR) are cleared	NEWDATA	Reception complete flag	0: Reception in progress or no reception (initial value) 1: Data frame and remote frame receive complete [Clearing condition] 0 is written.
IRR2	Remote frame request interrupt flag	0: Reception in progress or no reception (initial value) 1: Remote frame receive complete [Clearing condition] When all mailbox bits in remote request register (RFPR) are cleared			
IRR12	Bus operation interrupt flag	0: CAN bus idle state (initial value) 1: CAN bus operation in HCAN sleep mode [Clearing condition] 1 is written.	—	—	—

H8S/2636 (HCAN)			**RX65N (CAN)**		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
Interrupt register (IRR)			Error interrupt factor judge register (EIFR)		
IRR3	Transmit overload warning interrupt flag	0: Error warning not detected (initial value) 1: Error warning detected (when TEC ≥ 96) [Clearing condition] 1 is written.	EWIF	Error-warning detect flag	0: Error warning not detected (initial value) 1: Error warning detected (when TEC ≥ 96 or REC ≥ 96) [Clearing condition] 0 is written.
IRR4	Receive overload warning interrupt flag	0: Error warning not detected (initial value) 1: Error warning detected (when REC ≥ 96) [Clearing condition] 1 is written.			
IRR5	Error passive interrupt flag	0: Error passive state not detected (initial value) 1: Error passive state detected (when TEC ≥ 128 or REC ≥ 128) [Clearing condition] 1 is written.	EPIF	Error-passive detect flag	0: Error passive state not detected (initial value) 1: Error passive state detected (when TEC ≥ 128 or REC ≥ 128) [Clearing condition] 0 is written.
IRR6	Bus off interrupt flag	0: Not in bus-off state (initial value) 1: Bus-off state (when TEC ≥ 256) [Clearing condition] 1 is written.	BOEIF	Bus-off entry detect flag	0: Not in bus-off state (initial value) 1: Bus-off state (when TEC ≥ 256) [Clearing condition] 0 is written.
IRR7	Overload frame interrupt flag	0: Overload frame transmission not detected (initial value) 1: Overload frame transmission detected [Clearing condition] 1 is written.	OLIF	Overload frame transmission detect flag	0: Overload frame transmission not detected (initial value) 1: Overload frame transmission detected [Clearing condition] 0 is written.
IRR9	Unread interrupt flag	0: No overwrite (initial value) 1: Unread message overwrite	—	—	—

H8S/2636 (HCAN)			RX65N (CAN)		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
IRR0	Reset interrupt flag	0: Reset in progress or no reset 1: Reset processing completed after a hardware reset (HCAN module stop or software standby) (initial value) [Clearing condition] 1 is written.	—	—	—

2.7 Interrupt Source Request Enable/Disable Flag Details

Table 2.7 H8S/2636 (HCAN) and RX65N (CAN) Interrupt Source Request Enable/Disable Flags

H8S/2636 (HCAN)			RX65N (CAN)		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
Interrupt mask register (IMR)			—		
IMR8	Mailbox empty interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)	—	—	—
IMR1	Receive message interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)	—	—	—
IMR12	Bus operation interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)	—	—	—
IMR2	Remote frame request interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)	—	—	—
IMR9	Unread interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)	—	—	—
Interrupt mask register (IMR)			Error interrupt enable register (EIER)		
IMR3	Transmit overload warning interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)	EWIE	Error-warning interrupt enable bit	0: Interrupt request disabled (initial value) 1: Interrupt request enabled
IMR4	Receive overload warning interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)			
IMR5	Error passive interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)	EPIE	Error-passive interrupt enable bit	0: Interrupt request disabled (initial value) 1: Interrupt request enabled
IMR6	Bus off interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)	BOEIE	Bus-off entry interrupt enable bit	0: Interrupt request disabled (initial value) 1: Interrupt request enabled
IMR7	Overload frame/bus off recovery interrupt mask	0: Interrupt request enabled 1: Interrupt request disabled (initial value)	OLIE	Overload frame transmit interrupt enable bit	0: Interrupt request disabled (initial value) 1: Interrupt request enabled
Mailbox interrupt mask register (MBIMR)			Mailbox interrupt enable register (MIER)		
MBIMR [15:0]	Mailbox interrupt mask	0: Interrupt enabled 1: Interrupt disabled (initial value)	MB [31:0]	Interrupt enable bits	0: Interrupt disabled (initial value) 1: Interrupt enabled

The interrupt controller specifications differ on the H8S/2636 Group and RX65N Group. To control generation of interrupts on the RX65N Group it is necessary to make enable/disable settings for each interrupt in the interrupt controller. For details of the interrupt controller, refer to RX65N Group, RX651 Group User’s Manual: Hardware (R01UH0590).

The CAN interrupts on the RX65N Group are listed below.

[Software configurable interrupt B]

CANi reception complete interrupt (mailboxes 0 to 31) [RXMi]

CANi transmission complete interrupt (mailboxes 0 to 31) [TXMi]

CANi receive FIFO interrupt [RXFi]

CANi transmit FIFO interrupt [TXFi]

[Group BE0 interrupts]

CANi error interrupts [ERSi] (error interrupt sources)

- Bus error
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- Receive overrun
- Overload frame transmission
- Bus lock

2.8 Details of Settings for Filtering Using Receive Message Identifier

Table 2.8 H8S/2636 (HCAN) and RX65N (CAN) Settings for Filtering Using Receive Message Identifier

H8S/2636 (HCAN)			**RX65N (CAN)**		
Symbol	**Bit Name**	**Function**	**Symbol**	**Bit Name**	**Function**
Local acceptance filter masks (LAFML and LAFMH)			Mask register k (MKRk) (k = 0 to 7)		
LAFMH [15:8] LAFMH [7:5]	11 bits of standard/ extended identifier	0: Corresponding bits are compared (initial value) 1: Corresponding bits are not compared	SID[10:0]	Standard ID bits	0: Corresponding bits are not compared 1: Corresponding bits are compared Notes: The bit functions are the opposite of those on the HCAN. Initial values are undefined.
LAFMH [1:0] LAFML [15:0]	18 bits of extended identifier	0: Corresponding bits are compared (initial value) 1: Corresponding bits are not compared	EID[17:0]	Extended ID bits	0: Corresponding bits are not compared 1: Corresponding bits are compared Notes: The bit functions are the opposite of those on the HCAN. Initial values are undefined.
—			Mask invalid register (MKIVLR)		
—	—	—	MB[31:0]	Mask invalid bits	0: Mask valid for corresponding mailbox 1: Mask invalid for corresponding mailbox Note: Initial values are undefined.

3. Differences between Mailboxes

Table 3.1 shows the mailbox structure on the RX65N (CAN), and Table 3.2 shows the mailbox structure on the H8S/2636 (HCAN). Items that only exist on one group are indicated in **red**.

Table 3.1 Mailbox Structure of RX65N (CAN)

Register Name	b7	b6	b5	b4	b3	b2	b1	b0	Access Size*1	Field
MBj (j = 0 to 31)	IDE*2	RTR	—	SID[10:6]					8/16/32	Control
	SID[5:0]						EID[17:16]			
	EID[15:8]									
	EID[7:0]									
	—	—	—	—	—	—	—	—	8/16/32	
	—	—	—	—	DLC[3:0]					
	DATA0									Data
	DATA1									
	DATA2								8/16/32	
	DATA3									
	DATA4									
	DATA5									
	DATA6								8/16/32	
	DATA7									
	TSH									Time stamp
	TSL									

Note: 1. When accessing mailbox register j (MBj) (j = 0 to 31), access even addresses for 16-bit access and access addresses ending in 0h, 4h, 8h, or Ch for 32-bit access.

Note: 2. The IDE bit is enabled when the IDFM bit in CTLR register are mixed ID mode (10b). Write the IDE bits with 0 when the IDFM bits are not 10b. The value is 0 when it is read.

Table 3.2 Mailbox Structure of H8S/2636 (HCAN)

Register Name	b7	b6	b5	b4	b3	b2	B1	b0	Access Size*1	Field
MCx (x = 0 to 15)	—	—	—	—	DLC[3:0]				8/16	Control
	—	—	—	—	—	—	—	—		
	—	—	—	—	—	—	—	—	8/16	
	—	—	—	—	—	—	—	—		
	STD_ID[2:0]			RTR	IDE	—	EXD_ID [17:16]		8/16	
	STD_ID[10:3]									
	EXD_ID[7:0]								8/16	
	EXD_ID[15:8]									
MDx (x = 0 to 15)	DATA1								8/16	Data
	DATA2									
	DATA3								8/16	
	DATA4									
	DATA5								8/16	
	DATA6									
	DATA7								8/16	
	DATA8									

Note: 1. When accessing a message control register (MCx) (x = 0 to 15) or message data register (MDx) (x = 0 to 15), access even addresses for 16-bit access.

4. Other Differences

4.1 Sleep Mode Setting Procedure

The procedures for entering and clearing sleep mode differ between the H8S/2636 (HCAN) and RX65N (CAN). The sleep mode setting procedure on each device is shown below. For more information on detailed differences, refer to the User's Manual: Hardware of each device.

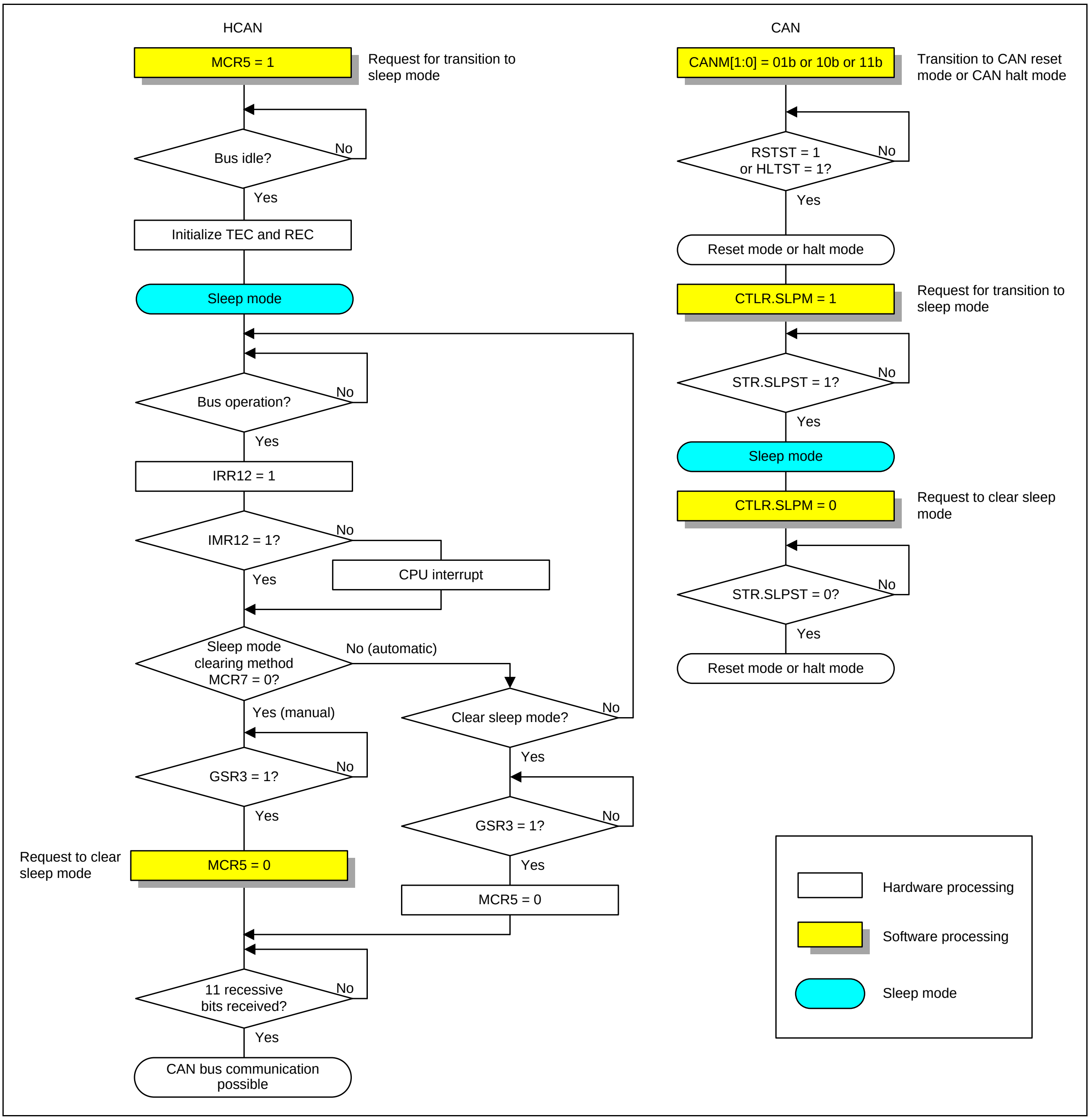

Figure 4.1 Sleep Mode Setting Procedure on H8S/2636 (HCAN) and RX65N (CAN)

4.2 Initialization by CAN Reset

The register initialization operation and transition timing after a CAN software reset differ between the H8S/2636 (HCAN) and RX65N (CAN). Table 4.1 lists the register initialization operation and transition timing differences between the two devices.

Table 4.1 Register Initialization Operation and Transition Timing after CAN Software Reset

Item	H8S/2636 (HCAN)	RX65N (CAN)
Register initialization	Only TEC and REC registers are initialized.	The following registers are initialized and the initialized state while in reset mode is retained: MCTLj, STR (except SLPST and TFST flags), EIFR, RECR, TECR, TSR, MSSR, MSMR, RFCR, TFCR, TCR, and ECSR (except EDPM bit)
Transition timing	After the MCR0 is set to 1, transition occurs after message handling has finished completely.	After the CTLR.CANM[1:0] bits are set to 01b, transition occurs after message transmission finishes (without waiting for reception to complete). [Forcible transition] Transition to reset mode occurs immediately when the CTLR.CANM[1:0] bits are set to 11b.

4.3 Endianness

The RX Family supports both littleendian and bigendian byte order. The H8S Family supports bigendian byte order only.

For details of endian settings for the RX Family, refer to the User’s Manual: Hardware of the specific RX Family device.

5. Related Documents

Related documents are listed below. Consult them in conjunction with this application note.

Application Notes

- RX Family Using the CAN (R01AN1448)
- RX65N/RX651 Group, RX230/RX231 Group Points of Difference Between RX65N Group and RX231 Group (R01AN3377)

User’s Manuals

- H8S/2639, H8S/2638, H8S/2636, H8S/2630, H8S/2635 Group Hardware Manual (REJ09B0103)
- RX65N Group, RX651 Group User’s Manual: Hardware (R01UH0590)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun.28.19	—	First edition issued.
1.01	Sep.30.19	3	Table 1.1 Differences between Functions of H8S/2636 (HCAN) and RX65N (CAN), added items related to ID format.
		10	Table 2.2 H8S/2636 (HCAN) and RX65N (CAN) Control Registers, added items related to ID format mode bits.
		22	Table 3.1 Mailbox Structure of RX65N (CAN), added note 2.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.