RX Family
Creating Workspace with RI600/4

Introduction

Target Device
Applicable MCU: RX Family

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1. **Guide in using this Document**

This document aims to equip users with the know-how of creating workspace with RI600/4.

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<tr>
<td>Reference Documents</td>
<td>Listing of documents that equip users with knowledge in the pre-requisite requirements</td>
<td>None</td>
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</table>
2. Preparing the Software

RI600/4 is a real-time operation system (RTOS) product developed for the RX Family RX600 Series target devices. To be able to create a workspace with RI600/4, users are required to install itron package: RI600/4 V1.00. Prior to its installation, it is necessary to ensure Renesas High-Performance Embedded Workshop (HEW), C/C++ Compiler package for RX family and E1/E20 Emulator Debugger package have been installed. Figure 1 illustrates the installation sequences.

<table>
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<th>Order of Installation</th>
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<tr>
<td>RI600/4 RTOS</td>
</tr>
<tr>
<td>E1/E20 Emulator Debugger</td>
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<tr>
<td>Simulator Debugger for RX Family</td>
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<tr>
<td>C/C++ Compiler Package for RX Family</td>
</tr>
<tr>
<td>High-performance Embedded Workshop (HEW)</td>
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</table>

Figure 1 Installation Sequences

3. Installing RI600/4

To verify that “C/C++ Compiler Package for RX Family” and “E1/E20 Emulator Debugger Package” has been installed, refer to the “Tools Administration” option of HEW (Figure 2).
Notes:

1. If “C/C++ Compiler Package for RX Family” has been installed correctly, Tools Administration in HEW should show “RX Standard Toolchain”, “RX600 Series CPU” and “RX600 Simulator Target Platform”.

2. If “E1/E20 Emulator Debugger Package” has been installed correctly, Tools Administration in HEW should show “RX E1/E20 SYSTEM”.

Figure 2 Validating Installation of RX Compiler and Debugger Package
After performing the validation, being the installation of RI600/4 by following the steps described below.

Figure 3 Procedures in RI600/4 Installation

Activate RI600/4 Installer Package. Select your preferred language and proceed.

Read through "License Agreement", depress "Yes" to proceed upon agreement.

Verify all user information provided and proceed if they are correct.

Select installation directory. Depress "Next" to proceed.

This dialog appeared upon successful installation.

Make your selection on reference method. Depress "Finish" to complete Setup.
Upon correct installation of the package, the following files can be found.

![Figure 4 RI600/4 Directory Listing](image)

4. Creating the First Workspace with RI600/4

Start High-Performance Embedded Workshop and follow the creation procedures described in Figure 5.
Activate HSW and the "Welcome" dialog box will appeared.
Select "Create a new project workspace" and depress "OK".

Input workspace name.
Select directory of the workspace.
Select "RX" for CPU family.
Select "Renesas RX Standard" for Toolchain.
Depress "OK"

Select "RX600" for CPU Series.
Select your device for CPU Type.
Depress "Next" to proceed.

Define "RX600" as Target type.
Select "RX600 Series RI600/4 V1.00 Release01" for RTOS.
Depress "Next" to proceed with selections of option settings, initialization routine and standard library settings.

Select your choice for the targets.
Verify Target type.
Verify Target CPU.
Depress "Next" to proceed.

This summary dialog appeared upon successful installation.

Figure 5 Procedures in Creating Workspace with RI600/4
Upon creation and compilation of the workspace “FIRST_RI6004_PROG”, user will get to see the following file structure. Figure 6 shows the file structure of a workspace created without RI600/4 for comparison.

**Figure 6 “FIRST_RI6004_PROG” File Structure**

Comparing both workspaces that are created with and without RI600/4 as shown in Figure 6 and Figure 7 respectively, it can be deduced few more files have been added for the former. Table 1 Description of RI600/4 Files provides a summary of the files added and their individual purpose.

**Figure 7 Workspace Created without RI600/4**
### Table 1 Description of RI600/4 Files

<table>
<thead>
<tr>
<th>File</th>
<th>Descriptions</th>
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<tbody>
<tr>
<td>FIRST_RI6004_PROG.cfg</td>
<td>The configuration file for the definition of RI600/4 RTOS resources</td>
</tr>
<tr>
<td>itrton.h</td>
<td>Contain definitions of data types, constants and macros, and other definitions specified in ITRON General Definitions section</td>
</tr>
<tr>
<td>kernel.h</td>
<td>Contain all service call declarations, data types, constants, and macro definitions specified in the kernel specification</td>
</tr>
<tr>
<td>kernel_api.h</td>
<td>Define service call functions declarations</td>
</tr>
<tr>
<td>kernel_id.h</td>
<td>Define ID names, kernel configuration macros specified in the cfg file, proto-type declaration of tasks and handlers, etc.</td>
</tr>
<tr>
<td>kernel_ram.h</td>
<td>Define kernel RAM data structures</td>
</tr>
<tr>
<td>kernel_rom.h</td>
<td>Define kernel ROM data structures</td>
</tr>
<tr>
<td>kernel_sysint.h</td>
<td>Contains definitions necessary to invoke service calls by an INT instruction</td>
</tr>
<tr>
<td>ri_cmt.h</td>
<td>Contains the timer driver source code</td>
</tr>
</tbody>
</table>

5. **A Walkthrough of “FIRST_RI6004_PROG” Workspace**

5.1 **Understanding the Configuration File “FIRST_RI6004_PROG.cfg” Settings**

Upon the creation of the workspace, few objects have been defined in the configuration file (i.e. “FIRST_RI6004_PROG.cfg”) and its corresponding handlers declared in the source file (i.e. “FIRST_RI6004_PROG.c”). Figure 8 to Figure 14 interpret the settings of respective objects definitions.

```c
// System Definition
system{
  stack_size = 1024;
  priority = 10;
  system_IPL = 4;
  message_pri = 1;
  tic_deno = 1;
  tic_nume = 1;
  context = FPSW,ACC;
};
```

- **System stack size defined at 1024 bytes.**
- **Only priority levels (1-10) can be used in the application.**
- **Interrupts with priority level 1-4 defined as kernel interrupts.**
- **Interrupts with priority level 5-7 defined as non-kernel interrupts.**
- **Not in use as no mailbox function is unused.**
- **Time tick (msec) = tic_nume/tic_deno = 1**
- **PSW, PC, R0-R7, R8-R13, R14, R15, FPSW & ACC registers will be used by tasks.**

**Figure 8 System Definition Settings**
Microcomputer's internal CMT channel 0 hardware timer is chosen as the system clock.

"rx610.tpl" is the template file storing all the hardware information and initialization function of CMT

Set peripheral module clock (PCLK) to 25MHz

Defined interrupt priority level of system timer at 3.

---

### Figure 9 System Clock Definition Settings

```c
// System Clock Definition
clock{
    timer = CMT0;
    template = rx610.tpl;
    timer_clock = 25MHz;
    IFL = 3;
};
```

ID number of this task is default '1' since its the first task declared and the ID number is not specified

"ID_TASK1" is the ID name of the task

"task1()" is the function name of the task

Task will be placed in the READY state at kernel startup

User stack size allocated for this task will be 512 bytes

Priority level of task is '1'

Since this is omitted, factory setting: SURI_STACK is applied for the section name assigned to the task stack area

Extended information of task is '1'

---

### Figure 10 Task Definition Settings

```c
// Task Definition

```

ID number of this task is default '2' since its the second task declared and the ID number is not specified

"ID_TASK2" is the ID name of the task

"task2()" is the function name of the task

Task will be placed in the READY state at kernel startup

User stack size allocated for this task will be 512 bytes

Priority level of task is '2'

Since this is omitted, factory setting: SURI_STACK is applied for the section name assigned to the task stack area

Extended information of task is '2'

---

### Figure 11 Semaphore Definition Settings

```c
// Semaphore Definition
semaphore[]{
    name = ID SEM1;
    max_count = 1;
    initial_count = 1;
    wait_queue = TA_TPRI;
};
```

ID number of this semaphore is default '1' since its the first semaphore to be declared and the ID number is not specified

"ID_SEM1" is the ID name of the semaphore

Maximum counter value of "ID_SEM1" is '1'.

Initial value of semaphore counter is '1'

Tasks waiting for the semaphore will be queued in a priority manner
5.2 Understanding the Program Flow in “FIRST_RI6004_PROG.c”

Figure 15 explains the program flows of the application.
Figure 15 Application Program Flows in “FIRST_RI6004_PROG.c”
6. Downloading Program with E1 Emulator

Upon the creation and compilation of the workspace, the next step is to download the program to the target device.

Figure 16 Procedures in Downloading Program with E1 Emulator
7. Reference Documents

User’s Manual
- RI600/4 V.1.00 User’s Manual
- RX Family Hardware Manual
- RX Family E1/E20 Emulator User’s Manual

The latest version can be downloaded from the Renesas Electronics website
Website and Support

Renesas Electronics Website
• http://www.renesas.com/

Inquiries
• http://www.renesas.com/inquiry

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### Revision Record

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<td>1.00</td>
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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   ⎯ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   ⎯ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   ⎯ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   ⎯ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   ⎯ The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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