Introduction

This application note discusses IH control (100V) using the 16-bit timer KB20 of the RL78/L13.

Target Device

RL78/L13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.
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1. Specifications

The sample program covered in this application note generates a PWM waveform for IH control (100 V) using the 16-bit timer KB20 and outputs it from the TKBO01-0 pin (100 V).

Table 1.1 lists the peripheral functions to be used and their uses and figure 1.1 illustrates the PWM output function for IH control.

Table 1.1 Peripheral Functions to Be Used and Their Uses

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-bit timer KB20 (timer KB20)</td>
<td>PWM output for IH control</td>
</tr>
<tr>
<td>External interrupt input INTP3</td>
<td>Restart of PWM output for IH control</td>
</tr>
<tr>
<td>External interrupt input INTP0</td>
<td>Forced output shutoff of PWM output for IH control</td>
</tr>
<tr>
<td>Timer array unit (TAU)</td>
<td>Generation of main period (10 ms)</td>
</tr>
</tbody>
</table>

Figure 1.1 PWM Output Function for IH Control
2. Operation Check Conditions

The operation of the sample code covered in this application note has been checked and verified under the conditions summarized below.

Table 2.1 Operation Check Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcomputer used</td>
<td>RL78/L13 (R5F10WMGA)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>• High-speed on-chip oscillator clock ($f_{HOCO}$): 24 MHz (standard)</td>
</tr>
<tr>
<td></td>
<td>• CPU/peripheral hardware clock ($f_{CLK}$): 24 MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5.0 V (can run at 2.9 V to 5.5 V)</td>
</tr>
<tr>
<td></td>
<td>LVD operation ($V_{LVD}$): Reset mode (rising edge: 2.81 V, falling edge: 2.75 V)</td>
</tr>
<tr>
<td>Integrated development</td>
<td>CS+ for CC V3.03.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>environment (CS+)</td>
<td></td>
</tr>
<tr>
<td>C compiler (CS+)</td>
<td>CC-RL V1.02.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development</td>
<td>e2studio V5.0.0.043 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>environment (e2studio)</td>
<td></td>
</tr>
<tr>
<td>C compiler (e2studio)</td>
<td>CC-RL V1.02.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>RL78/L13 code library</td>
<td>Code Generator for RL78/L13 V1.03.02.01 from Renesas Electronics Corp.</td>
</tr>
</tbody>
</table>
3. Description of Hardware

3.1 Hardware Configuration Example

Figure 3.1 shows a connection example.

```
<table>
<thead>
<tr>
<th>Pin name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P137/INTP0</td>
<td>Input</td>
<td>Forced output shutoff signal input:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Inputs the forced output shutoff signal (falling edge) to stop</td>
</tr>
<tr>
<td></td>
<td></td>
<td>the PWM output for IH control forcibly.</td>
</tr>
<tr>
<td>P31/INTP3</td>
<td>Input</td>
<td>External trigger signal input:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Inputs the resonance voltage signal (falling edge) which occurs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>when the IGBT is subjected to switching. This signal serves as</td>
</tr>
<tr>
<td></td>
<td></td>
<td>the trigger for regenerating the PWM waveform.</td>
</tr>
<tr>
<td>P77/TKBO01-0</td>
<td>Output</td>
<td>PWM output for IH control:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Outputs the PWM waveform for IH control.</td>
</tr>
</tbody>
</table>
```

Notes:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical characteristics conditions are met (connect the input-dedicated ports independently to VDD or VSS via a resistor).
2. Set VDD to a voltage higher than the reset release voltage (VLVD) that is set for the LVD.
4. Description of Software

4.1 Operation Outline

1. Generates the PWM waveform for 100V IH control via the timer KB20 and outputs it from the TKBO01-0 pin.

2. With the resonance voltage signal produced by switching of the IGBT as a feedback signal, an external trigger signal is input to the INTP3 pin.

3. An output signal which alternates between the output being stopped and output ON (high output for 10 μs) every second is generated.

4. The output is stopped if the forced output shutoff signal is input while PWM waveform generation is in progress. Once stopped, the output remains in the stopped state for 500 ms.

5. The output (output ON) is not resumed if the level on the forced output shutoff signal is low. The output (output ON) is resumed if the level on the forced output shutoff signal is high.

Figure 4.1 shows the timing diagram.

![Figure 4.1 Timing Diagram](image_url)

(1) Counter start (S/W: software)
   Setting the TKBCE0 bit to 1 starts counting by TKBCNT0.

(2) High level output (H/W: hardware)
   When the value of TKBCNT0 matches the value (0000H) of TKBCR02, the level on the TKBO01-0 pin goes high.

(3) Low level output (H/W)
   When the value of TKBCNT0 matches the value (00F0H) of TKBCR03, the level on the TKBO01-0 pin goes low.

(4) PWM period (H/W)
   When the value of TKBCNT0 matches the value (04AFH) of TKBCR00, TKBCNT0 is cleared to 0.

(5) Restart of PWM output (H/W)
   When a falling edge is input to INTP3, TKBCNT0 is cleared to 0.

(6) Stop of PWM output by forced output shutoff (H/W)
   When a falling edge is input to INTP0, the TKBO01-0 pin is placed in the high impedance state.
## 4.2 List of Option Byte Settings

Table 4.1 summarizes the settings of the option bytes.

### Table 4.1 Option Byte Settings

<table>
<thead>
<tr>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000C0H/010C0H</td>
<td>11101111B</td>
<td>Disables the watchdog timer. (Stops counting after the release of the reset state.)</td>
</tr>
<tr>
<td>000C1H/010C1H</td>
<td>01111111B</td>
<td>LVD reset mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Detection voltage: 2.81 V (rising edge), 2.75 V (falling edge)</td>
</tr>
<tr>
<td>000C2H/010C2H</td>
<td>11100000B</td>
<td>High-speed on-chip oscillator HS mode, 24 MHz</td>
</tr>
<tr>
<td>000C3H/010C3H</td>
<td>10000100B</td>
<td>Enables the on-chip debugger.</td>
</tr>
</tbody>
</table>

## 4.3 List of Variables

Table 4.2 lists the static variables and Table 4.3 lists const variables.

### Table 4.2 Static Variables

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>uint8_t</td>
<td>pwm_select</td>
<td>Selects high width</td>
<td>main</td>
</tr>
<tr>
<td></td>
<td>Period</td>
<td>IH output period</td>
<td>main</td>
</tr>
<tr>
<td>uint16_t</td>
<td>Ton_width</td>
<td>High width of IH output</td>
<td>main</td>
</tr>
<tr>
<td></td>
<td>delay_time</td>
<td>Delay time of IH output</td>
<td>main</td>
</tr>
<tr>
<td></td>
<td>pwm_change_period</td>
<td>PWM period control of IH output</td>
<td>main</td>
</tr>
<tr>
<td></td>
<td>release_time</td>
<td>Release time of IH output</td>
<td>main</td>
</tr>
</tbody>
</table>

### Table 4.3 const Variables

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>uint16_t</td>
<td>_H_Width_TBL</td>
<td>High width table</td>
<td>main</td>
</tr>
</tbody>
</table>
4.4 List of Functions

Table 4.4 gives the functions that are used.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>hdwinit</td>
<td>Initialization</td>
</tr>
<tr>
<td>R_Systeminit</td>
<td>Peripheral function initialization</td>
</tr>
<tr>
<td>R_CGC_Create</td>
<td>CPU initialization</td>
</tr>
<tr>
<td>R_TAU0_Create</td>
<td>TAU0 initialization</td>
</tr>
<tr>
<td>R_TAU0_Channel0_Start</td>
<td>Enable TAU00 operation</td>
</tr>
<tr>
<td>R_KB20_Create</td>
<td>Timer KB20 initialization</td>
</tr>
<tr>
<td>R_KB20_Start</td>
<td>Enable timer KB20 operation</td>
</tr>
<tr>
<td>R_KB20_Stop</td>
<td>Stop timer KB20 operation</td>
</tr>
<tr>
<td>Igbt_Outdrv</td>
<td>IGBT output driver setup</td>
</tr>
<tr>
<td>igbt_width_set</td>
<td>IGBT output setup</td>
</tr>
<tr>
<td>main</td>
<td>Main processing</td>
</tr>
<tr>
<td>R_MAIN_UserInit</td>
<td>Main initialization</td>
</tr>
</tbody>
</table>
4.5 Function Specifications

This section describes the function specifications for the sample code.

hdwinit

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>None</td>
</tr>
<tr>
<td>Declaration</td>
<td>void hdwinit(void)</td>
</tr>
<tr>
<td>Explanation</td>
<td>Initializes the peripheral functions.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return value</td>
<td>None</td>
</tr>
</tbody>
</table>

R_Systeminit

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Peripheral function initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>None</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_Systeminit(void)</td>
</tr>
<tr>
<td>Explanation</td>
<td>Initializes the peripheral functions that are used by the sample code covered in this application note.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return value</td>
<td>None</td>
</tr>
</tbody>
</table>

R_CGC_Create

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>CPU initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>r_cg_cgc.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_CGC_Create(void)</td>
</tr>
<tr>
<td>Explanation</td>
<td>Initializes the CPU.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return value</td>
<td>None</td>
</tr>
</tbody>
</table>

R_TAU0_Create

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>TAU0 initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>r_cg_timer.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_TAU0_Create(void)</td>
</tr>
<tr>
<td>Explanation</td>
<td>Initializes the TAU00 for use as an interval timer.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return value</td>
<td>None</td>
</tr>
</tbody>
</table>

R_TAU0_Channel0_Start

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Enable TAU00 operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>r_cg_timer.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_TAU0_Channel0_Start(void)</td>
</tr>
<tr>
<td>Explanation</td>
<td>Starts the TAU00 for counting.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return value</td>
<td>None</td>
</tr>
</tbody>
</table>
**R_KB20_Create**

**Synopsis**
Timer KB20 initialization

**Header**
r_cg_timer.h

**Declaration**
void R_KB20_Create(void)

**Explanation**
Initializes timer KB20 for use as the PWM output function for IH control

**Arguments**
None

**Return value**
None

---

**R_KB20_Start**

**Synopsis**
Enable timer KB20 operation

**Header**
r_cg_timer.h

**Declaration**
void R_KB20_Start(void)

**Explanation**
Starts counting and output by the timer KB20.

**Arguments**
None

**Return value**
None

---

**R_KB20_Stop**

**Synopsis**
Stop timer KB20 operation

**Header**
r_cg_timer.h

**Declaration**
void R_KB20_Stop(void)

**Explanation**
Stops counting and output by the timer KB20.

**Arguments**
None

**Return value**
None

---

**Igbt_Outdrv**

**Synopsis**
IGBT output driver setup

**Header**
r_cg_userdefine.h

**Declaration**
void Igbt_Outdrv(uint16_t period, uint16_t Ton_width, uint8_t delay_time)

**Explanation**
Calculates the values to be set in the general registers.

**Arguments**
uint16_t period Period
uint16_t Ton_width Ton width
uint8_t delay_time Delay time

**Return value**
None
**igbt_width_set**

**Synopsis**
IGBT output setup

**Declaration**
static void igbt_width_set(uint8_t out_mode, uint16_t tkbcr00_calc,  
uint16_t tkbcr02_calc, uint16_t tkbcr03_calc)

**Explanation**
Makes settings for IGBT output start, change, and stop processing.

**Arguments**
- `uint8_t out_mode` Output mode  
  0: Output stopped  
  1: Output started/changed
- `uint16_t tkbcr00_calc` TKBCR00 value
- `uint16_t tkbcr02_calc` TKBCR02 value
- `uint16_t tkbcr03_calc` TKBCR03 value

**Return value**
None

**main**

**Synopsis**
Main processing

**Declaration**
void main(void)

**Explanation**
Performs the main processing.

**Arguments**
None

**Return value**
None

**R_MAIN_UserInit**

**Synopsis**
Main initialization

**Declaration**
void R_MAIN_UserInit(void)

**Explanation**
Performs processing necessary for initializing the main processing.

**Arguments**
None

**Return value**
None
4.6  Flowcharts

4.6.1  Overall Flowchart
Figure 4.2 shows the overall flowchart.

![Overall Flowchart Diagram]

4.6.2  Initialization
Figure 4.3 shows the flowchart for initialization.

![Initialization Diagram]

4.6.3  Peripheral Function Initialization
Figure 4.4 shows the flowchart for peripheral function initialization.

![Peripheral Function Initialization Diagram]
### 4.6.4 CPU Initialization

Figure 4.5 shows the flowchart for CPU initialization.

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_CGC_Create</td>
<td></td>
</tr>
<tr>
<td>Set X1 oscillator to &quot;hot used&quot;, XT1 oscillator to &quot;hot used&quot;</td>
<td></td>
</tr>
<tr>
<td>Stop high-speed system clock</td>
<td></td>
</tr>
<tr>
<td>Set up main system clock</td>
<td></td>
</tr>
<tr>
<td>Stop subsystem clock</td>
<td></td>
</tr>
<tr>
<td>Select operation clock for real-time clock and interval timer</td>
<td></td>
</tr>
<tr>
<td>Set up CPU/peripheral hardware clock</td>
<td></td>
</tr>
<tr>
<td>Start high-speed on-chip oscillator</td>
<td></td>
</tr>
<tr>
<td>Return</td>
<td></td>
</tr>
</tbody>
</table>

- **CMC register**: 02H
  - EXCLK bit = 0: Operation mode of high-speed clock pin:
  - OSCSEL bit = 0: Input port mode
  - EXCLKS bit = 0: Operation mode of subsystem clock pin:
  - OSCSELS bit = 0: Input port mode
  - AMPHs1, AMPHs0 = 01B: Oscillation mode of XT1 oscillator circuit
    - Normal oscillation
    - Oscillation margin: High
- **CSC register**: 0M1
  - MSTOP bit = 1: Stops X1 oscillator circuit
- **CKC register**: 0M0
  - MCH bit = 0: Sets up the high-speed on-chip oscillator clock
- **CSC register**: 0X1
  - XTSTOP bit = 1: Stops the XT1 oscillator circuit.
- **OSMC register**: 00H
  - RTCLPC bit = 0: Enables supply of subsystem clock to peripheral functions.
  - WUTMCK0 bit = 0: Subsystem clock
- **CKC register**: 0S1
  - CSS bit = 0: Sets up the main system clock.
- **CSC register**: 0HI
  - HISTOP bit = 0: Sets up main system clock.

**Figure 4.5 CPU Initialization**
4.6.5 TAU0 Initialization

Figure 4.6 shows the flowchart for TAU0 initialization.

R_TAU0_Create
Enable clock supply to TAU0
Set up timer clock select register 0
Stop TAU00 count operation
Disable TAU00 interrupts
Disable TAU01 interrupts
Disable TAU01 higher 8-bit interrupts
Disable TAU02 interrupts
Disable TAU03 interrupts
Disable TAU03 higher 8-bit interrupts
Set up TAU00 operating mode
Set TAU00 counter value
Disable TAU00 output

return

PER0 register
TAU0EN bit ← 1
TPS0 register ← 0003H
PRS031, PRS030 bits = 00B : CK72
PRS021, PRS020 bits = 000B : CK22
PRS013 to PRS010 bits = 0000B : CK1
PRS003 to PRS000 bits = 0011B : CK00 = CK72 (3 MHz)
TTO register ← 0A0FH
TTO0 bit = 1

MK1L register
TMMK00 bit ← 1 : Disables INTT0 interrupts,
IF1L register
TIMF00 bit ← 0 : Clears the INTT0 interrupt request flag.

MK1L register
TMMK01 bit ← 1 : Disables INTT1 interrupts,
IF1L register
TIMF01 bit ← 0 : Clears the INTT1 interrupt request flag.

MK1L register
TMMK01H bit ← 1 : Disables INTT1H interrupts,
IF1L register
TIMF01H bit ← 0 : Clears the INTT1H interrupt request flag.

MK1H register
TMMK02 bit ← 1 : Disables INTT2 interrupts
IF1H register
TIMF02 bit ← 0 : Clears the INTT2 interrupt request flag.

MK1H register
TMMK03 bit ← 1 : Disables the INTT3 interrupts
IF1H register
TIMF03 bit ← 0 : Clears the INTT3 interrupt request flag.

MK1L register
TMMK03H bit ← 1 : Disables INTT3H interrupts
IF1L register
TIMF03H bit ← 0 : Clears the INTT3H interrupt request flag.

TM00 register ← 0000H
CK8001, CK8000 bits = 00B : Operating clock : Operating clock CK0 set up in timer clock select register 0 (TPS0)
CC800 bit= 0 : Count clock: Operating clock designated by bits CK8001 and CK8000
STS802 to STS800 bits = 000B : Set the start trigger; Enable only software trigger startup (deselct the other trigger sources).
MD803 to MD8001 bits = 000B : Operating modes: Interval timer mode
MD80 bit= 0 : Timer Interrupt is not generated when counting is started.
TDR80 register ← 752FH : 10 ms measurement (1/3 MHz × 30000 = 10 ms)

TO0 register
TO0 bit ← 0
TOE0 register
TOE0 bit ← 0

Figure 4.6 TAU0 Initialization
4.6.6 Enable TAU00 Operation

Figure 4.7 shows the flowchart for enabling TAU00 operation.

![Flowchart for enabling TAU00 operation]

Figure 4.7  Enable TAU00 Operation
4.6.7 Timer KB20 Initialization

Figure 4.8, figure 4.9, figure 4.10, and figure 4.11 show the flowcharts for timer KB20 initialization.

- **R_KB20_Create**
  - Enable clock supply to timer KB20
    - PER1 register
      - TKB2EN bit ← 1
  - Disable timer KB20 interrupts
    - MK2L register
      - TKBMK20 bit ← 1
      - IF2L register
      - TKBIF01 bit ← 0
  - Stop timer operation
    - TKBCTL01 register
      - TKBCE0 bit = 0
  - Set up timer KB20 operation control register 00
    - TKBCTL00 register ← 8000H
      - TKBHIE0 bit = 1
      - TKBSSSE01 bit = 0
      - TKBDE01 bit = 0
      - TKBSSSE00 bit = 0
      - TKBDMFE0 bit = 0
      - TKBTSO1, TKBSTSO0 bits = 00B
  - Set up timer KB20 operation control register 01
    - TKBCTL01 register ← 00H
      - TKBCE0 bit = 0
      - TKBCKSO bit = 0
      - TKBMD01, TKBMD00 bits = 00B
  - Set up timer KB20 output control register 00
    - TKBIOC00 register ← 00H
      - TKBTOLO1 bit = 0
      - TKBTOLO0 bit = 0
      - TKBTOOD1 bit = 0
      - TKBTOOD0 bit = 0
  - Selects TKBO01-0 for the outputs of timer KB20.
    - PWCTKB register ← 00H
      - TKBPWO1, TKBPW00 bits = 00B

**Figure 4.8 Timer KB20 Initialization (1/4)**
Figure 4.9 Timer KB20 Initialization (2/4)
<table>
<thead>
<tr>
<th>Register</th>
<th>Bits</th>
<th>Count restart trigger inputs:</th>
<th>Restart source:</th>
<th>Post-restart operation:</th>
</tr>
</thead>
<tbody>
<tr>
<td>ELSELR00</td>
<td>00H</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>ELSELR00</td>
<td>000B</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>ELSELR01</td>
<td>00H</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>ELSELR01</td>
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<td>None</td>
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</tr>
<tr>
<td>ELSELR02</td>
<td>00H</td>
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<td>None</td>
</tr>
<tr>
<td>ELSELR02</td>
<td>000B</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>ELSELR03</td>
<td>04H</td>
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<td>None</td>
</tr>
<tr>
<td>ELSELR03</td>
<td>100B</td>
<td>TMBK2 IH-PWM output restart request signal</td>
<td>TMBK2 IH-PWM output restart</td>
<td>IH-PWM output restart</td>
</tr>
<tr>
<td>ELSELR04</td>
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<td>ELSELR04</td>
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<td>ELSELR05</td>
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<td>None</td>
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<td>ELSELR06</td>
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<td>ELSELR08</td>
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<tr>
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<td>None</td>
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<td>ELSELR09</td>
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<td>ELSELR09</td>
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</table>

Figure 4.10  Timer KB20 Initialization (3/4)
Set up forced output stop function control register 2

TKBPACTL02 register → 00H
TKBPACE01 bit = 0: Disables the forced output stop function for TKBO01-0, TKBO01-1, and TKBO01-2 pins.
TKBPACE00 bit = 0: Disables the forced output stop function for TKBO00 pin (note 1).

TKBPACTL00 register → 0000H (note 2)

TKBPACTL01 register → 0010H
TKBPACHI01 bit = 1: Selects the forced output stop function 1 trigger input: Uses INTP0 which does not pass through the noise filter as the trigger (note 3).

TKBPAHFS0 register → 00H (note 4)

TKBPAHFT0 register → 00H (note 5)

Initialize forced output stop function 1 start register

Initialize forced output stop function 1 stop register

Clear the flags of 16-bit timer KB2 flag register 0 (TKBFLG0)

TKBCLR0 register → 3EH
TKBCLI01 bit = 1: Clears the error flag for the PWM output smooth start function of TKBO01-0, TKBO01-1, and TKBO01-2 pins.
TKBCLI00 bit = 1: Clears the error flag for the PWM output smooth start function of the TKBO pin.
TKBCLI10 bit = 1: Clears the undetected restart trigger source 1 trigger error flag for interleave PFC mode.
TKBCLI01 bit = 1: Clears restart trigger source 1 trigger multiple detection error flag for interleave PFC mode.
TKBCLMF0 bit = 1: Clears the status flag for the maximum frequency limit function.

Set up pins TKBO01-0

PFSEG2 register
PFSEG19 bit ← 0: Uses as a port (except for segment output).
P7 register
P77 bit ← 0: Outputs "0".
PM7 register
PM77 bit ← 0: Output mode

Set up pin INTP3

PFSEG2 register
PFSEG21 bit ← 0: Uses as a port (except for segment output).
PM3 register
PM31 bit ← 1: Input mode

Note 1. Bit 0 (TKBPACE00) of the TKBPACTL02 register cannot be used when the IH-PWM output function is to be used. Be sure to set this bit to 0.

Note 2. The TKBPACTL00 register cannot be used when the IH-PWM output function is to be used. Be sure to set the register to its initial value (0000H).

Note 3. Only bit 4 (TKBPACHI01) of the TKBPACTL01 register can be used when the IH-PWM output function is to be used. Be sure to set the other bits to 0.

Note 4. The TKBPAHFS0 register cannot be used when the IH-PWM output function is to be used. Be sure to set the register to its initial value (00H). Be sure to set the other bits to 0.

Note 5. Bit 0 (TKBPAHFT0) of the TKBPAHFT0 register cannot be used when the IH-PWM output function is to be used. Be sure to set this bit to 0.

Figure 4.11 Timer KB20 Initialization (4/4)
4.6.8 Enable Timer KB20 Operation

Figure 4.12 shows the flowchart for enabling timer KB20 operation.

```
R_KB20_Start
  Set up timer KB20 operation control register 00
    TKBCTL00 register
      TKBSE0 bit ← 1
      : Uses the compare register batch overwrite function activated by the external trigger.
  Enable timer KB20 operation
  Set up the valid edge of restart trigger
  Set up forced output stop function control register 2
    TKBACTL02 register ← 02H
    TKBPACE01 bit = 1
      : Enables the forced output stop function of pins TKBO01-0, TKBO01-1, and TKBO01-2.
  return
```

Figure 4.12 Enable Timer KB20 Operation

4.6.9 Stop Timer KB20 Operation

Figure 4.13 shows the flowchart for stopping timer KB20 operation.

```
R_KB20_Stop
  Set up timer KB20 operation control register 00
    TKBCTL00 register
      TKBSE0 bit ← 0
      : Does not use the compare register batch overwrite function activated by the external trigger.
  Stops timer KB20 operation
  Set up the valid edge of restart trigger
  Set up forced output stop function control register 2
    TKBACTL02 register ← 00H
    TKBPACE01 bit = 0
      : Disables the forced output stop function of pins TKBO01-0, TKBO01-1, and TKBO01-2.
  return
```

Figure 4.13 Stop Timer KB20 Operation
4.6.10 IGBT Output Driver Setup

Figure 4.14 shows the flowchart for IGBT output driver setup.

![Figure 4.14 IGBT Output Driver Setup](image)

**[Arguments]**
- Uint16_t period : Period
- Uint16_t Ton_width : Ton width
- Uint8_t delay_time : Delay time

Load tkbcr02_calc with delay_time

Load tkbcr03_calc with tkbcr02_calc + Ton_width

Load tkbcr00_calc with period - 1

Is Ton width 0?
- Yes: Set out_mode to 1
- No: IGBT output setup processing Igbt_width_set()

return
4.6.11 IGBT Output Setup

Figure 4.15 shows the flowchart for IGBT output setup.

```
igbt_width_set

out_mode

0 (Stop output)

Set up TKBCR02

Set up TKBCR03

Set up TKBCR00

Set up compare register batch overwrite request trigger

Read TKBCTL01 register

TKBC0 bit : 0: Stops the timer.

1: Enables the timer.

No

1 (Start/change output)

Timer enabled?

Yes

Set up TKCR02

Set up TKCR03

Set up TKCR00

TKBTRG0 register

TKBRTD0 bit ← 1 : Compare register batch overwrite request

default

return

Stop 16-bit timer KB20
R_KB20_Stop()

Start 16-bit timer KB20
R_KB20_Start()
```

Figure 4.15 IGBT Output Setup
4.6.12 Main Processing

Figure 4.16 and figure 4.17 show the flowchart for main processing.

```
main

Enable maskable interrupts
R_MAIN_UserInit()

Check for occurrence of TAU00 interrupt request signal

Interrupt request signal generated

Clear TAU00 interrupt request flag

release_time=0?

Yes

Decrement release_time by 1

Set pwm_change_period to 0

No

Forced output shutoff signal reset level ?

Yes

Increment pwm_change_period by 1

pwm_change_period greater than 100?

No

Set pwm_change_period to 0

Add 1 to pwm_select

pwm_select &= 0x01

Yes

Set delay_time to 0

Set up Ton_width

Set Period to 1200

IGBT output driver processing
Igbt_Outdrv()

No interrupt request signal generated

Read IF0H register
TMIF00 bit : 0: No interrupt request.
1: Interrupt request present.

IF0H register
TMIF00 bit ← 0

Read P13 register
P137 bit : 0: Low level
1: High level

E

Figure 4.16   Main Processing (1/2)
```
4.6.13 Main Initialization

Figure 4.18 shows the flowchart for main initialization.

Figure 4.17 Main Processing (2/2)
5. Sample Code
The sample code is available on the Renesas Electronics Website.

6. Documents for Reference
RL78/L13 User's Manual: Hardware
RL78 Family User’s Manual: Software
(The latest versions of the documents are available on the Renesas Electronics Website.)

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https://www.renesas.com/en-us/support/contact.html
<table>
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<td>Mar 31, 2016</td>
<td>—</td>
<td>First edition issued</td>
</tr>
<tr>
<td>2.00</td>
<td>June 10, 2016</td>
<td>4</td>
<td>Added e2studio</td>
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<table>
<thead>
<tr>
<th>1. Handling of Unused Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.</td>
</tr>
<tr>
<td>The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2. Processing at Power-on</th>
</tr>
</thead>
<tbody>
<tr>
<td>The state of the product is undefined at the moment when power is supplied.</td>
</tr>
<tr>
<td>The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>3. Prohibition of Access to Reserved Addresses</th>
</tr>
</thead>
<tbody>
<tr>
<td>Access to reserved addresses is prohibited.</td>
</tr>
<tr>
<td>The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>4. Clock Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.</td>
</tr>
<tr>
<td>When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>5. Differences between Products</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.</td>
</tr>
<tr>
<td>The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.</td>
</tr>
</tbody>
</table>
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