RL78/L13

How to Output Remote Control Signals

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Abstract

This document describes the how to output remote control signals using the RL78/L13 timer array unit (remote control output function).

Products

RL78/L13

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

In this application note, a PWM waveform for remote control is generated by the remote control output function of the timer array unit (TAU).

When the sample program detects that the key connected to port P137 has been pressed, the RL78/L13 outputs remote control signals.

The system clock frequency is set low (operation enabled from 1.8 V) to reduce the operating voltage of the remote control.

Table 1.1 lists the peripheral function and its application. Figure 1.1 shows the remote control signal output.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
TAU	Generates and outputs remote control signals

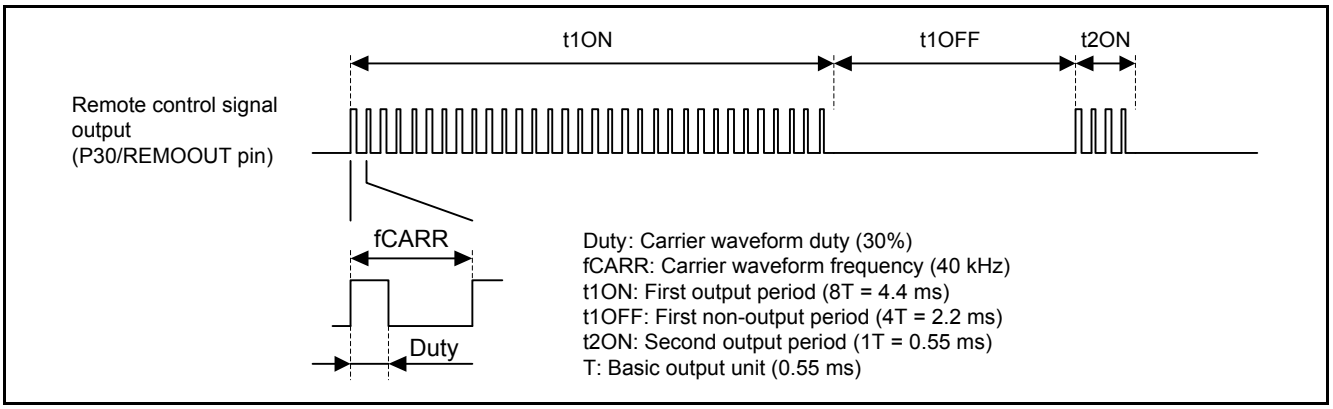


Figure 1.1 Remote Control Signal Output

2. Operating Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

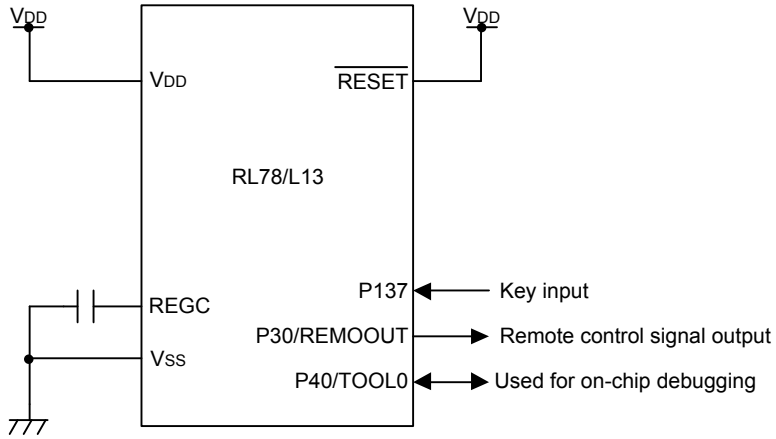
Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/L13 (R5F10WMGA)
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}): 8 MHz • CPU/peripheral hardware clock (f_{CLK}): 8 MHz
Operating voltage	3.3 V (operation enabled from 1.8 to 5.5 V) LVD operation (V_{LVD}): 1.77 V at the rising edge or 1.73 V at the falling edge in reset mode
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V2.00.00
C compiler	Renesas Electronics Corporation CA78K0R V1.60
RL78/L13 code library	Renesas Electronics Corporation AP4 for RL78/L13 V1.00.00.02
Board used	Renesas Starter Kit for RL78/L13 CPU Board (R0K5010WMS000BE)

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows a connection example.



Notes:
1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins as appropriate to satisfy the electrical characteristics. Connect input-only ports independently to either V_{DD} or V_{SS}.
2. Make sure to set V_{DD} greater than the detection voltage (V_{LVD}) specified by the LVD.

Figure 3.1 Connection Example

3.2 Pins Used

Table 3.1 lists the pins used and their functions.

Table 3.1 Pin Used and Their Functions

Pin Name	I/O	Function
P30/REMOOUT	Output	Outputs remote control signals
P137	Input	Key input

4. Software

4.1 Operation Overview

The sample program detects that a key (SW1) on the Renesas Starter Kit for RL78/L13 CPU board has been pressed and held down, and remote control signals are output from the RL78/L13 REMOOUT pin.

TAU generates a carrier waveform and mask waveform to synthesize a PWM waveform to output remote control signals.

TAU settings:

- Specify the remote control output function of the PWM output function as the operating mode
- Use channels 4 and 5 to generate a carrier waveform
- Set the carrier waveform frequency to 40 kHz, and duty cycle to 30% (active high period)
- Use channels 2 and 3 to generate a mask waveform
- Specify f_{CLK} at 8 MHz as the count source
- Disable interrupts INTTM02, INTTM03, INTTM04, and INTTM05

Figure 4.1 shows the behavior of remote control output.

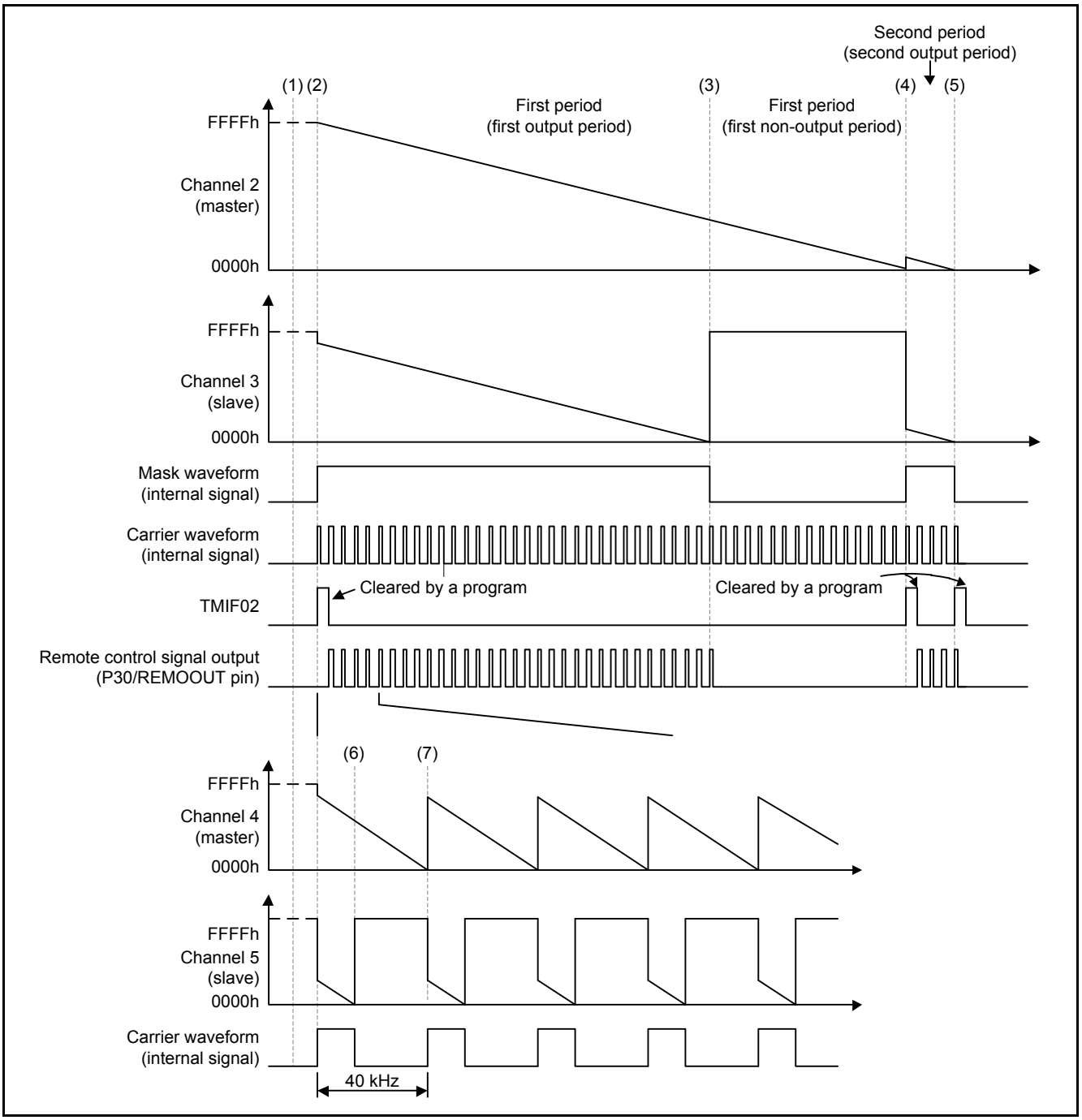


Figure 4.1 Behavior of Remote Control Output

(1) Detects a key has been pressed

RL78/L13 waits until the switch (SW1) connected to port P137 is pressed (low signal). RL78/L13 starts remote control output when it detects the key has been pressed.

(2) Remote control output is started

RL78/L13 starts remote control output. Set the count value of the first period in channels 4 (TDR04 register), 5 (TDR05 register), 2 (TDR02 register), and 3 (TDR03 register) to start timers on each channel. Then, set the count value of the second period in registers TDR02 and TDR03.

(3) Starts the first non-output period

When channel 3 underflows, the remote control output is stopped.

(4) Starts the second period

When the INTTM02 interrupt request is generated at the rising edge of the mask waveform, RL78/L13 starts remote control output in the second period. Set the TDR03 register to 0000H to stop the remote control output.

(5) Remote control output is stopped

When the INTTM02 interrupt request is generated at the rising edge of the mask waveform, the RL78/L13 waits until the INTTM05 interrupt request is generated, and stops timers for each channel.

(6) A carrier waveform (internal signal) is at low-level

When the count value of channel 5 underflows, RL78/L13 outputs the carrier waveform (internal signal) at low.

(7) A carrier waveform (internal signal) is at high-level

When channel 4 underflows, channel 5 starts counting and RL78/L13 outputs the carrier waveform (internal signal) at high.

4.2 Option Byte Settings

Table 4.1 lists the option byte settings.

Table 4.1 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Stops the watchdog timer (counting is stopped when a reset is canceled)
000C1H/010C1H	00011011B	Sets the LVD in reset mode Detection voltage: 1.77 V at the rising edge, 1.73 V at the falling edge
000C2H/010C2H	10101010B	Sets the high-speed on-chip oscillator clock to 8 MHz, and in LS (low-speed main) mode
000C3H/010C3H	10000100B	Enables on-chip debugging

4.3 Constants

Table 4.2 lists the constants used in the sample code.

Table 4.2 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
_112F_TAU_TDR02_VALUE	112FH	TDR02 register setting value
_1130_TAU_TDR03_VALUE	1130H	TDR03 register setting value
_0000_TAU_TDR03_VALUE	0	TDR03 register setting value
KEY_IN	P137	Key input port
KEY_OFF	1	Key input is off
KEY_ON	0	Key input is on

4.4 Functions

Table 4.3 lists the functions.

Table 4.3 Functions

Function Name	Outline
hdwinit	Initialization
R_Systeminit	Peripheral function initialization
R_CGC_Create	CPU clock initialization
R_TAU0_Create	TAU0 initialization
R_TAU0_Channel2_Start	TAU02 start setting
R_TAU0_Channel2_Stop	TAU02 stop setting
main	Main processing
R_MAIN_UserInit	Main initialization
remocon_transmit_control	Remote control output control processing

4.5 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initialization
Header	None
Declaration	void hdwinit(void)
Description	Initializes the peripheral functions.
Arguments	None
Return Value	None

R_Systeminit	
Outline	Peripheral function initialization
Header	None
Declaration	void R_Systeminit(void)
Description	Initializes the peripheral functions used in this application note.
Arguments	None
Return Value	None

R_CGC_Create	
Outline	CPU clock initialization
Header	r_cg_cgc.h
Declaration	void R_CGC_Create(void)
Description	Initializes the CPU clock.
Arguments	None
Return Value	None

R_TAU0_Create	
Outline	TAU0 initialization
Header	r_cg_tau.h
Declaration	void R_TAU0_Create(void)
Description	Initializes TAU0 to use as the remote control output function.
Arguments	None
Return Value	None

R_TAU0_Channel2_Start	
Outline	TAU02 start setting
Header	r_cg_tau.h
Declaration	void R_TAU0_Channel2_Start(void)
Description	Starts count of TAU0 channels 2 through 5.
Arguments	None
Return Value	None

R_TAU0_Channel2_Stop	
Outline	TAU02 stop setting
Header	r_cg_tau.h
Declaration	void R_TAU0_Channel2_Stop(void)
Description	Sets channels 2, 3, 4, and 5 of TAU0 to stop counting and outputting values.
Arguments	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Performs the main processing.
Arguments	None
Return Value	None

R_MAIN_UserInit	
Outline	Main initialization
Header	None
Declaration	void R_MAIN_UserInit(void)
Description	Performs processing required to initialize the main processing.
Arguments	None
Return Value	None

remocon_transmit_control	
Outline	Remote control output control processing
Header	None
Declaration	static void remocon_transmit_control(void)
Description	Controls the remote control output.
Arguments	None
Return Value	None

4.6 Flowcharts

4.6.1 Overall Flowchart

Figure 4.2 shows the overall flow.

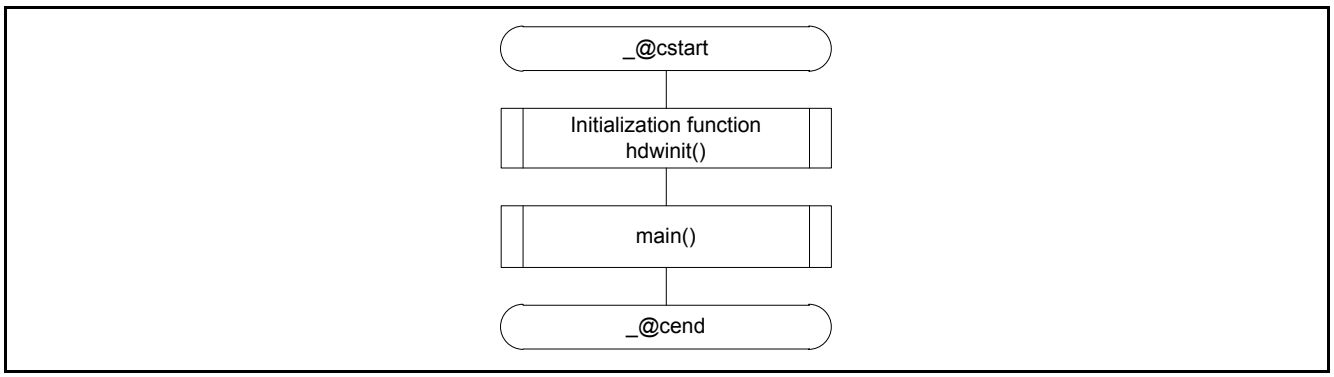


Figure 4.2 Overall Flow

4.6.2 Initialization

Figure 4.3 shows the initialization.

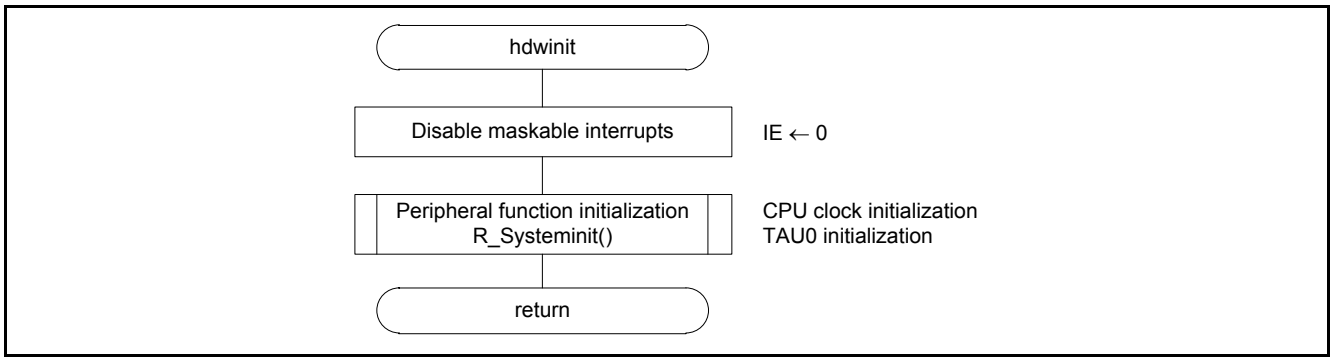


Figure 4.3 Initialization

4.6.3 Peripheral Function Initialization

Figure 4.4 shows the peripheral function initialization.

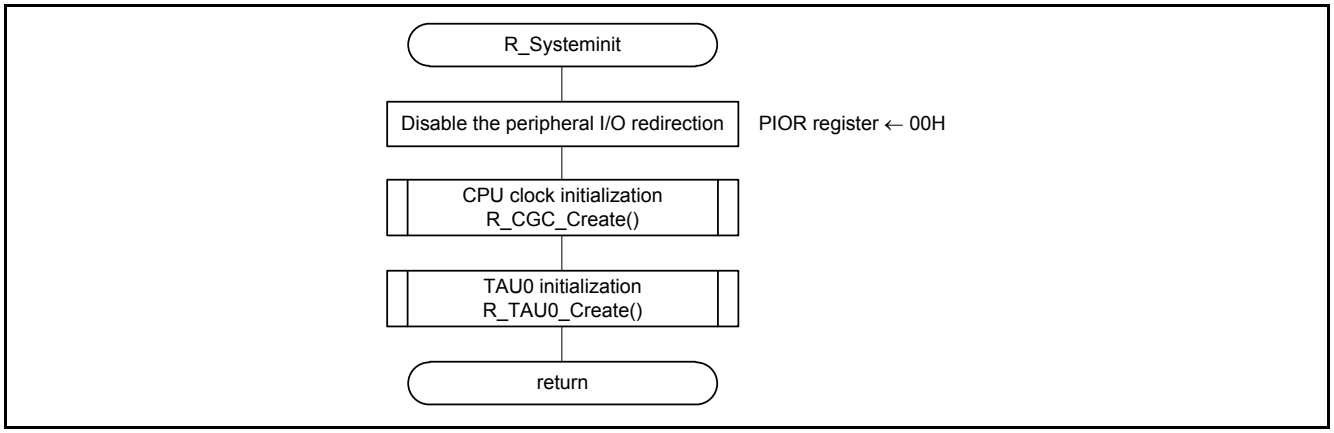


Figure 4.4 Peripheral Function Initialization

4.6.4 CPU Clock Initialization

Figure 4.5 shows the CPU clock initialization.

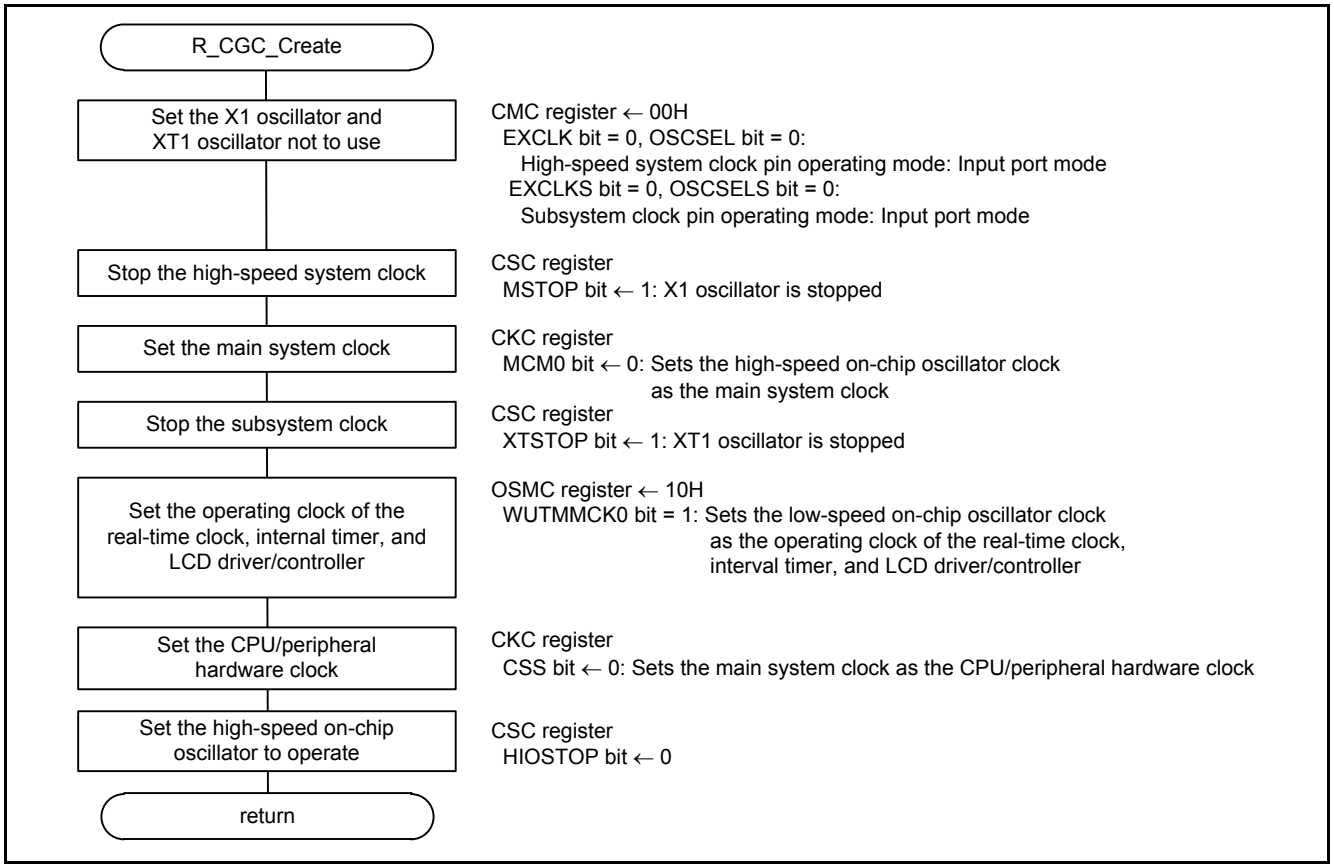


Figure 4.5 CPU Clock Initialization

4.6.5 TAU0 Initialization

Figure 4.6 to Figure 4.9 show TAU0 initialization.

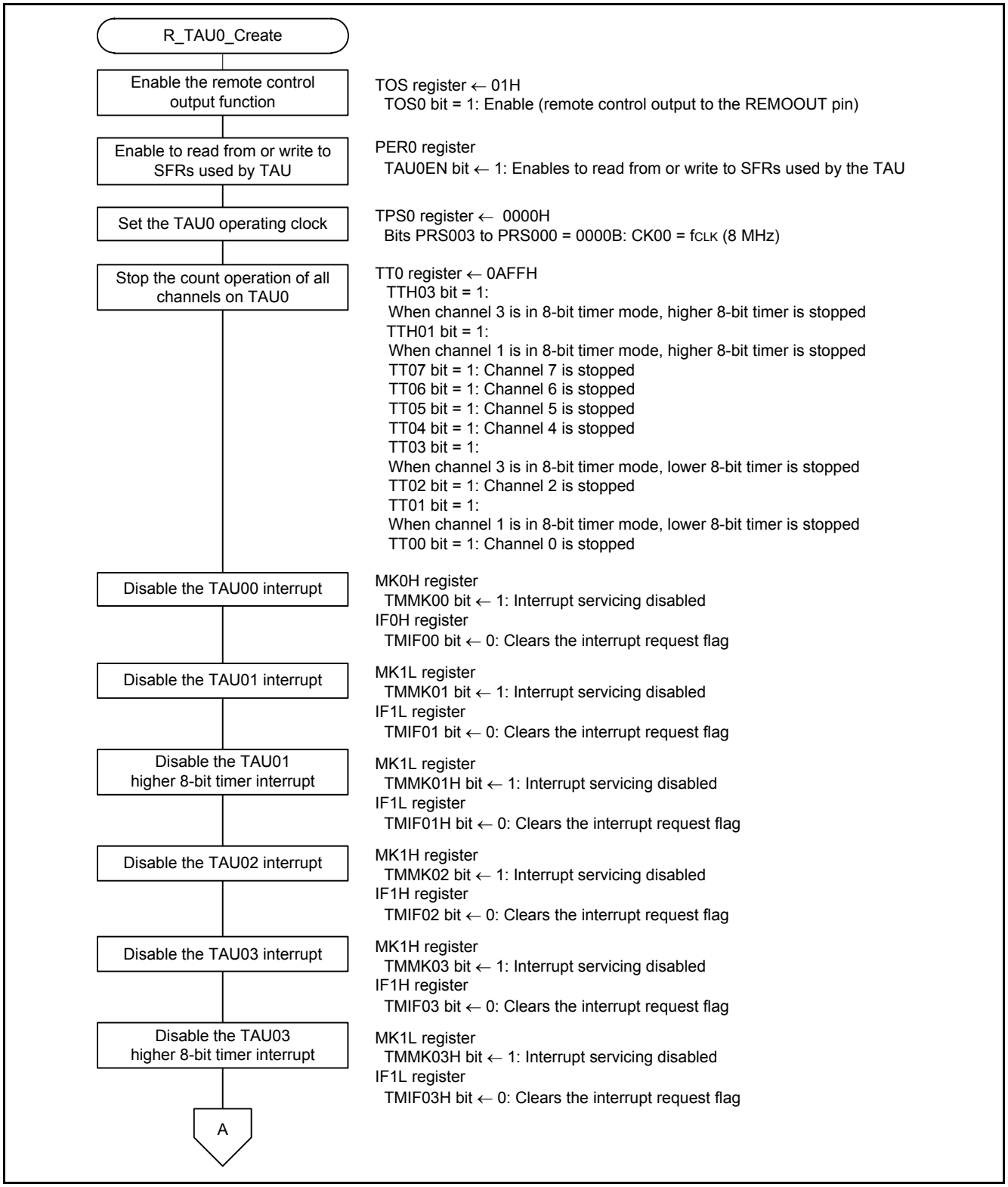


Figure 4.6 TAU0 Initialization (1/4)

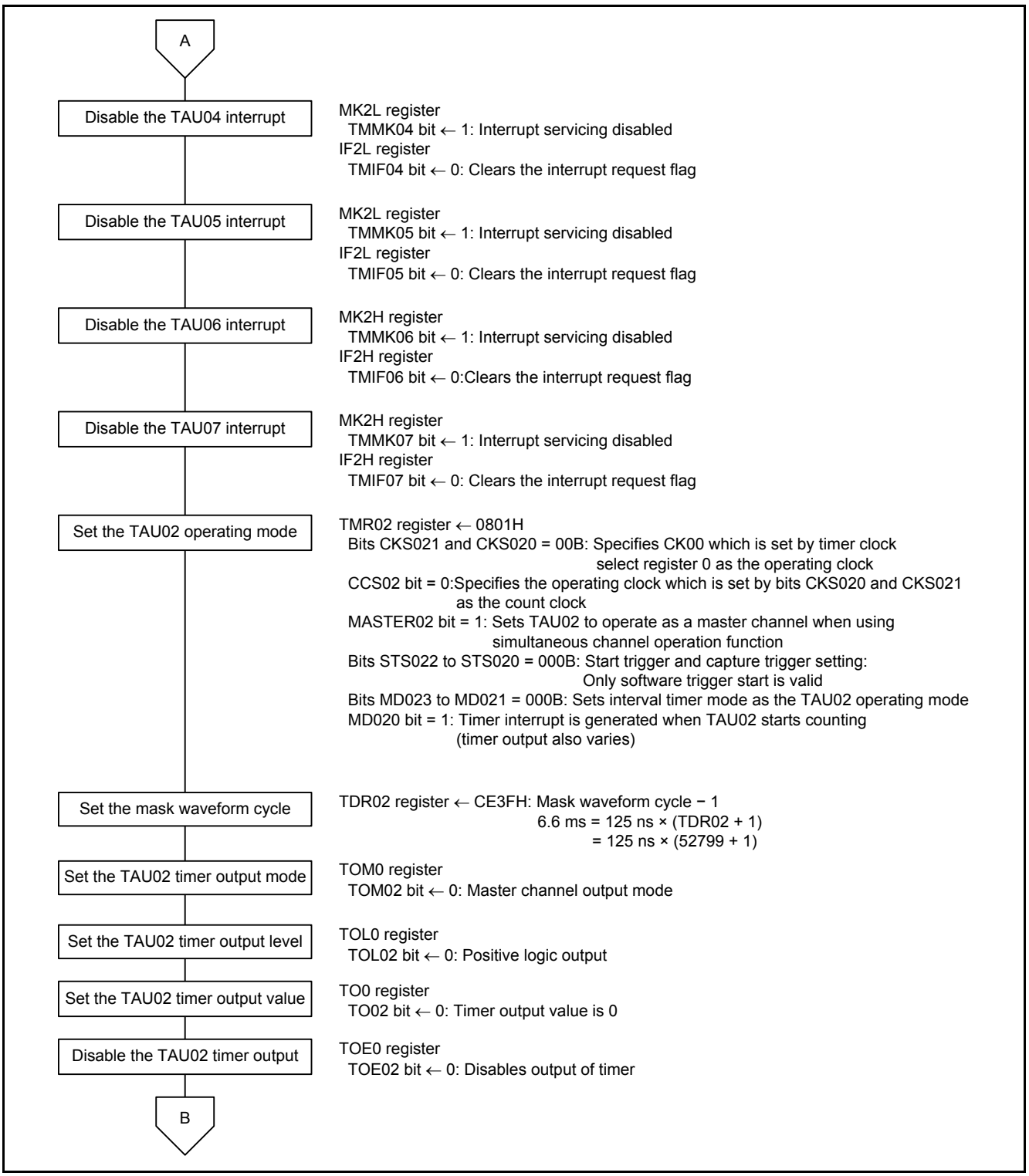


Figure 4.7 TAU0 Initialization (2/4)

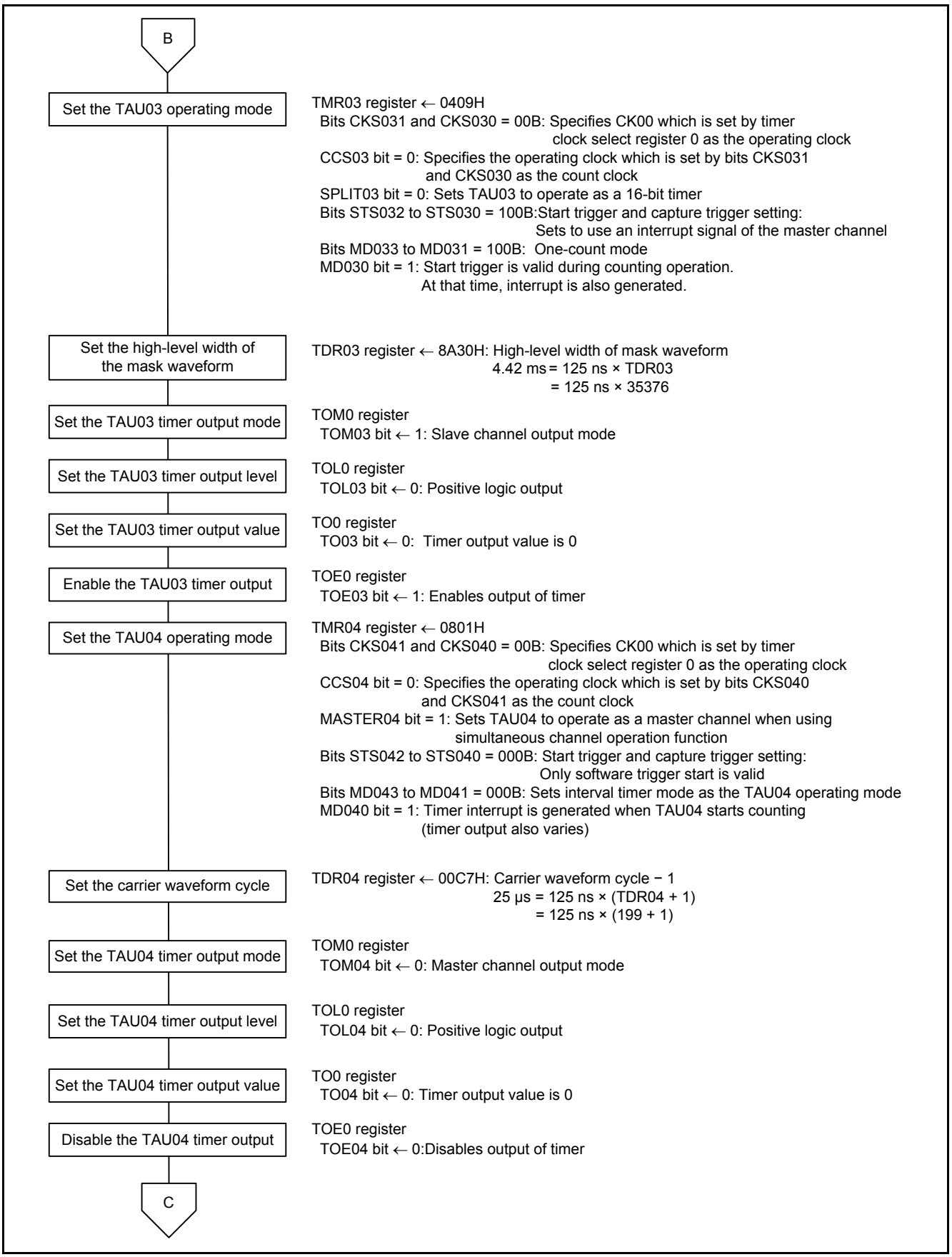


Figure 4.8 TAU0 Initialization (3/4)

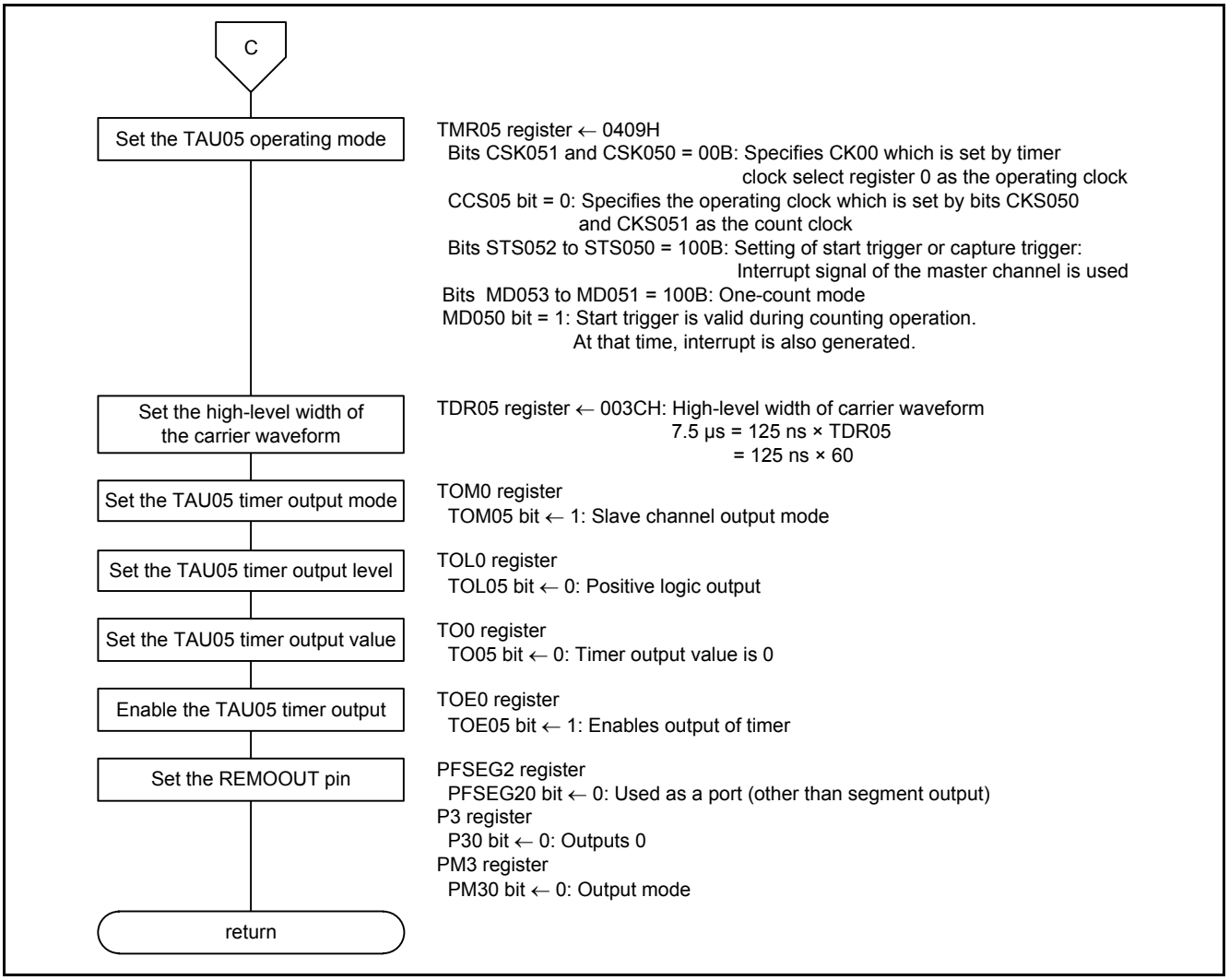


Figure 4.9 TAU0 Initialization (4/4)

Enabling the remote control output function

- Timer output select register (TOS)

Symbol	7	6	5	4	3	2	1	0
TOS	0	0	0	0	0	0	0	**TOS0**
Value	–	–	–	–	–	–	–	**1**

- Bit 0

TOS0 bit	Function
0	Disable (channels 2, 3, 4, and 5 are used for timer output)
1	Enable (remote control output to the REMOOUT pin)

Enabling to read from or write to SFRs used by TAU

- Peripheral enable register 0 (PER0)

Symbol	7	6	5	4	3	2	1	0
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	**TAU0EN**
Value	×	–	×	×	×	×	–	**1**

- Bit 0

TAU0EN bit	Function
0	Stops supplying an input clock • Writing to SFRs used by timer array unit is disabled • Timer array unit is in reset status
1	Enables supplying an input clock • Reading from or writing to SFRs used by timer array unit is enabled

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU0 operating clock

- Timer clock select register 0 (TPS0)

Sets the TAU0 operating clock to 8 MHz.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPS0	0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	**PRS 003**	**PRS 002**	**PRS 001**	**PRS 000**
Value	–	–	×	×	–	–	×	×	×	×	×	×	**0**	**0**	**0**	**0**

- Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000		Select the operating clock (CK00)				
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	24 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	46. 9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Stopping the count operation of all channels on TAU0

- Timer channel stop register 0 (TT0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT0	0	0	0	0	TTH03	0	TTH01	0	TT07	TT06	TT05	TT04	TT03	TT02	TT01	TT00
Value	–	–	–	–	1	–	1	–	1	1	1	1	1	1	1	1

- Bit 11

TTH03 bit	Function
0	No trigger operation
1	Operation is stopped (stop trigger is generated)

- Bit 9

TTH01 bit	Function
0	No trigger operation
1	Operation is stopped (stop trigger is generated)

- Bits 7 to 0

TT0n bit	Function (n = 0 to 7)
0	No trigger operation
1	Operation is stopped (stop trigger is generated) This bit is the trigger to stop operation of the lower 8-bit timer for TT01 and TT03 when channel 1 or 3 is in 8-bit timer mode.

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Disabling the TAU00 interrupt

- Interrupt mask flag register (MK0H)

Symbol	7	6	5	4	3	2	1	0
MK0H	SRMK0	**TMMK00**	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2	SRMK2	STMK2
Value	×	**1**	×	×	×	×	×	×

- Bit 6

TMMK00 bit	Function
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt request flag register (IF0H)

Symbol	7	6	5	4	3	2	1	0
IF0H	SRIF0	**TMIF00**	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2	SRIF2	STIF2
Value	×	**0**	×	×	×	×	×	×

- Bit 6

TMIF00 bit	Function
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Disabling the TAU01 interrupt

- Interrupt mask flag register (MK1L)

Symbol	7	6	5	4	3	2	1	0
MK1L	**TMMK01**	1	RTITMK	IICAMK0	SREMK1 TMMK03H	SRMK1	STMK1 CSIMK10 IICMK10	SREMK0 TMMK01H
Value	**1**	–	×	×		×	×	

- Bit 7

TMMK01 bit	Function
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt request flag register (IF1L)

Symbol	7	6	5	4	3	2	1	0
IF1L	**TMIF01**	0	RTITIF	IICAIF0	SREIF1 TMIF03H	SRIF1	STIF1 CSIIF10 IICIF10	SREIF0 TMIF01H
Value	**0**	–	×	×		×	×	

- Bit 7

TMIF01 bit	Function
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

Disabling the TAU01 higher 8-bit timer interrupt

- Interrupt mask flag register (MK1L)

Symbol	7	6	5	4	3	2	1	0
MK1L	TMMK01	1	RTITMK	IICAMK0	SREMK1 TMMK03H	SRMK1	STMK1 CSIMK10 IICMK10	SREMK0 **TMMK01H**
Value		–	×	×		×	×	**1**

- Bit 0

TMMK01H bit	Function
0	Interrupt servicing enabled
1	Interrupt servicing disabled

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Interrupt request flag register (IF1L)

Symbol	7	6	5	4	3	2	1	0
IF1L	TMIF01	0	RTITIF	IICAIF0	SREIF1 TMIF03H	SRIF1	STIF1 CSIIF10 IICIF10	SREIF0 **TMIF01H**
Value		–	×	×		×	×	**0**

- Bit 0

TMIF01H bit	**Function**
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

Disabling the TAU02 interrupt

- Interrupt mask flag register (MK1H)

Symbol	7	6	5	4	3	2	1	0
MK1H	SRMK3	STMK3	KRMK	TMKAMK	RTCMK	ADMK	TMMK03	**TMMK02**
Value	×	×	×	×	×	×		**1**

- Bit 0

TMMK02 bit	**Function**
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt request flag register (IF1H)

Symbol	7	6	5	4	3	2	1	0
IF1H	SRIF3	STIF3	KRIF	TMKAIF	RTCIF	ADIF	TMIF03	**TMIF02**
Value	×	×	×	×	×	×		**0**

- Bit 0

TMIF02 bit	**Function**
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Disabling the TAU03 interrupt

- Interrupt mask flag register (MK1H)

Symbol	7	6	5	4	3	2	1	0
MK1H	SRMK3	STMK3	KRMK	TMKAMK	RTCMK	ADMK	**TMMK03**	TMMK02
Value	×	×	×	×	×	×	**1**	

- Bit 1

TMMK03 bit	**Function**
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt request flag register (IF1H)

Symbol	7	6	5	4	3	2	1	0
IF1H	SRIF3	STIF3	KRIF	TMKAIF	RTCIF	ADIF	**TMIF03**	TMIF02
Value	×	×	×	×	×	×	**0**	

- Bit 1

TMIF03 bit	**Function**
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

Disabling the TAU03 higher 8-bit timer interrupt

- Interrupt mask flag register (MK1L)

Symbol	7	6	5	4	3	2	1	0
MK1L	TMMK01	1	RTITMK	IICAMK0	SREMK1 **TMMK03H**	SRMK1	STMK1 CSIMK10 IICMK10	SREMK0 TMMK01H
Value		–	×	×	**1**	×	×	

- Bit 3

TMMK03H bit	**Function**
0	Interrupt servicing enabled
1	Interrupt servicing disabled

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Interrupt request flag register (IF1L)

Symbol	7	6	5	4	3	2	1	0
IF1L	TMIF01	0	RTITIF	IICAIF0	SREIF1 **TMIF03H**	SRIF1	STIF1 CSIIF10 IICIF10	SREIF0 TMIF01H
Value		–	×	×	**0**	×	×	

- Bit 3

TMIF03H bit	Function
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

Disabling the TAU04 interrupt

- Interrupt mask flag register (MK2L)

Symbol	7	6	5	4	3	2	1	0
MK2L	CMPMK1	CMPMK0	LCDMK0	PMK7	PMK6	TMMK05	**TMMK04**	TKBMK20
Value	×	×	×	×	×		**1**	×

- Bit 1

TMMK04 bit	Function
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt request flag register (IF2L)

Symbol	7	6	5	4	3	2	1	0
IF2L	CMPIF1	CMPIF0	LCDIF0	PIF7	PIF6	TMIF05	**TMIF04**	TKBIF20
Value	×	×	×	×	×		**0**	×

- Bit 1

TMIF04 bit	Function
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Disabling the TAU05 interrupt

- Interrupt mask flag register (MK2L)

Symbol	7	6	5	4	3	2	1	0
MK2L	CMPMK1	CMPMK0	LCDMK0	PMK7	PMK6	**TMMK05**	TMMK04	TKBMK20
Value	×	×	×	×	×	**1**		×

- Bit 2

TMMK05 bit	Function
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt request flag register (IF2L)

Symbol	7	6	5	4	3	2	1	0
IF2L	CMPIF1	CMPIF0	LCDIF0	PIF7	PIF6	**TMIF05**	TMIF04	TKBIF20
Value	×	×	×	×	×	**0**		×

- Bit 2

TMIF05 bit	Function
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

Disabling the TAU06 interrupt

- Interrupt mask flag register (MK2H)

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	1	MDMK	SREMK3	1	1	TMMK07	**TMMK06**
Value	×	–	×	×	–	–		**1**

- Bit 2

TMMK06 bit	Function
0	Interrupt servicing enabled
1	Interrupt servicing disabled

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Interrupt request flag register (IF2H)

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	0	MDIF	SREIF3	0	0	TMIF07	**TMIF06**
Value	×	–	×	×	–	–		**0**

- Bit 0

TMIF06 bit	**Function**
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

Disabling the TAU07 interrupt

- Interrupt mask flag register (MK2H)

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	1	MDMK	SREMK3	1	1	**TMMK07**	TMMK06
Value	×	–	×	×	–	–	**1**	

- Bit 1

TMMK07 bit	**Function**
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt request flag register (IF2H)

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	0	MDIF	SREIF3	0	0	**TMIF07**	TMIF06
Value	×	–	×	×	–	–	**0**	

- Bit 1

TMIF07 bit	**Function**
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU02 operating mode

- Timer mode register 02 (TMR02)
  - Operating clock (f_{MCK}): CK00
  - Count clock (f_{TCLK}): f_{MCK}
  - TAU02 operates as: Master channel when using simultaneous channel operation function
  - Start trigger: Only software trigger start is valid
  - Operating mode: Interval timer mode (timer interrupt is generated when TAU02 starts counting)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR02	CKS021	CKS020	0	CCS02	MASTER02	STS022	STS021	STS020	CIS021	CIS020	0	0	MD023	MD022	MD021	MD020
Value	0	0	–	0	1	0	0	0	×	×	–	–	0	0	0	1

- Bits 15 and 14

CKS021 bit	CKS020 bit	Function
0	0	Operating clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operating clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operating clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operating clock CK03 set by timer clock select register 0 (TPS0)
Operating clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated according to the setting of the CCS00 bit. Operating clocks CK02 and CK03 can only be selected on channels 1 and 3.		

- Bit 12

CCS02 bit	Function
0	Operating clock (f_{MCK}) specified by bits CKS020 and CKS021
1	Valid edge of the input signal input from the TI02 pin
Count clock (f_{TCLK}) is used by the timer counter, output controller, and interrupt controller.	

- Bit 11

MASTER02 bit	Function
0	Operates in independent channel operation function or as a slave channel in simultaneous channel operation function
1	Operates as the master channel in simultaneous channel operation function

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Bits 10 to 8

STS 022	STS 021	STS 020	Function
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	0	1	Valid edge of the TI02 pin input is used as both the start trigger and capture trigger
0	1	0	Both edges of the TI02 pin input are used as a start trigger and a capture trigger
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function)
Other than above			Setting prohibited

- Bits 3 to 1

MD 023	MD 022	MD 021	Function	Corresponding function	TCR operation
0	0	0	Interval timer mode	Interval timer, square wave output, PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter, one-shot pulse output, PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Bit 0

Operating mode (Value set by bits MD023 to MD021, see the previous table)	MD 020	Function
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when TAU02 starts counting (timer output does not vary, either).
	1	Timer interrupt is generated when TAU02 starts counting (timer output also varies).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when TAU02 starts counting (timer output does not vary, either)
• One-count mode (1, 0, 0)	0	Start trigger is invalid while TAU02 is counting. At that time, interrupt is not generated, either.
	1	Start trigger is valid while TAU02 is counting. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when TAU02 starts counting (timer output does not vary, either). Start trigger is invalid while TAU02 is counting. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Setting the mask waveform cycle

- Timer data register 02 (TDR02)

Sets the mask waveform cycle to 6.6 ms.

[6.6 ms = 1/f_{TCLK} × (TDR02 + 1) = 1/8 MHz × (52799 + 1)]

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR02	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	CE3FH (52799)															

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU02 timer output mode

- Timer output mode register 0 (TOM0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOM0	0	0	0	0	0	0	0	0	TOM 07	TOM 06	TOM 05	TOM 04	TOM 03	**TOM 02**	TOM 01	**0**
Value	–	–	–	–	–	–	–	–	×	×				**0**	×	–

- Bit 2

TOM02 bit	Function
0	Master channel output mode (to produce toggle output by timer interrupt request signal, INTTM02)
1	Slave channel output mode (output is set by timer interrupt request signal INTTM02 of the master channel, and reset by timer interrupt request signal INTTM0p of the slave channel) (p is greater than 2 and less than or equal to 7)

Setting the TAU02 timer output level

- Timer output level register 0 (TOL0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOL0	0	0	0	0	0	0	0	0	TOL 07	TOL 06	TOL 05	TOL 04	TOL 03	**TOL 02**	TOL 01	**0**
Value	–	–	–	–	–	–	–	–	×	×				**0**	×	–

- Bit 2

TOL02 bit	Function
0	Positive logic output (high active)
1	Negative logic output (low active)

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU02 timer output value

- Timer output register 0 (TO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO0	0	0	0	0	0	0	0	0	TO07	TO06	TO05	TO04	TO03	**TO02**	TO01	TO00
Value	–	–	–	–	–	–	–	–	×	×				**0**	×	×

- Bit 2

TO02 bit	Function
0	Timer output value is 0
1	Timer output value is 1

Disabling the TAU02 timer output

- Timer output enable register 0 (TOE0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	TOE 07	TOE 06	TOE 05	TOE 04	TOE 03	**TOE 02**	TOE 01	TOE 00
Value	–	–	–	–	–	–	–	–	×	×				**0**	×	×

- Bit 2

TOE02 bit	Function
0	Disables output of timer. Output is fixed without reflecting the timer operation on the TO02 bit. Writing to the TO02 bit is enabled.
1	Enables output of timer. Reflects the timer operation on the TO02 bit, and generates an output waveform. Writing to the TO02 bit is ignored.

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU03 operating mode

- Timer mode register 03 (TMR03)
  - Operating clock (f_{MCK}): CK00
  - Count clock (f_{TCLK}): f_{MCK}
  - TAU03 operates as: 16-bit timer
  - Start trigger: Interrupt signal of the master channel is used
  - Operating mode: One-count mode (Start trigger while TAU03 is counting is valid)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR03	CKS 031	CKS 030	0	CCS 03	SPLIT 03	STS 032	STS 031	STS 030	CIS 031	CIS 030	0	0	MD 033	MD 032	MD 031	MD 030
Value	0	0	–	0	0	1	0	0	×	×	–	–	1	0	0	1

- Bits 15 and 14

CKS031 bit	CKS030 bit	Function
0	0	Operating clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operating clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operating clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operating clock CK03 set by timer clock select register 0 (TPS0)
Operating clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated according to the setting of the CCS00 bit. Operating clocks CK02 and CK03 can only be selected on channels 1 and 3.		

- Bit 12

CCS03 bit	Function
0	Operating clock (f_{MCK}) specified by bits CKS030 and CKS031
1	Valid edge of the input signal input from the TI03 pin
Count clock (f_{TCLK}) is used by the timer counter, output controller, and interrupt controller.	

- Bit 11

SPLIT03 bit	Function
0	Operates as a 16-bit timer (Operates in independent channel operation function or as a slave channel in simultaneous channel operation function)
1	Operates as an 8-bit timer

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Bits 10 to 8

STS 032	STS 031	STS 030	Function
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	0	1	Valid edge of the TI03 pin input is used as both the start trigger and capture trigger
0	1	0	Both edges of the TI03 pin input are used as a start trigger and a capture trigger
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function)
Other than above			Setting prohibited

- Bits 3 to 1

MD 033	MD 032	MD 031	Function	Corresponding function	TCR operation
0	0	0	Interval timer mode	Interval timer, square wave output, PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter, one-shot pulse output, PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Bit 0

Operating mode (Value set by bits MD033 to MD031, see the previous table)	MD 030	Function
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when TAU03 starts counting (timer output does not vary, either).
	1	Timer interrupt is generated when TAU03 starts counting (timer output also varies).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when TAU03 starts counting (timer output does not vary, either)
• One-count mode (1, 0, 0)	0	Start trigger is invalid while TAU03 is counting. At that time, interrupt is not generated, either.
	1	Start trigger is valid while TAU03 is counting. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when TAU03 starts counting (timer output does not vary, either). Start trigger is invalid while TAU03 is counting. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Setting the high-level width of the mask waveform

- Timer data register 03 (TDR03)

Sets the high-level width of the mask waveform to 4.42 ms.

(4.42 ms = 1/f_{TCLK} × TDR03 = 1/8 MHz × 35376)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR03	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	8A30H (35376)															

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU03 timer output mode

- Timer output mode register 0 (TOM0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOM0	0	0	0	0	0	0	0	0	TOM 07	TOM 06	TOM 05	TOM 04	**TOM 03**	TOM 02	TOM 01	**0**
Value	–	–	–	–	–	–	–	–	×	×			**1**		×	–

- Bit 3

TOM03 bit	Function
0	Master channel output mode (to produce toggle output by timer interrupt request signal, INTTM03)
1	Slave channel output mode (output is set by timer interrupt request signal INTTM03 of the master channel, and reset by timer interrupt request signal INTTM0p of the slave channel) (p is greater than 3 and less than or equal to 7)

Setting the TAU03 timer output level

- Timer output level register 0 (TOL0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOL0	0	0	0	0	0	0	0	0	TOL 07	TOL 06	TOL 05	TOL 04	**TOL 03**	TOL 02	TOL 01	**0**
Value	–	–	–	–	–	–	–	–	×	×			**0**		×	–

- Bit 3

TOL03 bit	Function
0	Positive logic output (high active)
1	Negative logic output (low active)

Setting the TAU03 timer output value

- Timer output register 0 (TO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO0	0	0	0	0	0	0	0	0	TO07	TO06	TO05	TO04	**TO03**	TO02	TO01	TO00
Value	–	–	–	–	–	–	–	–	×	×			**0**		×	×

- Bit 3

TO03 bit	Function
0	Timer output value is 0
1	Timer output value is 1

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Enabling the TAU03 timer output

- Timer output enable register 0 (TOE0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	TOE 07	TOE 06	TOE 05	TOE 04	**TOE 03**	TOE 02	TOE 01	TOE 00
Value	–	–	–	–	–	–	–	–	×	×			**1**		×	×

- Bit 3

TOE03 bit	Function
0	Disables output of timer. Output is fixed without reflecting the timer operation on the TO03 bit. Writing to the TO03 bit is enabled.
1	Enables output of timer. Reflects the timer operation on the TO03 bit, and generates an output waveform. Writing to the TO03 bit is ignored.

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU04 operating mode

- Timer mode register 04 (TMR04)
  - Operating clock (f_{MCK}): CK00
  - Count clock (f_{TCLK}): f_{MCK}
  - TAU03 operates as: Master channel when using simultaneous channel operation function
  - Start trigger: Only software trigger start is valid
  - Operating mode: Interval timer mode (Timer interrupt is generated when TAU04 starts counting)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR04	CKS 041	CKS 040	0	CCS 04	MASTER 04	STS 042	STS 041	STS 040	CIS 041	CIS 040	0	0	MD 043	MD 042	MD 041	MD 040
Value	0	0	–	0	1	0	0	0	×	×	–	–	0	0	0	1

- Bits 15 and 14

CKS041 bit	CKS040 bit	Function
0	0	Operating clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operating clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operating clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operating clock CK03 set by timer clock select register 0 (TPS0)
Operating clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated according to the setting of the CCS00 bit. Operating clocks CK02 and CK03 can only be selected on channels 1 and 3.		

- Bit 12

CCS04 bit	Function
0	Operating clock (f_{MCK}) specified by bits CKS040 and CKS041
1	Valid edge of the input signal input from the TI04 pin
Count clock (f_{TCLK}) is used by the timer counter, output controller, and interrupt controller.	

- Bit 11

MASTER04 bit	Function
0	Operates in independent channel operation function or as a slave channel in simultaneous channel operation function
1	Operates as the master channel in simultaneous channel operation function

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Bits 10 to 8

STS 042	STS 041	STS 040	Function
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	0	1	Valid edge of the TI04 pin input is used as both the start trigger and capture trigger
0	1	0	Both edges of the TI04 pin input are used as a start trigger and a capture trigger
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function)
Other than above			Setting prohibited

- Bits 3 to 1

MD 043	MD 042	MD 041	Function	Corresponding function	TCR operation
0	0	0	Interval timer mode	Interval timer, square wave output, PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter, one-shot pulse output, PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Bit 0

Operating mode (Value set by bits MD043 to MD041, see the previous table)	MD 040	Function
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when TAU04 starts counting (timer output does not vary, either).
	1	Timer interrupt is generated when TAU04 starts counting (timer output also varies).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when TAU04 starts counting (timer output does not vary, either)
• One-count mode (1, 0, 0)	0	Start trigger is invalid while TAU04 is counting. At that time, interrupt is not generated, either.
	1	Start trigger is valid while TAU04 is counting. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when TAU04 starts counting (timer output does not vary, either). Start trigger is invalid while TAU04 is counting. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Setting the carrier waveform cycle

- Timer data register 04 (TDR04)

Sets the carrier waveform cycle to 25 μs.

[25 μs = 1/f_{TCLK} × (TDR04 + 1) = 1/8 MHz × (199 + 1)]

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR04	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	00C7H (199)															

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU04 timer output mode

- Timer output mode register 0 (TOM0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOM0	0	0	0	0	0	0	0	0	TOM 07	TOM 06	TOM 05	**TOM 04**	TOM 03	TOM 02	TOM 01	**0**
Value	–	–	–	–	–	–	–	–	×	×		**0**			×	–

- Bit 4

TOM04 bit	Function
0	Master channel output mode (to produce toggle output by timer interrupt request signal, INTTM04)
1	Slave channel output mode (output is set by timer interrupt request signal INTTM04 of the master channel, and reset by timer interrupt request signal INTTM0p of the slave channel) (p is greater than 4 and less than or equal to 7)

Setting the TAU04 timer output level

- Timer output level register 0 (TOL0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOL0	0	0	0	0	0	0	0	0	TOL 07	TOL 06	TOL 05	**TOL 04**	TOL 03	TOL 02	TOL 01	**0**
Value	–	–	–	–	–	–	–	–	×	×		**0**			×	–

- Bit 4

TOL04 bit	Function
0	Positive logic output (high active)
1	Negative logic output (low active)

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU04 timer output value

- Timer output register 0 (TO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO0	0	0	0	0	0	0	0	0	TO07	TO06	TO05	**TO04**	TO03	TO02	TO01	TO00
Value	–	–	–	–	–	–	–	–	×	×		**0**			×	×

- Bit 4

TO04 bit	Function
0	Timer output value is 0
1	Timer output value is 1

Disabling the TAU04 timer output

- Timer output enable register 0 (TOE0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	TOE 07	TOE 06	TOE 05	**TOE 04**	TOE 03	TOE 02	TOE 01	TOE 00
Value	–	–	–	–	–	–	–	–	×	×		**0**			×	×

- Bit 4

TOE04 bit	Function
0	Disables output of timer. Output is fixed without reflecting the timer operation on the TO04 bit. Writing to the TO04 bit is enabled.
1	Enables output of timer. Reflects the timer operation on the TO04 bit, and generates an output waveform. Writing to the TO04 bit is ignored.

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU05 operating mode

- Timer mode register 05 (TMR05)
  - Operating clock (f_{MCK}): CK00
  - Count clock (f_{TCLK}): f_{MCK}
  - Start trigger: Interrupt signal of the master channel is used
  - Operating mode: One-count mode (Start trigger while TAU05 is counting is valid)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR05	CKS 051	CKS 050	0	CCS 05	0	STS 052	STS 051	STS 050	CIS 051	CIS 050	0	0	MD 053	MD 052	MD 051	MD 050
Value	0	0	–	0	–	1	0	0	×	×	–	–	1	0	0	1

- Bits 15 and 14

CKS051 bit	CKS050 bit	Function
0	0	Operating clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operating clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operating clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operating clock CK03 set by timer clock select register 0 (TPS0)
Operating clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated according to the setting of the CCS00 bit. Operating clocks CK02 and CK03 can only be selected on channels 1 and 3.		

- Bit 12

CCS05 bit	Function
0	Operating clock (f_{MCK}) specified by bits CKS050 and CKS051
1	Valid edge of the input signal input from the TI05 pin
Count clock (f_{TCLK}) is used by the timer counter, output controller, and interrupt controller.	

- Bits 10 to 8

STS 052	STS 051	STS 050	Function
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	0	1	Valid edge of the TI03 pin input is used as both the start trigger and capture trigger
0	1	0	Both edges of the TI03 pin input are used as a start trigger and a capture trigger
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function)
Other than above			Setting prohibited

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Bits 3 to 1

MD 053	MD 052	MD 051	Function	Corresponding function	TCR operation
0	0	0	Interval timer mode	Interval timer, square wave output, PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter, one-shot pulse output, PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		

- Bit 0

Operating mode (Value set by bits MD053 to MD051, see the previous table)	MD 050	Function
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when TAU05 starts counting (timer output does not vary, either).
	1	Timer interrupt is generated when TAU05 starts counting (timer output also varies).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when TAU05 starts counting (timer output does not vary, either)
• One-count mode (1, 0, 0)	0	Start trigger is invalid while TAU05 is counting. At that time, interrupt is not generated, either.
	1	Start trigger is valid while TAU05 is counting. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when TAU05 starts counting (timer output does not vary, either). Start trigger is invalid while TAU05 is counting. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the high-level width of the carrier waveform

- Timer data register 05 (TDR05)

Sets the high-level width of the carrier waveform to 7.5 μs.

(7.5 μs = 1/fCLK ×TDR05 = 1/8 MHz × 60)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR05	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	003CH (60)															

Setting the TAU05 timer output mode

- Timer output mode register 0 (TOM0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOM0	0	0	0	0	0	0	0	0	TOM 07	TOM 06	**TOM 05**	TOM 04	TOM 03	TOM 02	TOM 01	0
Value	–	–	–	–	–	–	–	–	×	×	**1**				×	

- Bit 5

TOM05 bit	Function
0	Master channel output mode (to produce toggle output by timer interrupt request signal, INTTM05)
1	Slave channel output mode (output is set by timer interrupt request signal INTTM05 of the master channel, and reset by timer interrupt request signal INTTM0p of the slave channel) (p is greater than 5 and less than or equal to 7)

Setting the TAU05 timer output level

- Timer output level register 0 (TOL0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOL0	0	0	0	0	0	0	0	0	TOL 07	TOL 06	**TOL 05**	TOL 04	TOL 03	TOL 02	TOL 01	0
Value	–	–	–	–	–	–	–	–	×	×	**0**				×	–

- Bit 5

TOL05 bit	Function
0	Positive logic output (high active)
1	Negative logic output (low active)

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the TAU05 timer output value

- Timer output register 0 (TO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO0	0	0	0	0	0	0	0	0	TO07	TO06	**TO05**	TO04	TO03	TO02	TO01	TO00
Value	–	–	–	–	–	–	–	–	×	×	**0**				×	×

- Bit 5

TO05 bit	Function
0	Timer output value is 0
1	Timer output value is 1

Enabling the TAU05 timer output

- Timer output enable register 0 (TOE0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	TOE 07	TOE 06	**TOE 05**	TOE 04	TOE 03	TOE 02	TOE 01	TOE 00
Value	–	–	–	–	–	–	–	–	×	×	**1**				×	×

- Bit 5

TOE05 bit	Function
0	Disables output of timer. Output is fixed without reflecting the timer operation on the TO05 bit. Writing to the TO05 bit is enabled.
1	Enables output of timer. Reflects the timer operation on the TO05 bit, and generates an output waveform. Writing to the TO05 bit is ignored.

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the REMOOUT pin

- LCD port function register 2 (PFSEG2)

Symbol	7	6	5	4	3	2	1	0
PFSEG2	PFSEG23	PFSEG22	PFSEG21	**PFSEG20**	PFSEG19	PFSEG18	PFSEG17	PFSEG16
Value	×	×	×	**0**	×	×	×	×

- Bit 4

PFSEG20 bit	Function
0	P30 pin is used as a port (other than segment output)
1	P30 is used as segment output

- Port register 3 (P3)

Symbol	7	6	5	4	3	2	1	0
P3	0	0	P35	P34	P33	P32	P31	**P30**
Value	–	–	×	×	×	×	×	**0**

- Bit 0

P30 bit	Function
0	Outputs 0
1	Outputs 1

- Port mode register 3 (PM3)

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	PM35	PM34	PM3	PM32	PM31	**PM30**
Value	–	–	×	×	×	×	×	**0**

- Bit 0

PM30 bit	Function
0	Output mode (output buffer on)
1	Input mode (output buffer off)

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.6.6 TAU02 Start Setting

Figure 4.10 shows TAU02 start setting.

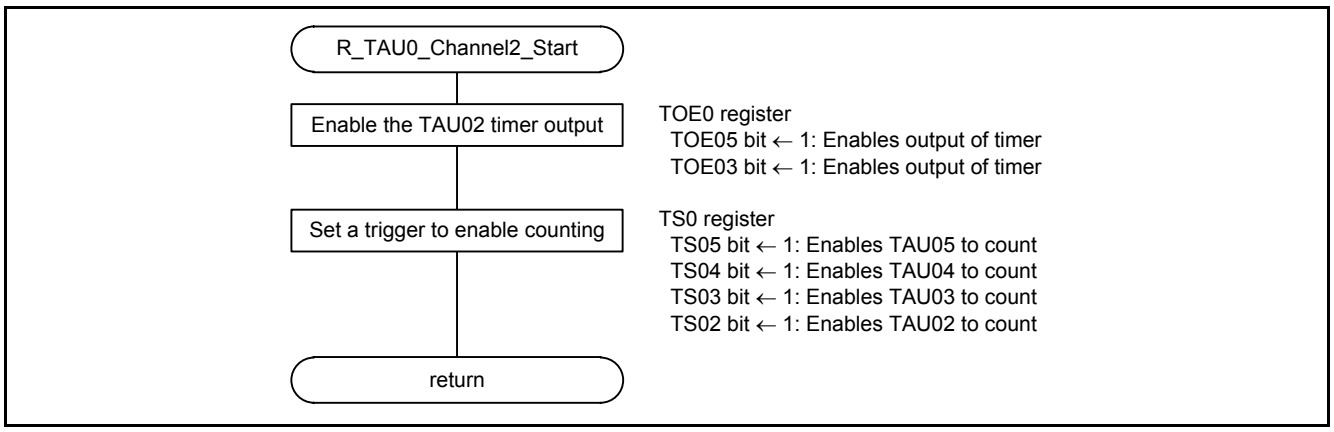


Figure 4.10 TAU02 Start Setting

Enabling the TAU02 timer output

- Timer output enable register 0 (TOE0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	TOE 07	TOE 06	**TOE 05**	TOE 04	**TOE 03**	TOE 02	TOE 01	TOE 00
Value	–	–	–	–	–	–	–	–	×	×	**1**		**1**		×	×

- Bits 5 and 3

TOE0n bit	Function (n = 3 and 5)
0	Disables output of timer. Output is fixed without reflecting the timer operation on the TO0n bit. Writing to the TO0n bit is enabled.
1	Enables output of timer. Reflects the timer operation on the TO0n bit, and generates an output waveform. Writing to the TO0n bit is ignored.

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting a trigger to enable counting

- Timer channel start register 0 (TS0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS0	0	0	0	0	TSH 03	0	TSH 01	0	TS07	TS06	**TS05**	**TS04**	**TS03**	**TS02**	TS01	TS00
Value	–	–	–	–	×	–	×	–	×	×	**1**	**1**	**1**	**1**	×	×

- Bits 5 to 2

TS0n bit	Function (n = 2 to 5)
0	No trigger operation
1	The TE0n bit is set to 1 and count operation is enabled.

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.6.7 TAU02 Stop Setting

Figure 4.11 shows TAU02 stop setting.

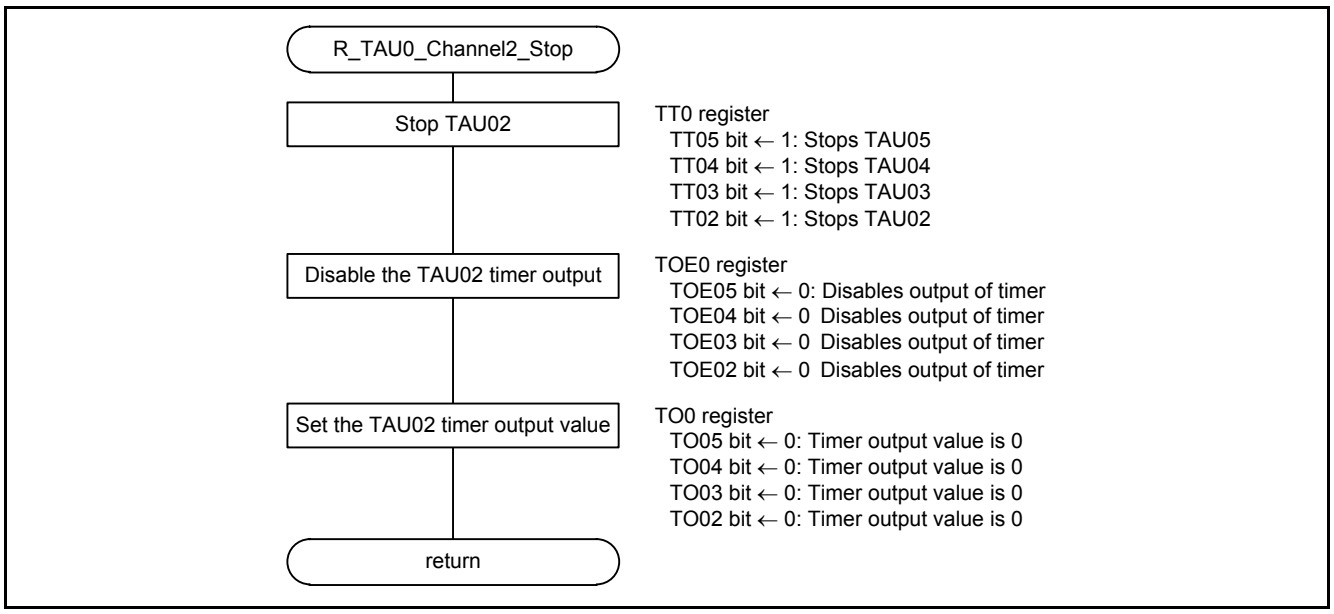


Figure 4.11 TAU02 Stop Setting

Stopping TAU02

- Timer channel stop register 0 (TT0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT0	0	0	0	0	TTH 03	0	TTH 01	0	TT 07	TT 06	**TT 05**	**TT 04**	**TT 03**	**TT 02**	TT 01	TT 00
Value	–	–	–	–	×	–	×	–	×	×	**1**	**1**	**1**	**1**	×	×

- Bits 5 to 2

TT0n bit	Function (n = 2 to 5)
0	No trigger operation
1	Operation is stopped (stop trigger is generated) This bit is the trigger to stop operation of the lower 8-bit timer for TT01 and TT03 when channel 1 or 3 is in 8-bit timer mode.

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Disabling the TAU02 timer output

- Timer output enable register 0 (TOE0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	TOE 07	TOE 06	**TOE 05**	**TOE 04**	**TOE 03**	**TOE 02**	TOE 01	TOE 00
Value	–	–	–	–	–	–	–	–	×	×	**0**	**0**	**0**	**0**	×	×

- Bits 5 to 2

TOE0n bit	Function (n = 2 to 5)
0	Disables output of timer. Output is fixed without reflecting the timer operation on the TO0n bit. Writing to the TO0n bit is enabled.
1	Enables output of timer. Reflects the timer operation on the TO0n bit, and generates an output waveform. Writing to the TO0n bit is ignored.

Setting the TAU02 timer output value

- Timer output register 0 (TO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO0	0	0	0	0	0	0	0	0	TO07	TO06	**TO05**	**TO04**	**TO03**	**TO02**	TO01	TO00
Value	–	–	–	–	–	–	–	–	×	×	**0**	**0**	**0**	**0**	×	×

- Bits 5 to 2

TO0n bit	Function
0	Timer output value is 0
1	Timer output value is 1

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.6.8 Main Processing

Figure 4.12 shows the main processing.

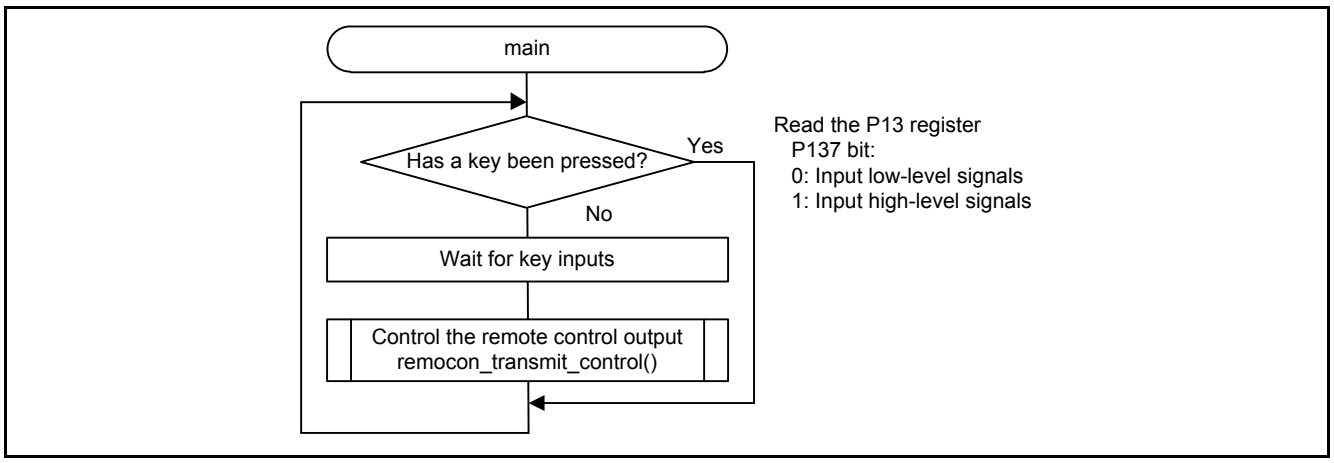


Figure 4.12 Main Processing

Reading port P137

- Port register 13 (P13)

Symbol	7	6	5	4	3	2	1	0
P13	**P137**	0	0	0	0	0	0	P130

- Bit 7

P137 bit	Function
0	Input low-level signals
1	Input high-level signals

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

4.6.9 Main Initialization

Figure 4.13 shows the main initialization.

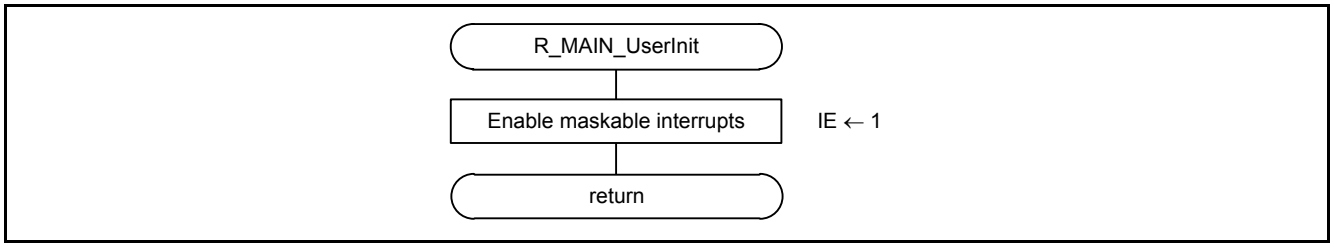


Figure 4.13 Main Initialization

4.6.10 Remote Control Output Control Processing

Figure 4.14 and Figure 4.15 shows the remote control output control processing.

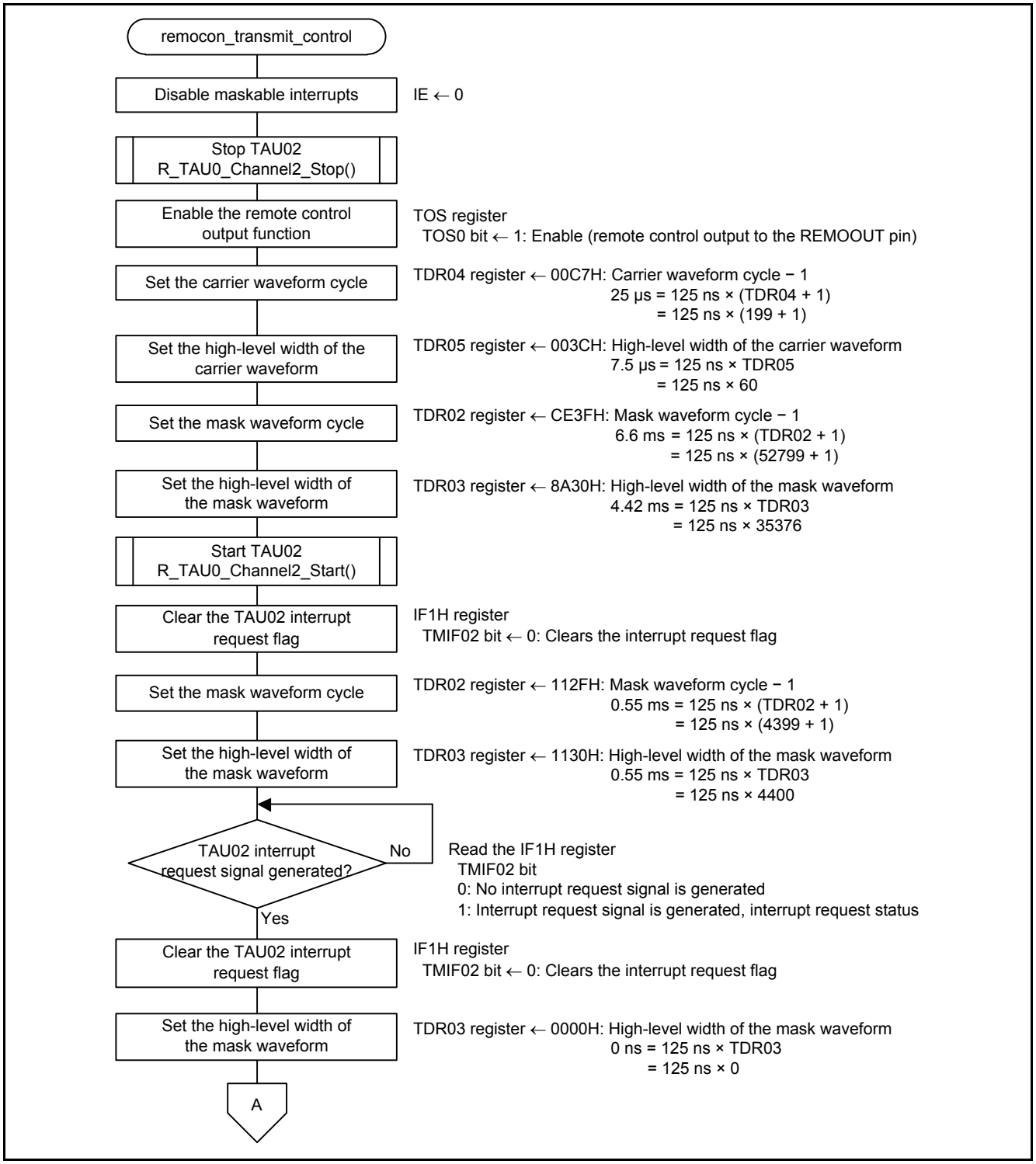


Figure 4.14 Remote Control Output Control Setting (1/2)

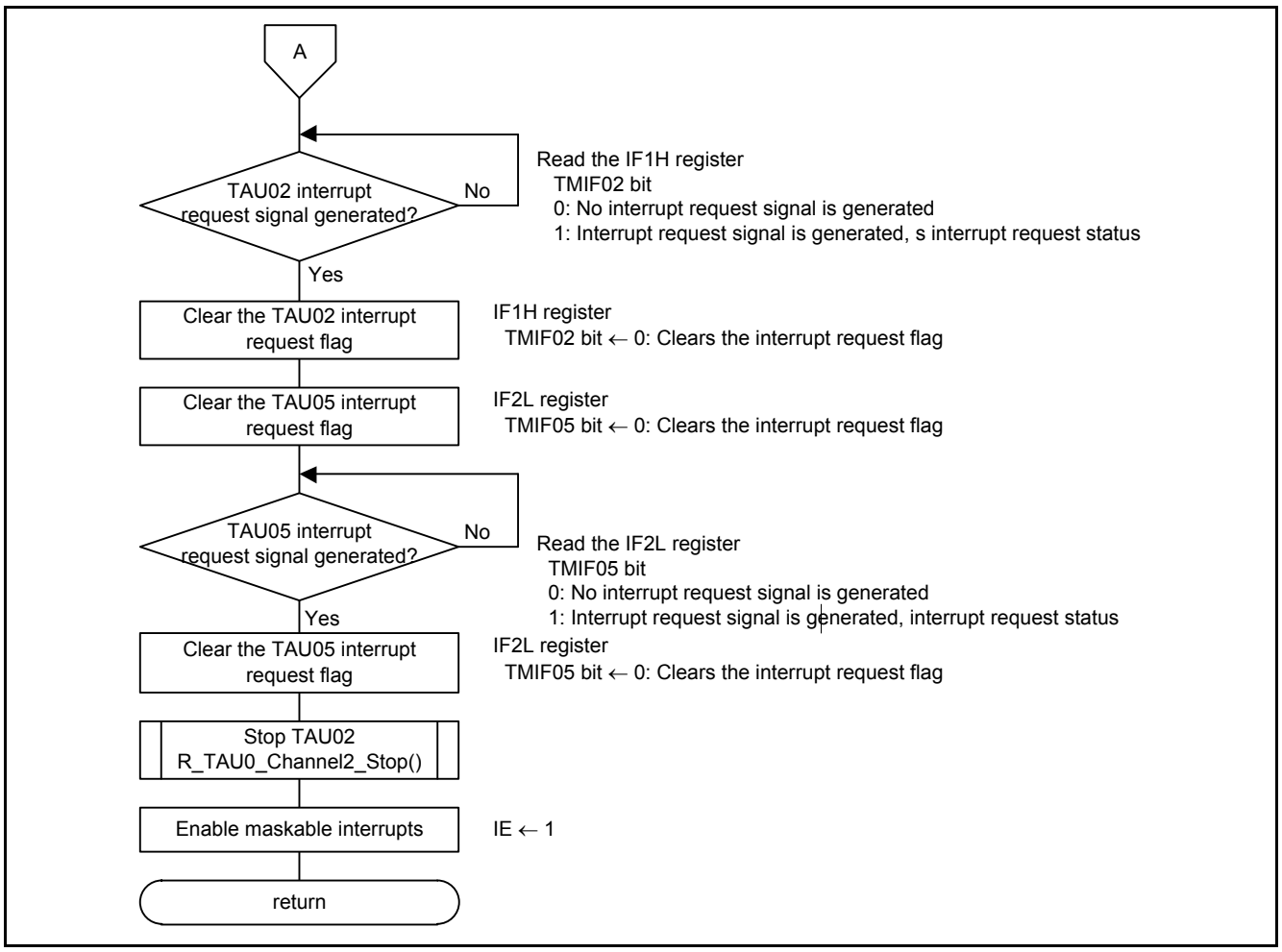


Figure 4.15 Remote Control Output Control Setting (2/2)

Enabling the remote control output function

- Timer output select register (TOS)

Symbol	7	6	5	4	3	2	1	0
TOS	0	0	0	0	0	0	0	**TOS0**
Value	–	–	–	–	–	–	–	**1**

- Bit 0

TOS0 bit	Function
0	Disable (channels 2, 3, 4, and 5 are used for timer output)
1	Enable (remote control output to the REMOOUT pin)

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the carrier waveform cycle

- Timer data register 04 (TDR04)

Sets the carrier waveform cycle to 25 µs.

[25 µs = 1/f_{TCLK} × (TDR04 + 1) = 1/8 MHz × (199 + 1)]

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR04	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	00C7H (199)															

Setting the high-level width of the carrier waveform

- Timer data register 05 (TDR05)

Sets the high-level width of the carrier waveform to 7.5 µs.

(7.5 µs = 1/f_{TCLK} ×TDR05 = 1/8 MHz × 60)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR05	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	003CH (60)															

Setting the mask waveform cycle

- Timer data register 02 (TDR02)

Sets the mask waveform cycle to 6.6 ms.

[6.6 ms = 1/f_{TCLK} × (TDR02 + 1) = 1/8 MHz × (52799 + 1)]

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR02	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	CE3FH (52799)															

Setting the high-level width of the mask waveform

- Timer data register 03 (TDR03)

Sets the high-level width of the mask waveform to 4.42 ms.

(4.42 ms = 1/f_{TCLK} × TDR03 = 1/8 MHz × 35376)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR03	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	8A30H (35376)															

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Clearing the TAU02 interrupt request flag

- Interrupt request flag register (IF1H)

Symbol	7	6	5	4	3	2	1	0
IF1H	SRIF3	STIF3	KRIF	TMKAIF	RTCIF	ADIF	TMIF03	**TMIF02**
Value	×	×	×	×	×	×		**0**

- Bit 0

TMIF02 bit	Function
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

Setting the mask waveform cycle

- Timer data register 02 (TDR02)

Sets the mask waveform cycle to 0.55 ms.

[0.55 ms = 1/f_{TCLK} × (TDR02 + 1) = 1/8 MHz × (4399 + 1)]

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR02	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	**112FH (4399)**															

Setting the high-level width of the mask waveform

- Timer data register 03 (TDR03)

Sets the high-level width of the mask waveform to 0.55 ms.

(0.55 ms = 1/f_{TCLK} × TDR03 = 1/8 MHz × 4400)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR03	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	**1130H (4400)**															

Waiting until the TAU02 interrupt request signal is generated

- Interrupt request flag register (IF1H)

Symbol	7	6	5	4	3	2	1	0
IF1H	SRIF3	STIF3	KRIF	TMKAIF	RTCIF	ADIF	TMIF03	**TMIF02**

- Bit 0

TMIF02 bit	Function
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the high-level width of the mask waveform

- Timer data register 03 (TDR03)

Sets the high-level width of the mask waveform to 0 ns.

(0 ns = 1/f_{TCLK} × TDR03 = 1/8 MHz ×0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR03	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	0000H (0)															

Clearing the TAU05 interrupt request flag

- Interrupt request flag register (IF2L)

Symbol	7	6	5	4	3	2	1	0
IF2L	CMPIF1	CMPIF0	LCDIF0	PIF7	PIF6	**TMIF05**	TMIF04	TKBIF20
Value	×	×	×	×	×	**0**		×

- Bit 2

TMIF05 bit	Function
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

Waiting until the TAU05 interrupt request signal is generated

- Interrupt request flag register (IF2L)

Symbol	7	6	5	4	3	2	1	0
IF2L	CMPIF1	CMPIF0	LCDIF0	PIF7	PIF6	**TMIF05**	TMIF04	TKBIF20

- Bit 2

TMIF05 bit	Function
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware

RL78/L13 User's Manual: Hardware Rev.1.00

RL78 Family User's Manual: Software Rev.1.00

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/L13 How to Output the Remote Control Signals

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 16, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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