RL78/L13

24-Hour Clock Displayed on an LCD CC-RL

R01AN3135EJ0100
Rev. 1.00
Feb. 08, 2016

Abstract

This document describes how to control the LCD panel using the RL78/L13 LCD controller/driver and how the sample code works.

The sample code uses the RL78/L13 LCD controller/driver to display a clock in 24-hour mode. The sample code stores the time measured by the real-time clock (RTC) in the LCD display data memory area, and changes the time at each time an RTC constant-period interrupt occurs (once a minute).

Additionally, by pressing the SET and UP switches, the time can be adjusted and displayed on the LCD.

Products

RL78/L13

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This application describes using the RL78/L13 LCD controller/driver to display a clock in 24-hour mode on an LCD. The sample code stores the time measured by the RTC in the LCD display data memory area, and changes the time at each time an RTC constant-period interrupt occurs (once a minute).

When the SET switch is pressed, the hour indicator and minute indicator can be adjusted (hour setting mode or minute setting mode), the LCD controller/driver adjusts the time, and the adjusted time is displayed on the LCD by pressing the UP switch.

When adjusting the time using hour setting mode and minute setting mode, the corresponding hours and minutes are blinking.

Table 1.1 lists the peripheral functions and their applications. Figure 1.1 shows an operation overview.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
LCD controller/driver	Controls the LCD panel
RTC	Counts the time
12-bit interval timer (IT)	Generates a 10 ms wait time to prevent switch chattering
External interrupt INTP0	Detects input from the UP switch and increments the hours and minutes displayed on the LCD
External interrupt INTP7	Detects input from the SET switch and enters hour setting mode or minute setting mode

The RL78/L13 LCD controller/driver can use external resistance division, internal voltage boosting, or capacitor split to generate LCD drive voltage. For details, refer to 3.3 LCD Drive Voltage Generator.

The sample code uses internal voltage boosting for the LCD drive voltage generator.

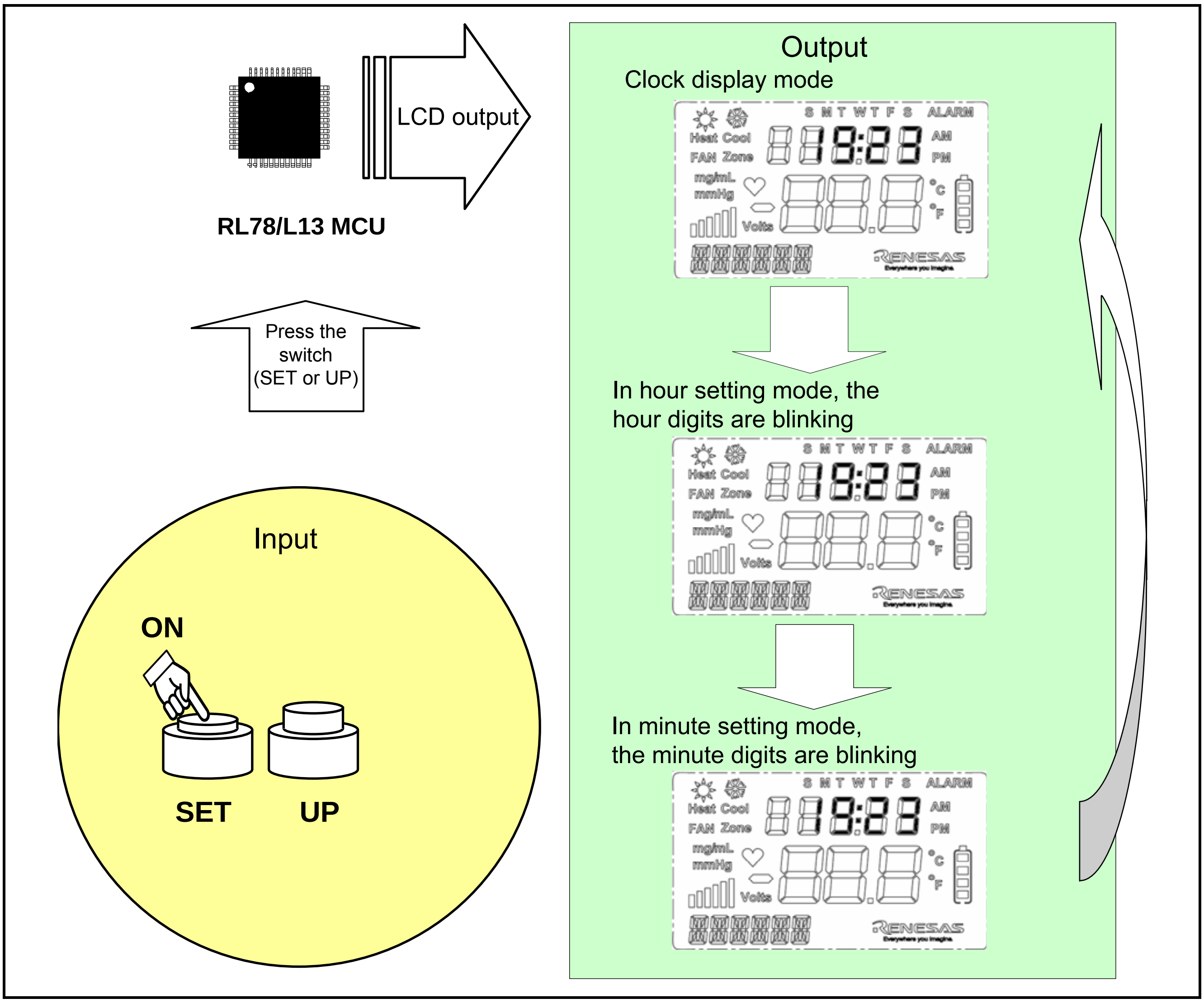


Figure 1.1 Operation Overview

After power-on or after a reset, the LCD enters clock display mode and displays 00:00. The first time the SET switch is pressed, the board enters hour setting mode, and the hour digits blink. The second time the SET switch is pressed, the board enters minute setting mode, and the minute digits blink.

The third time the SET switch is pressed, the LCD returns to clock display mode.

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/L13 (R5F10WMGA)
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}): 24 MHz (typ.) • CPU/peripheral hardware clock (f_{CLK}): 24 MHz • RTC/IT/LCD operating clock (f_{SUB}): 32.768 kHz
Operating voltage	5.0 V (operation possible from 2.9 to 5.5 V) LVD operation (V_{LVD}) in reset mode is 2.81 V at the rising edge or 2.75 V at the falling edge.
Integrated development environment(CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
C compiler(CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment(e²studio)	e²studio V4.2.0.012 from Renesas Electronics Corp.
C compiler(e²studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
RL78/L13 code library	RL78/L13 code library V1.03.02.01 from Renesas Electronics Corp.
Board used	Renesas Starter Kit for RL78/L13 CPU board (R0K5010WMC001BR)
LCD module	Custom glass twisted nematic LCD • 48 pins, 176 segments • Number of pins used: 9 (26 to 34) • Number of digits used: 5 (tens place of hours, ones place of hours, colon, tens place of minutes, and ones place of minutes) • 1/4 duty cycle • 4.2 V operating voltage, 1/3 voltage bias • Six o'clock viewing angle, reflective positive

3. Peripheral Function

This chapter describes the LCD controller/driver.

3.1 Basic Features of RL78/L13 LCD Controller/Driver

RL78/L13 LCD controller/driver includes the following features:

- Waveform A or B selectable
- LCD driver voltage generator can be switched between internal voltage boosting, capacitor split, or external resistance division
- Segment and common signals can be output automatically by reading the LCD display data register automatically
- Reference voltage generated when the voltage boost circuit is operating can be selected from 16 levels (contrast adjustment)
- LCD blinking is available

3.2 LCD Controller/Driver Display Mode

LCD controller/driver display modes are combinations of the LCD drive waveform and LCD voltage generator. Table 3.1 lists the maximum number of pixels in each display mode.

Table 3.1 Maximum Number of Pixels for an 80-pin Package

Drive Waveform for LCD Driver	LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Maximum Number of Pixels
waveform A	External resistance division	–	Static	51 (51 segment signals, 1 common signal)
		1/2	2	102 (51 segment signals, 2 common signals)
			3	153 (51 segment signals, 3 common signals)
		1/3	3	
			4	204 (51 segment signals, 4 common signals)
		1/4	8	376 (47 segment signals, 8 common signals)
	Internal voltage boosting	1/3	3	153 (51 segment signals, 3 common signals)
			4	204 (51 segment signals, 4 common signals)
		1/4	8	376 (47 segment signals, 8 common signals)
	Capacitor split	1/3	3	153 (51 segment signals, 3 common signals)
			4	204 (51 segment signals, 4 common signals)
waveform B	External resistance division, internal voltage boosting	1/3	4	
		1/4	8	376 (47 segment signals, 8 common signals)
	Capacitor split	1/3	4	204 (51 segment signals, 4 common signals)

3.3 LCD Drive Voltage Generator

The RL78/L13 LCD controller/driver can use external resistance division, internal voltage boosting, or capacitor split to generate LCD drive voltage. This chapter covers the features of each method.

Table 3.2 LCD Drive Method and Its Application

LCD Drive Method	Feature/Usage			Application
	Drive capacity	Operating current	Drive voltage	
External resistance division	High	Standard 10.3 µA (typ.) (1)	V_{DD}-dependent	**Suitable for large format LCDs or AC power supply sets** The LCD drive capacity is high and the drive voltage is generated by a resistor divider, which contributes to cost reduction. This method generates the LVD drive voltage by an external resistor divider. As the voltage is applied externally, the operating current and drive capacity can be adjusted by an external resistor.
	Supports large LCDs		LCD display becomes dim with the supply voltage decreased	
Internal voltage boosting	Standard	Small 1.0 µA (typ.) (2)	Constant	**Suitable for battery sets** The operating current is small and the LCD display does not become dim as the drive voltage is constant even when the battery voltage is reduced. This method generates the reference voltage internally and boosts it by an external capacitor. As the reference voltage is adjusted by software, the LCD contrast can be adjusted from 16 levels in RL78/L13.
			As the drive voltage is constant, the LCD display does not change with the battery voltage decreased	
Capacitor split	Standard	Much smaller 0.13 µA (typ.) (2)	V_{DD}-dependent	**Suitable for battery sets** This method has the smallest operating current among three LCD drive modes, and thus the LCD display becomes dim with decreasing the supply voltage. Use this method to allow the screen to be dim according to the battery level. If you do not want the screen to be dim when the battery voltage is decreased, change the LCD drive method to internal voltage boosting. It works in an external circuit of the capacitor split method.
			LCD display becomes dim with the supply voltage decreased	

Notes: 1. This value applies when using an external resistor at 100 kΩ, with 1/3 bias.
2. These are target values when designing the MCU. For more information, refer to the RL78/L13 User's manual: Hardware.

3.3.1 External Resistance Division Method

This is suitable for large format LCDs or AC power sets. As it has a large drive capacity and generates the drive voltage by a resistor divider, which contributes to cost reduction.

To be more specific, this method generates an LCD drive voltage using an external resistor divider. As the voltage is applied externally, the operating current or the drive capacity can be adjusted by the external resistor.

Figure 3.1 and Figure 3.2 show connection examples of external resistance division method.

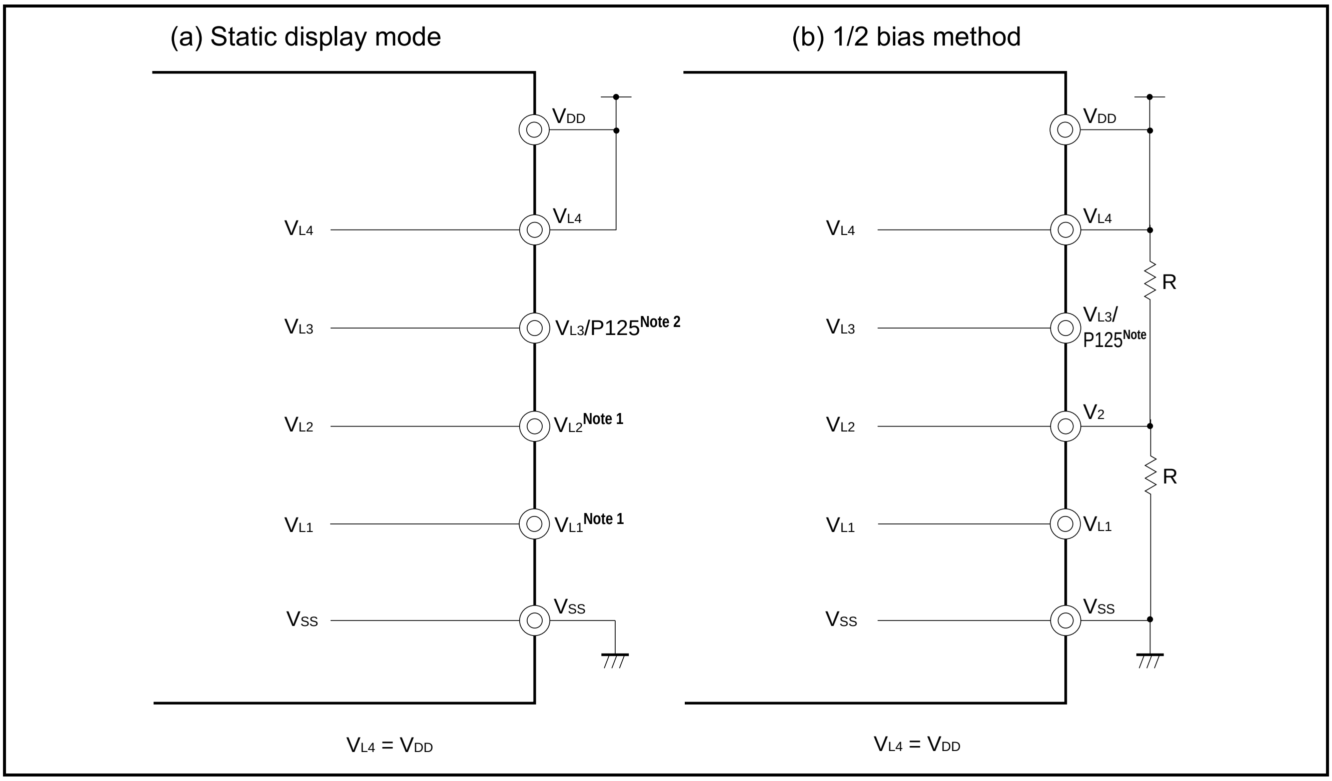


Figure 3.1 Connection Example of External Resistance Division Method (1/2)

Notes for Figure 3.1 (a)
Note 1: Connect V_{L1} and V_{L2} to GND or leave them open.
Note 2: V_{L3} can be used as a port (P125).

Note for Figure 3.1 (b)
V_{L3} can be used as a port (P125).

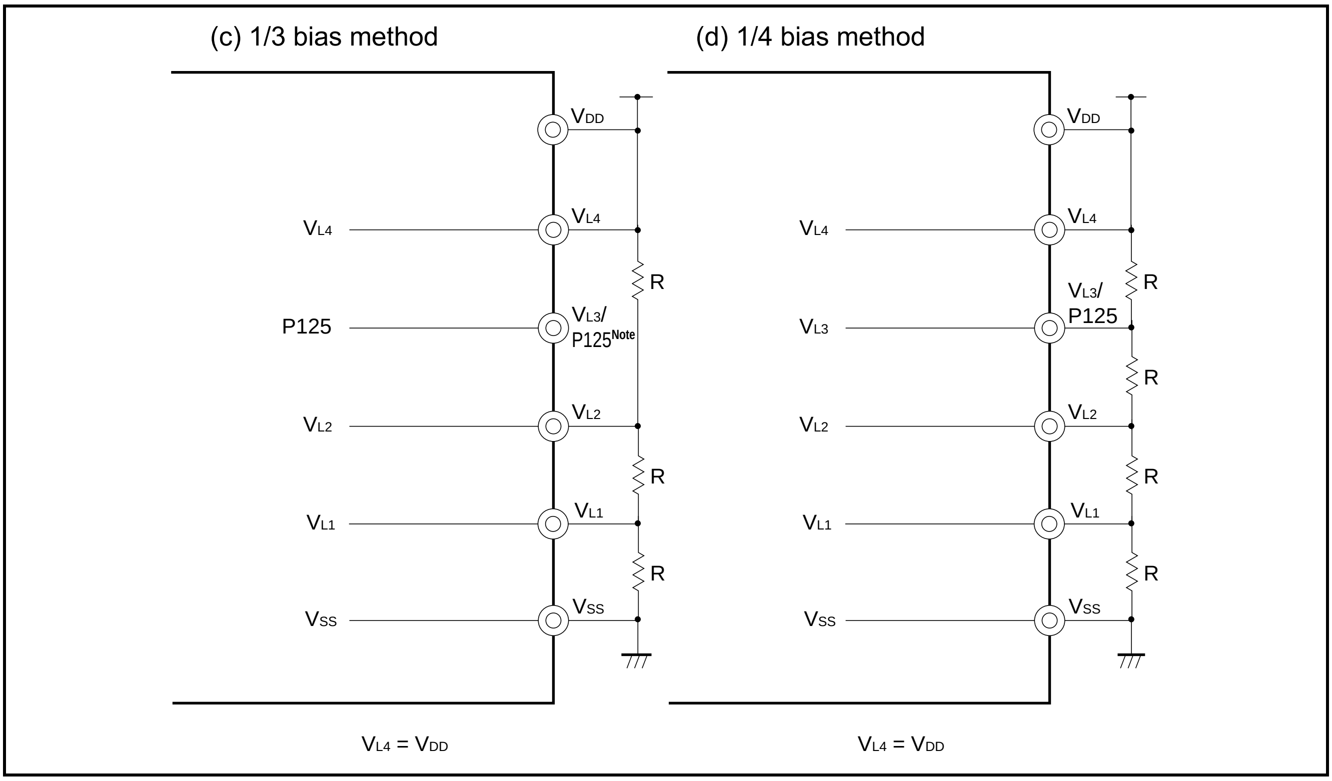


Figure 3.2 Connection Example of External Resistance Division Method (2/2)

Note: V_{L3} can be used as a port (P125).

3.3.2 Internal Voltage Boosting Method

This is suitable for a battery set.

The operating current is small and the LCD display does not become dim as the drive voltage is constant even when the battery voltage is reduced.

This method generates the reference voltage internally and boosts it by an external capacitor. As the reference voltage is adjusted by software (the LCD boost level control register, VLCD), the LCD contrast can be adjusted from 16 levels in RL78/L13.

Figure 3.3 shows a connection example of internal voltage boosting method.

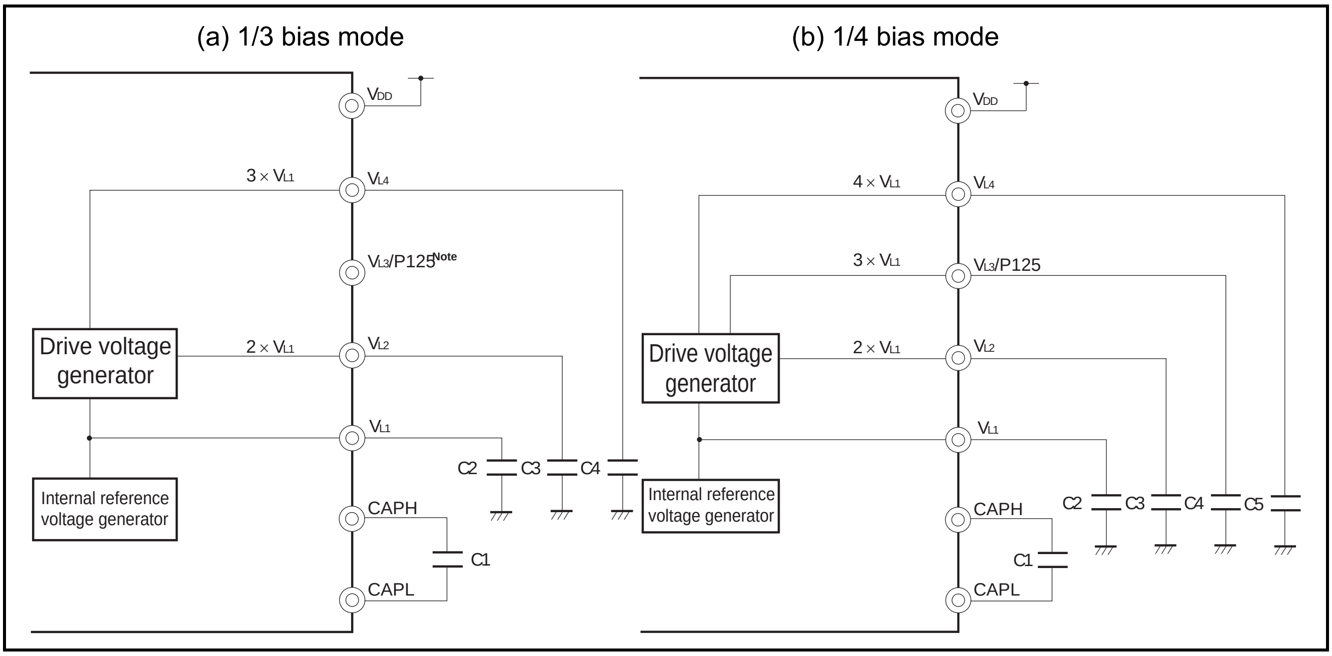


Figure 3.3 Connection Example of Internal Voltage Boosting Method

Note: V_{L3} can be used as a port (P125).

Remark: Use a capacitor with as little leakage as possible. Make sure to use a non-polar capacitor for C1.

3.3.3 Capacitor Split Method

This is also suitable for a battery set.

This method has the smallest operating current among three LCD drive modes, and thus the LCD display becomes dim with the supply voltage decreased.

If you do not want the screen to be dim when the battery voltage is decreased, change the LCD drive method to internal voltage boosting method. The method works in an external circuit of the capacitor split method.

Figure 3.4 shows a connection example of capacitor split method.

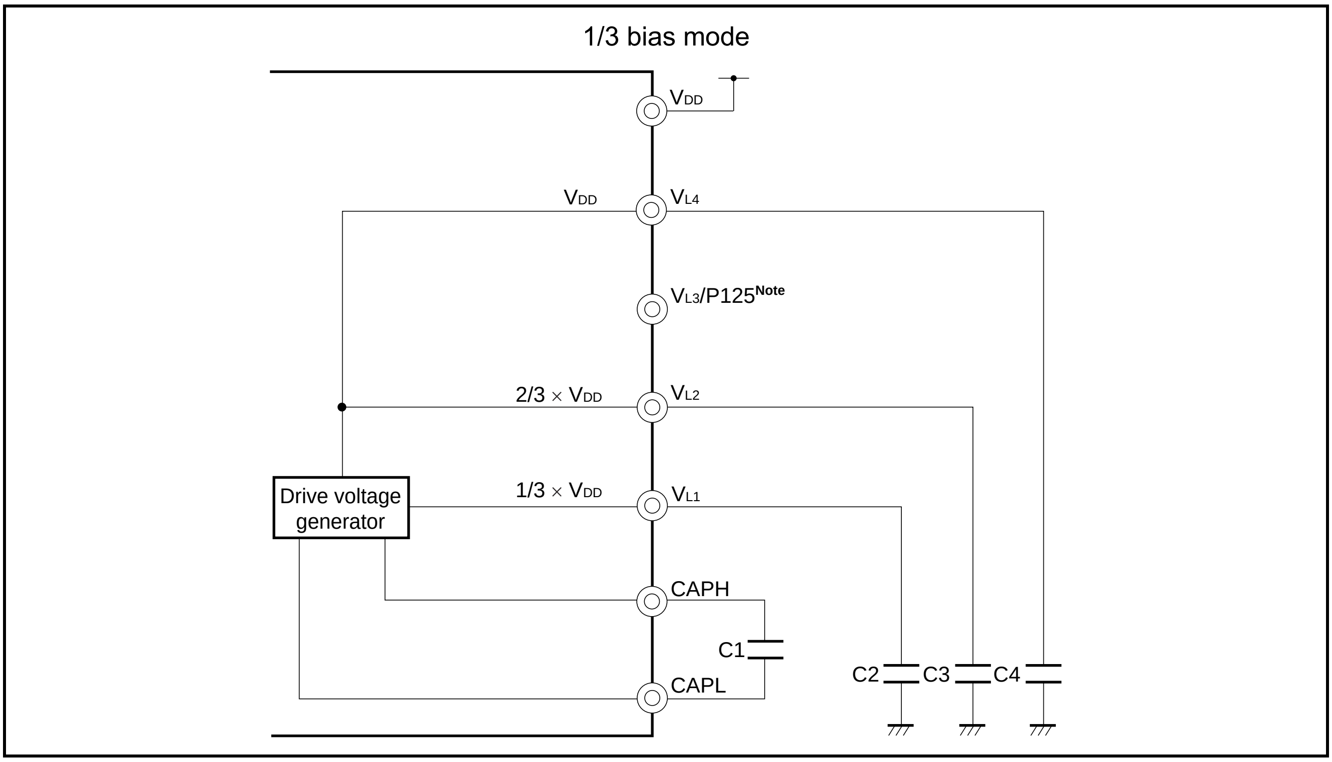


Figure 3.4 Connection Example of Capacitor Split Method

Note: V_{L3} can be used as a port (P125).
Remark: Use a capacitor with as little leakage as possible. Make sure to use a non-polar capacitor for C1.

Unlike external resistance division method which always requires current flowing, internal voltage boosting method and capacitor split method do not always require applying the current, and thus, current consumption can be reduced.

4. Hardware

4.1 Hardware Example

Figure 4.1 shows the hardware configuration used in this application note.

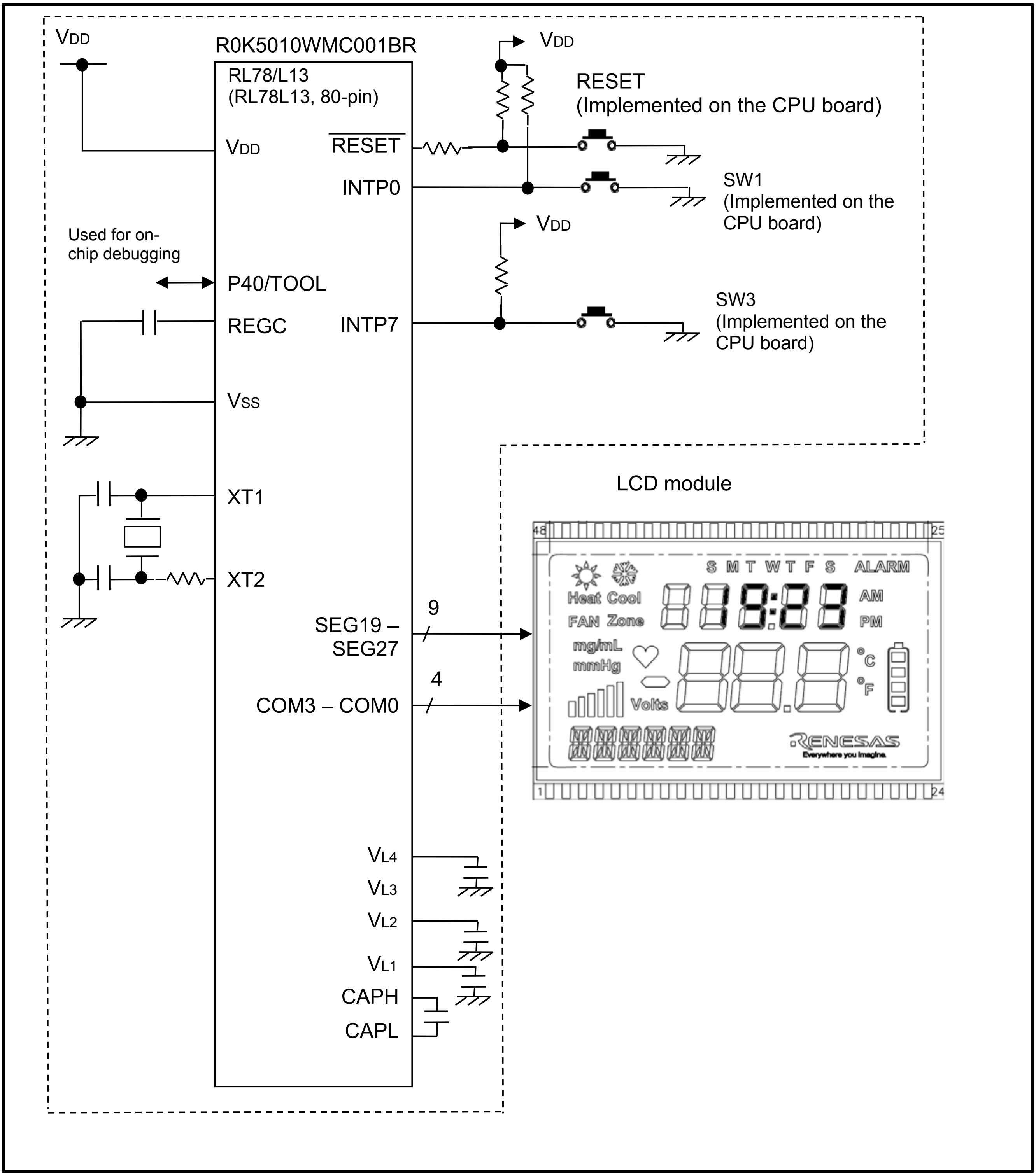


Figure 4.1 Hardware Configuration

Notes 1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics (connect input-only ports independently to either V_{DD} or V_{SS} via resistors).

2. Make sure to set V_{DD} greater than the detection voltage (V_{LVD}) specified by the LVD.

4.2 LCD Module

This section describes the LCD module used in the sample code accompanying this application note.

RL78/L13 and an LCD module are connected as shown in Figure 4.2.

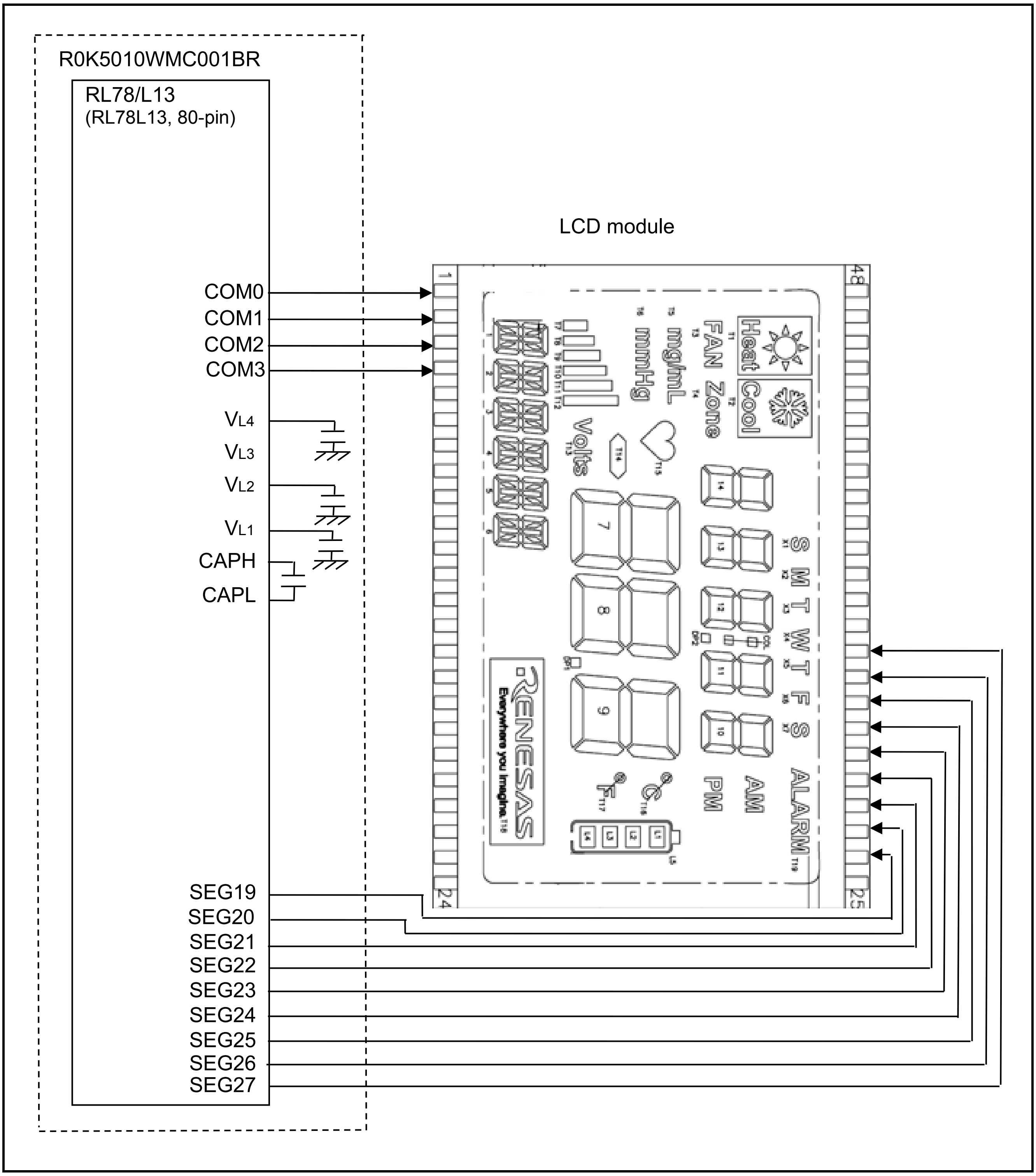


Figure 4.2 Connection Example between RL78/L13 and LCD Module

Symbols correspond to the segment signals (SEG) as shown in Figure 4.3.

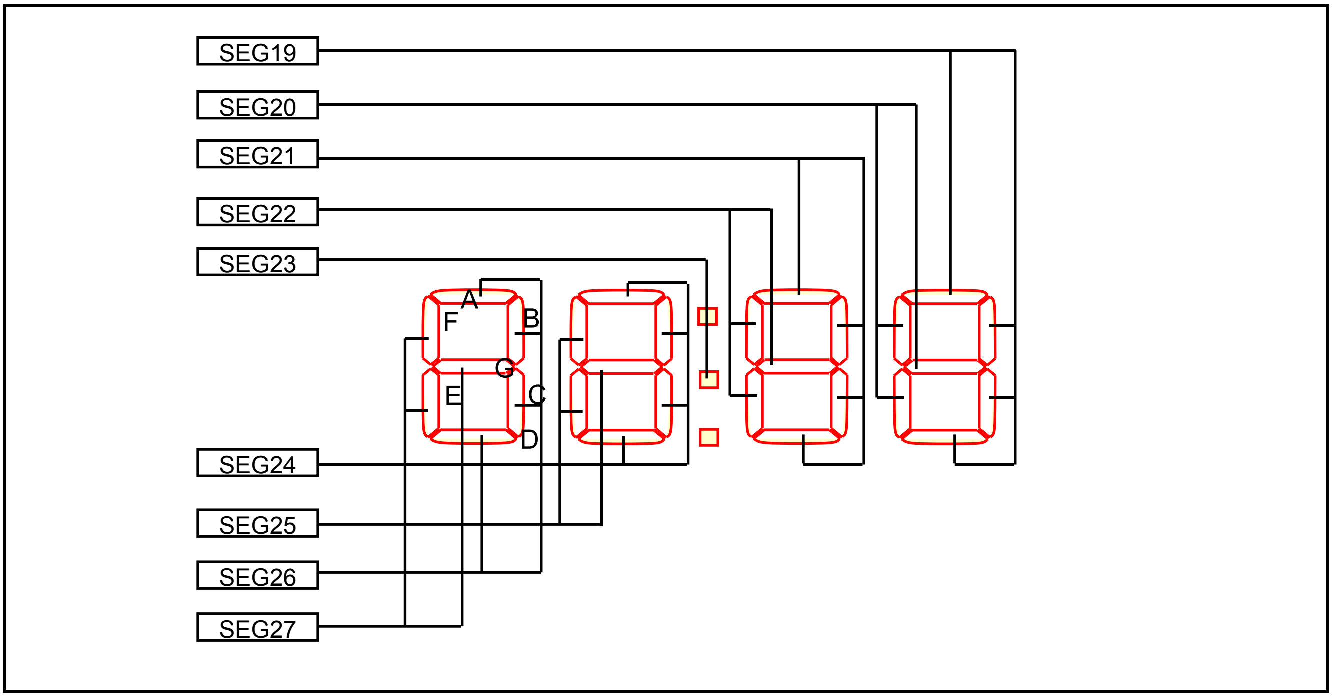


Figure 4.3 Segments and Reference Letters of LCD Digits

Segments are corresponding to common signals (COM) as listed in Table 4.1.

Table 4.1 Segments and Commons Mapping Table

LCD Display Data Register	Address	COM3	COM2	COM1	COM0
		bit 3	bit 2	bit 1	bit 0
SEG19	F0413H	A in ones place of minutes	B in ones place of minutes	C in ones place of minutes	D in ones place of minutes
SEG20	F0414H	F in ones place of minutes	G in ones place of minutes	E in ones place of minutes	0
SEG21	F0415H	A in tens place of minutes	B in tens place of minutes	C in tens place of minutes	D in tens place of minutes
SEG22	F0416H	F in tens place of minutes	G in tens place of minutes	E in tens place of minutes	0
SEG23	F0417H	0	0	: (colon)	0
SEG24	F0418H	A in ones place of hours	B in ones place of hours	C in ones place of hours	D in ones place of hours
SEG25	F0419H	F in ones place of hours	G in ones place of hours	E in ones place of hours	0
SEG26	F041BH	A in tens place of hours	B in tens place of hours	C in tens place of hours	D in tens place of hours
SEG27	F041CH	F in tens place of hours	G in tens place of hours	E in tens place of hours	0

Table 4.2 lists the setting for display data (0 to 9).

Table 4.2 SEG19 to SEG27 Display Data Setting (0 to 9)

	LCD display data register setting							
Tens place of hours	SEG26 (0F041BH)				SEG27 (0F041CH)			
Ones place of hours	SEG24 (0F0418H)				SEG25 (0F0419H)			
Tens place of minutes	SEG21 (0F0415H)				SEG22 (0F0416H)			
Ones place of hours	SEG19 (0F0413H)				SEG20 (0F0414H)			
Bit position	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
Segment	**A**	**B**	**C**	**D**	**F**	**G**	**E**	**0**
0	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**0**
1	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
2	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**0**
3	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
4	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**0**
5	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**0**
6	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**0**
7	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**
8	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
9	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**

4.3 Pins Used

Table 4.3 lists the pins used and their functions.

Table 4.3 Pins Used and Their Functions

Pin Name	I/O	Function
P137/INTP0	Input	Detects input from the UP switch and increments hours and minutes displayed on the LCD
P02/INTP7		Detects input from the SET switch and enters hour setting mode or minute setting mode
P30/SEG20	Output	LCD controller/driver segment signals (Note)
P31/SEG21		
P32/SEG22		
P33/SEG23		
P34/SEG24		
P35/SEG25		
P46/SEG26		
P47/SEG27		
P77/SEG19		
COM0	Output	LCD controller/driver common signals
COM1		
COM2		
COM3		

Note: These are segment signals controlled by the sample code accompanying this application note. In addition, segment signals (SEG0 to SEG18 and SEG28 to SEG39) connected to the LCD module on the CPU board are also set as segment pins in the sample code.

5. Software

5.1 Operation Overview

This sample code uses the RL78/L13 LCD controller/driver to display a clock in 24-hour mode. It stores the time measured by the RTC in the LCD display data memory area to change the time at each time an RTC constant-period interrupt occurs (once a minute).

When the SET switch is pressed, the hour indicator and minute indicator can be adjusted (hour setting mode or minute setting mode), and the LCD controller/driver adjusts the time by pressing the UP switch and then displays the adjusted time.

In hour setting mode or minute setting mode, the corresponding digits on the LCD are blinking.

In the initial settings, the clock frequency, I/O ports, RTC, IT, and LCD controller/driver are configured.

After configuration, RL78/L13 enters STOP mode and exits STOP mode by the RTC constant-period interrupt or detecting the INTP7 falling edge. When the RTC constant-period interrupt is generated, RL78/L13 changes the time. When the SET switch is pressed (INTP7 interrupt is detected), RL78/L13 generates a wait time to prevent switch chattering. The clock is set if the SET switch has been pressed.

The UP switch is not valid in clock display mode; it can only be used in hour setting mode or minute setting mode.

The board enters hour setting mode the first time the SET switch is pressed; the board enters minute setting mode the second time the SET switch is pressed, and the third time the SET switch is pressed, the LCD returns to displaying the set time.

In hour setting mode, push the UP switch to increment the hours by 1. In minute setting mode, push the UP switch to increment the minutes by 1.

For more information, refer to the state transition diagram on the next page.

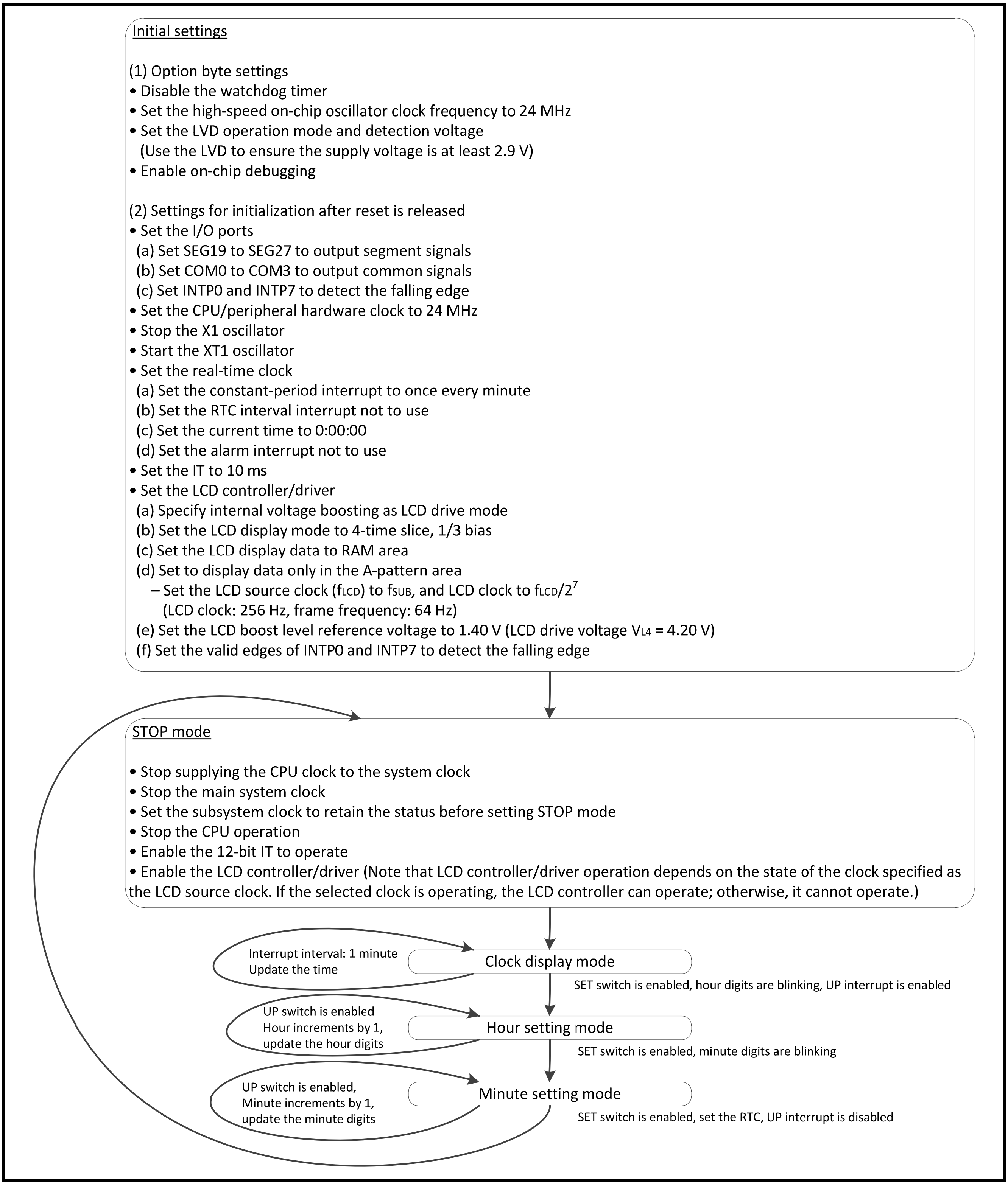


Figure 5.1 State Transition Diagram

5.2 File Composition

Table 5.1 lists the files used in the sample code. Files generated by the integrated development environment are not included in this table.

Table 5.1 Files Used in the Sample Code

File Name	Outline	Remarks
r_cg_rtc_user.c	Processing associated with the RTC: RTC operation start setting	Function added: r_rtc_operation_start
r_main.c	main Interrupt source retrieval Switch analysis Switch status retrieval Command analysis Processing when pressing the SET switch Processing when pressing the UP switch Time display Hour data blinking Minute data blinking Normal data display setting Display data setting BCD data addition processing	Functions added: r_main_get_interrupt r_main _analyze_switch r_main _get_switch_status r_main _command_analyze r_main _set_switch_process r_main _up_switch_process r_main _lcd_display_time r_main _lcd_hour_blink r_main _lcd_minute_blink r_main _lcd_display_normal r_main_seg_data_set r_main_bcd_inc
r_cg_it_user.c	Processing associated with IT: IT operation start setting IT operation stop setting	Functions added: r_it_operatio_start r_it_operation_stop

5.3 Option Byte Settings

Table 5.2 lists the option byte settings.

Table 5.2 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	01101110B	Stops the watchdog timer (counting is stopped when a reset is released)
000C1H/010C1H	01111111B	Sets the LVD in reset mode Detection voltage: 2.81 V at the rising edge, 2.75 V at the falling edge
000C2H/010C2H	11100000B	Sets the high-speed on-chip oscillator clock to 24 MHz in HS (high-speed main) mode
000C3H/010C3H	10000100B	Enables on-chip debugging

5.4 Constants

Table 5.3 lists the constants used in the sample code.

Table 5.3 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
LCD_POSITION_HOUR_HIGH _ABCD_SYMBOL	&SEG26	LCD display data address (tens place of hours symbol A,B,C,D)
LCD_POSITION_HOUR_HIGH _EFG_SYMBOL	&SEG27	LCD display data address (tens place of hours symbol E,F,G)
LCD_POSITION_HOUR_LOW _ABCD_SYMBOL	&SEG24	LCD display data address (ones place of hours symbol A,B,C,D)
LCD_POSITION_HOUR_LOW _EFG_SYMBOL	&SEG25	LCD display data address (ones place of hours symbol E,F,G)
LCD_POSITION_COLON	&SEG23	LCD display data address (colon)
LCD_POSITION_MINUTE_HIGH _ABCD_SYMBOL	&SEG21	LCD display data address (tens place of minutes symbol A,B,C,D)
LCD_POSITION_MINUTE_HIGH _EFG_SYMBOL	&SEG22	LCD display data address (tens place of minutes symbol E,F,G)
LCD_POSITION_MINUTE_LOW _ABCD_SYMBOL	&SEG19	LCD display data address (ones place of minutes symbol A,B,C,D)
LCD_POSITION_MINUTE_LOW _EFG_SYMBOL	&SEG20	LCD display data address (ones place of minutes symbol E,F,G)
LCD_DATA_0	0x0A0F	LCD display data (0)
LCD_DATA_1	0x0006	LCD display data (1)
LCD_DATA_2	0x060D	LCD display data (2)
LCD_DATA_3	0x040F	LCD display data (3)
LCD_DATA_4	0x0C06	LCD display data (4)
LCD_DATA_5	0x0C0B	LCD display data (5)
LCD_DATA_6	0x0E0B	LCD display data (6)
LCD_DATA_7	0x080E	LCD display data (7)
LCD_DATA_8	0x0E0F	LCD display data (8)
LCD_DATA_9	0x0C0F	LCD display data (9)
LCD_DATA_COLON	0x02	LCD display data (colon)
LCD_DATA_NONE	0x0000	LCD display data ( ) no display data
INTERRUPT_OFF	0x00	Interrupt request is not generated
INTRC_ON	0x01	RTC constant-period interrupt request is generated
INTPN_ON	0x02	External interrupt (INTPn: n = 0, 7) request is generated
LCD_NUM_DATA_SIZE	0x02	Byte size of the LCD numeric data
LCD_COLON_DATA_SIZE	0x01	Byte size of colon data
LCD_NUM_DATA_FONT_COUNT	0x0C	Number of fonts of LCD numeric data, “, (comma)” and “: (colon)” in total: 12
LCD_DATA_NONE_INDEX	0x0A	LCD data ‘ (space)’ g_FontData index
LCD_DATA_COLON_INDEX	0x0B	LCD data ‘: (colon)’ g_FontData index
WATCH_DISPLAY	0x00	Clock display mode
HOUR_ADJUST	0x01	Hour setting mode
MINUTE_ADJUST	0x02	Minute setting mode

SET_SWITCH_ON	0x01	SET switch is ON
UP_SWITCH_ON	0x02	UP switch is ON
SWITCH_ALL_OFF	0x00	Switches are OFF
LCD_DISPLAY_NORMAL	0x00	LCD display mode (normal mode)
LCD_DISPLAY_BLINK	0x01	LCD display mode (blinking)

5.5 Variables

Table 5.4 lists the static variables.

Table 5.4 static Variables

Type	Variable Name	Contents	Function Used
uint16_t	g_font_data[LCD_NUM_DATA_FONT_COUNT]	LCD font data • Array index is numeric data • g_font_data[10] is ‘ (space)’ data • g_font_data[11] is ‘: (colon)’ data	r_main_lcd_hour_blink, r_main_LcdMinuteBlink, r_main_LcdDisplayNormal
unit8_t	g_watch_status	Clock status variable	R_MAIN_UserInit, r_main_Set_SwitchProcess, r_main_Up_SwitchProcess, r_main_LcdDisplayTime
uint8_t	g_hour	Clock hour data	main, R_MAIN_UserInit, r_main_SetSwitchProcess, r_main_Up_SwitchProcess, r_main_LcdHourBlink, r_main_LcdMinuteBlink, r_main_LcdDisplayNormal
uint8_t	g_minute	Clock minute data	main R_MAIN_UserInit, r_main_SetSwitchProcess, r_main_Up_SwitchProcess, r_main_LcdHourBlink, r_main_LcdMinuteBlink, r_main_LcdDisplayNormal
uint8_t	g_lcd_blink	LCD display status variable	r_main_UserInit, r_main_SetSwitchProcess, r_main_LcdDisplayTime

5.6 Functions

Table 5.5 lists the functions.

Table 5.5 Functions

Function Name	Outline
R_MAIN_UserInit [Note]	User application initialization
R_LCD_Voltage_On [Note]	LCD voltage boost circuit operation start processing
R_LCD_Start [Note]	LCD display start processing
R_INTCn_Start [Note]	INTPn operation start processing (n = 0, 7)
R_RTC_Set_ConstPeriodInterruptOn [Note]	RTC constant-period interrupt enable
r_rtc_operation_start	RTC operation start processing
R_RTC_Start [Note]	RTC counter operation start processing
r_main_get_interrupt	Interrupt source retrieval
R_RTC_Get_CounterValue [Note]	RTC read (SEC to YEAR)
r_main_analyze_switch	Switch analysis
r_main_get_switch_status	Switch status retrieval
r_main_command_analyze	Command analysis
r_main_set_switch_process	Processing when pressing the SET switch
r_it_operation_start	IT operation start processing
R_IT_Start [Note]	IT counter operation start processing
r_it_operation_stop	IT operation stop processing
R_IT_Stop [Note]	IT counter operation stop processing
R_RTC_Set_CounterValue [Note]	RTC write (SEC to YEAR)
r_main_up_switch_process	Processing when pressing the UP switch
r_rtc_set_counter_value_hour_min	Write minute and hour data to the RTC
r_main_lcd_display_time	LCD time display
r_main_lcd_hour_blink	Set hour blinking data in the LCD display data register
r_main_lcd_minute_blink	Set minute blinking data in the LCD display data register
r_main_lcd_display_normal	Set normal display data in the LCD display data register
r_main_seg_data_set	Set display data in the LCD display data register
r_main_bcd_inc	Addition processing of BCD data

Note: These functions are automatically generated by the integrated development environment.

5.7 Function Specifications

The following tables list the sample code function specifications.

R_MAIN_UserInit	
Outline	User application initialization
Header	None
Declaration	void R_MAIN_UserInit(void)
Description	Initializes the peripheral functions necessary for using application.
Arguments	None
Return Value	None
Remarks	None

R_LCD_Voltage_On	
Outline	LCD voltage boost circuit operation start processing
Header	r_cg_lcd.h
Declaration	void R_LCD_Voltage_On(void)
Description	Starts the LCD voltage boost circuit operation (VLCON bit = 1).
Arguments	None
Return Value	None
Remarks	None

R_LCD_Start	
Outline	LCD display start processing
Header	r_cg_lcd.h
Declaration	void R_LCD_Start(void)
Description	Enables the LCD display (LCDON bit = 1).
Arguments	None
Return Value	None
Remarks	None

R_INTCn_Start (n = 0, 7)	
Outline	INTPn operation start processing (n = 0, 7)
Header	r_cg_intc_h
Declaration	void R_INTCn_Start(void) (n = 0, 7)
Description	Clears the INTPn interrupt request flag before enabling the interrupt.
Arguments	None
Return Value	None
Remarks	None

R_RTC_Set_ConstPeriodInterruptOn	
Outline	RTC constant-period interrupt enable
Header	r_cg_rtc.h
Declaration	MD_STATUS R_RTC_Set_ConstPeriodInterruptOn(rtc_int_period_t period)
Description	Enables the interrupt after setting the RTC constant-period interrupt.
Arguments	rtc_int_period_t period : Constant-period interrupt setting value
Return Value	MD_OK: Normal end MD_ARGERROR: Specified argument is invalid
Remarks	None

r_rtc_operation_start	
Outline	RTC operation start processing
Header	r_cg_rtc.h
Declaration	void r_rtc_operation_start(void)
Description	After the RTC starts counter operation, the program performs processing to enter STOP mode after the RTC is started.
Arguments	None
Return Value	None
Remarks	None

R_RTC_Start	
Outline	RTC counter operation start processing
Header	r_cg_rtc.h
Declaration	void R_RTC_Start(void)
Description	Clears the interrupt request flag, enables the interrupt, and starts the RTC counter operation and waits until the RTC starts.
Arguments	None
Return Value	None
Remarks	None

r_main_get_interrupt	
Outline	Interrupt source retrieval
Header	r_cg_userdefine.h
Declaration	uint8_t r_main_get_interrupt (void)
Description	Returns an interrupt with an interrupt request flag.
Arguments	None
Return Value	INTERRUPT_OFF: Interrupt request is not generated INTRC_ON: RTC constant-period interrupt request is generated INTPN_ON: External interrupt (INTPn: n = 0, 7) request is generated
Remarks	None

R_RTC_Get_CounterValue	
Outline	RTC read (SEC to YEAR)
Header	r_cg_rtc.h
Declaration	MD_STATUS R_RTC_Get_CounterValue(rtc_counter_value_t *const counter_read_val)
Description	Reads the RTC counter values (SEC to YEAR).
Arguments	rtc_counter_value_t* const counter_read_val : Pointer to the structure to store the read counter value
Return Value	MD_OK: Normal end MD_BUSY1: Executing the count processing (before reading) MD_BUSY2: Executing the count processing (after reading)
Remarks	None

r_main_analyze_switch	
Outline	Switch analysis
Header	r_cg_userdefine.h
Declaration	void r_main_analyze_switch(void)
Description	Waits to prevent switch chattering and retrieves the status of the switch. When the program detects that a switch has been pressed, the program jumps to each switch processing.
Arguments	None
Return Value	None
Remarks	None

r_main_get_switch_status	
Outline	Switch status retrieval
Header	r_cg_userdefine.h
Declaration	uint8_t r_main_get_switch_status(void)
Description	Retrieves the status of the switch which has been pressed.
Arguments	None
Return Value	SWITCH_ALL_OFF: Switches are OFF SET_SWITCH_ON: SET switch is ON UP_SWITCH_ON: UP switch is ON
Remarks	This function ignores the case when the switch is pressed multiple times.

r_main_command_analyze	
Outline	Command analysis
Header	r_cg_userdefine.h
Declaration	void r_main_command_analyze(uint8_t t_switch)
Description	Calls the processing of the switch which has been pressed.
Arguments	uint8_t t_switch SET_SWITCH_ON: Set this when the SET switch is pressed UP_SWITCH_ON: Set this when the UP switch is pressed
Return Value	None
Remarks	None

r_main_set_switch_process	
Outline	Processing when pressing the SET switch
Header	r_cg_userdefine.h
Declaration	void r_main_set_switch_process(void)
Description	Performs the SET switch processing. Processing depends on the clock mode. (a) When in clock display mode 1. Enable the UP switch. 2. Enter hour setting mode. 3. Set the LCD display mode to blinking. 4. Set the RTC constant-period interval to 0.5 seconds. 5. Enable LCD blinking. (b) When in hour setting mode 1. Enter minute setting mode. (c) When in minute setting mode 1. Disable the UP switch. 2. Set the LCD display mode to normal mode. 3. Set the RTC constant-period interrupt interval to 1 minute. 4. Disable the LCD blinking. 5. Set the seconds to 00 to update the RTC counter. 6. Enter clock display mode.
Arguments	None
Return Value	None
Remarks	None

r_it_operation_start	
Outline	IT operation start processing
Header	r_cg_it.h
Declaration	void r_it_operation_start(void)
Description	Starts the IT and clears the interrupt request flag.
Arguments	None
Return Value	None
Remarks	None

R_IT_Start	
Outline	ITcounter operation start processing
Header	r_cg_it.h
Declaration	void R_IT_Start(void)
Description	Starts the IT counter operation.
Arguments	None
Return Value	None
Remarks	None

r_it_operation_stop	
Outline	IT operation stop processing
Header	r_cg_it.h
Declaration	void r_it_operation_stop(void)
Description	Clears the interrupt request flag and stops the IT counter operation.
Arguments	None
Return Value	None
Remarks	None

R_IT_Stop	
Outline	IT counter operation stop processing
Header	r_cg_it.h
Declaration	void R_IT_Stop(void)
Description	Stops the IT counter operation.
Arguments	None
Return Value	None
Remarks	None

R_RTC_Set_CounterValue	
Outline	RTC write (SEC to YEAR)
Header	r_cg_rtc.h
Declaration	MD_STATUS R_RTC_Set_CounterValue(rtc_counter_value_t counter_write_val)
Description	Sets the counter values (SEC to YEAR) to the RTC.
Arguments	rtc_counter_value_t counter_write_val : Counter value
Return Value	MD_OK: Normal end MD_BUSY1: Executing the count processing (before changing the setting) MD_BUSY2: Executing the count processing (after changing the setting)
Remarks	None

r_main_up_switch_process	
Outline	Processing when pressing the UP switch
Header	r_cg_userdefine.h
Declaration	void r_main_up_switch_process(void)
Description	Performs the UP switch processing. Processing depends on the clock mode status. (a) When in hour setting mode 1: Hour data is incremented by 1 to set the clock data to the RTC. (b) When in minute setting mode 1: Minute data is incremented by 1 to set the clock data to the RTC.
Arguments	None
Return Value	None
Remarks	None

r_rtc_set_counter_value_hour_min		
Outline	Write minute and hour data to the RTC	
Header	r_cg_rtc.h	
Declaration	MD_STATUS r_rtc_set_counter_value_hour_min(uint8_t hour, uint8_t minute)	
Description	Sets the counter values (MIN, HOUR) to the RTC.	
Arguments	uint8_t hour	: Counter value (hour)
	unit8_minute	: Counter value (minute)
Return Value	MD_OK: Normal end MD_BUSY1: Executing the counter processing (before changing the setting) MD_BUSY2: Executing the counter processing (after changing the setting)	
Remarks	None	

r_main_lcd_display_time	
Outline	LCD time display
Header	r_cg_userdefine.h
Declaration	void r_main_lcd_display_time(void)
Description	Depending on the LCD display mode (normal or blinking), clock mode (clock display mode, hour setting mode, minute setting mode), the program branches to the processing to set each data to the LCD display data address.
Arguments	None
Return Value	None
Remarks	None

r_main_lcd_hour_blink	
Outline	Set hour blinking data in the LCD display data register
Header	r_cg_userdefine.h
Declaration	void r_main_lcd_hour_blink(void)
Description	Writes the font data of the current time in SEG19 to SEG27 in the LCD display data register to display the hour on LCD. Write the same minute data both in A-pattern area and B-pattern area so only the hour data blinks.
Arguments	None
Return Value	None
Remarks	None

r_main_lcd_minute_blink	
Outline	Set minute blinking data in the LCD display data register
Header	r_cg_userdefine.h
Declaration	void r_main_lcd_minute_blink(void)
Description	Writes the font data of the current time in SEG19 to SEG27 in the LCD display data register to display the minutes on LCD. Write the same hour data both in A-pattern area and B-pattern area so only the minute data blinks.
Arguments	None
Return Value	None
Remarks	None

r_main_lcd_display_normal	
Outline	Set normal display data in the LCD display data register
Header	r_cg_userdefine.h
Declaration	void r_main_lcd_display_normal(void)
Description	Writes the font data of the current time in SEG19 to SEG27 in the LCD display data register to display the data on LCD.
Arguments	None
Return Value	None
Remarks	None

r_main_seg_data_set	
Outline	Set display data in the LCD display data register
Header	r_cg_userdefine.h
Declaration	void r_main_seg_data_set(void)
Description	Set the display data to LCD display data register.
Arguments	None
Return Value	None
Remarks	None

r_main_bcd_inc	
Outline	Addition processing of BCD data
Header	r_cg_userdefine.h
Declaration	void r_main_bcd_inc(void)
Description	BCD data convert to the decimal. Add the value to decimal, and converted to BCD data.
Arguments	None
Return Value	None
Remarks	None

5.8 Flowcharts

Figure 5.2 shows the overall flow of the sample code.

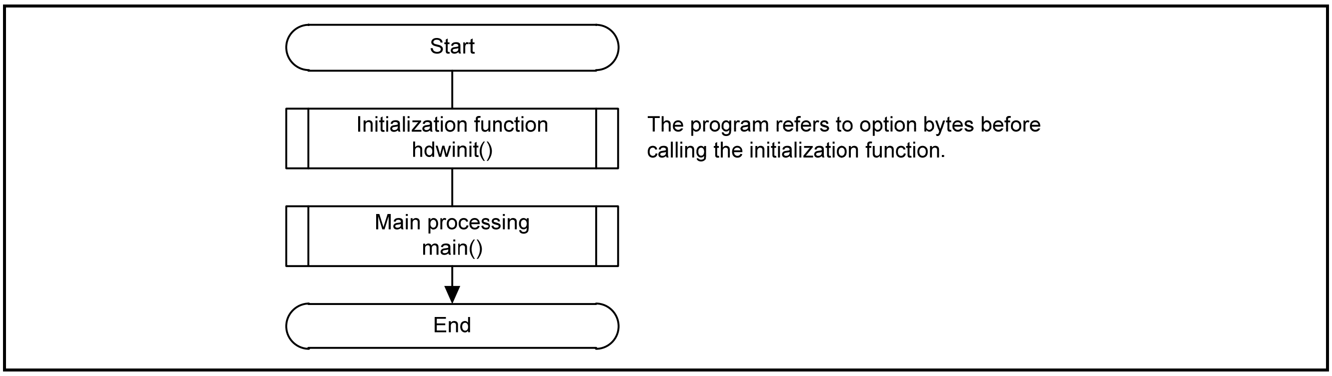


Figure 5.2 Overall Flow

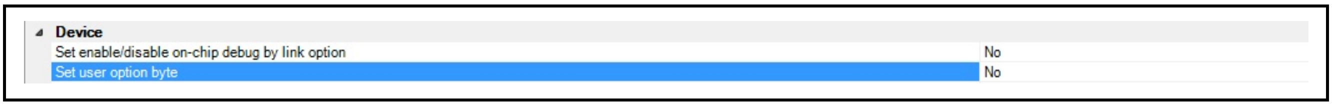
Option byte setting overview:

RL78/L13 option bytes consist of user option bytes (000C0H to 000C2H) and on-chip debug option bytes (000C3H). At power-on or when a reset is released, RL78/L13 automatically refers to the option bytes to set the function specified.

User option bytes:

- Settings associated with the WDT (000C0H)
- Settings associated with the LVD (000C1H)
- HOCO and flash memory operation (000C2H)
- On-chip debug option bytes (000C3H)

Option bytes can also be specified in the [Device] category of the [Link Options] tab. As link options setting is prior to settings in the program, select [No] in the [Set user option byte] property.



Note: To learn more on how to set Link Options in CS+, refer to the CS+ Tutorial manual.

(1) 000C0H (WDT settings)

7	6	5	4	3	2	1	0
WDTINT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON
0	1	1	0	1	1	1	0

- Bit 7

WDTINT bit	Use of interval interrupt of watchdog timer
0	Interval interrupt is not used
1	Interval interrupt is generated when 75% of the overflow time is reached

- Bits 6 and 5

Bits WINDOW1 and WINDOW0	Watchdog timer window open period
0	Setting prohibited
1	50%
10	75%
11	100%

- Bit 4

WDTON bit	Operation control of watchdog timer counter
0	Counter operation disabled (counting stopped after reset)
1	Counter operation enabled (counting started after reset)

- Bits 3 to 1

Bits WDCS2 to WDCS0	Watchdog timer overflow time
000	$2^6/f_{IL}$
001	$2^7/f_{IL}$
010	$2^8/f_{IL}$
011	$2^9/f_{IL}$
100	$2^{11}/f_{IL}$
101	$2^{13}/f_{IL}$
110	$2^{14}/f_{IL}$
111	$2^{16}/f_{IL}$

- Bit 0

WDSTBYON bit	Operation control of watchdog timer counter
0	Counter operation stopped in HALT/STOP mode
1	Counter operation enabled in HALT/STOP mode

(2) 000C1H (LVD settings)

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0
0	**1**	**1**	1	**1**	**1**	**1**	**1**

- Setting in interrupt & reset mode

Detection Voltage			**Option Byte Setting Value**							
V_{LVDH}		V_{LVDL}	Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	Falling edge	LVIMDS1	LVIMDS0					
1.77 V	1.73 V	1.63 V	1	0	0	0	0	1	0
1.88 V	1.84 V							0	1
2.92 V	2.86 V							0	0
1.98 V	1.94 V	1.84 V				0	1	1	0
2.09 V	2.04 V							0	1
3.13 V	3.06 V							0	0
2.61 V	2.55 V	2.45 V				1	0	1	0
2.71 V	2.65 V							0	1
3.75 V	3.67 V							0	0
2.92 V	2.86 V	2.75 V				1	1	1	0
3.02 V	2.96 V							0	1
4.06 V	3.98 V							0	0
Other than above			Setting prohibited						

- Setting in reset mode

Detection Voltage		**Option Byte Setting Value**						
V_{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
1.67 V	1.63 V	1	1	0	0	0	1	1
1.77 V	1.73 V				0	0	1	0
1.88 V	1.84 V				0	1	1	1
1.98 V	1.94 V				0	1	1	0
2.09 V	2.04 V				0	1	0	1
2.50 V	2.45 V				1	0	1	1
2.61 V	2.55 V				1	0	1	0
2.71 V	2.65 V				1	0	0	1
2.81 V	2.75 V				1	1	1	1
2.92 V	2.86 V				1	1	1	0
3.02 V	2.96 V				1	1	0	1
3.13 V	3.06 V				0	1	0	0
3.75 V	3.67 V				1	0	0	0
4.06 V	3.98 V				1	1	0	0
Other than above		Setting prohibited						

- Setting in interrupt mode

Detection Voltage		**Option Byte Setting Value**						
V_{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
1.67 V	1.63 V	0	1	0	0	1	1	1
1.77 V	1.73 V				0	0	1	0
1.88 V	1.84 V				0	1	1	1
1.98 V	1.94 V				0	1	1	0
2.09 V	2.04 V				0	1	0	1
2.50 V	2.45 V				1	0	1	1
2.61 V	2.55 V				1	0	1	0
2.71 V	2.65 V				1	0	0	1
2.81 V	2.75 V				1	1	1	1
2.92 V	2.86 V				1	1	1	0
3.02 V	2.96 V				1	1	0	1
3.13 V	3.06 V				0	1	0	0
3.75 V	3.67 V				1	0	0	0
4.06 V	3.98 V				1	1	0	0
Other than above		Setting prohibited						

- Setting when LVD is off

Detection Voltage		**Option Byte Setting Value**						
V_{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
–	–	×	1	1	×	×	×	×
Other than above		Setting prohibited						

Note: ×: don’t care

(3) 000C2H (HOCO and flash operation mode settings)

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0
1	**1**	**1**	**0**	**0**	**0**	**0**	**0**

- Bits 7 and 6

CMODE1 bit	CMODE0 bit	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low-voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low-speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high-speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 24 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

- Bits 3 to 0

FRQSEL4 bit	FRQSEL3 bit	FRQSEL2 bit	FRQSEL1 bit	FRQSEL0 bit	Frequency of the high-speed on-chip oscillator clock	
					f_{HOCO}	f_{IH}
1	0	0	0	0	48 MHz	24 MHz
0	0	0	0	0	24 MHz	24 MHz
0	1	0	0	1	16 MHz	16 MHz
0	0	0	0	1	12 MHz	12 MHz
0	1	0	1	0	8 MHz	8 MHz
0	1	0	1	1	4 MHz	4 MHz
0	1	1	0	1	1 MHz	1 MHz
Other than above					Setting prohibited	

(4) 000C3H (On-chip debug option byte)

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	0	OCDERSD
1	0	0	0	0	1	0	**0**

- Bits 7, 0

OCDENSET bit	OCDERSD bit	Control of on-chip debug operation
0	0	Disables on-chip debug operation
0	1	Setting prohibited
1	0	Enables on-chip debugging. Erases data of flash memory in case of failures in authenticating on-chip debug security ID.
1	1	Enables on-chip debugging. Does not erases data of flash memory in case of failures in authenticating on-chip debug security ID.

5.8.1 Initialization

Figure 5.3 shows the initialization.

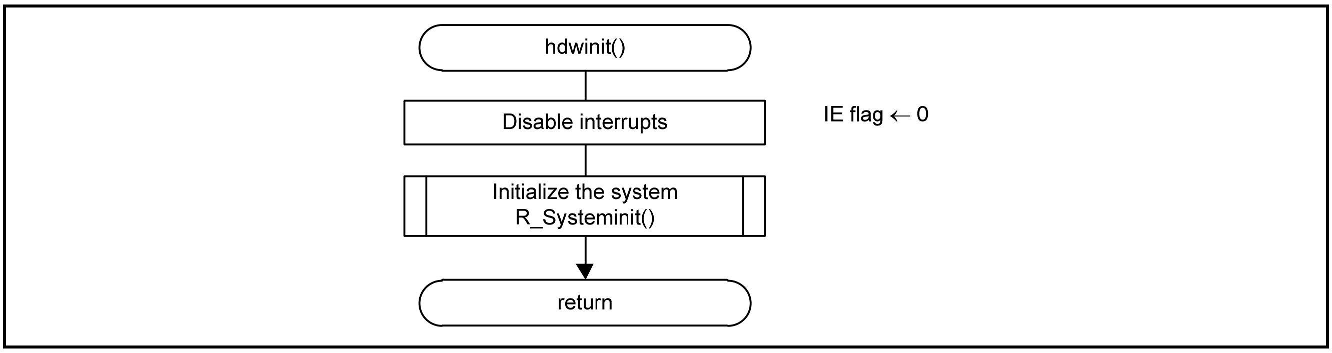


Figure 5.3 Initialization

5.8.2 System Initialization

Figure 5.4 shows the system initialization.

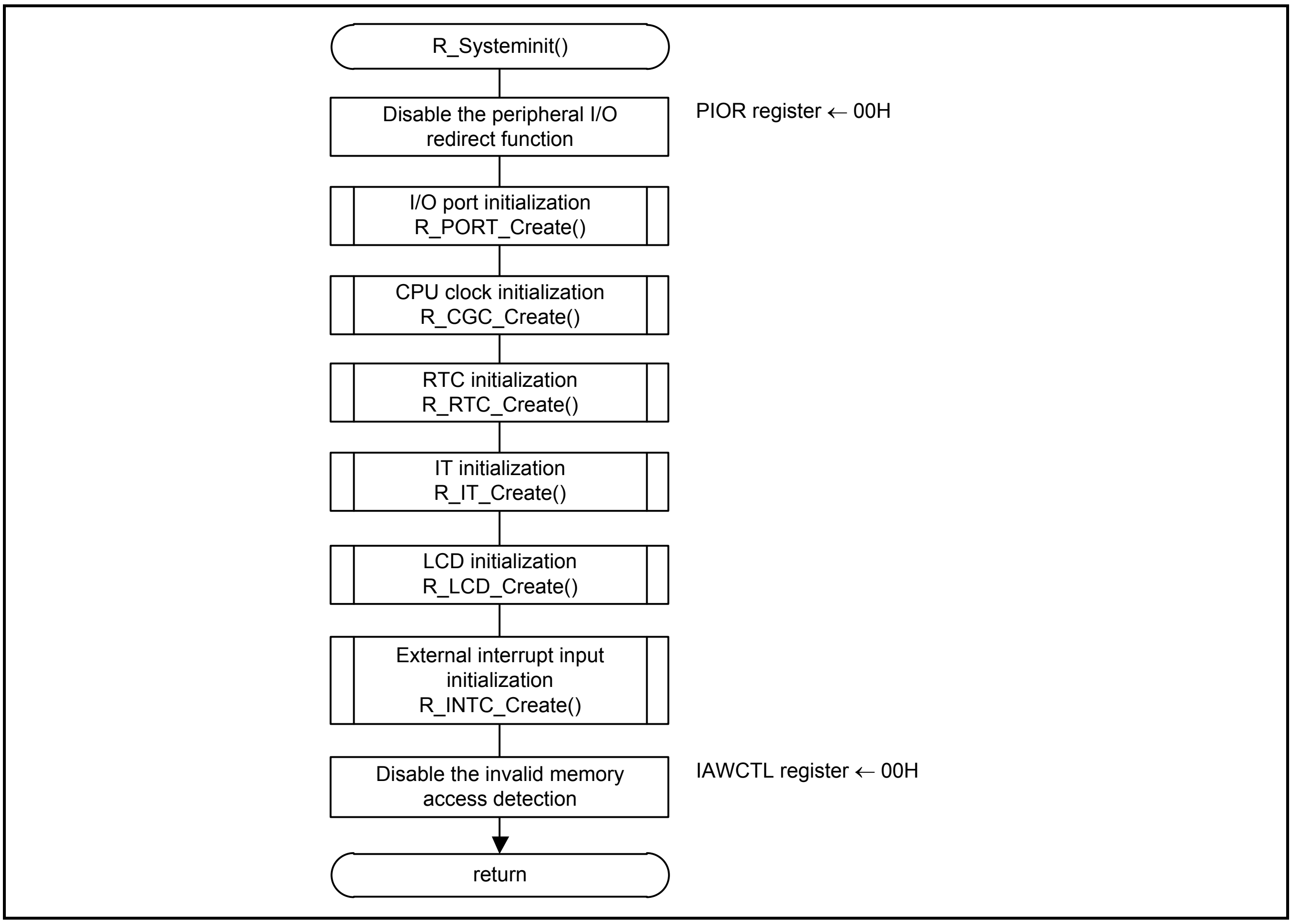


Figure 5.4 System Initialization

5.8.3 I/O Port Setting

Figure 5.5 shows the I/O port setting.

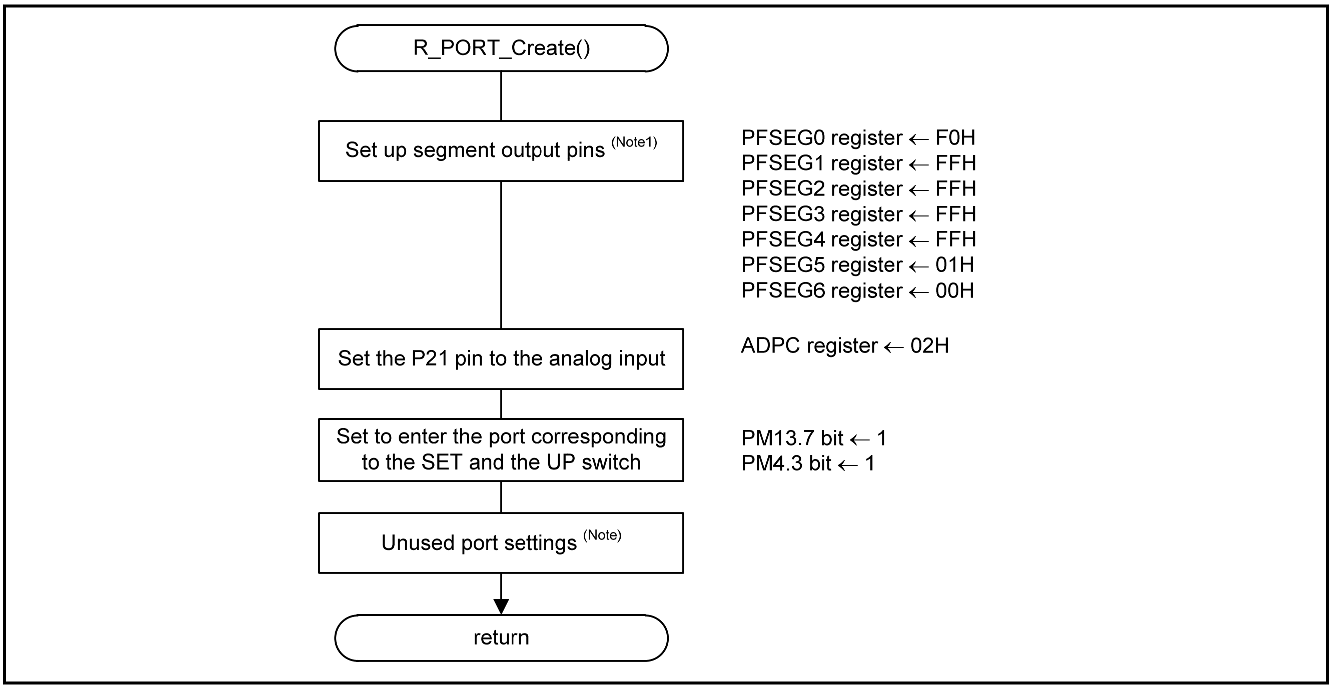


Figure 5.5 I/O Port Setting

Note1: Refer to the RL78/L13 User's Manual: Hardware for the setting of the unused port.

Note2: Segment signals (SEG0 to SEG18, and SEG28 to SEG39) connected to the LCD module on the CPU board are also set as segment pins in the sample code.

5.8.4 CPU Clock Setting

Figure 5.6 shows the CPU clock setting.

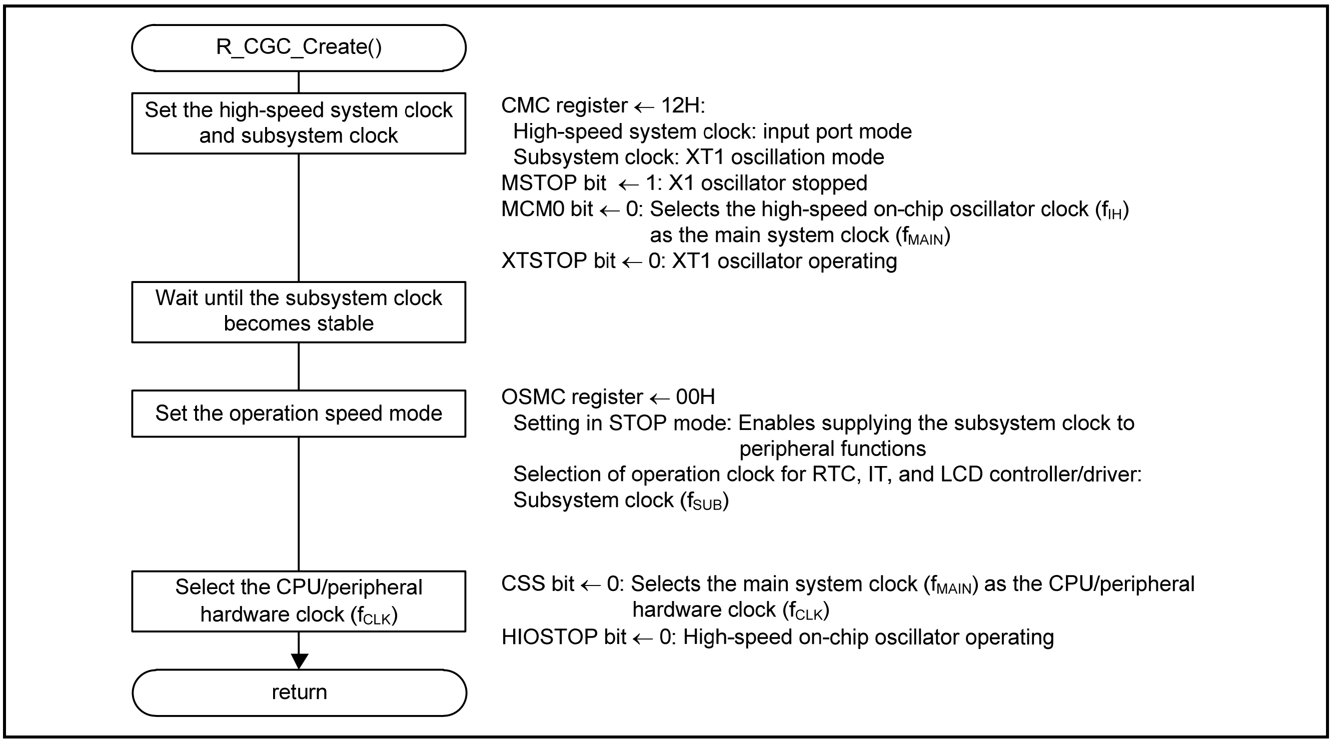


Figure 5.6 CPU Clock Setting

5.8.5 RTC Setting

Figure 5.7 shows the RTC setting.

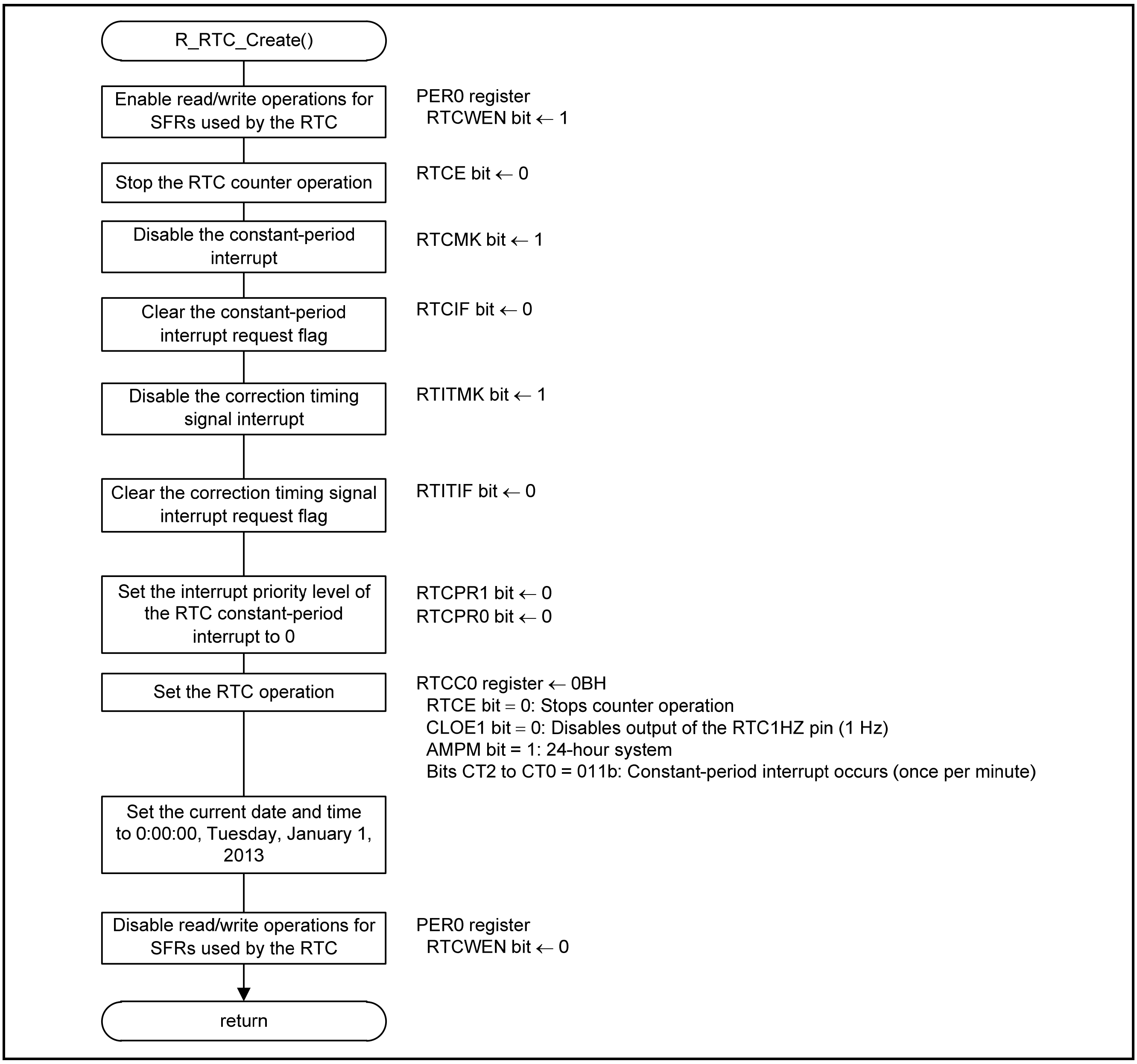


Figure 5.7 RTC Setting

Enabling read and write operations for SFRs used by the RTC

- Peripheral enable register 0 (PER0)

Enable read/write operations for SFRs used by the RTC.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN
1	0	0	0	0	0	0	0

- Bit 7

RTCWEN bit	Control of high-accuracy real-time clock (RTC) input clock supply
0	Stops input clock supply • SFRs used by the high-accuracy real-time clock (RTC) cannot be written • The high accuracy real-time clock (RTC) is operable
1	Enables input clock supply • SFRs used by the high-accuracy real-time clock (RTC) can be read and written • The high accuracy real-time clock (RTC) is operable

Note: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Setting the RTC operation

- Real-time clock control register 0 (RTCC0)
  - Real-time clock: Counter operation is stopped
  - Output signals from the RTC1HZ pin: Disabled
  - 12-hour or 24-hour system: 24-hour system
  - Constant-period interrupt function: Once per minute

Symbol: RTCC0

7	6	5	4	3	2	1	0
RTCE	0	RCLOE1	0	AMPM	CT2	CT1	CT0
0	0	0	0	1	0	1	1

- Bit 7

RTCE bit	High accuracy real-time clock operation control
0	Stops counter operation
1	Starts counter operation

- Bit 5

RCLOE1 bit	RTC1HZ pin output control
0	Disables output of the RTC1HZ pin (1 Hz)
1	Enables output of the RTC1HZ pin (1 Hz)

- Bit 3

AMPM bit	12-/24-hour system select
0	12-hour system (a.m. and p.m. are displayed)
1	24-hour system

- Bits 2 to 0

CT2 bit	CT1 bit	CT0 bit	Constant-period interrupt (INTRTC) selection
0	0	0	Does not use constant-period interrupt function
0	0	1	Once every 0.5 seconds (synchronized with counting up seconds)
0	1	0	Once per second (same time as counting up seconds)
0	**1**	**1**	**Once per minute (second 00 every minute)**
1	0	0	Once per hour (minute 00 and second 00 every hour)
1	0	1	Once per day (hour 00, minute 00, and second 00 every day)
1	1	×	Once per month (date 1, hour 00 a.m., minute 00, and second 00 every month)

Note: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Disabling read and write operations for SFRs used by the RTC

- Peripheral enable register 0 (PER0)

Disable read/write operations for SFRs used by the RTC.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN
0	0	0	0	0	0	0	0

- Bit 7

RTCWEN bit	Control of high-accuracy real-time clock (RTC) input clock supply
0	Stops input clock supply • SFRs used by the high-accuracy real-time clock (RTC) cannot be written • The high-accuracy real-time clock (RTC) is operable
1	Enables input clock supply • SFRs used by the high-accuracy real-time clock (RTC) can be read and written • The high-accuracy real-time clock (RTC) is operable

Note: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

5.8.6 IT Setting

Figure 5.8 shows the IT setting.

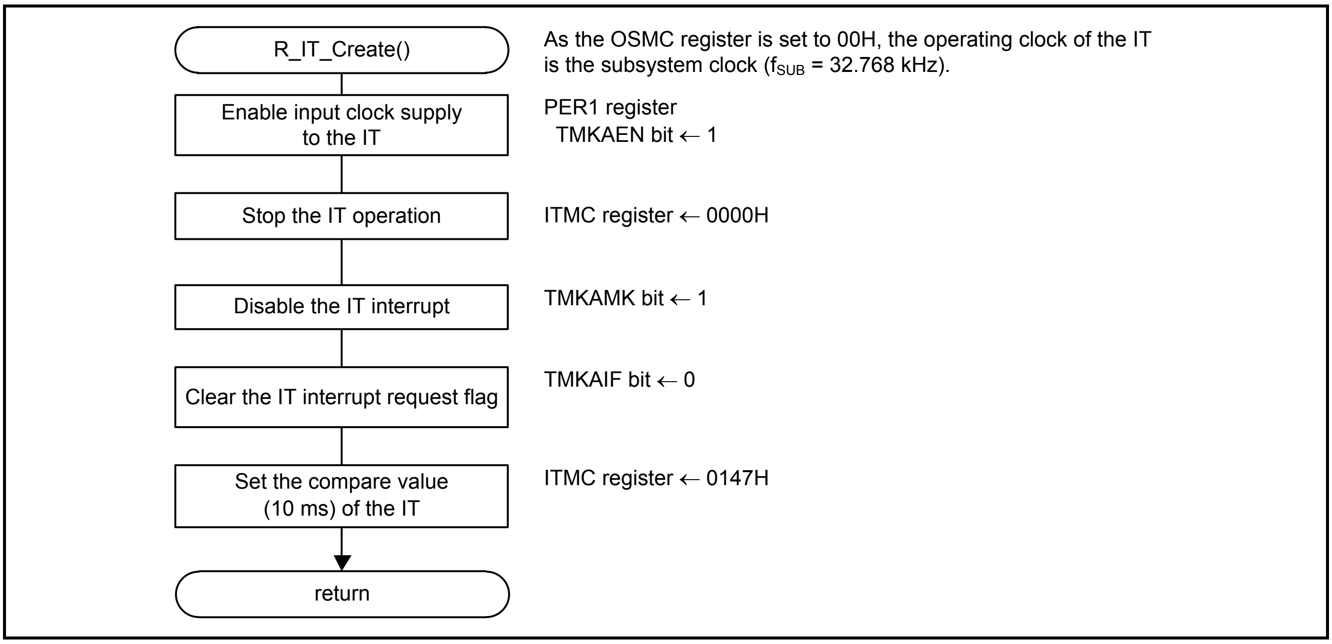


Figure 5.8 IT Setting

5.8.7 External Interrupt Input Setting

The sample code accompanying this application note uses external interrupts INTP0 and INTP7.

Figure 5.9 shows the interrupt setting.

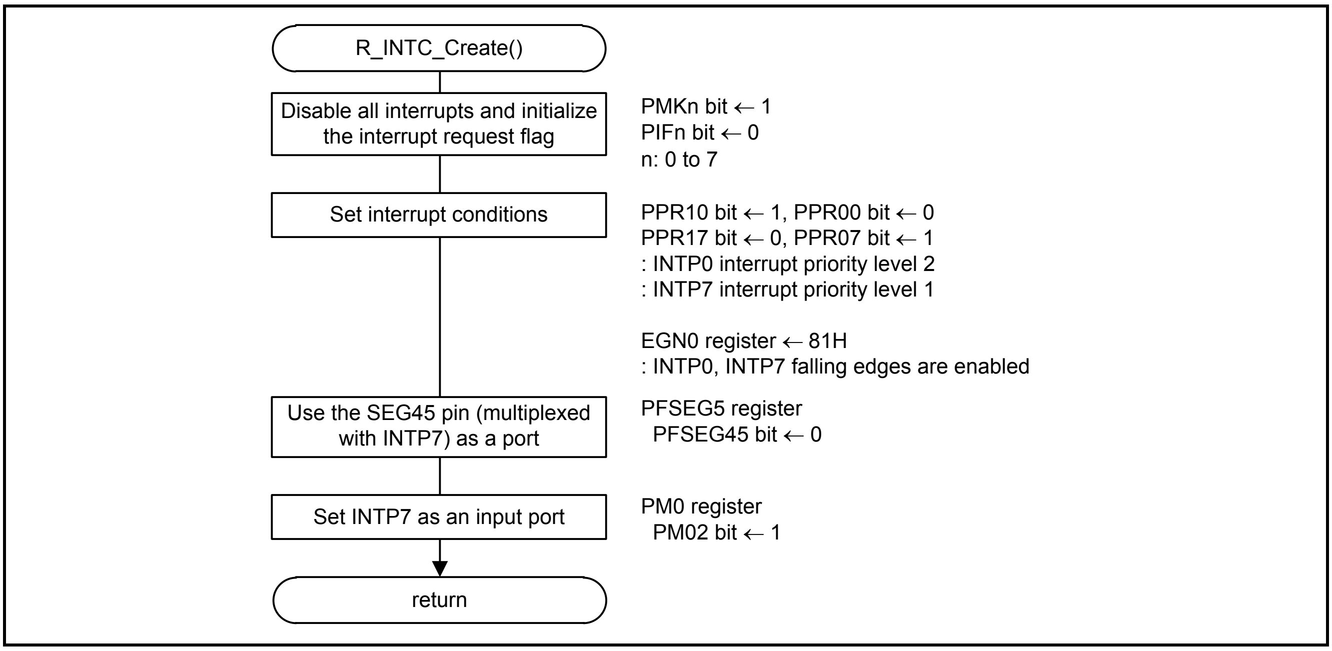


Figure 5.9 Interrupt Setting

5.8.8 LCD Controller/Driver Setting

Figure 5.10 and Figure 5.11 show the LCD controller/driver setting.

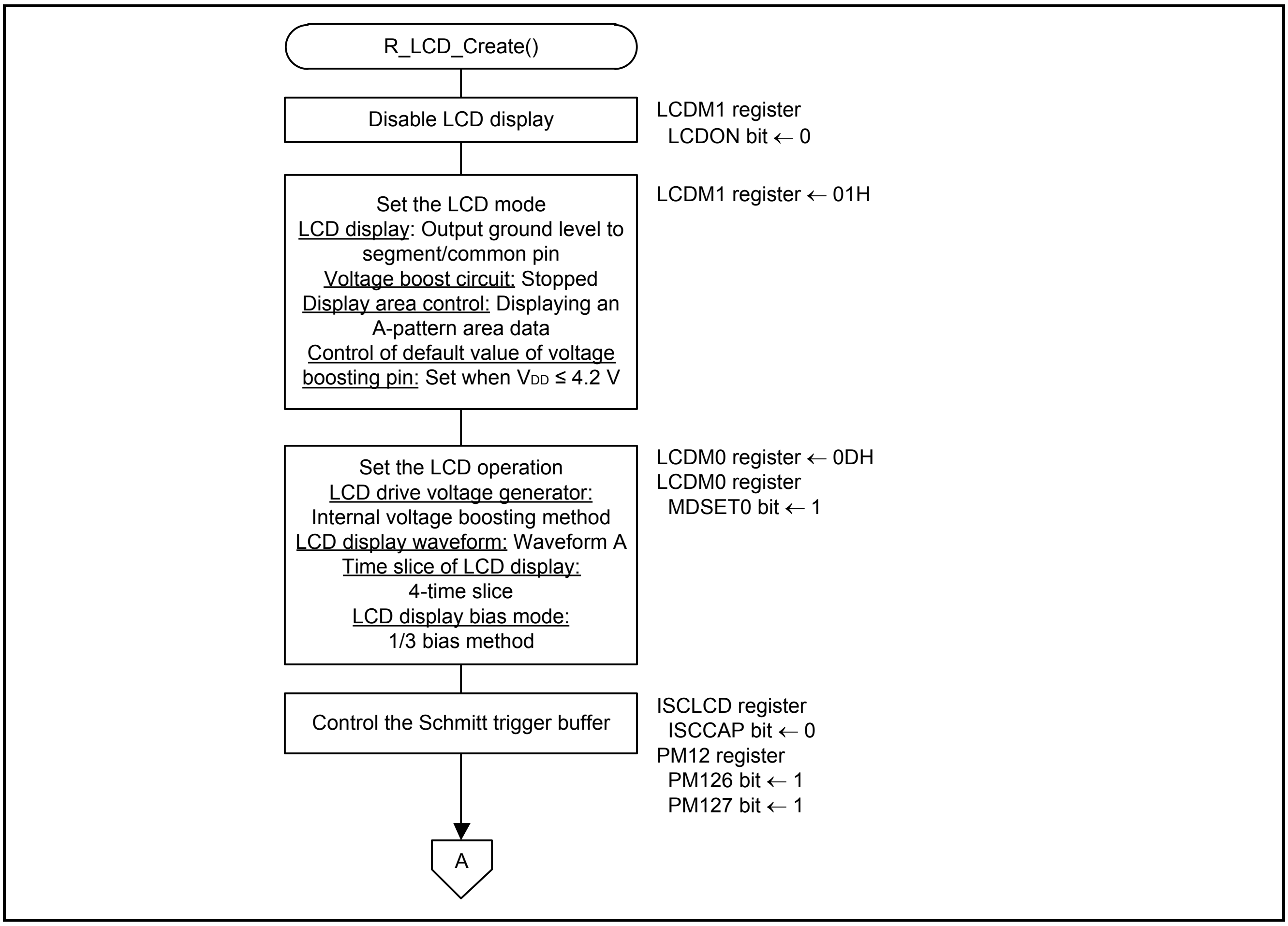


Figure 5.10 LCD Controller/Driver Setting (1/2)

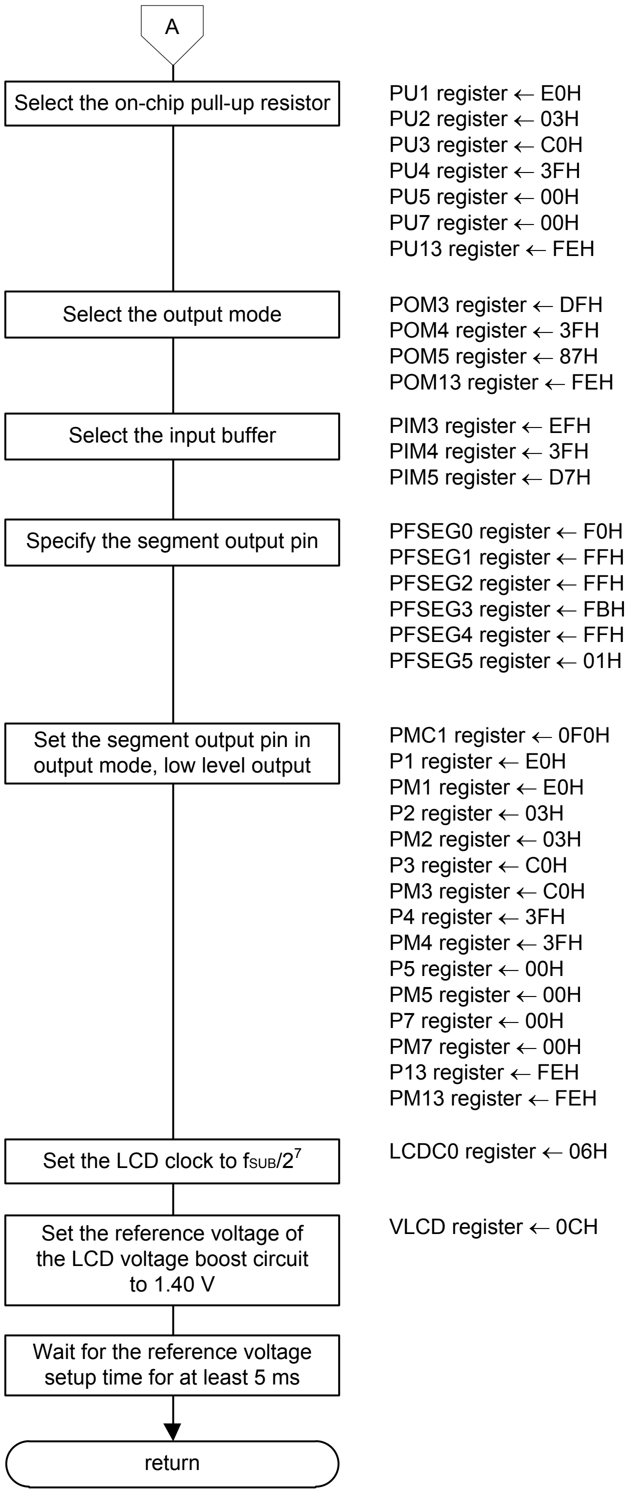


Figure 5.11 LCD Controller/Driver Setting (2/2)

Setting the LCD mode

- LCD mode register 1 (LCDM1)
  — Outputs ground level to segment/common pin
  — Stops the voltage boost circuit
  — Displays an A-pattern area data
  — Sets the default value of the voltage boosting pin when $V_{DD} \leq 3.8$ V

Symbol: LCDM1

7	6	5	4	3	2	1	0
LCDON	SCOC	VLCON	BLON	LCDSEL	0	0	LCDVLM
0	0	0	0	0	0	0	1

- Bits 7 and 6

SCOC bit	LCDON bit	LCD display enable/disable Waveform A or B is output
0	0	Output ground level to segment/common pin
0	1	
1	0	Display off (all segment outputs are deselected)
1	1	Display on

- Bit 5

VLCON bit	Voltage boost circuit or capacitor split circuit operation enable/disable
0	Stops voltage boost circuit or capacitor split circuit operation
1	Enables voltage boost circuit or capacitor split circuit operation

- Bits 4 and 3

BLON bit Note	LCDSEL bit	Display data area control
0	0	Displaying an A-pattern area data (lower four bits of LCD display data register)
0	1	Displaying a B-pattern area data (higher four bits of LCD display data register)
1	0	Alternately displaying A-pattern and B-pattern area data (blinking display corresponding to the constant-period interrupt (INTRTC) timing of the high-accuracy real-time clock (RTC))
1	1	

Note: When f_{IL} is selected as the LCD source clock (f_{LCD}), be sure to set the BLON bit to “0”.

- Bit 1

LCDVLM bit Note	Control of default value of voltage boosting pin
0	Set when $V_{DD} \geq 2.7$ V
1	Set when $V_{DD} \leq 4.2$ V

Note: This function is used to shorten the boost stabilization time by setting the V_{LX} pin to the default status when the voltage boost circuit is used. If the V_{DD} voltage is 2.7V or higher when boosting is started, set the LCDVLM bit to “0”; if the V_{DD} voltage is 4.2 V or less, set the LCDVLM bit to “1”. However, when $2.7V \leq V_{DD} \leq 4.2V$, operation is possible with LCDVLM = 0 or LCDVLM = 1.

Note: For details on register setting, refer to the RL78/L13 User’s Manual: Hardware.

Setting the LCD operation

- LCD mode register 0 (LCDM0)
  - Time slice of LCD display: 4-time slice
  - LCD display bias mode: 1/3 bias method
  - LCD drive voltage generator: Internal voltage boosting method

Symbol: LCDM0

7	6	5	4	3	2	1	0
MDSET1	MDSET0	LWAVE	LDTY2	LDTY1	LDTY0	LBAS1	LBAS0
0	1	0	0	1	1	0	1

- Bits 7 and 6

MDSET1 bit	MDSET0 bit	LCD drive voltage generator selection
0	0	External resistance division method
0	1	Internal voltage boosting method
1	0	Capacitor split method Note 1
1	1	Setting prohibited

- Bit 5

LWAVE bit	LCD display waveform selection
0	Waveform A
1	Waveform B

- Bits 4 to 2

LDTY2 bit	LDTY1 bit	LDTY0 bit	Selection of time slice of LCD display
0	0	0	Static
0	0	1	2-time slice
0	1	0	3-time slice
0	1	1	4-time slice
1	0	1	8-time slice
Other than above			Setting prohibited

- Bits 1 and 0

LBAS1 bit	LBAS0 bit	LCD display bias mode selection
0	0	1/2 bias method
0	1	1/3 bias method
1	0	1/4 bias method
1	1	Setting prohibited

Note: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Controlling the Schmitt trigger buffer

- LCD input switch control register (ISCLCD)

Input to the Schmitt trigger: Input invalid

Symbol: ISCLCD

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ISCVL3	ISCCAP
0	1	0	0	1	1	0	0

- Bit 0

ISCCAP bit	CAPL/P126, CAPH/P127 pins Schmitt trigger buffer control
0	Input invalid
1	Input valid

The functions of the CAPL/P126, and CAPH/P127 pins can be selected by using the LCD input switch control register (ISCLCD), LCD mode register 0 (LCDM0), and port mode register 12 (PM12).

CAPL/P126, CAPH/P127 Pin Function Settings:

LCD Drive Voltage Generator	ISCCAP Bit in the ISCLCD Register	Bits PM126 and PM127 in the PM12 Register	Pin Function	Initial Status
External resistance division	0	1	Digital input invalid mode	✓
	1	0	Digital output mode	–
	1	1	Digital input mode	–
Internal voltage boosting or capacitor split	0	1	CAPL/CAPH function mode	–
Other than above			Setting prohibited	

Note: For details on register setting, refer to the RL78/L13 User’s Manual: Hardware.

Selecting the on-chip pull-up resistor

- Pull-up resistor option registers (PU3 to PU7)

On-chip pull-up resistor: Not connected

Symbol: PU1

7	6	5	4	3	2	1	0
PU17	PU16	PU15	**PU14**	**PU13**	**PU12**	**PU11**	**PU10**
0	0	0	**0**	**0**	**0**	**0**	**0**

- Bits 4 to 0

PUmn bit	Pmn pin on-chip pull-up resistor selection (m = 1, n = 0 to 4)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol: PU2

7	6	5	4	3	2	1	0
PU27	**PU26**	**PU25**	**PU24**	**PU23**	**PU22**	0	0
0	**0**	**0**	**0**	**0**	**0**	0	0

- Bits 7 to 2

PUmn bit	Pmn pin on-chip pull-up resistor selection (m = 2, n = 2 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol: PU3

7	6	5	4	3	2	1	0
0	0	**PU35**	**PU34**	**PU33**	**PU32**	**PU31**	**PU30**
0	0	**0**	**0**	**0**	**0**	**0**	**0**

- Bits 5 to 0

PUmn bit	Pmn pin on-chip pull-up resistor selection (m = 3, n = 0 to 5)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol: PU4

7	6	5	4	3	2	1	0
PU47	**PU46**	PU45	PU44	PU43	PU42	PU41	PU40
0	**0**	0	0	0	0	0	0

- Bits 7 to 6

PUmn bit	Pmn pin on-chip pull-up resistor selection (m = 4, n = 6 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol: PU5

7	6	5	4	3	2	1	0
PU57	**PU56**	**PU55**	**PU54**	**PU53**	**PU52**	**PU51**	**PU50**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

- Bits 7 and 0

PUmn bit	Pmn pin on-chip pull-up resistor selection (m = 5, n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol: PU7

7	6	5	4	3	2	1	0
PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70
0	0	0	0	0	0	0	0

- Bits 7 and 6

PUmn bit	Pmn pin on-chip pull-up resistor selection, m = 7, n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol: PU13

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PU130
0	0	0	0	0	0	0	**0**

- Bits 0

PUmn bit	Pmn pin on-chip pull-up resistor selection, m = 13, n = 0)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Note: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Specifying the segment output pin

- LCD port function registers 2 and 3 (PFSEG2, PFSEG3)

P30 to P35, P46, P47, and P77: Used as the segment output (Note)

Note: Segment signals (SEG0 to SEG18, and SEG28 to SEG39) connected to the LCD module on the CPU board are also set as the segment pins in the sample code.

Symbol: PFSEG2

7	6	5	4	3	2	1	0
PFSEG23	**PFSEG22**	**PFSEG21**	**PFSEG20**	**PFSEG19**	PFSEG18	PFSEG17	PFSEG16
1	**1**	**1**	**1**	**1**	1	1	1

- Bits 7 to 3

Bits PFSEG23 to PFSEG19	Port (other than segment output)/segment outputs specification of Pmn pins, mn = 77, 30 to 33
0	Used the Pmn pin as port (other than segment output)
1	Used the Pmn pin as segment output

Symbol: PFSEG3

7	6	5	4	3	2	1	0
PFSEG30	PFSEG29	PFSEG28	**PFSEG27**	**PFSEG26**	PFDEG	**PFSEG25**	**PFSEG24**
1	1	1	**1**	**1**	0	**1**	**1**

- Bits 4, 3, 1, 0

Bits PFSEG24 to PFSEG27	Port (other than segment output)/segment outputs specification of Pmn pins, mn = 34, 35, 46, 47
0	Used the Pmn pin as port (other than segment output)
1	Used the Pmn pin as segment output

Note: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Setting the LCD clock

- LCD clock control register 0 (LCDC0)

Sets the LCD clock to $f_{SUB}/2^7$.

Symbol: LCDC0

7	6	5	4	3	2	1	0
0	0	**LCDC05**	**LCDC04**	**LCDC03**	**LCDC02**	**LCDC01**	**LCDC00**
0	0	**0**	**0**	**0**	**1**	**1**	**0**

- Bits 5 to 0

LCDC05 Bit	LCDC04 Bit	LCDC03 Bit	LCDC02 Bit	LCDC01 Bit	LCDC00 Bit	LCD Clock (LCDCL)
0	0	0	1	0	0	$f_{SUB}/2^5$ or $f_{IL}/2^5$
0	0	0	1	0	1	$f_{SUB}/2^6$ or $f_{IL}/2^6$
0	0	0	1	1	0	$f_{SUB}/2^7$ or $f_{IL}/2^7$
0	0	0	1	1	1	$f_{SUB}/2^8$ or $f_{IL}/2^8$
0	0	1	0	0	0	$f_{SUB}/2^9$ or $f_{IL}/2^9$
0	0	1	0	0	1	$f_{SUB}/2^{10}$
0	1	0	0	1	1	$f_{MAIN}/2^{10}$
0	1	0	1	0	0	$f_{MAIN}/2^{11}$
0	1	0	1	0	1	$f_{MAIN}/2^{12}$
0	1	0	1	1	0	$f_{MAIN}/2^{13}$
0	1	0	1	1	1	$f_{MAIN}/2^{14}$
0	1	1	0	0	0	$f_{MAIN}/2^{15}$
0	1	1	0	0	1	$f_{MAIN}/2^{16}$
0	1	1	0	1	0	$f_{MAIN}/2^{17}$
0	1	1	0	1	1	$f_{MAIN}/2^{18}$
1	0	1	0	1	1	$f_{MAIN}/2^{19}$
Other than above						Setting prohibited

Note: When the capacitor split method or memory liquid crystal waveform has been specified, selecting f_{IL} as the LCD source clock (f_{LCD}) is prohibited.

Note: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Setting the reference voltage of the voltage boost circuit

- LCD boost level control register (VLCD)

Sets the reference voltage to 1.40 V (V_{L4} = 4.20 V).

Symbol: VLCD

7	6	5	4	3	2	1	0
0	0	0	**VLCD4**	**VLCD3**	**VLCD2**	**VLCD1**	**VLCD0**
0	0	0	**0**	**1**	**1**	**0**	**0**

- Bits 4 to 0

VLCD4 Bit	VLCD3 Bit	VLCD2 Bit	VLCD1 Bit	VLCD0 Bit	Reference voltage selection (contrast adjustment)	V_{L4} voltage	
						1/3 bias method	1/4 bias method
0	0	1	0	0	1.00 V (default)	3.00 V	4.00 V
0	0	1	0	1	1.05 V	3.15 V	4.20 V
0	0	1	1	0	1.10 V	3.30 V	4.40 V
0	0	1	1	1	1.15 V	3.45 V	4.60 V
0	1	0	0	0	1.20 V	3.60 V	4.80 V
0	1	0	0	1	1.25 V	3.75 V	5.00 V
0	1	0	1	0	1.30 V	3.90 V	5.20 V
0	1	0	1	1	1.35 V	4.05 V	Setting prohibited
0	**1**	**1**	**0**	**0**	**1.40 V**	**4.20 V**	
0	1	1	0	1	1.45 V	4.35 V	
0	1	1	1	0	1.50 V	4.50 V	
0	1	1	1	1	1.55 V	4.65 V	
1	0	0	0	0	1.60 V	4.80 V	
1	0	0	0	1	1.65 V	4.95 V	
1	0	0	1	0	1.70 V	5.10 V	
1	0	0	1	1	1.75 V	5.25 V	
Other than above					Setting prohibited		

Note: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

5.8.9 Main Processing

Figure 5.12 shows the main processing.

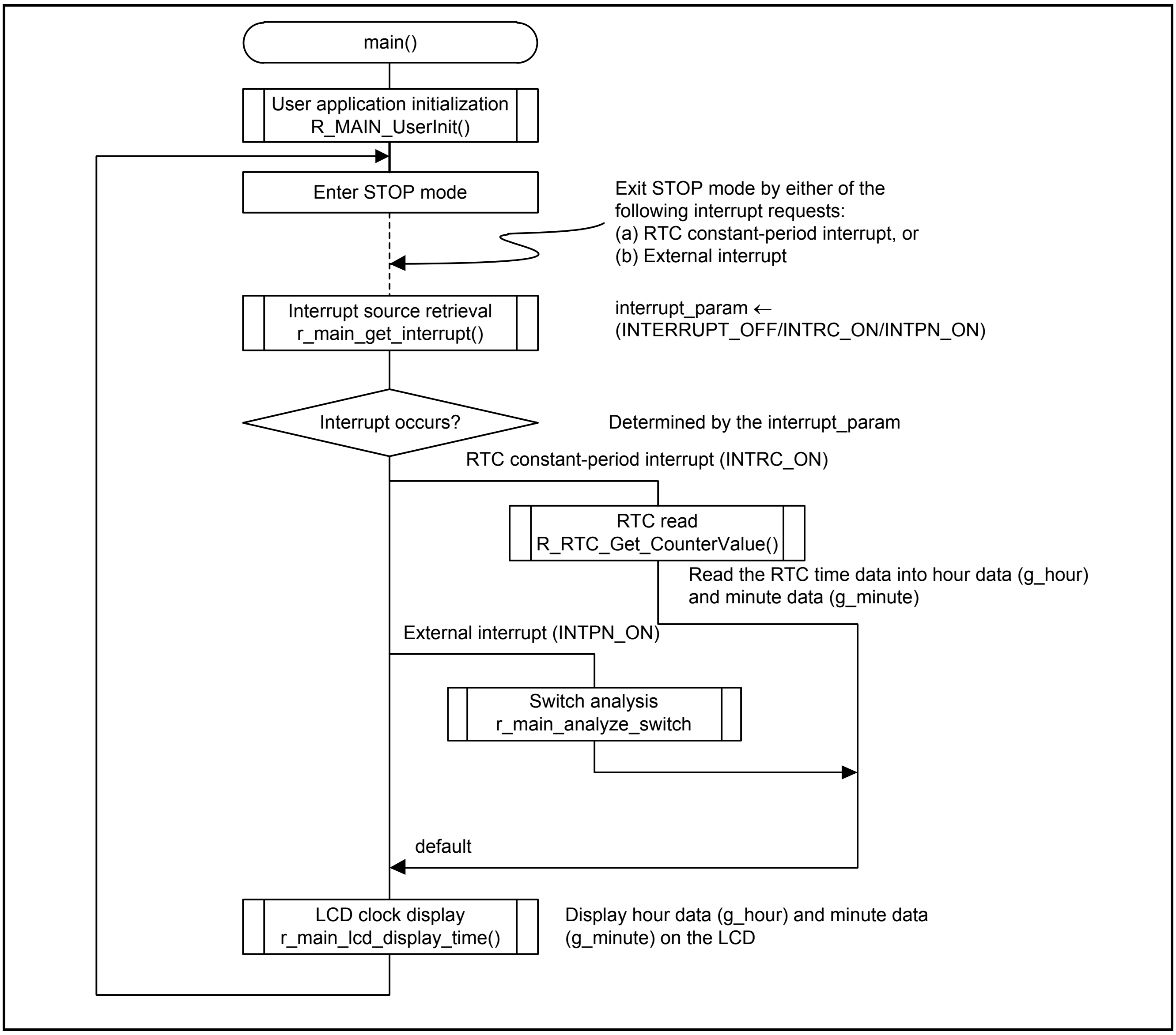


Figure 5.12 Main Processing

5.8.10 User Application Initialization

Figure 5.13 shows the user application initialization.

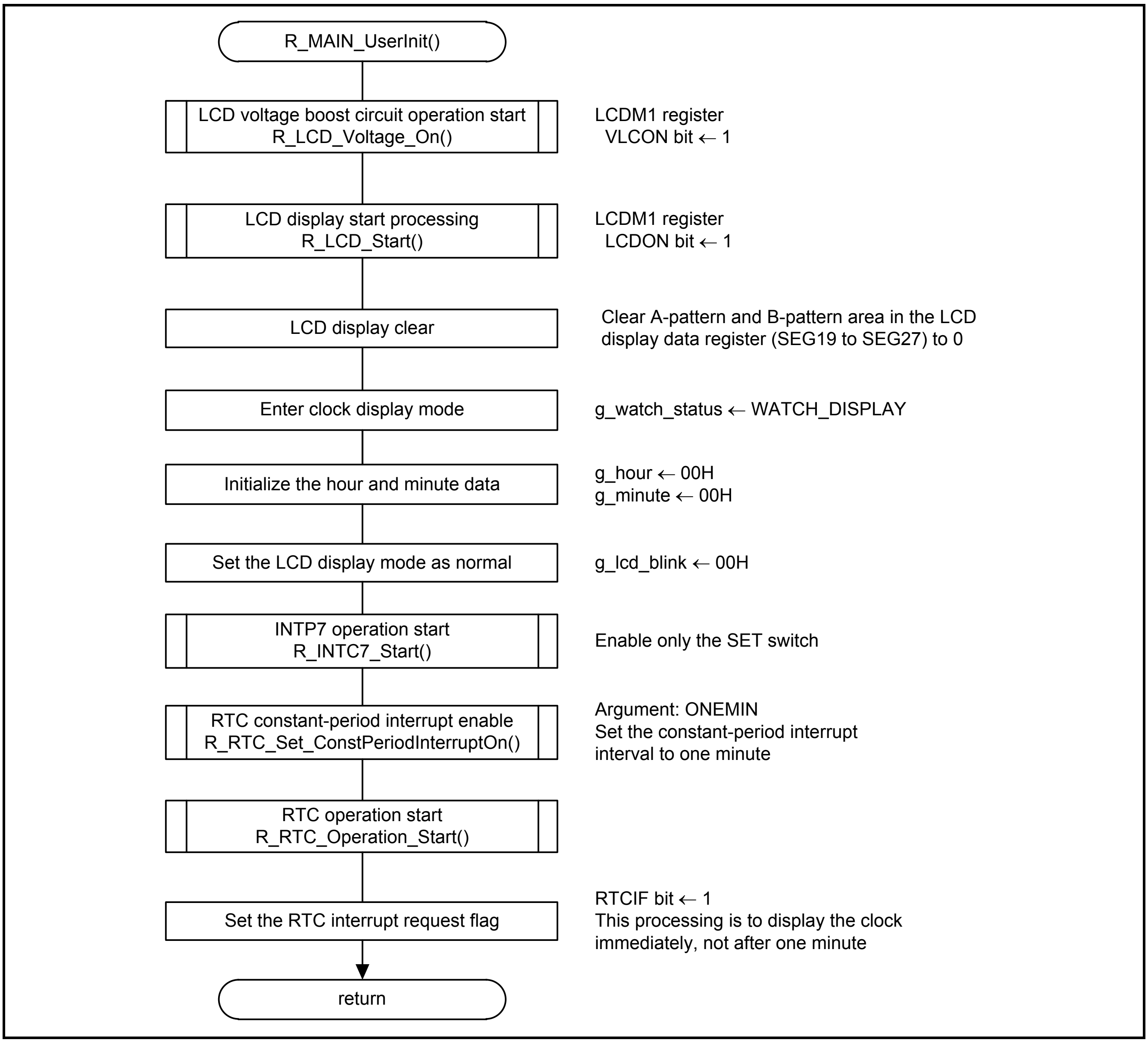


Figure 5.13 User Application Initialization

5.8.11 LCD Voltage Boost Circuit Operation Start Setting

Figure 5.14 shows the LCD voltage boost circuit operation start.

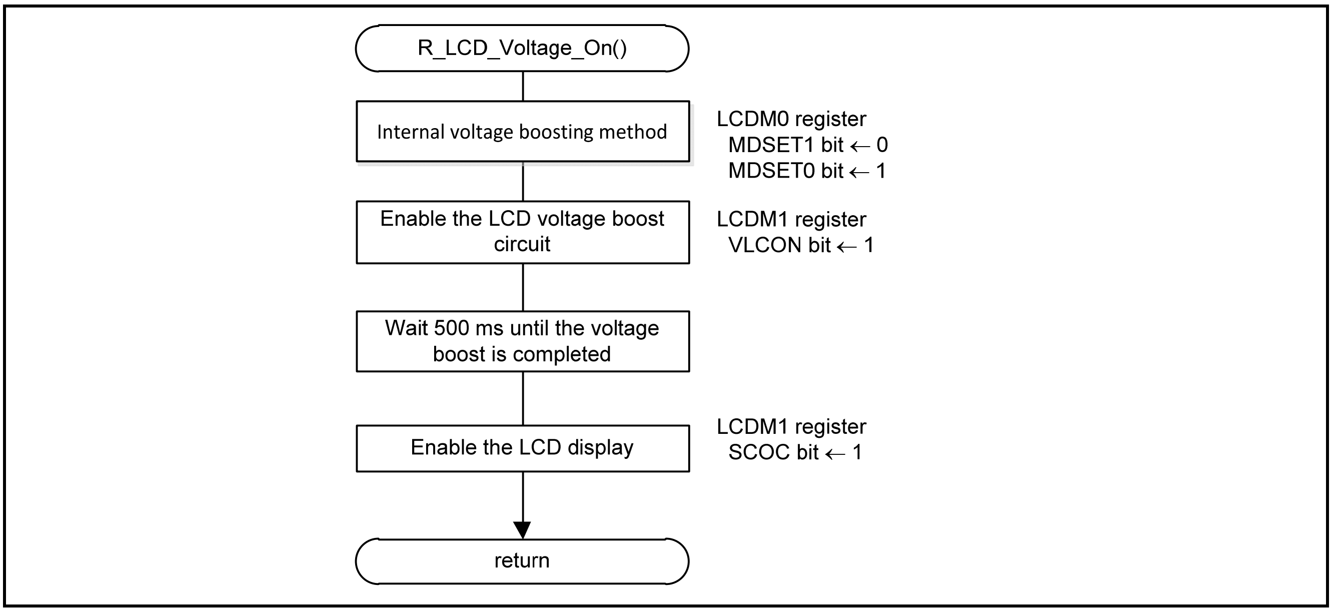


Figure 5.14 LCD Voltage Boost Circuit Operation Start Setting

Setting the LCD mode

- LCD mode register (LCDM1)
  - Output ground level to segment/common pin
  - Stops voltage boost circuit
  - Display data area: A-pattern area
  - Controls the default value of the voltage boosting pin: when $V_{DD} \leq 3.8$ V

Symbol: LCDM1

7	6	5	4	3	2	1	0
LCDON	**SCOC**	**VLCON**	BLON	LCDSEL	0	0	LCDVLM
0	**1**	**1**	0	0	0	0	1

- Bit 6

SCOC bit	LCDON bit	LCD display enable/disable waveform A or B is output
0	0	Output ground level to segment/common pin
0	1	
1	0	Display off (all segment outputs are deselected).
1	1	Display on

- Bit 5

VLCON bit	Voltage boost circuit or capacitor split circuit operation enable/disable
0	Stops voltage boost circuit or capacitor split circuit operation
1	Enables voltage boost circuit or capacitor split circuit operation

Note: For details on register setting, refer to the RL78/L13 User’s Manual: Hardware.

5.8.12 LCD Display Start Processing

Figure 5.15 shows the LCD display start processing.

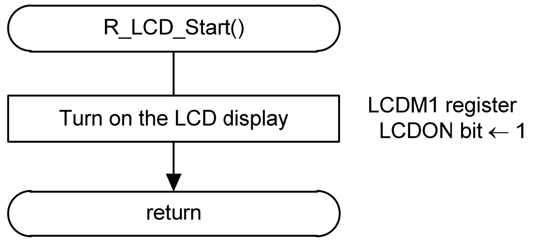


Figure 5.15 LCD Display Start Processing

Setting the LCD mode

- LCD mode register (LCDM1)
  - Output ground level to segment/common pin
  - Stops voltage boost circuit
  - Display data area: A-pattern area
  - Controls the default value of the voltage boosting pin: when $V_{DD} \leq 3.8$ V

Symbol: LCDM1

7	6	5	4	3	2	1	0
LCDON	SCOC	VLCON	BLON	LCDSEL	0	0	LCDVLM
1	1	1	0	0	0	0	1

- Bit 7

SCOC bit	LCDON bit	LCD display enable/disable waveform A or B is output
0	0	Output ground level to segment/common pin,
0	1	
1	0	Display off (all segment outputs are deselected).
1	1	Display on

Note: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

5.8.13 INTPn Operation Start Processing (n = 0, 7)

Figure 5.16 shows the INTPn operation start processing.

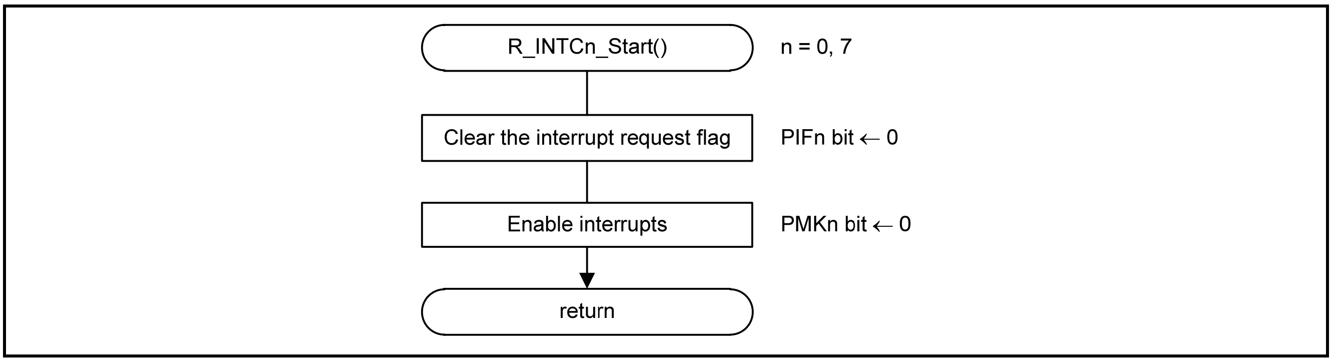


Figure 5.16 INTPn Operation Start Processing (n = 0, 7)

5.8.14 RTC Constant-period Interrupt Enable

Figure 5.17 shows the RTC constant-period interrupt enable.

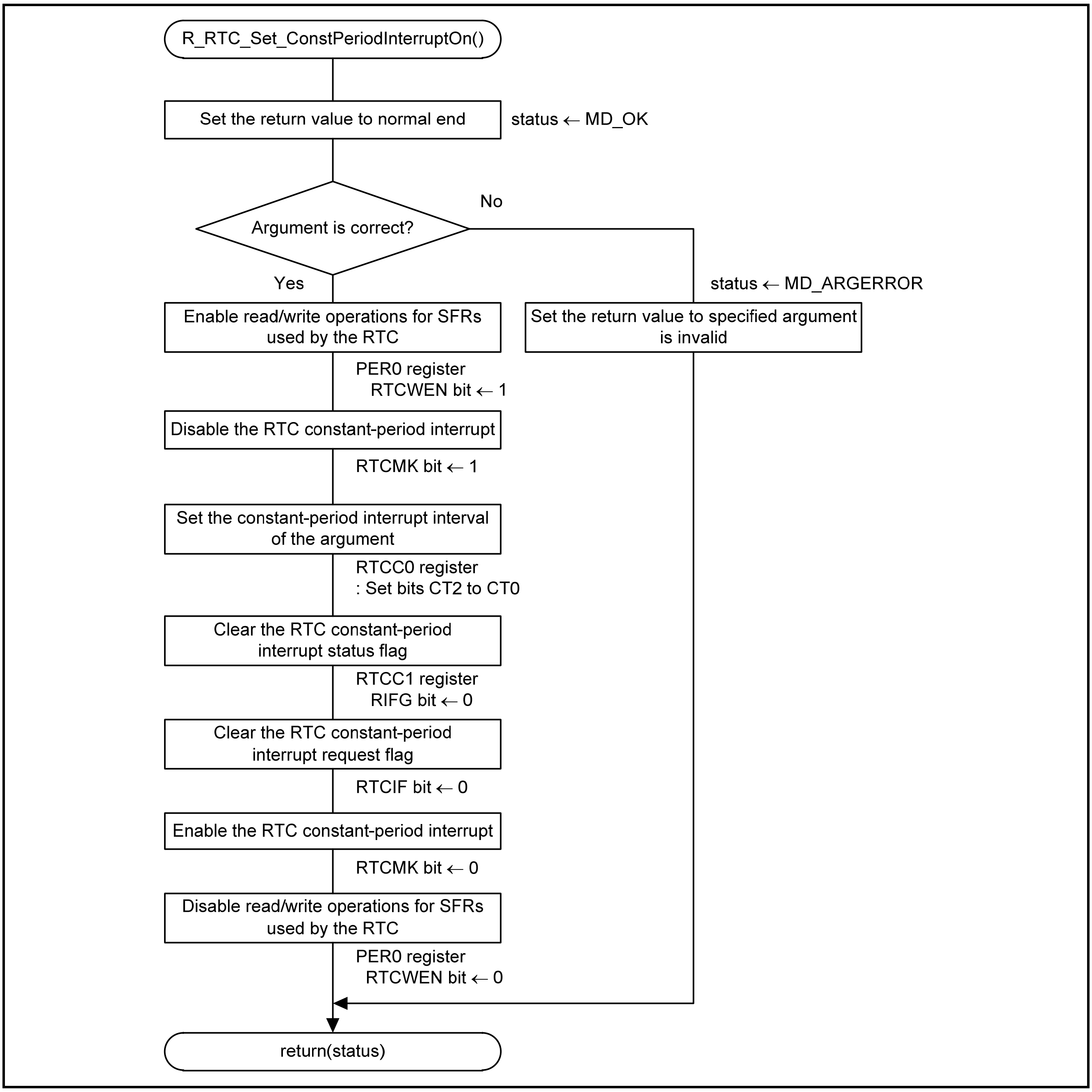


Figure 5.17 RTC Constant-period Interrupt Enable

5.8.15 RTC Operation Start Processing

Figure 5.18 shows the RTC operation start processing.

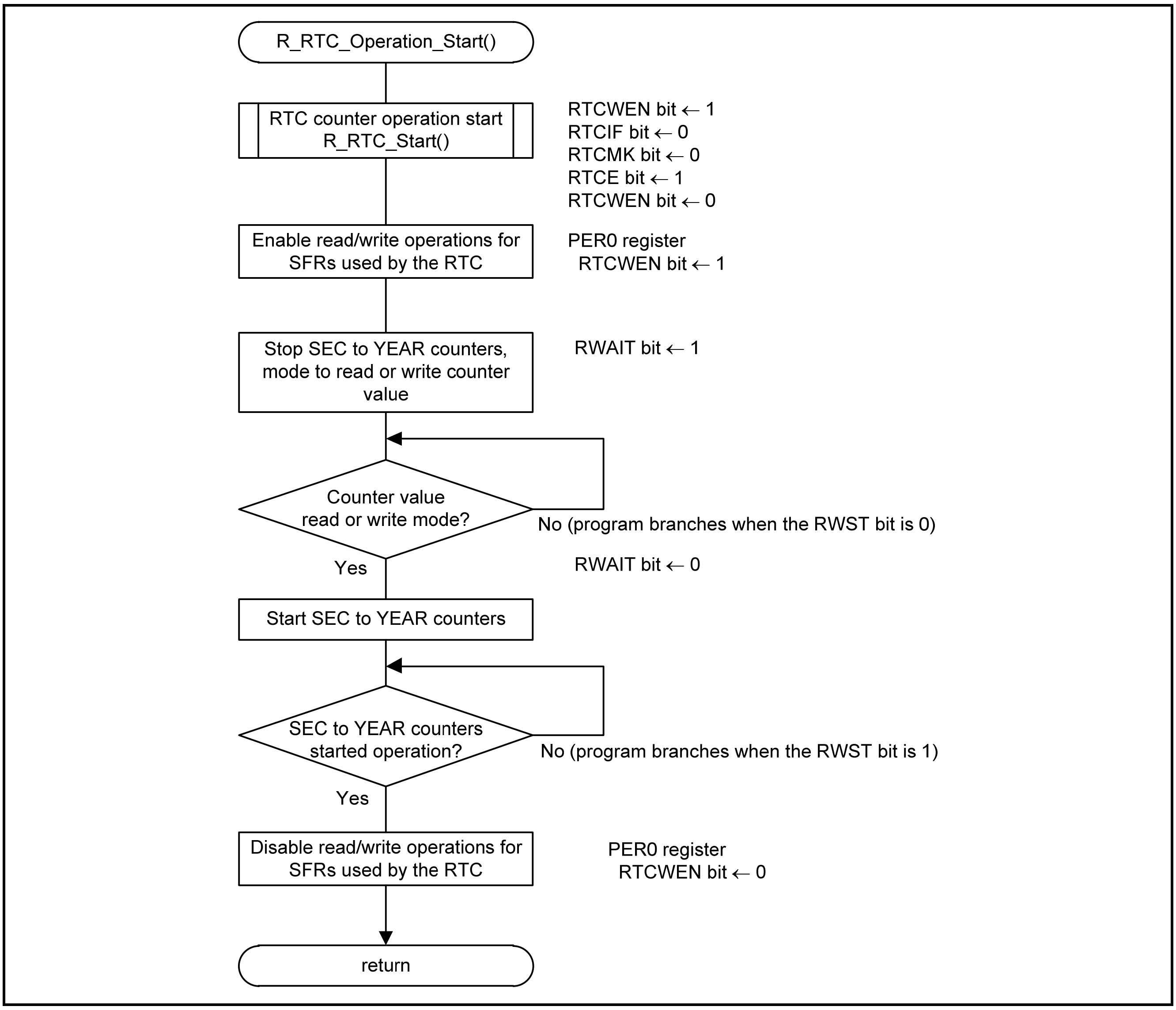


Figure 5.18 RTC Operation Start Processing

5.8.16 RTC Counter Operation Start Processing

Figure 5.19 shows the RTC counter operation start processing.

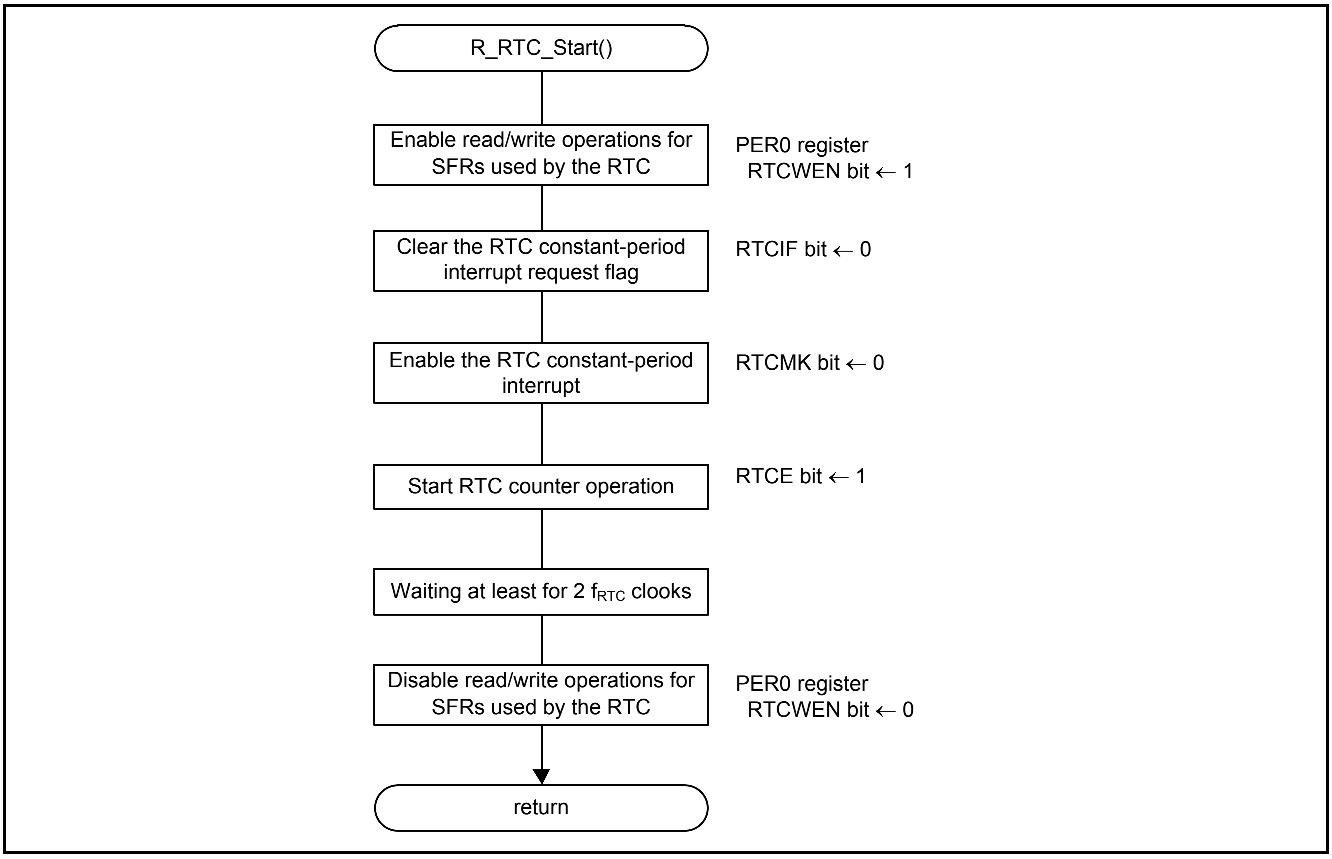


Figure 5.19 RTC Counter Operation Start Processing

5.8.17 Interrupt Source Retrieval

Figure 5.20 shows the interrupt source retrieval.

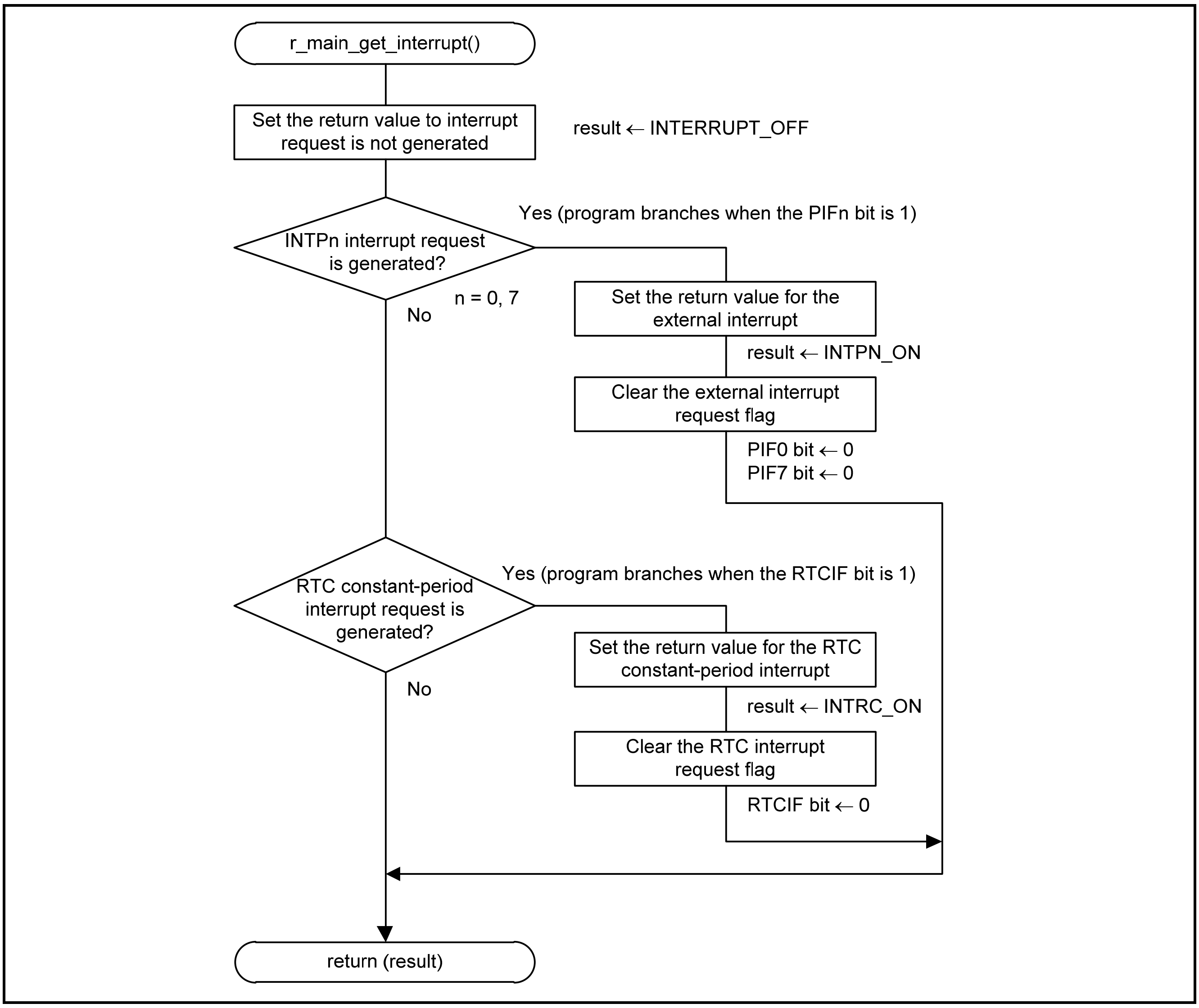


Figure 5.20 Interrupt Source Retrieval

5.8.18 RTC Read

Figure 5.21 and Figure 5.22 show the RTC read.

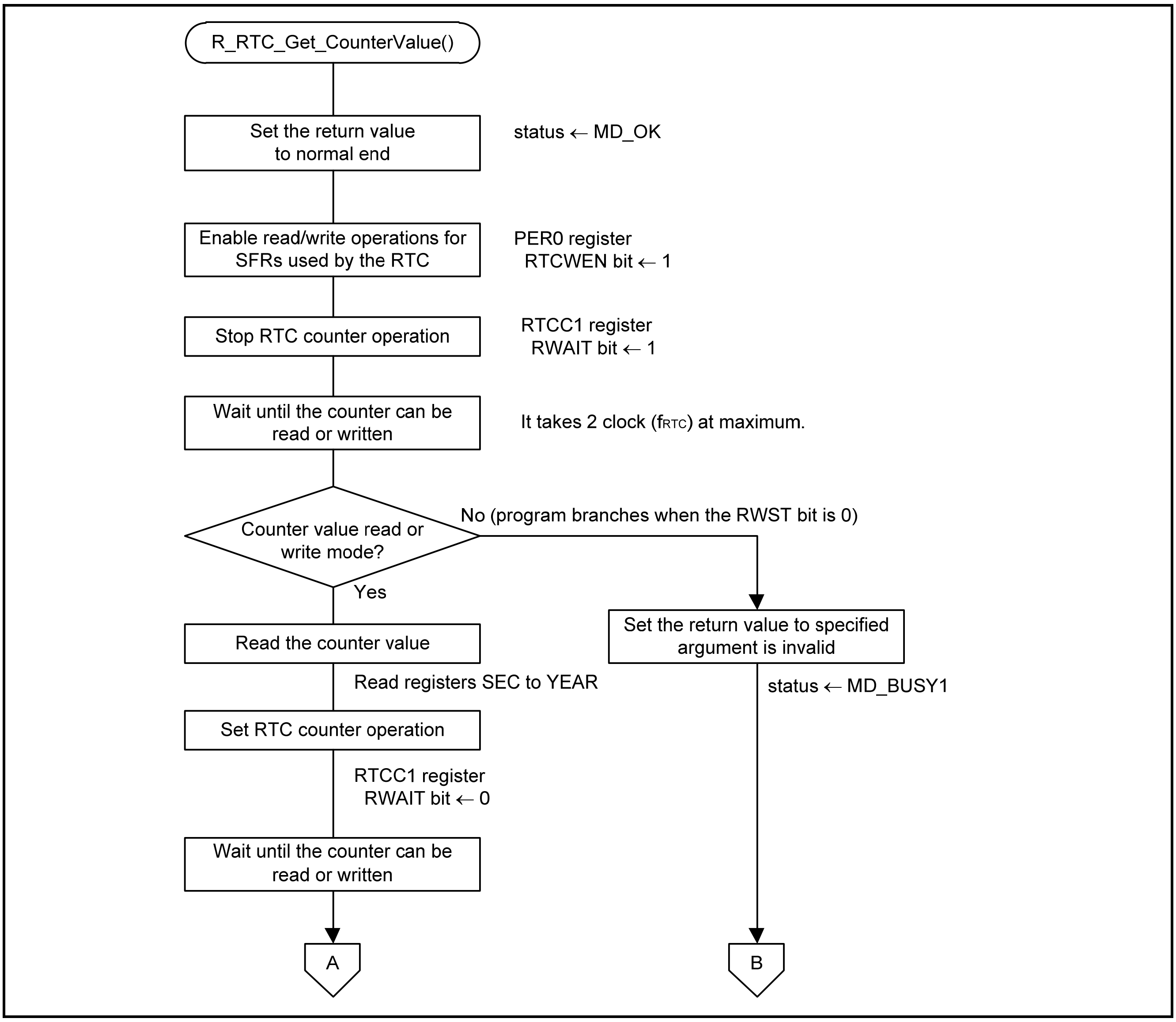


Figure 5.21 RTC Read (1/2)

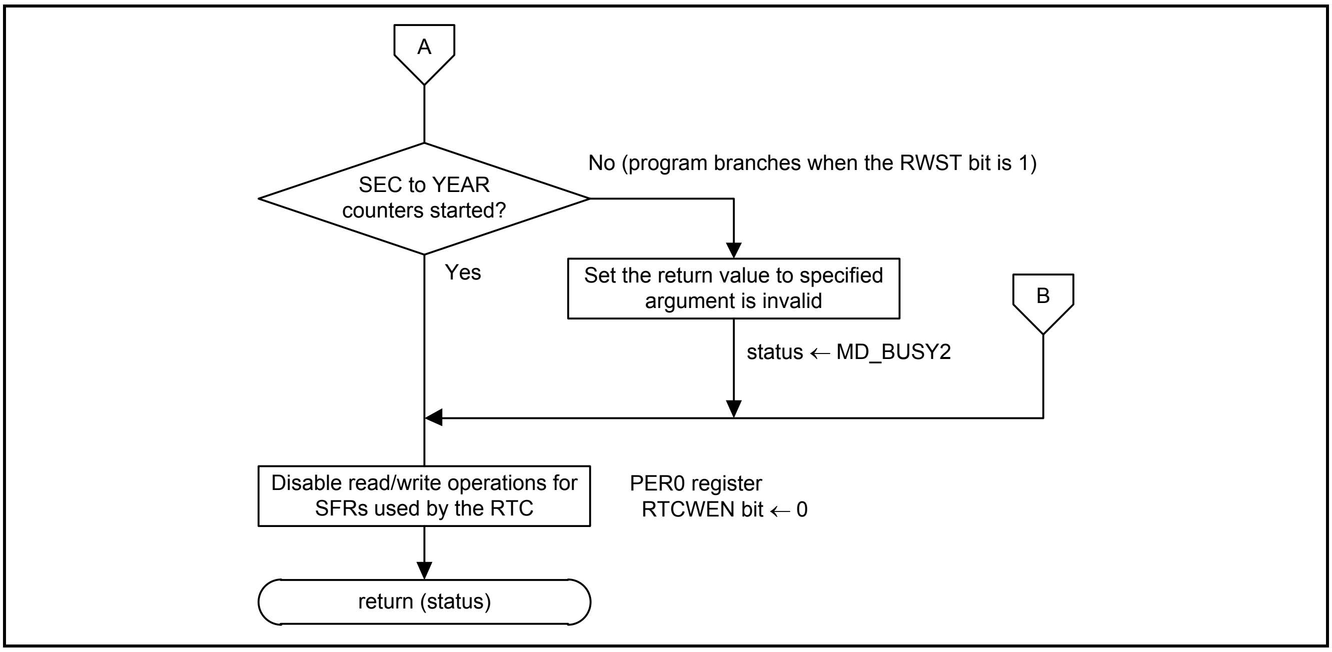


Figure 5.22 RTC Read (2/2)

5.8.19 Switch Analysis

Figure 5.23 shows the switch analysis.

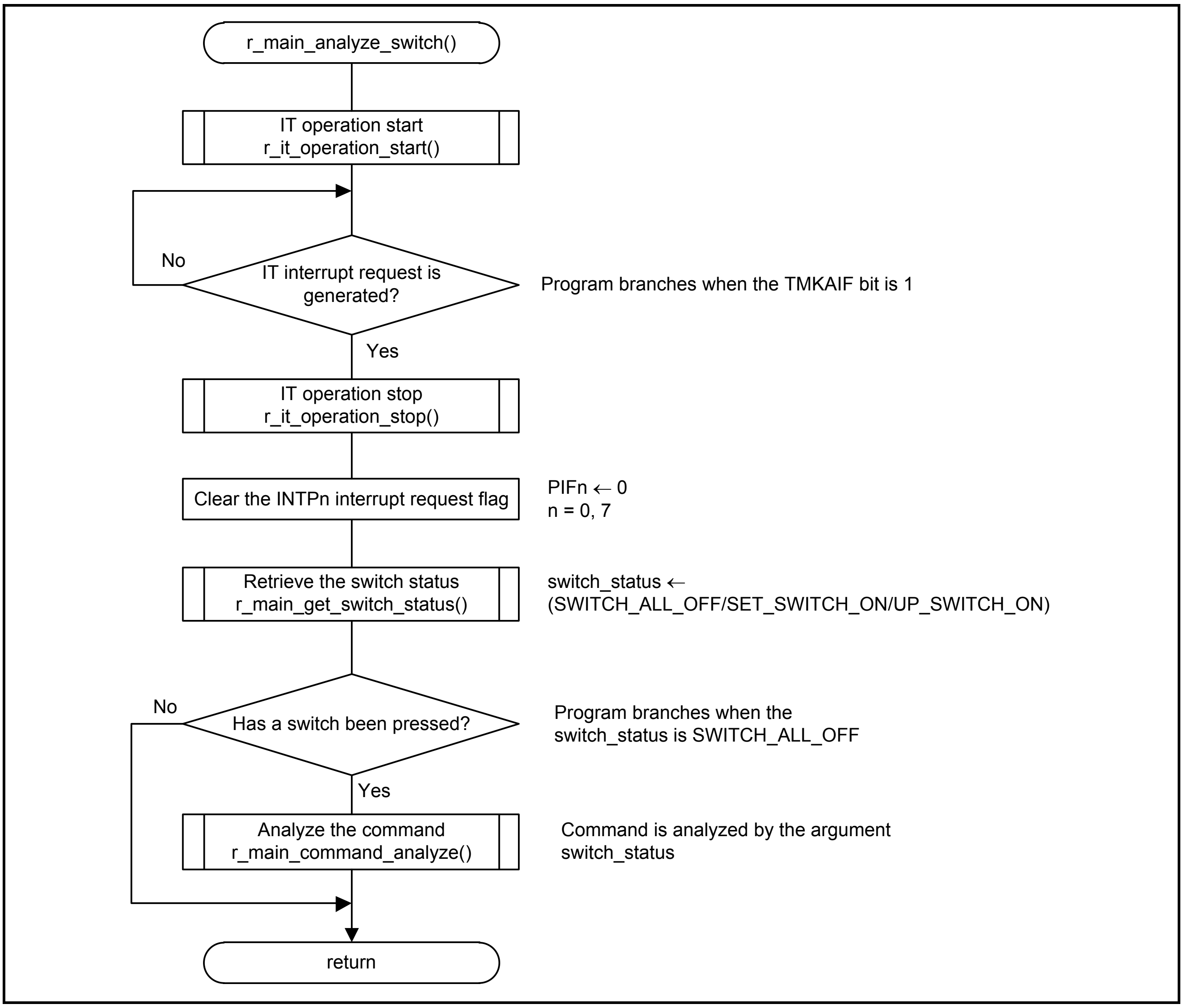


Figure 5.23 Switch Analysis

5.8.20 IT Operation Start Processing

Figure 5.24 shows the IT operation start processing.

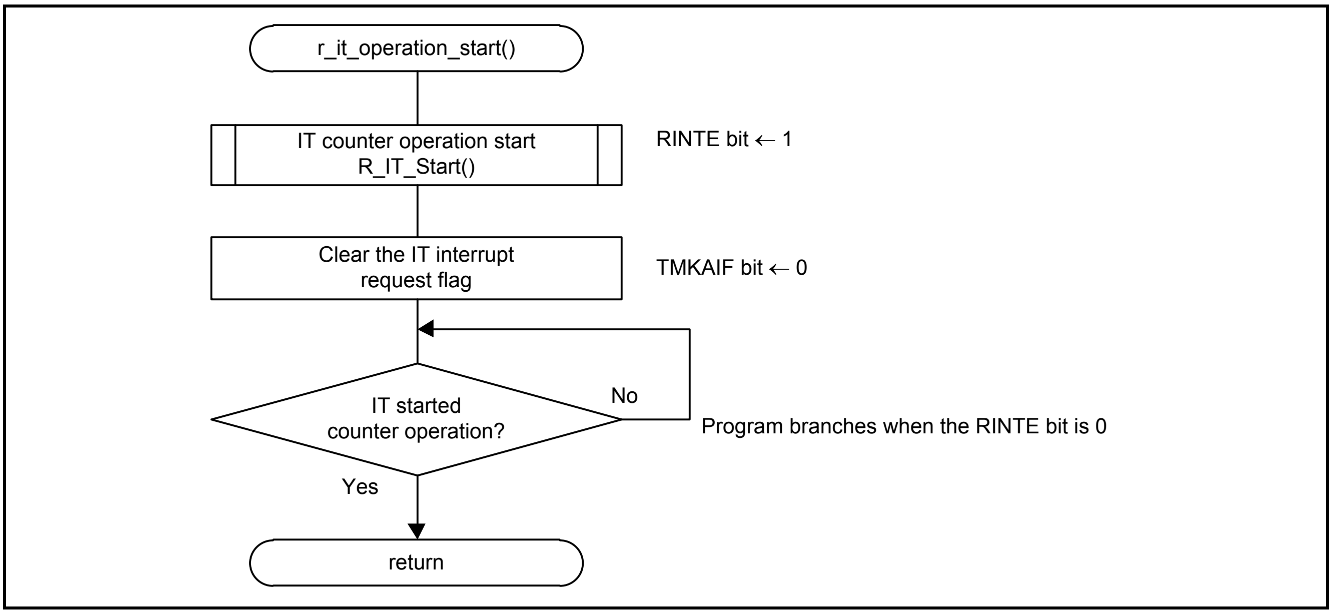


Figure 5.24 IT Operation Start Processing

5.8.21 IT Counter Operation Start Processing

Figure 5.25 shows the IT counter operation start processing.

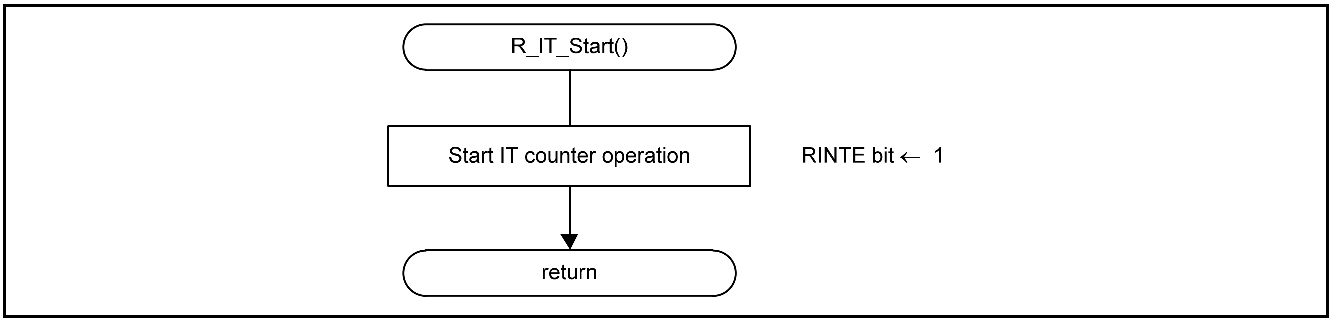


Figure 5.25 IT Counter Operation Start Processing

5.8.22 IT Operation Stop Processing

Figure 5.26 shows the IT operation stop processing.

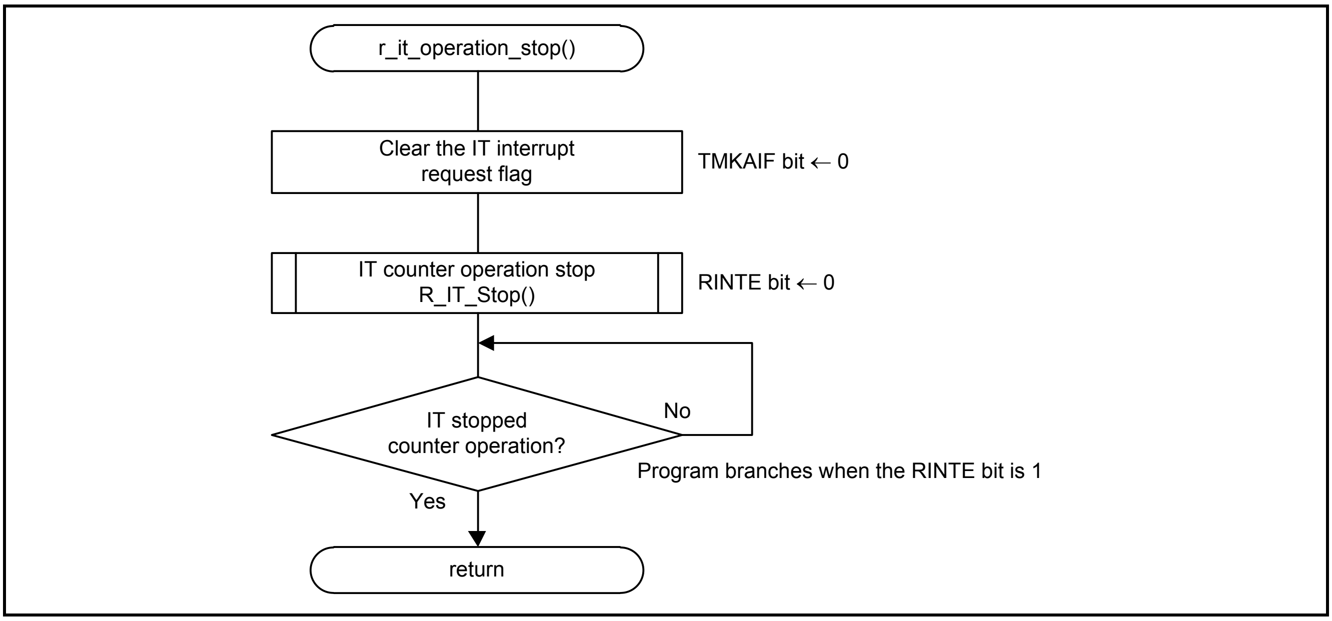


Figure 5.26 IT Operation Stop Processing

5.8.23 IT Counter Operation Stop Processing

Figure 5.27 shows the IT counter operation stop processing.

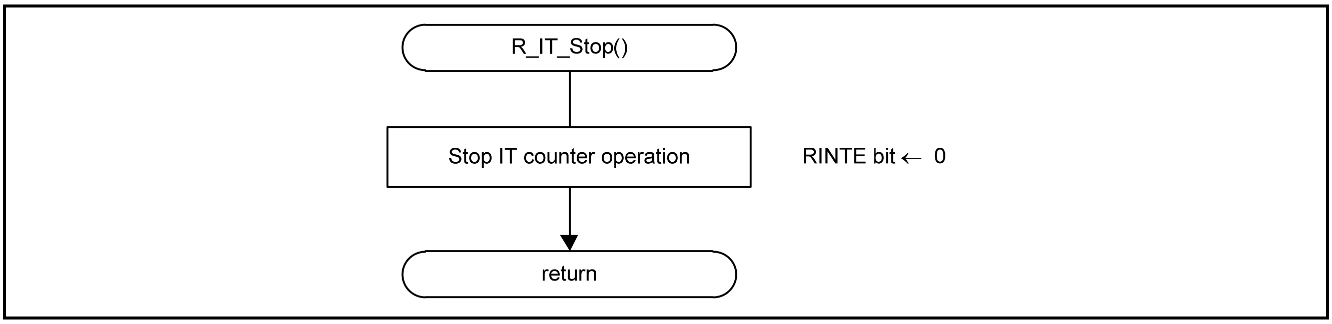


Figure 5.27 IT Counter Operation Stop Processing

5.8.24 Switch Status Retrieval

Figure 5.28 shows the switch status retrieval.

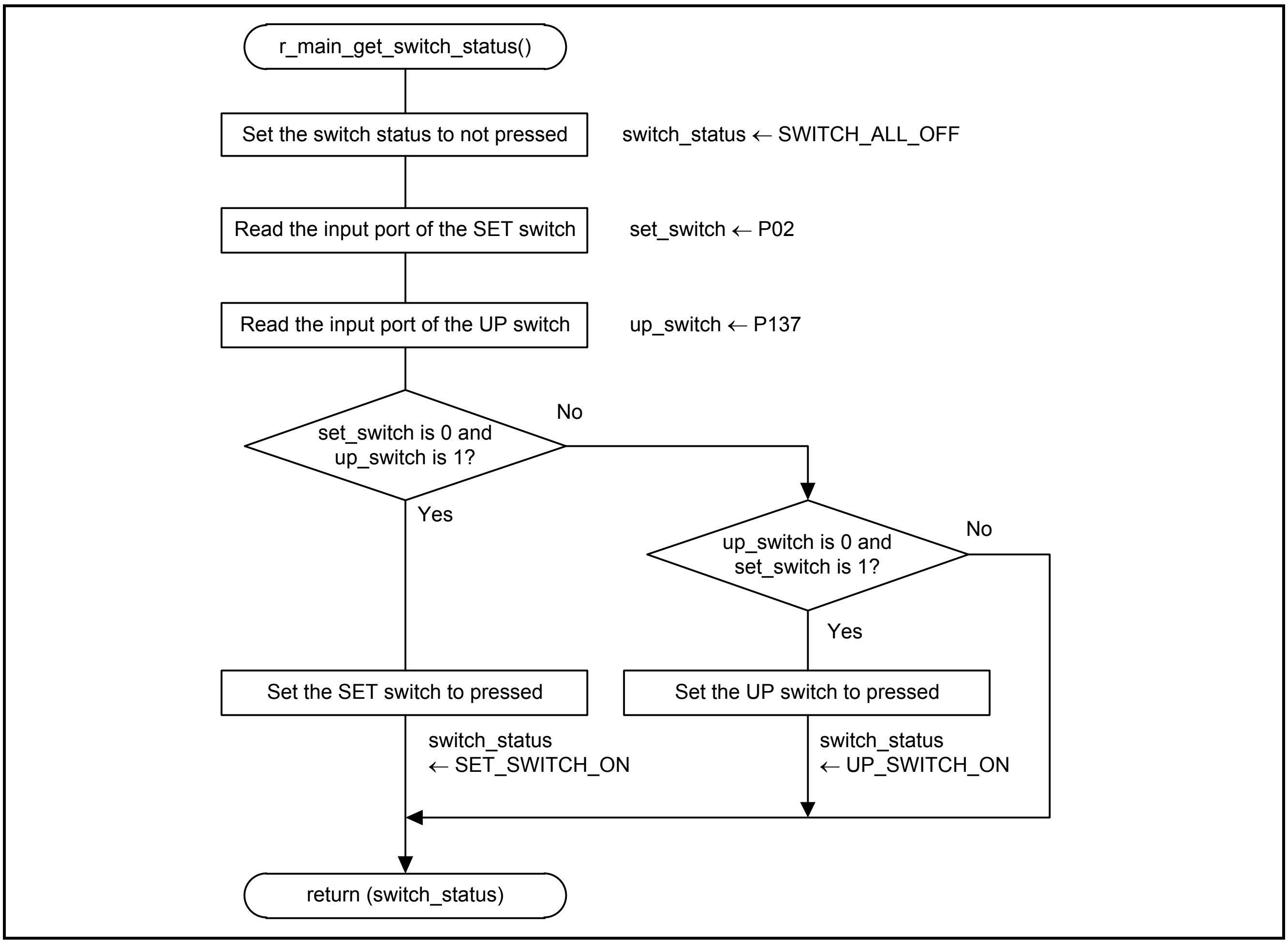


Figure 5.28 Switch Status Retrieval

5.8.25 Command Analysis

Figure 5.29 shows the command analysis.

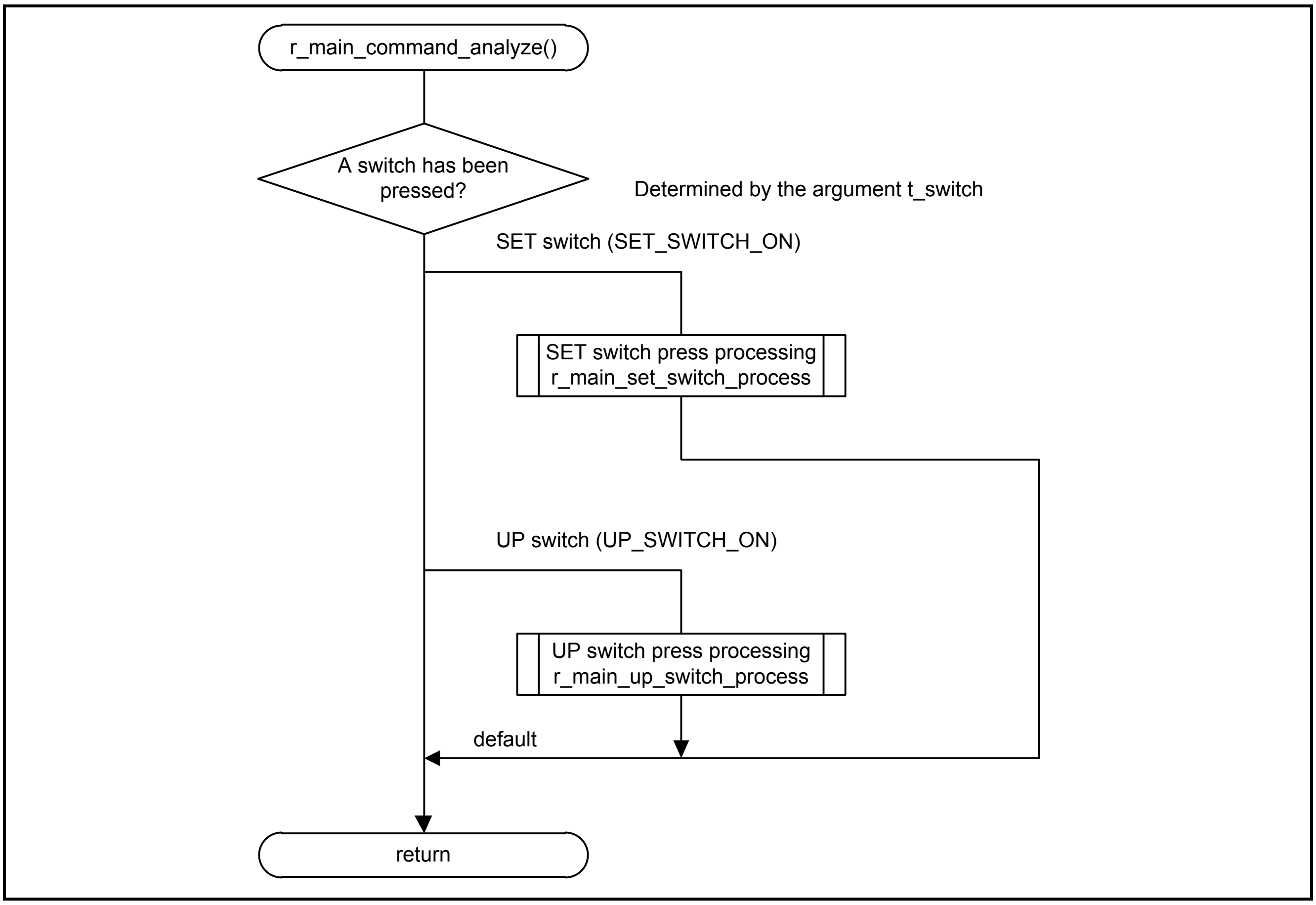


Figure 5.29 Command Analysis

5.8.26 Processing when Pressing the SET Switch

Figure 5.30 and Figure 5.31 show the processing when pressing the SET switch.

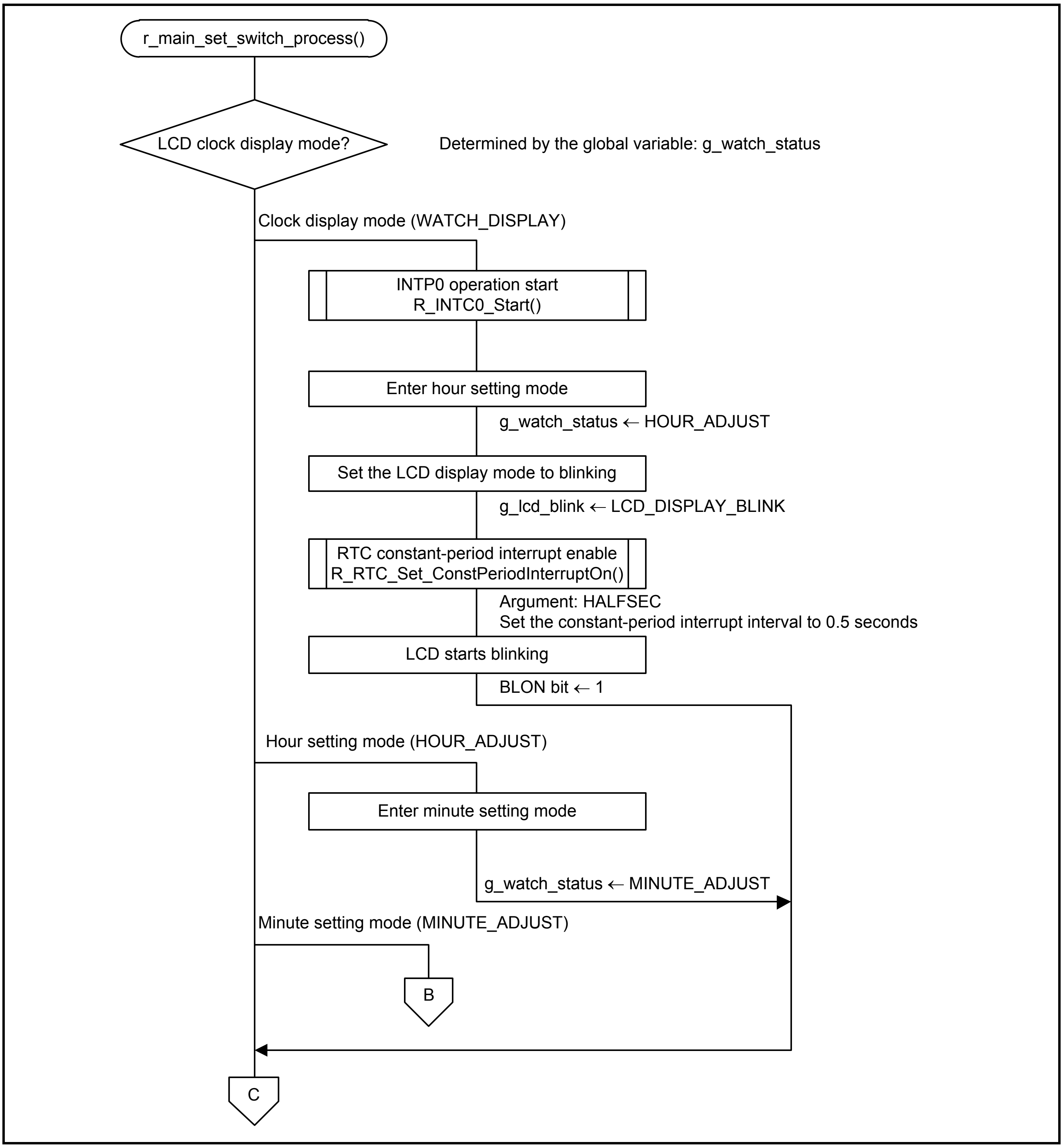


Figure 5.30 Processing when Pressing the SET Switch (1/2)

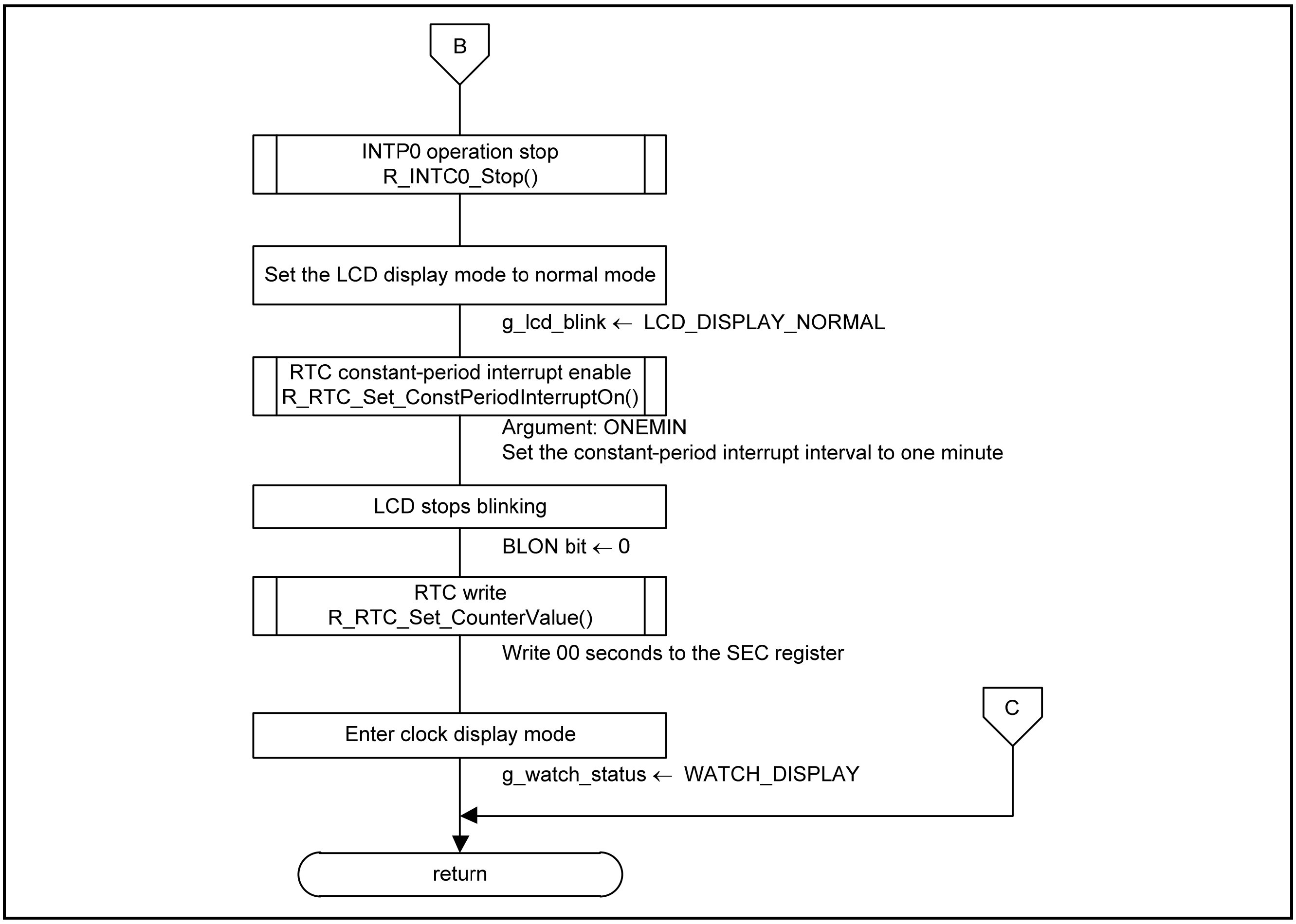


Figure 5.31 Processing when Pressing the SET Switch (2/2)

5.8.27 RTC Write

Figure 5.32 and Figure 5.33 show the RTC write.

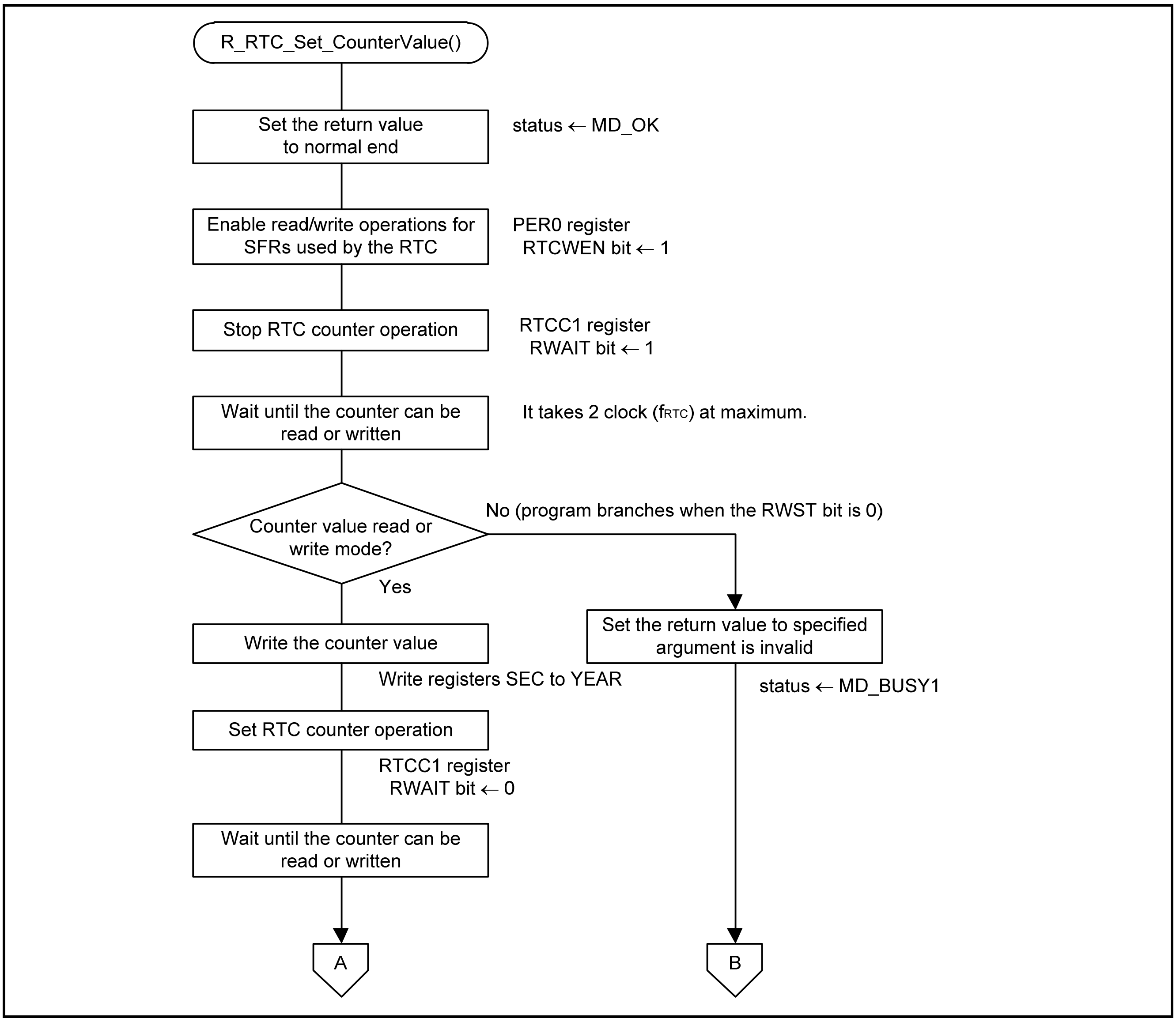


Figure 5.32 RTC Write (1/2)

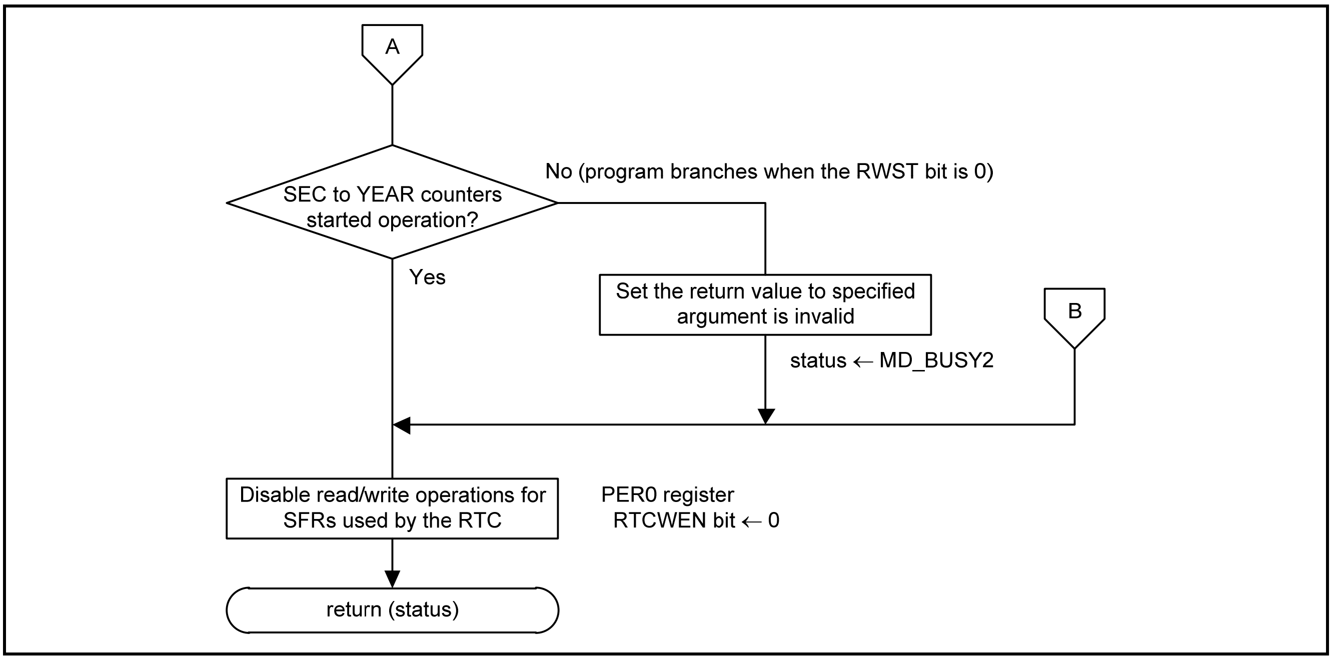


Figure 5.33 RTC Write (2/2)

5.8.28 Processing when Pressing the UP Switch

Figure 5.34 shows the processing when pressing the UP switch.

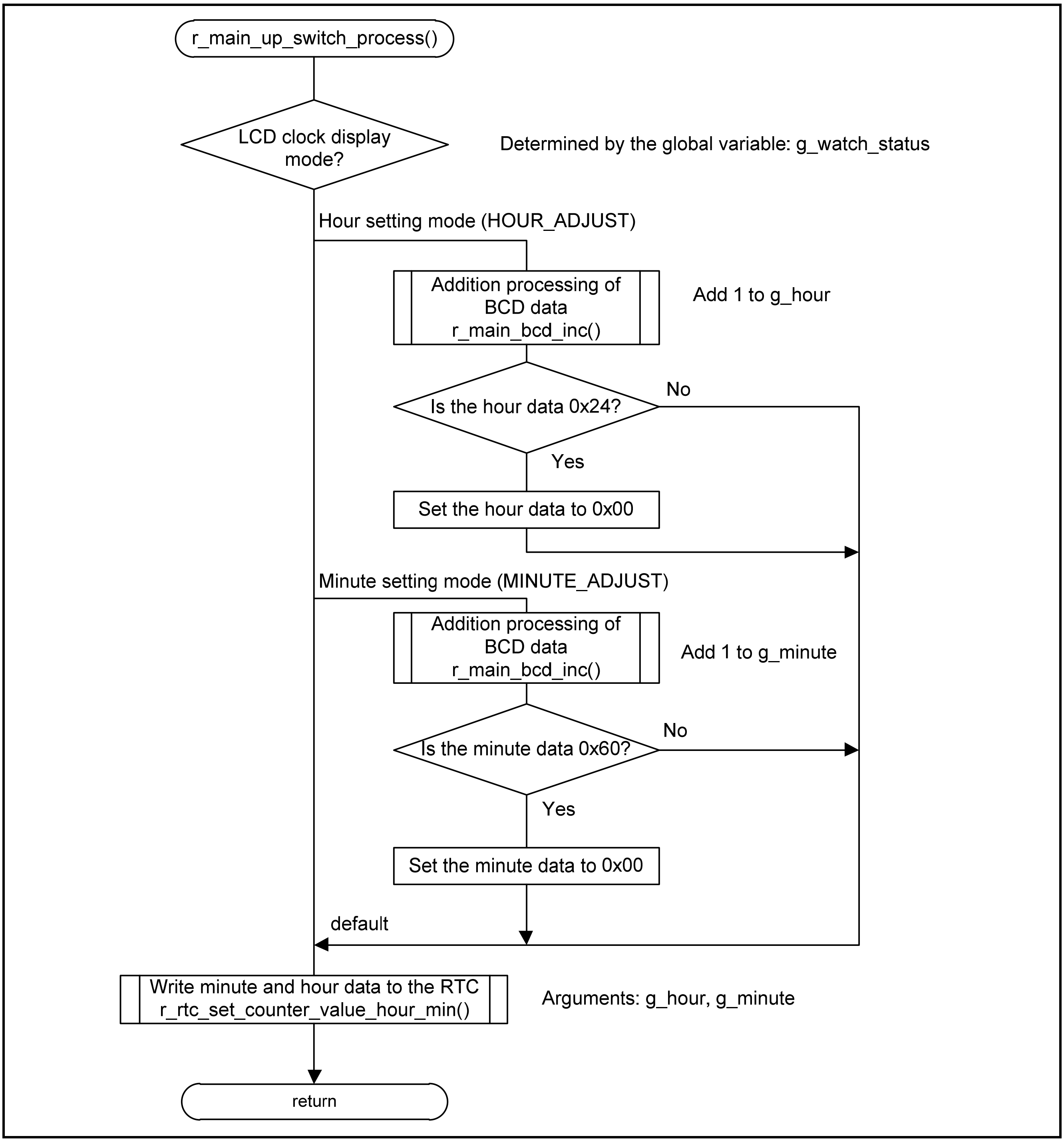


Figure 5.34 Processing when Pressing the UP Switch

5.8.29 Addition processing of BCD data

Figure 5.35 shows the addition processing of BCD data.

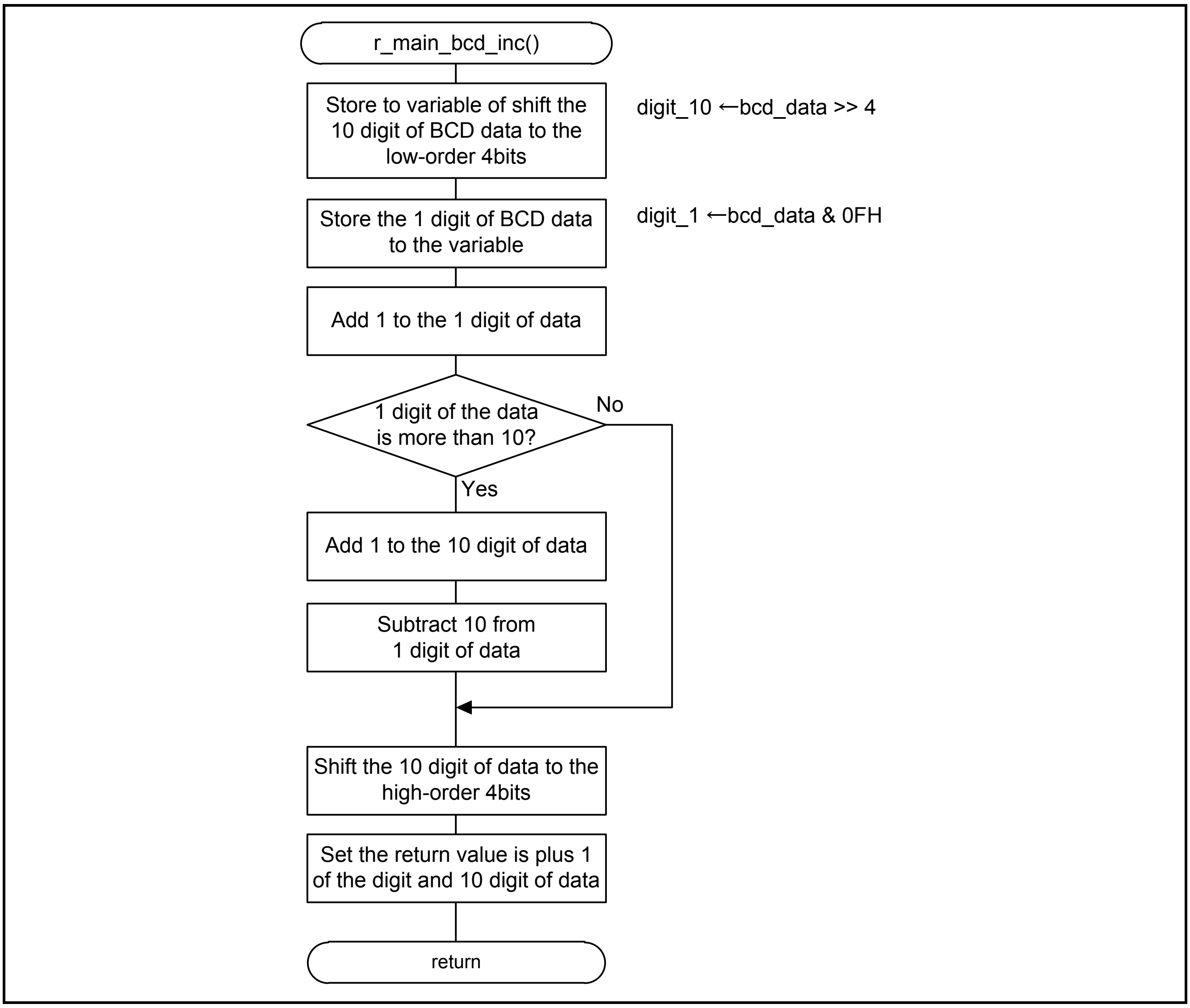


Figure 5.35 Addition processing of BCD data

5.8.30 Writing Minute and Hour Data to the RTC

Figure 5.36 and Figure 5.37 show writing minute and hour data to the RTC.

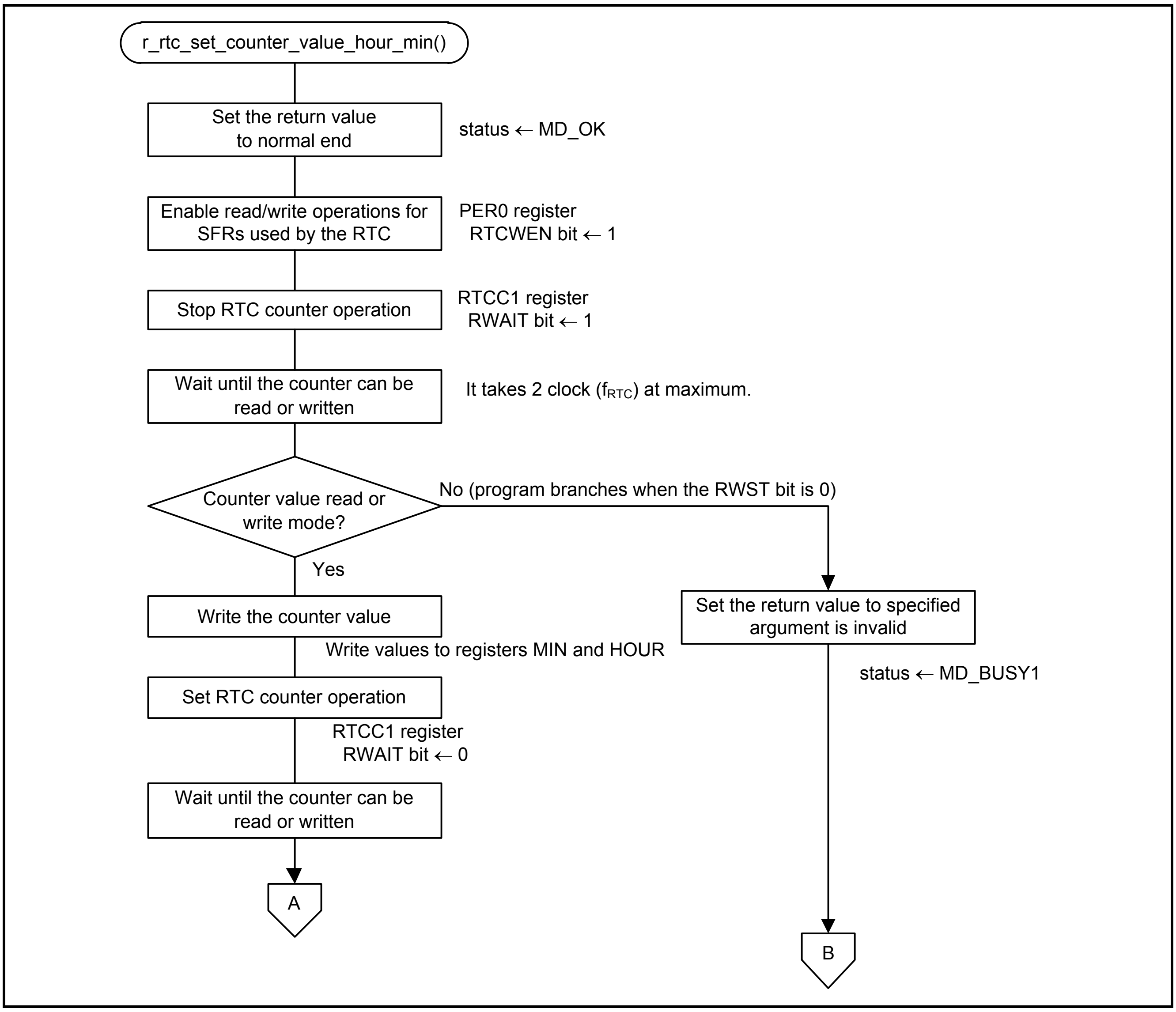


Figure 5.36 Writing Minute and Hour Data to the RTC (1/2)

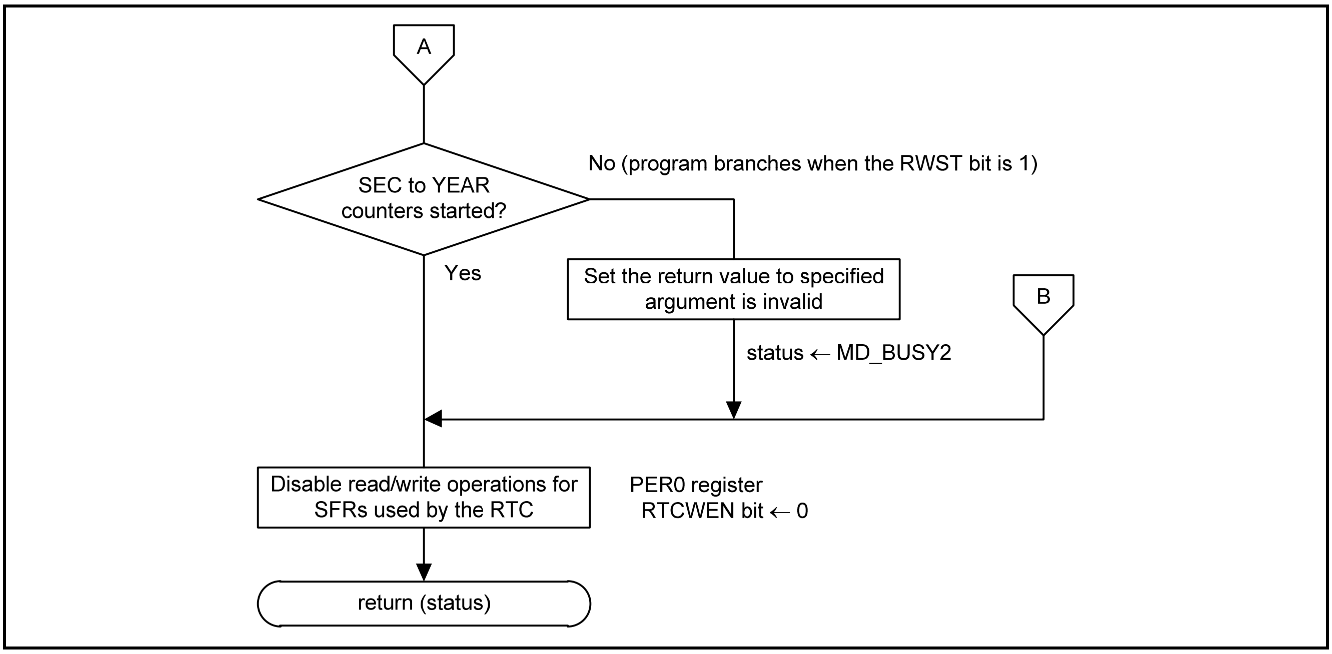


Figure 5.37 Writing Minute and Hour Data to the RTC (2/2)

5.8.31 LCD Time Display

Figure 3.38 shows the LCD time display.

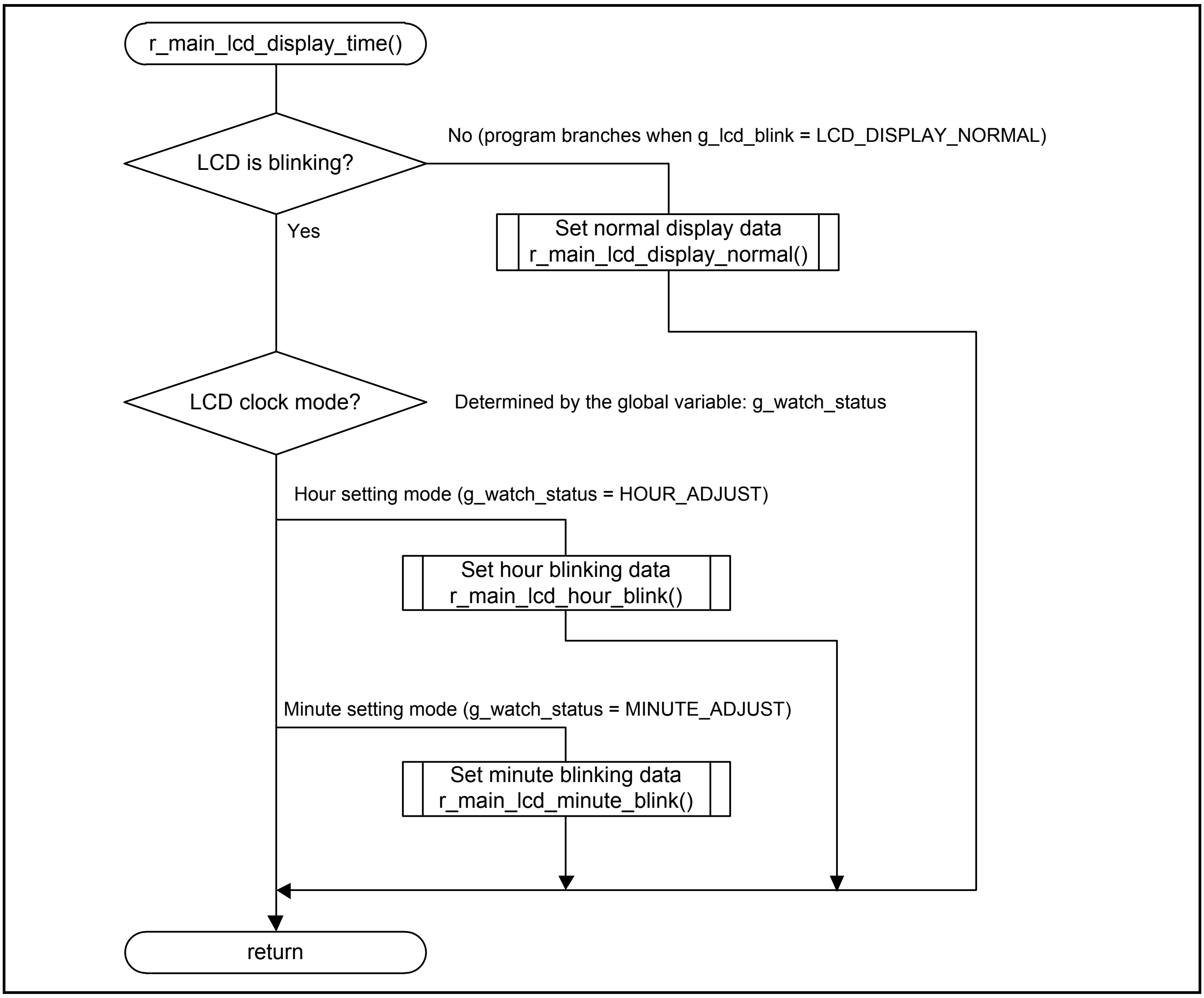


Figure 5.38 LCD Time Display

5.8.32 Set Normal Data in the LCD Display Data Register

Figure 5.39 and Figure 5.40 show the set normal data in the LCD display data register.

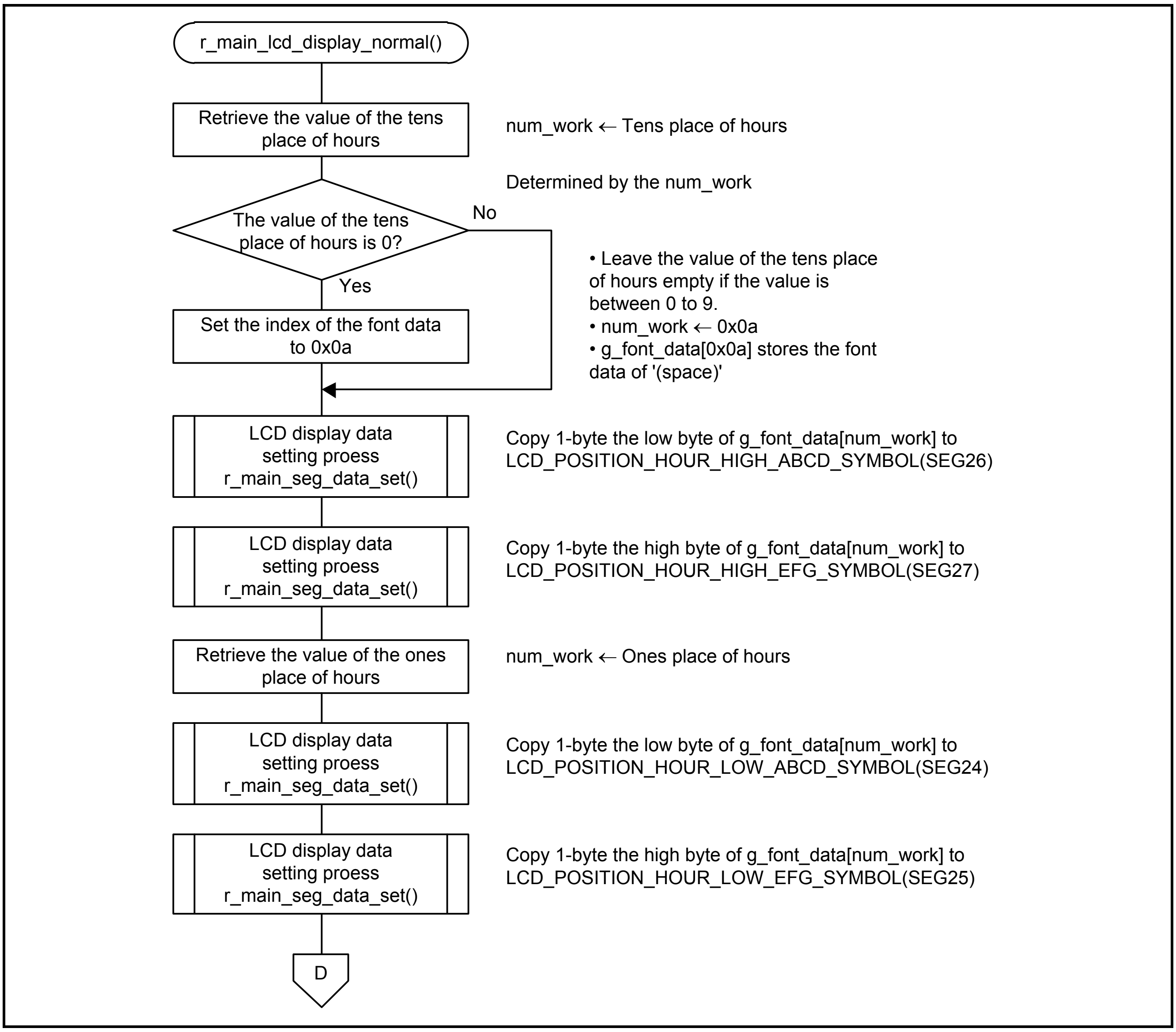


Figure 5.39 Set Normal Data in the LCD Display Data Register (1/2)

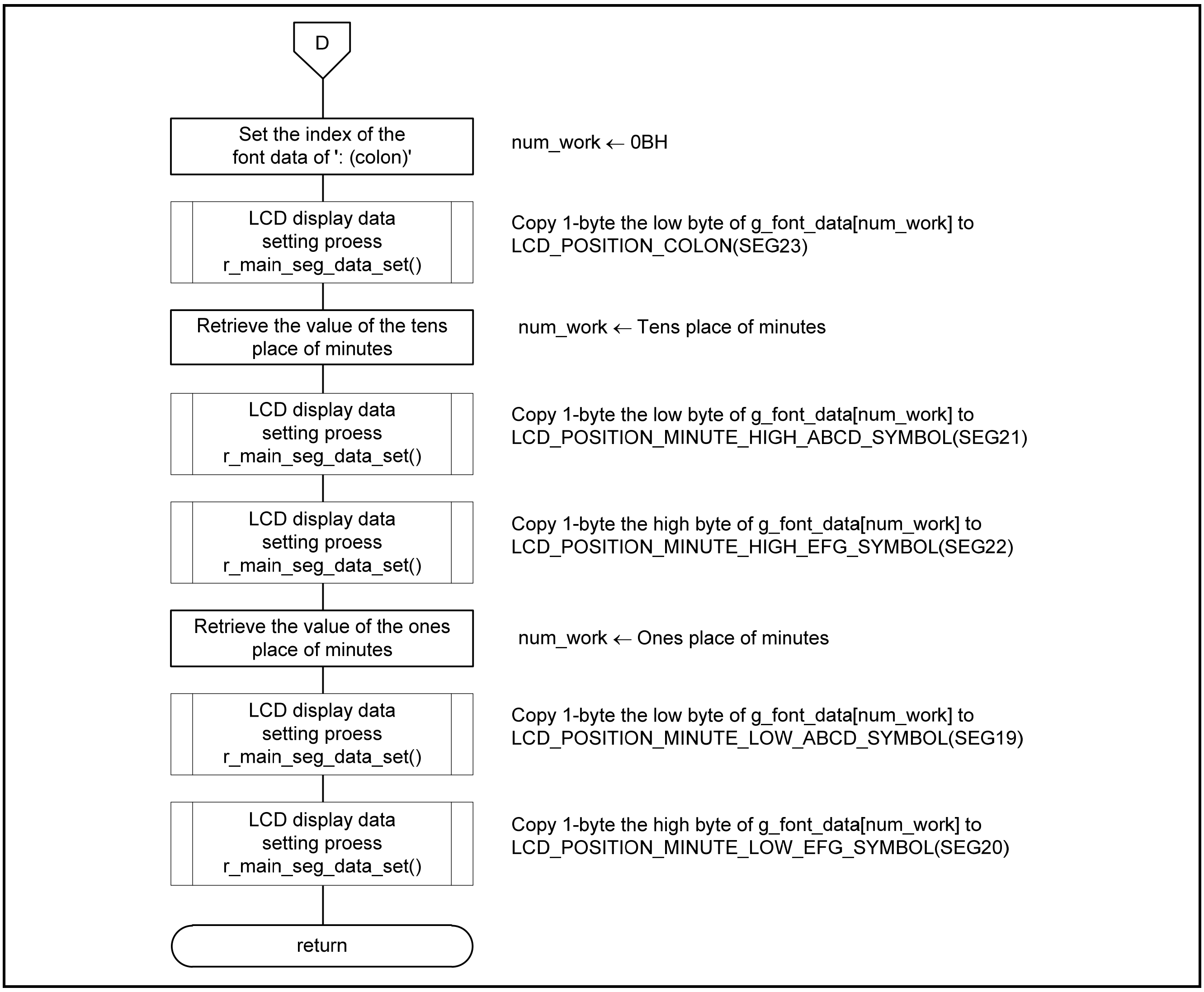


Figure 5.40 Set Normal Data in the LCD Display Data Register (2/2)

5.8.33 Set Hour Blinking Data in the LCD Display Data Register

Figure 5.41 and Figure 5.42 show the set hour blinking data in the LCD display data register.

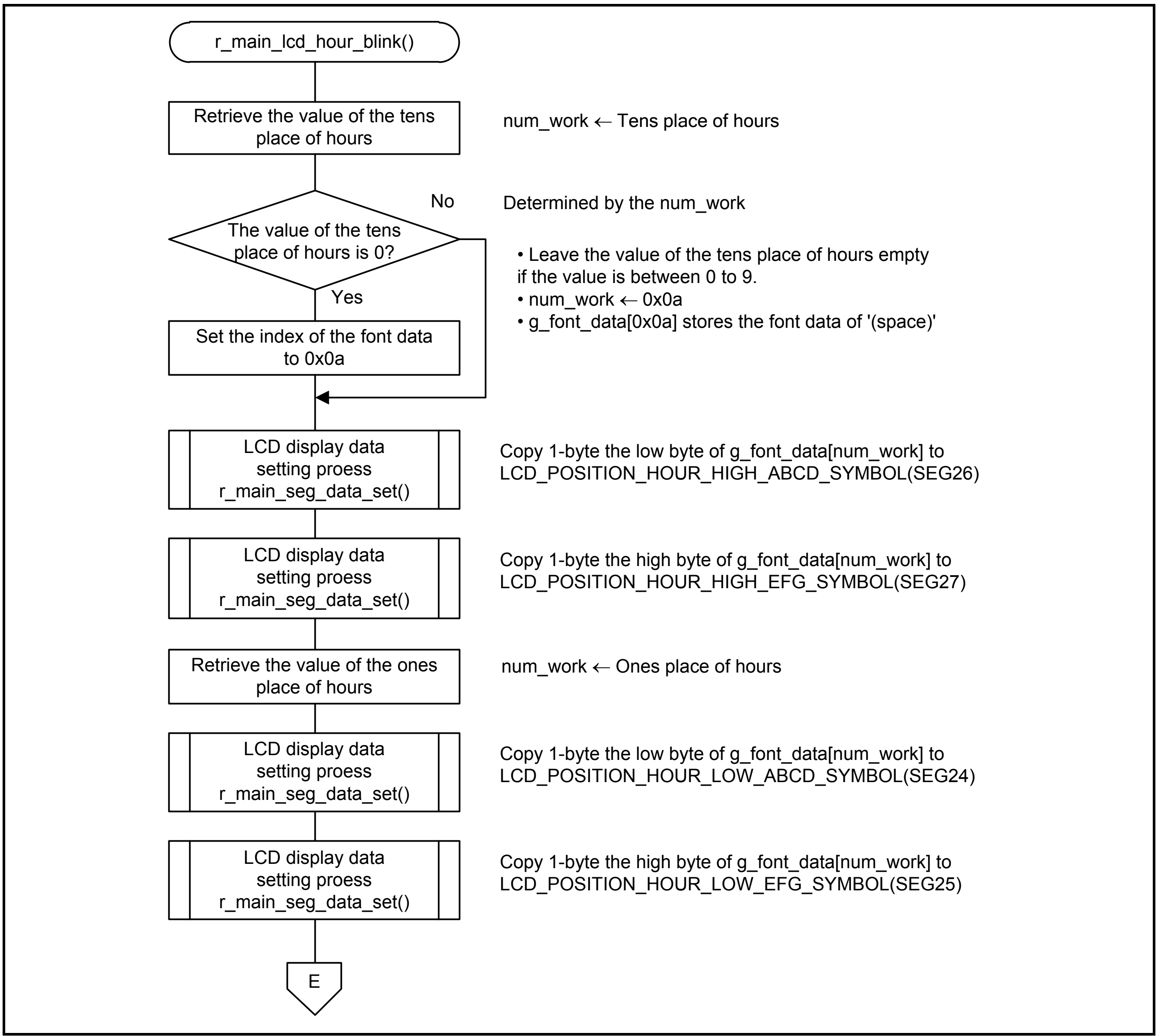


Figure 5.41 Set Hour Blinking Data in the LCD Display Data Register (1/2)

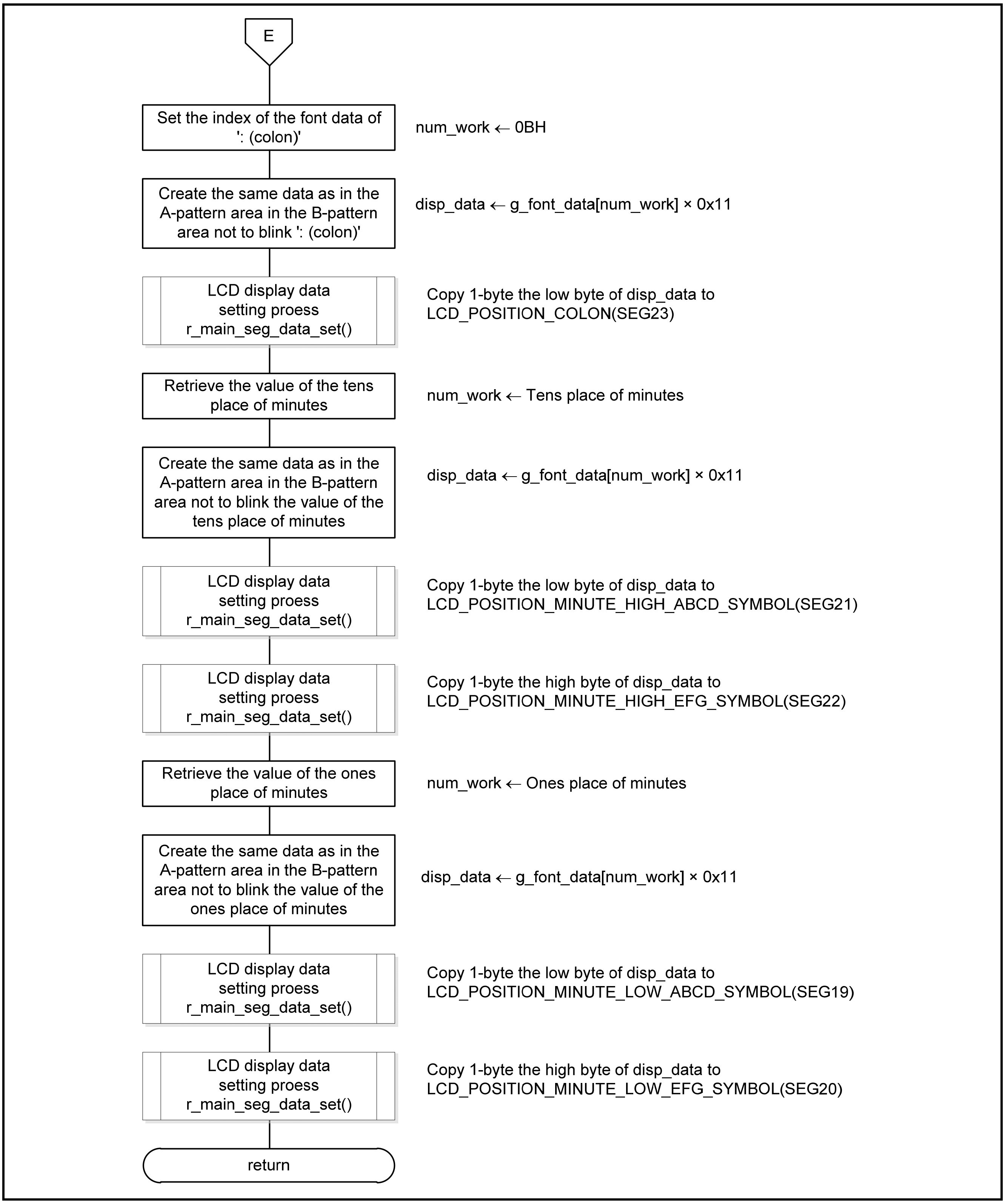


Figure 5.42 Set Hour Blinking Data in the LCD Display Data Register (2/2)

5.8.34 Set Minute Blinking Data in the LCD Display Data Register

Figure 5.43 and Figure 5.44 show the set hour blinking data in the LCD display data register.

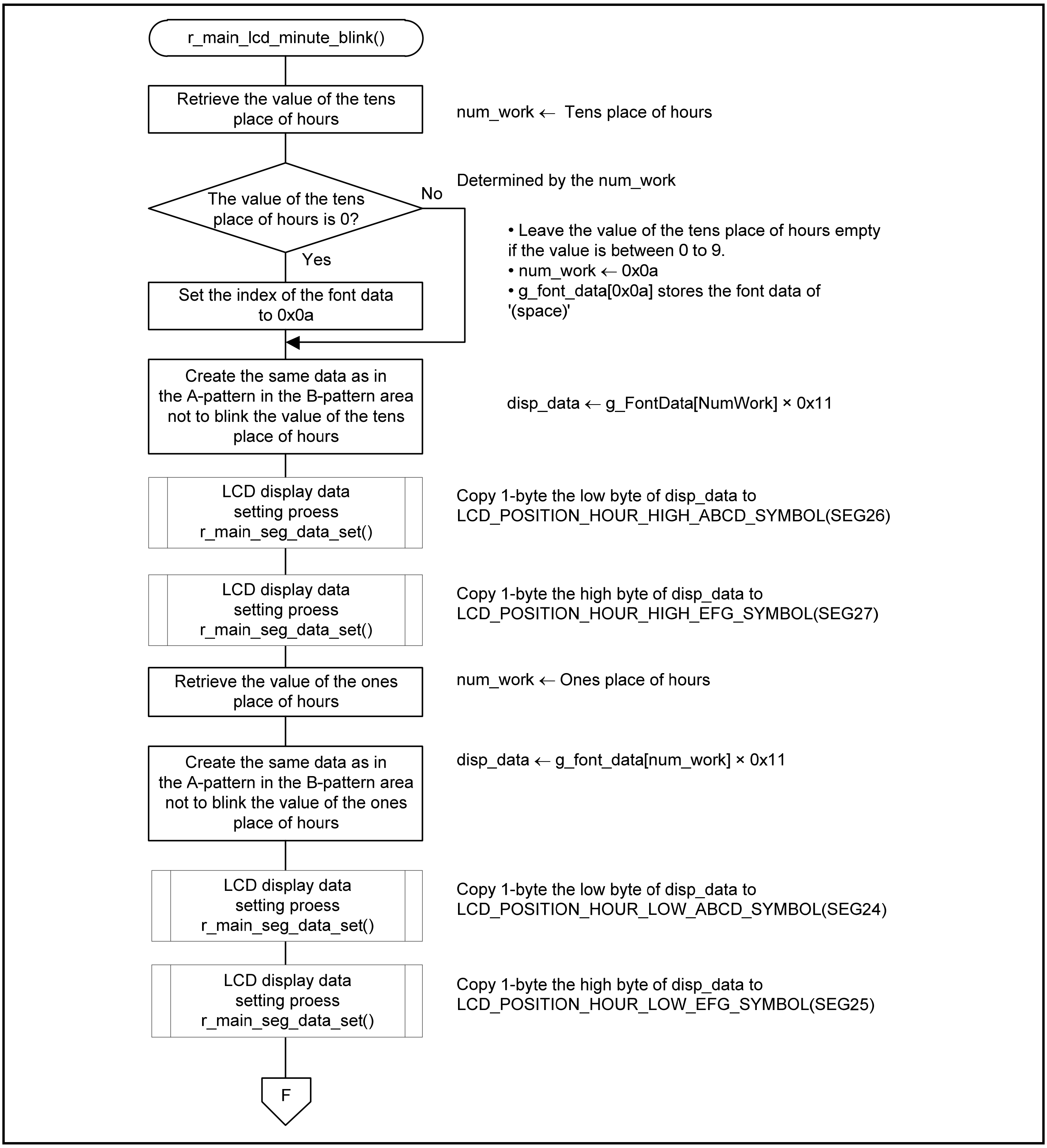


Figure 5.43 Set Minute Blinking Data in the LCD Display Data Register (1/2)

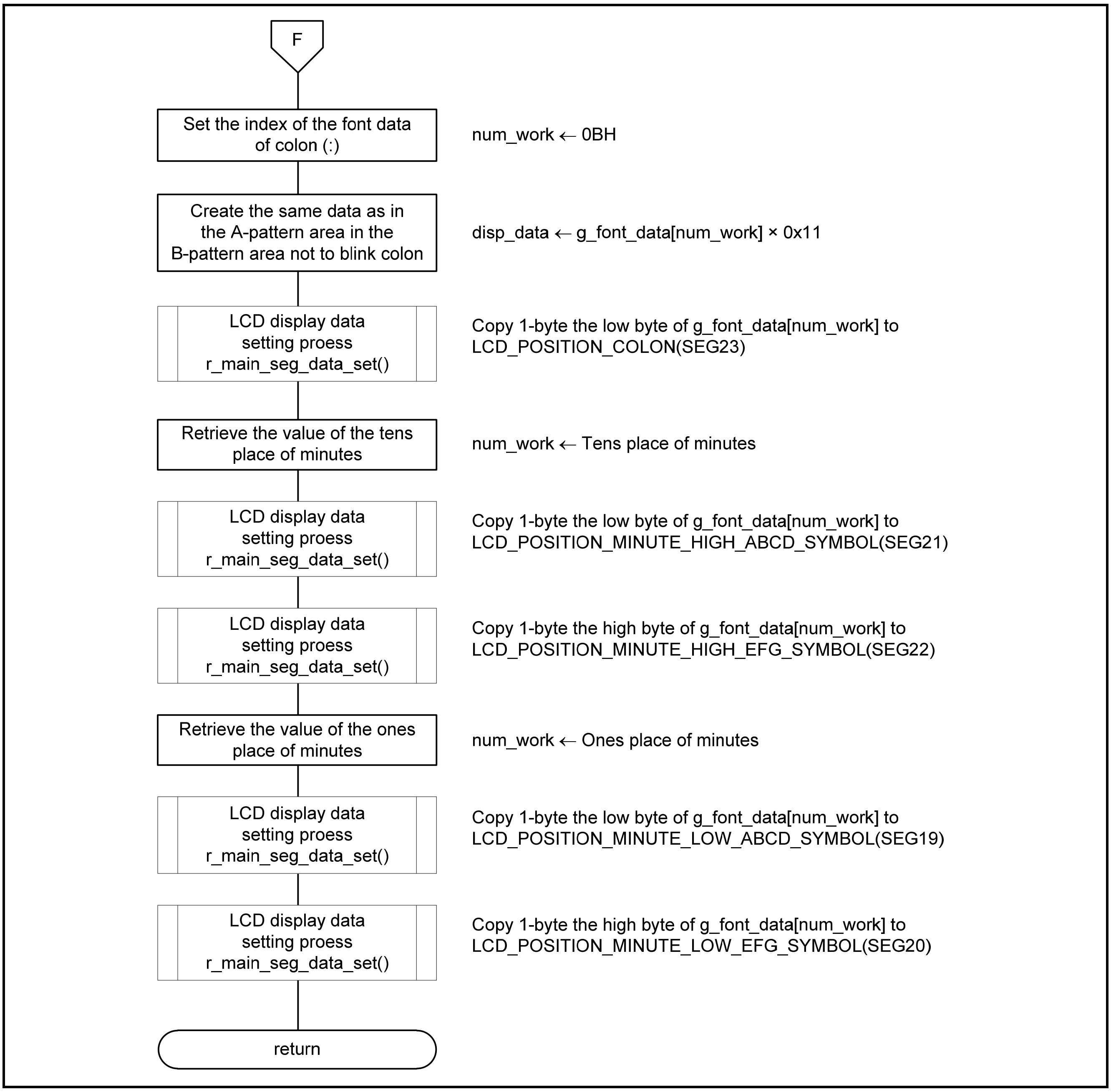


Figure 5.44 Set Minute Blinking Data in the LCD Display Data Register (2/2)

5.8.35 Set display data in the LCD display data register

Figure 5.45 show the set display data in the LCD display data register.

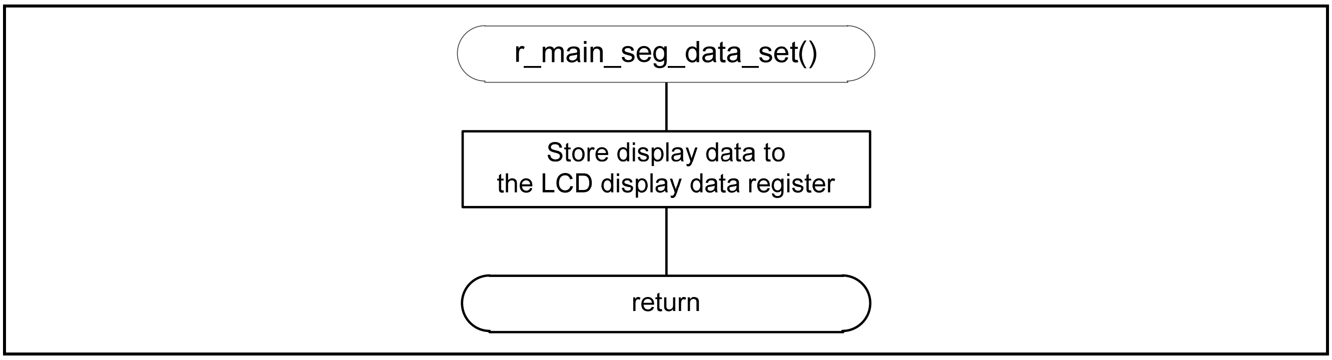


Figure 5.45 Set display data in the LCD display data register

6. Selecting or Changing the Target Device

6.1 Changing the Target Device

To change the target device, create a new project for the target device. Use the file composition of the sample project (existing project) for the new project.

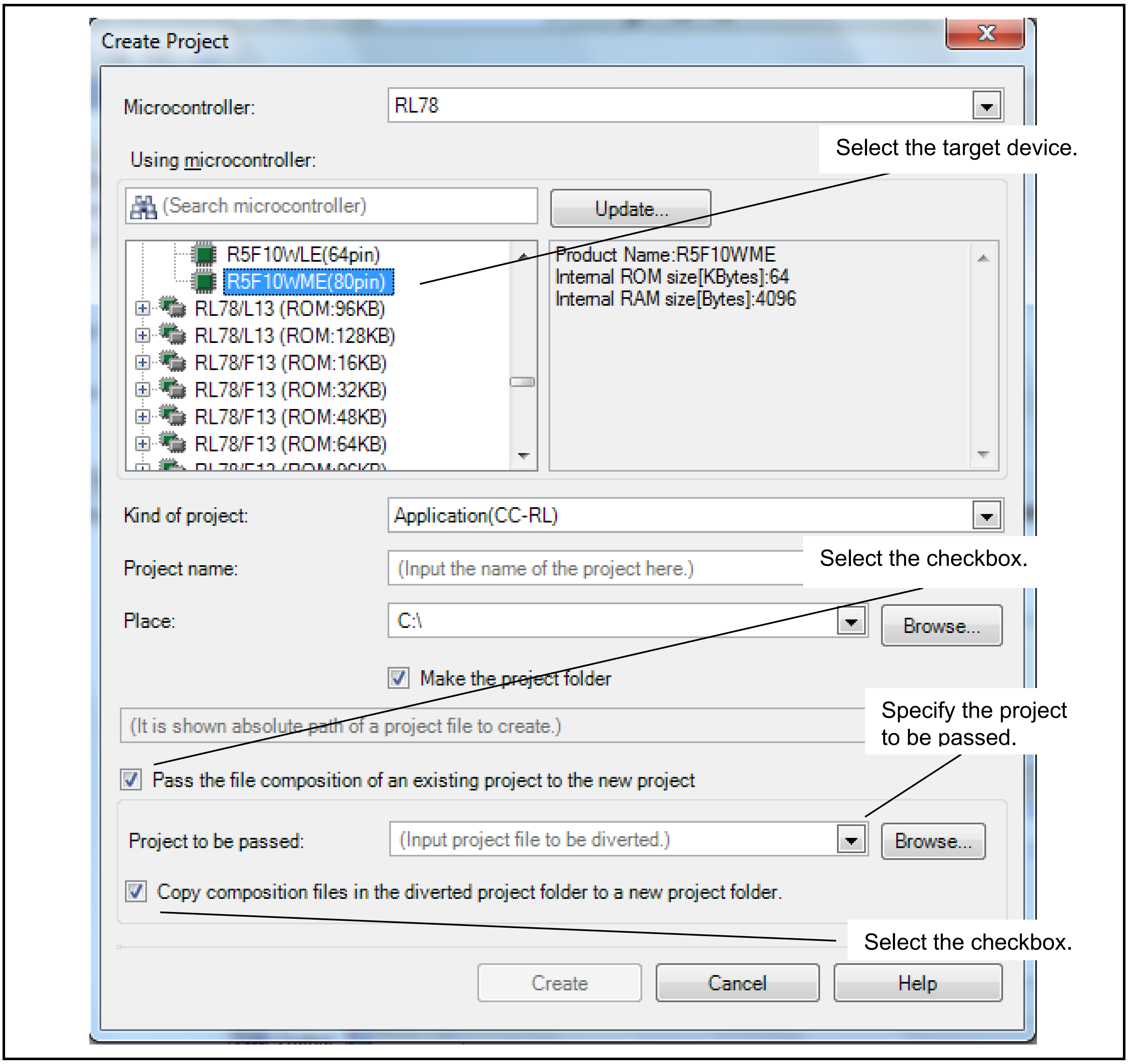


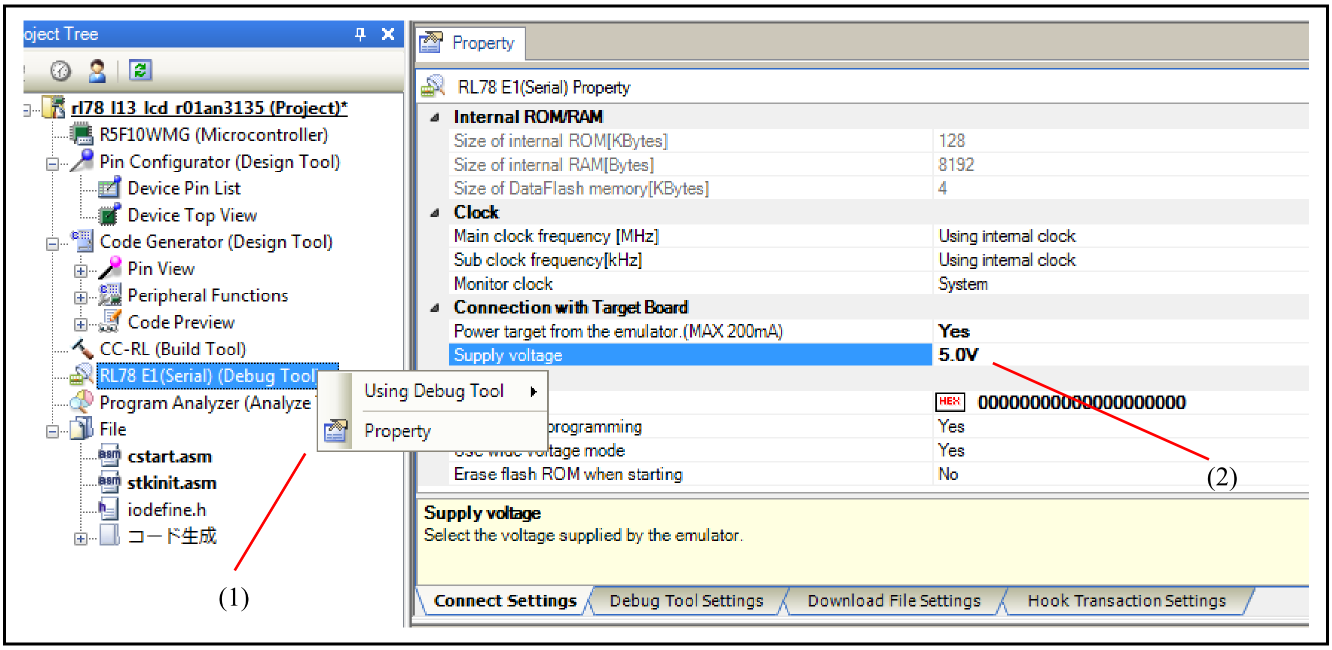
Figure 6.1 Example of Creating a New Project When Changing the Target Device

7. Setting the Debug Tool

Operation of the sample code accompanying with this application note can be verified (debugged) simply by installing the Renesas Starter Kit LCD Application Board on the Renesas Starter Kit for RL78/L13 CPU board (R0K5010WMC001BR) and powering the target board (CPU board) from the emulator.

(1) Right-click on "RL78 E1(Serial) (Debug Tool) and select "Property".

(2) On the "Property" tab, select "Power target from the emulator (MAX 200mA)". Click on the drop-down menu button on the right and select "Yes". Then click on the "Supply voltage" and change the voltage to 5.0V from the drop-down menu.



8. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

9. Reference Documents

User's Manual: Hardware
RL78/L13 User's Manual: Hardware Rev.1.00
RL78 Family User's Manual: Software Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com

Inquiries
http://www.renesas.com/contact/

REVISION HISTORY	RL78/L13 24-Hour Clock Displayed on an LCD CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 08, 2016	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Refer to "http://www.renesas.com/" for the latest and detailed information.

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